



**THE DATASHEET OF
CDCVF111FNRG4**



CDCVF111 1:9 DIFFERENTIAL LVPECL CLOCK DRIVER

SCAS670B – SEPTEMBER 2001 – REVISED JUNE 2002

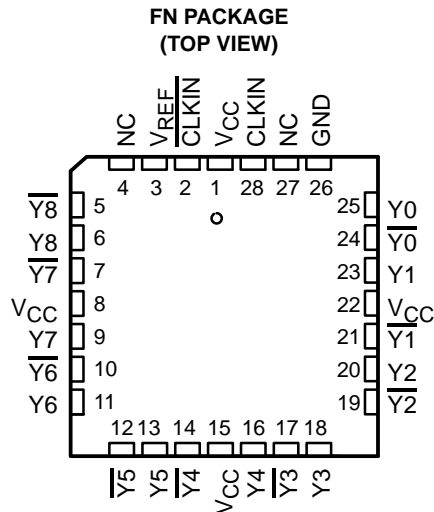
- Low-Output Skew for Clock-Distribution Applications
- Differential Low-Voltage Pseudo-ECL (LVPECL) Compatible Inputs and Outputs
- Distributes Differential Clock Inputs to Nine Differential Clock Outputs
- Output Reference Voltage (V_{REF}) Allows Distribution From a Single-Ended Clock Input
- Packaged In a 28-Pin Plastic Chip Carrier

description

The differential LVPECL clock-driver circuit distributes one pair of differential LVPECL clock inputs (\overline{CLKIN} , $CLKIN$) to nine pairs of differential clock (Y , \overline{Y}) outputs with minimum skew for clock distribution. It is specifically designed for driving 50- Ω transmission lines.

The V_{REF} output can be strapped to the \overline{CLKIN} input for a single-ended $CLKIN$ input.

The CDCVF111 is characterized for operation from -40°C to 85°C .



NC – No internal connection

FUNCTION TABLE

INPUTS		OUTPUTS	
$CLKIN$	\overline{CLKIN}	Y_n	\overline{Y}_n
X	X	L	H
L	H	L	H
H	L	H	L
L	V_{REF}	L	H
H	V_{REF}	H	L
V_{REF}	L	H	L
V_{REF}	H	L	H



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 **TEXAS
INSTRUMENTS**

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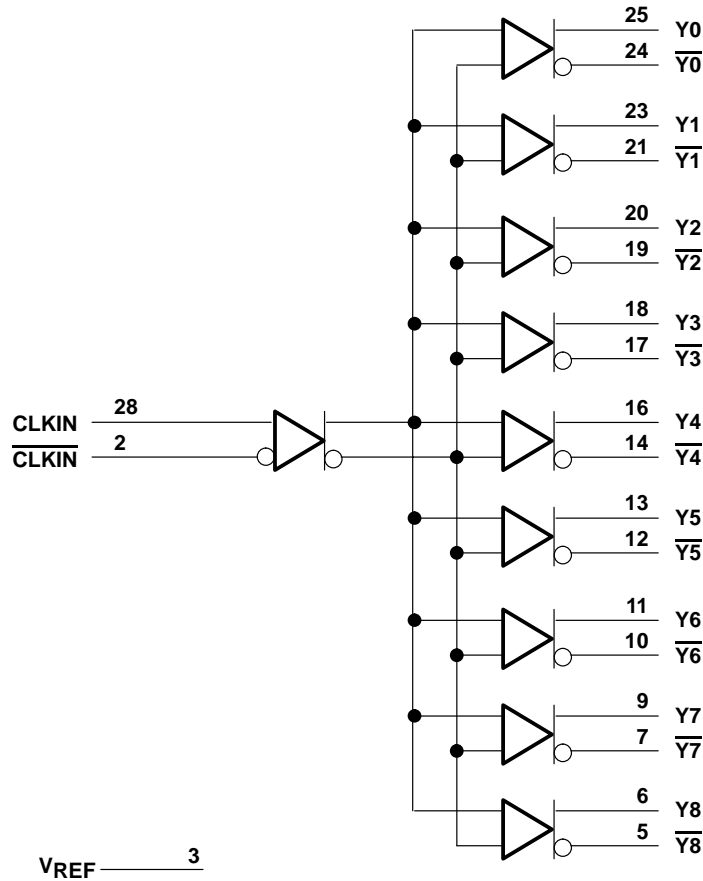
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CDCVF111

1:9 DIFFERENTIAL LVPECL CLOCK DRIVER

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	-18 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	-50 mA
Continuous current through V_{CC} or GND	± 80 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	525 mW
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.



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recommended operating conditions

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	3	3.6	V	
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	V _{CC} -1.165	V _{CC} -0.88	V
		V _{CC} = 3.3 V	2.135	2.42	V
V _{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V	V _{CC} -1.81	V _{CC} -1.475	V
		V _{CC} = 3.3 V	1.49	1.825	V
T _A	Operating free-air temperature	-40	85	°C	
f _{clock}	Input frequency		650	MHz	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
V _{REF}	V _{CC} = 3 V to 3.6 V	I _{REF} = 100 μA	V _{CC} -1.38	V _{CC} -1.26	V
	V _{CC} = 3.3 V		1.92	2.04	
V _{OH}	V _{CC} = 3 V to 3.6 V, T _A = 0°C to 85°C, f _(max) = 650 MHz		V _{CC} -1.12	V _{CC} -0.83	V
	V _{CC} = 3 V to 3.6 V, T _A = -40°C to 85°C, f _(max) = 650 MHz		V _{CC} -1.15	V _{CC} -0.83	
	V _{CC} = 3.3 V		2.275	2.42	
V _{OL}	V _{CC} = 3 V to 3.6 V, T _A = 0°C to 85°C, f _(max) = 650 MHz		V _{CC} -1.86	V _{CC} -1.49	V
	V _{CC} = 3 V to 3.6 V, T _A = -40°C to 85°C, f _(max) = 650 MHz		V _{CC} -1.86	V _{CC} -1.52	
	V _{CC} = 3.3 V		1.49	1.68	
I _I	V _I = 2.4 V,	V _{CC} = 3.6 V		150	μA
I _{CC} (Internal)	I _O = 0,	V _{CC} = 3.6 V		100	mA

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{PLH}	CLKIN, $\overline{\text{CLKIN}}$	Y, $\overline{\text{Y}}$	450	600	ps
t _{PHL}					
t _{sk(o)}		Y, $\overline{\text{Y}}$		50	ps
t _{sk(pr)}		Y, $\overline{\text{Y}}$		150	ps
t _r		Y, $\overline{\text{Y}}$	200	600	ps
t _f					

CDCVF111

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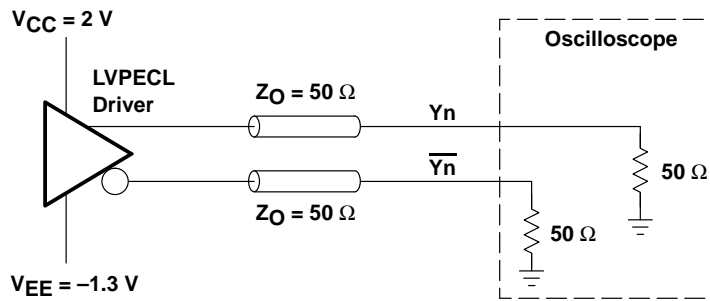
ESD information

ESD MODELS	LIMIT
Human Body Model (HBM)	2.0 kV
Machine Model (MM)	200 V
Charge Device Model (CDM)	2.0 kV

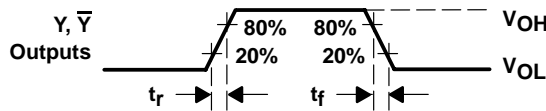
thermal information

CDCVF111 28-PIN PLCC		THERMAL AIR FLOW (CFM)				UNIT
		0	150	250	500	
R θ JA	High K	48	44	42	39	°C/W
R θ JA	Low K	70	58	52	46	°C/W
R θ JC	High K	22				°C/W
R θ JC	Low K	28				°C/W

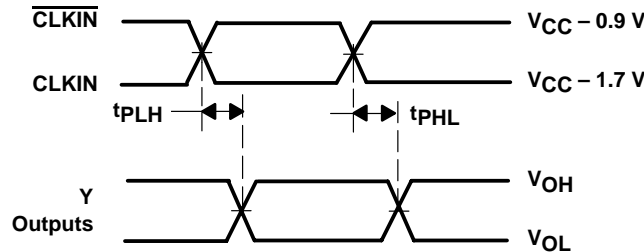
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT (See Note B)



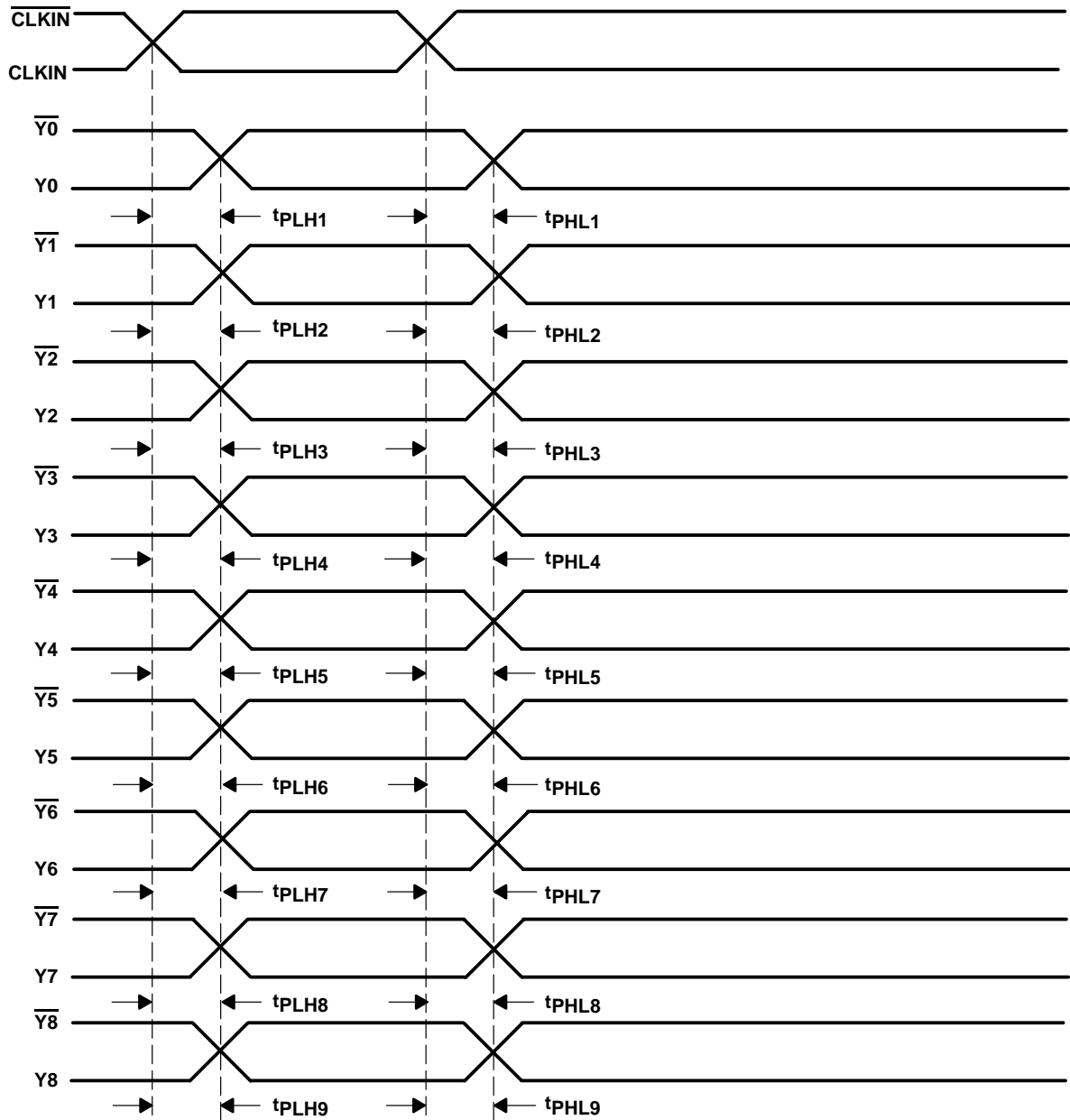
VOLTAGE WAVEFORMS
RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

- NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR \leq 45 MHz, $Z_O = 50 \Omega$, $t_r \leq 1$ ns, $t_f \leq 1$ ns.
 B. For additional signal interface, see the *Interfacing Between LVPECL, LVDS, and CML* application note, Literature Number SCAA056.

Figure 1. Load Circuit and Voltage Waveforms



- NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest t_{PLHn} ($n = 1, 2, \dots, 9$)
 - The difference between the fastest and slowest t_{PHLn} ($n = 1, 2, \dots, 9$)
- B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest t_{PLHn} ($n = 1, 2, \dots, 9$)
 - The difference between the fastest and slowest t_{PHLn} ($n = 1, 2, \dots, 9$) across multiple devices
- C. For additional information on skew and propagation delay parameters, see the *Defining Skew, Propagation Delay, Phase-Offset (Phase Error)* application note, literature number SCAA055.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(pr)}$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCVF111FN	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF111	Samples
CDCVF111FNG4	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF111	Samples
CDCVF111FNR	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF111	Samples
CDCVF111FNRG4	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF111	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF111FNR	PLCC	FN	28	750	330.0	24.4	12.95	12.95	5.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF111FNR	PLCC	FN	28	750	346.0	346.0	41.0

FN 28

GENERIC PACKAGE VIEW
PLCC - 4.57 mm max height
PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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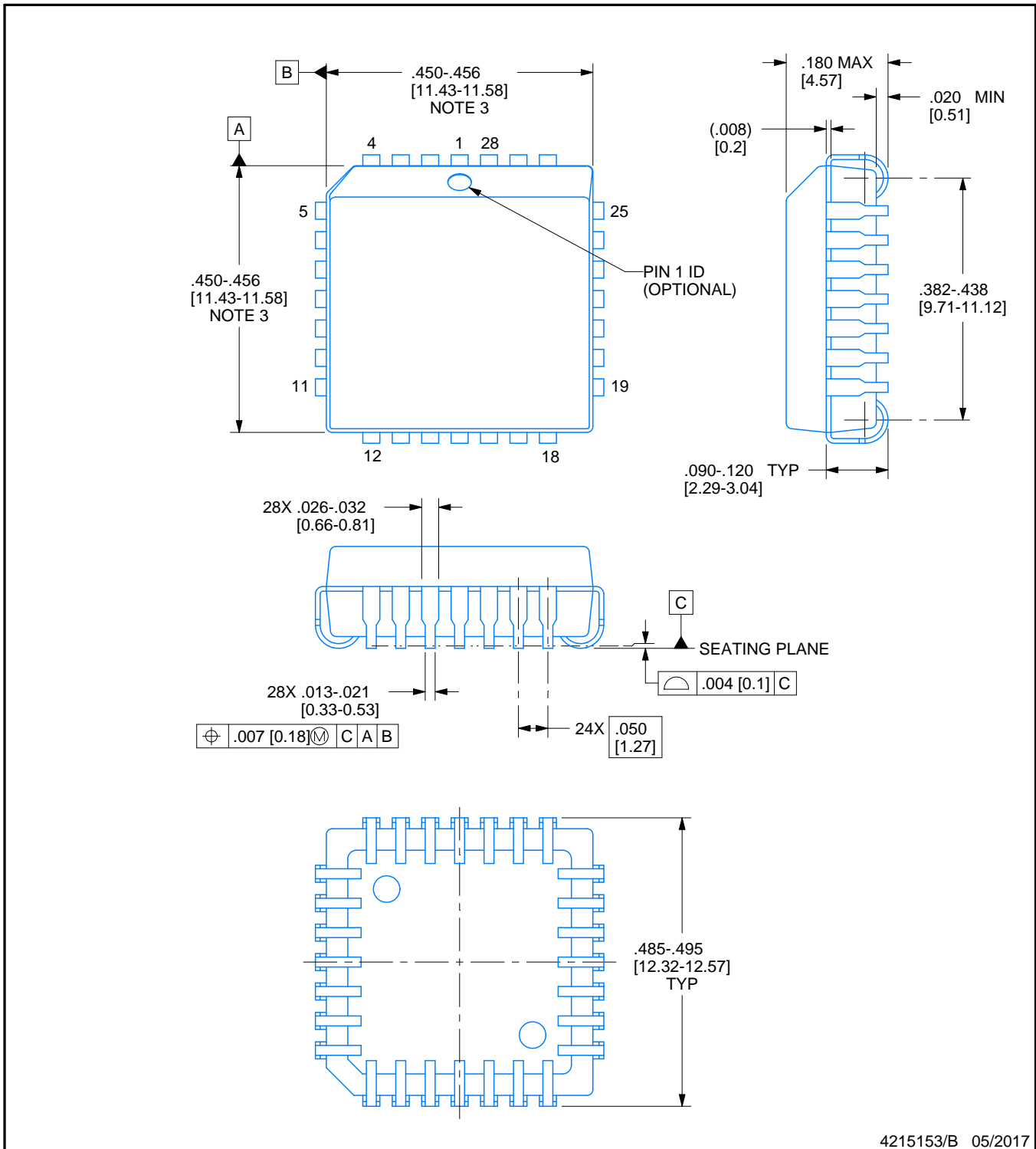


PACKAGE OUTLINE

FN0028A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



4215153/B 05/2017

NOTES:

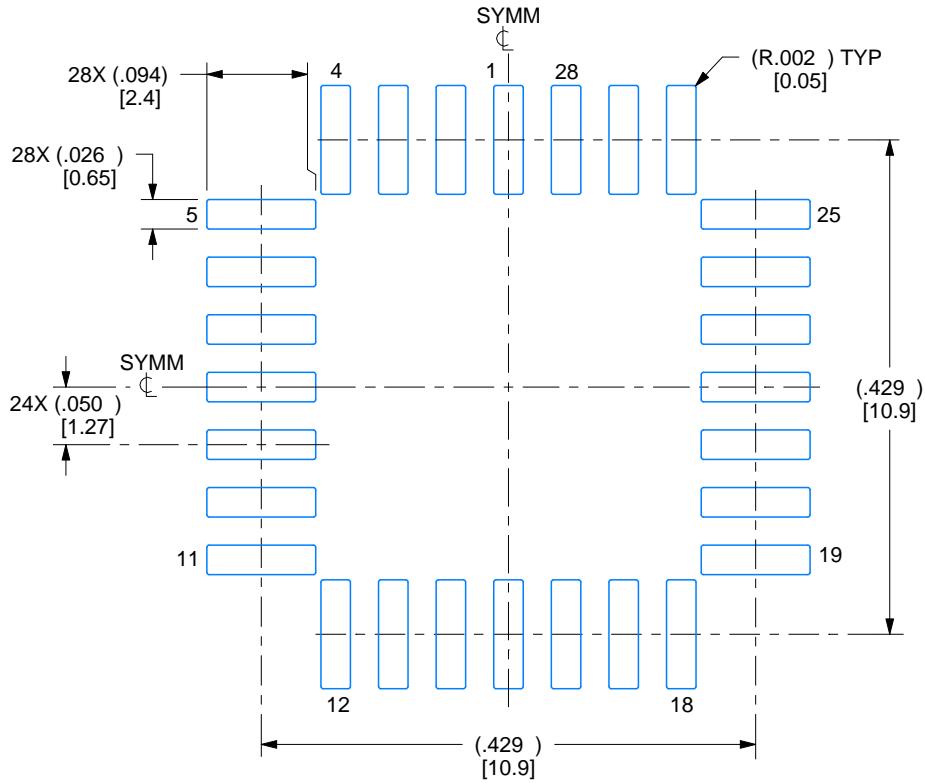
1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.

EXAMPLE BOARD LAYOUT

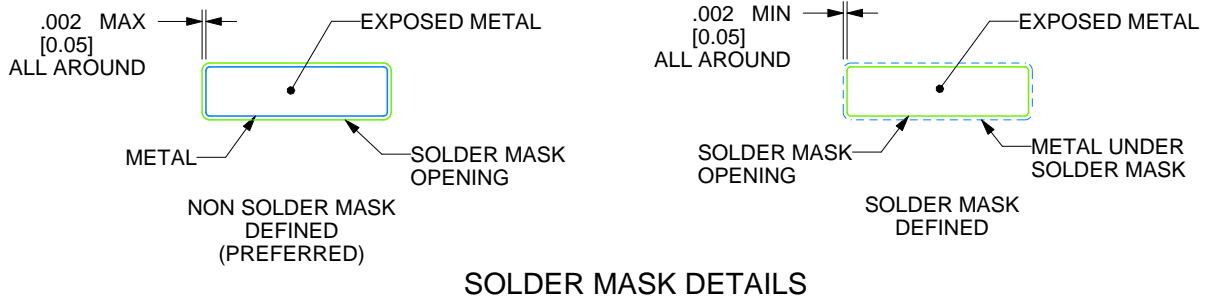
FN0028A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

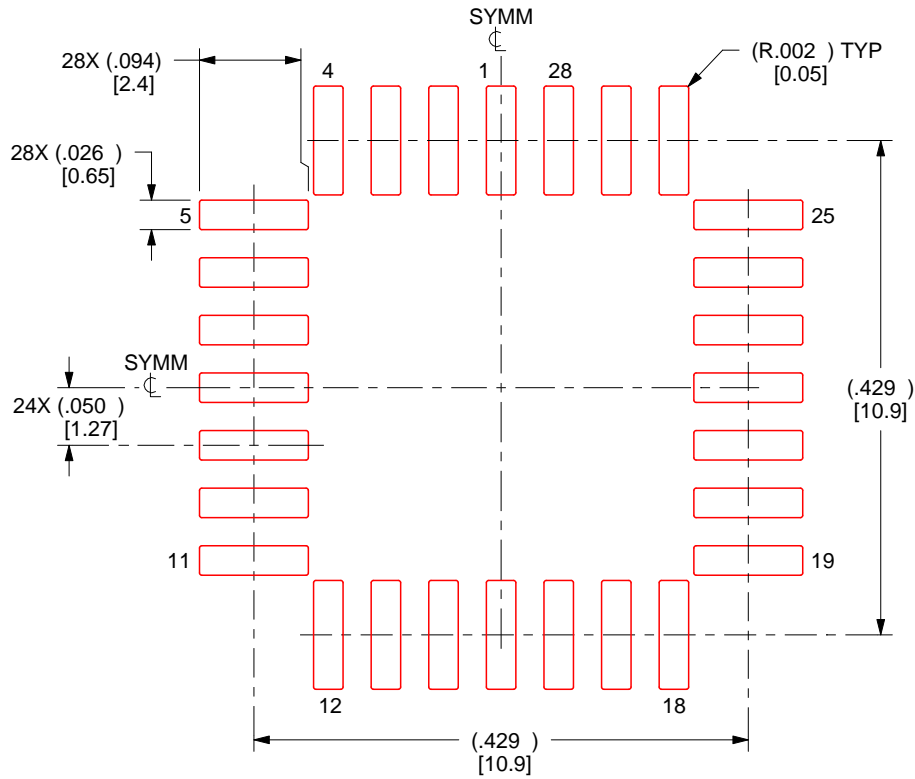
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

FN0028A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215153/B 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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