THE DATASHEET OF

LTC6803HG-1#TRPBF

Multicell Battery Stack Monitor

FEATURES

- **Measures Up to 12 Battery Cells in Series**
- **Stackable Architecture**
- **Supports Multiple Battery Chemistries and Supercapacitors**
- **Serial Interface Daisy Chains to Adjacent Devices**
- **0.25% Maximum Total Measurement Error**
- **Engineered for ISO26262 Compliant Systems**
- 13ms to Measure All Cells in a System
- Passive Cell Balancing:
  - Integrated Cell Balancing MOSFETs
  - Ability to Drive External Balancing MOSFETs
- Onboard Temperature Sensor and Thermistor Inputs
- 1MHz Serial Interface with Packet Error Checking
- Safe with Random Connection of Cells
- Built-In Self Tests
- Delta-Sigma Converter With Built-In Noise Filter
- Open-Wire Connection Fault Detection
- 12µA Standby Mode Supply Current
- High EMI Immunity
- 44-Lead SSOP Package

APPLICATIONS

- Electric and Hybrid Electric Vehicles
- High Power Portable Equipment
- Backup Battery Systems
- Electric Bicycles, Motorcycles, Scooters

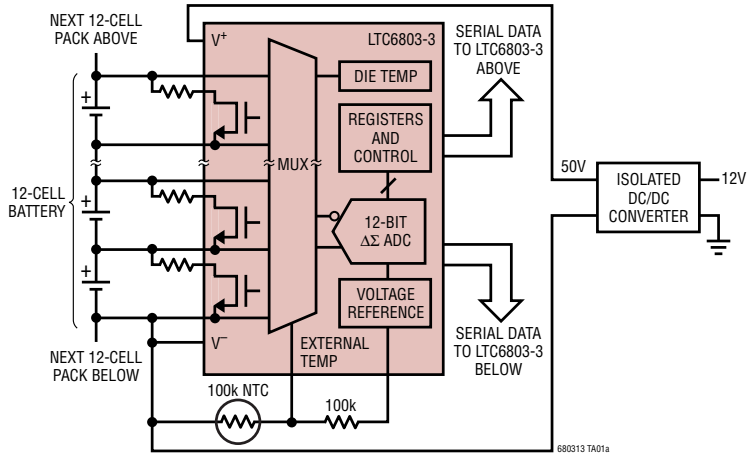
DESCRIPTION

The LTC®6803 is a 2nd generation, complete battery monitoring IC that includes a 12-bit ADC, a precision voltage reference, a high voltage input multiplexer and a serial interface. Each LTC6803 can measure up to 12 series-connected battery cells or supercapacitors. Using a unique level shifting serial interface, multiple LTC6803-1/LTC6803-3 devices can be connected in series, without opto-couplers or isolators, allowing for monitoring of every cell in a long string of series-connected batteries. Each cell input has an associated MOSFET switch for discharging overcharged cells. The LTC6803-1 connects the bottom of the stack to V^- internally. It is pin compatible with the LTC6802-1, providing a drop-in upgrade. The LTC6803-3 separates the bottom of the stack from V^-, improving cell 1 measurement accuracy.

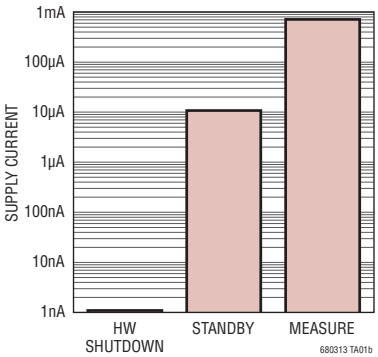
The LTC6803 provides a standby mode to reduce supply current to 12µA. Furthermore, the LTC6803 can be powered from an isolated supply, providing a technique to reduce battery stack current draw to zero.

For applications requiring individually addressable serial communications, see the LTC6803-2/LTC6803-4.

TYPICAL APPLICATION



Supply Current vs Modes of Operation



ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 75V
Input Voltage (Relative to V^-)
- C0 ..... –0.3V to 8V
- C12 ..... –0.3V to 75V
- C*n* (Note 5) ..... –0.3V to Min (8 • *n*, 75V)
- S*n* (Note 5) ..... –0.3V to Min (8 • *n*, 75V)
- CSBO, SCKO, SDOI ..... – 0.3V to 75V
- All Other Pins ..... –0.3V to 7V

Voltage Between Inputs
- C*n* to C*n* – 1 ..... –0.3V to 8V
- S*n* to C*n* – 1 ..... –0.3V to 8V
- C12 to C8 ..... –0.3V to 25V
- C8 to C4 ..... –0.3V to 25V
- C4 to C0 ..... –0.3V to 25V

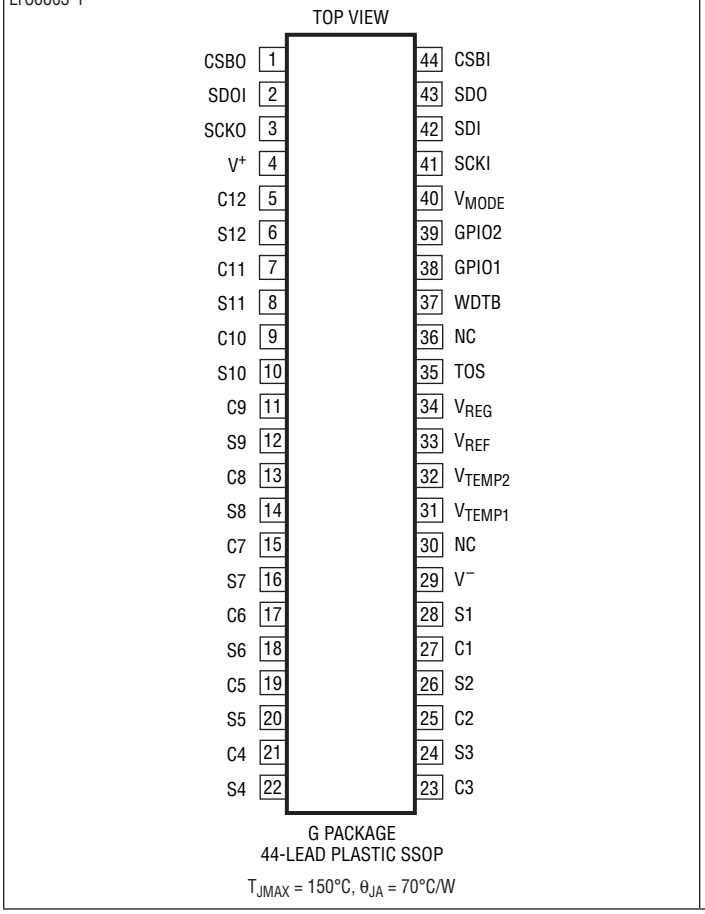
Operating Temperature Range
- LTC6803I ..... –40°C to 85°C
- LTC6803H ..... –40°C to 125°C

Specified Temperature Range
- LTC6803I ..... –40°C to 85°C
- LTC6803H ..... –40°C to 125°C

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Note: *n* = 1 to 12

PIN CONFIGURATION

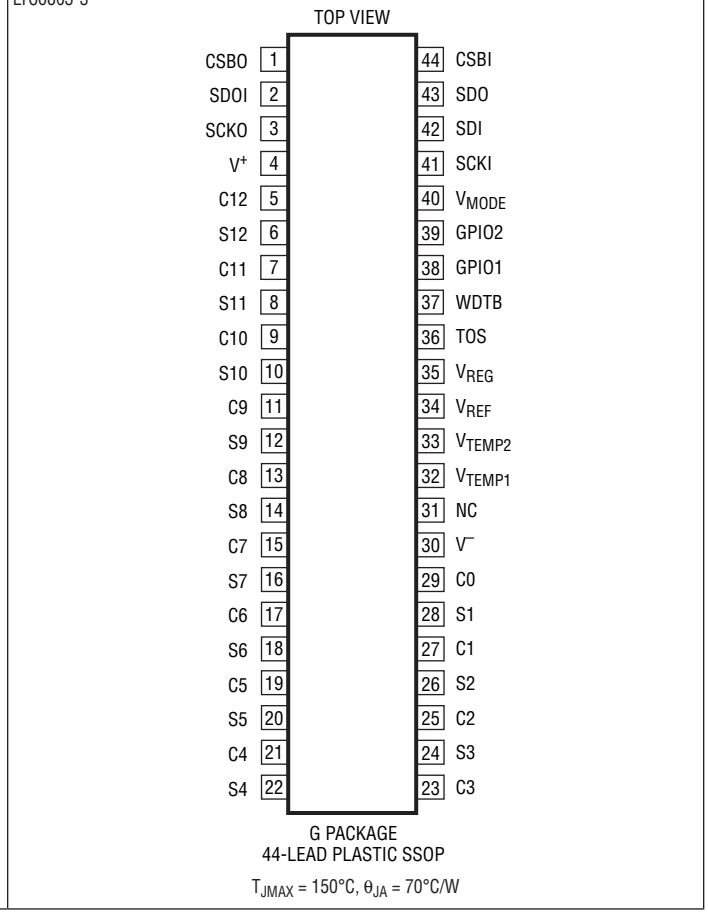
LTC6803-1



G PACKAGE
44-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

LTC6803-3



G PACKAGE
44-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFICED TEMPERATURE RANGE
LTC6803IG-1#PBF	LTC6803IG-1#TRPBF	LTC6803G-1	44-Lead Plastic SSOP	–40°C to 85°C
LTC6803IG-3#PBF	LTC6803IG-3#TRPBF	LTC6803G-3	44-Lead Plastic SSOP	–40°C to 85°C
LTC6803HG-1#PBF	LTC6803HG-1#TRPBF	LTC6803G-1	44-Lead Plastic SSOP	–40°C to 125°C
LTC6803HG-3#PBF	LTC6803HG-3#TRPBF	LTC6803G-3	44-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 43.2V, V^- = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Specifications							
V_S	Supply Voltage, V^+ Relative to V^-	V_{ERR} Specification Met Timing Specification Met	● ●	10 4		55 55	V V
V_{LSB}	Measurement Resolution	Quantization of the ADC	●		1.5		mV/Bit
	ADC Offset	(Note 2)	●	–0.5		0.5	mV
	ADC Gain Error	(Note 2)	 ●	–0.12 –0.22		0.12 0.22	% %
V_{ERR}	Total Measurement Error	(Note4) V_{CELL} = –0.3V V_{CELL} = 2.3V V_{CELL} = 2.3V V_{CELL} = 3.6V V_{CELL} = 3.6V, LTC6803IG V_{CELL} = 3.6V, LTC6803HG V_{CELL} = 4.2V V_{CELL} = 4.2V, LTC6803IG V_{CELL} = 4.2V, LTC6803HG V_{CELL} = 5V 2.3V < V_{TEMP} < 4.2V, LTC6803IG 2.3V < V_{TEMP} < 4.2V, LTC6803HG	 ● ● ● ● ● ● ●	 –2.8 –5.1 –4.3 –7.9 –9 –5 –9.2 –10 –9.2 –10	 ±2.5 ±3 	 2.8 5.1 4.3 7.9 9 5 9.2 10 9.2 10	 mV mV mV mV mV mV mV mV mV mV mV mV
V_{CELL}	Cell Voltage Range	Full-Scale Voltage Range		–0.3		5	V
V_{CM}	Common Mode Voltage Range Measured Relative to V^-	Range of Inputs C*n* < 0.25% Gain Error, *n* = 2 to 11, LTC6803IG	●	1.8		5 • *n*	V
		Range of Inputs C0, C1 < 0.25% Gain Error, LTC6803IG	●	0		5	V
		Range of Inputs C*n* < 0.5% Gain Error, *n* = 2 to 11, LTC6803HG	●	1.8		5 • *n*	V
		Range of Inputs C0, C1 < 0.5% Gain Error, LTC6803HG	●	0		5	V
	Die Temperature Measurement Error	Error in Measurement of 125°C			5		°C
V_{REF}	Reference Pin Voltage	R_{LOAD} = 100k to V^-	 ●	3.020 3.015	3.065 3.065	3.110 3.115	V V
	Reference Voltage Temperature Coefficient				8		ppm/°C
	Reference Voltage Thermal Hysteresis	25°C to 85°C and 25°C to –40°C			100		ppm
	Reference Voltage Long-Term Drift				60		ppm/$\sqrt{kHr}$

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 43.2V, V^- = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF2}	2nd Reference Voltage			2.25	2.5	2.75	V
			●	2.1	2.5	2.9	V
V_{REG}	Regulator Pin Voltage	10V < V^+ < 50V, No Load	●	4.5	5.0	5.5	V
		I_{LOAD} = 4mA	●	4.5	5.0		V
	Regulator Pin Short-Circuit Limit		●	8			mA
I_B	Input Bias Current	In/Out of Pins C1 Through C12					
		When Measuring Cell		–10		10	µA
		When Not Measuring Cell			1		nA
I_S	Supply Current, Measure Mode (Note 7)	Current Into the V^+ Pin When Measuring					
		Continuous Measuring (CDC = 2)		620	780	1000	µA
		Continuous Measuring (CDC = 2)	●	600	780	1150	µA
		Measure Every 130ms (CDC = 5)	●	190	250	360	µA
		Measure Every 500ms (CDC = 6)	●	140	175	250	µA
		Measure Every 2 Seconds (CDC = 7)	●	55	70	105	µA
I_{QS}	Supply Current, Standby	Current Into V^+ Pin When In Standby, All Serial Port Pin at Logic "1"		8	12	16.5	µA
		LTC6803IG	●	6	12	18	µA
		LTC6803HG	●	6	12	19	µA
I_{CS}	Supply Current, Serial I/O	Current Into V^+ Pin During Serial Communications, All Serial Port Pins at Logic "0". V_{MODE} = "0", This Current is Added to I_S or I_{QS}		3.1	3.9	4.3	mA
		LTC6803IG	●	3	3.9	4.5	mA
		LTC6803HG	●	3	3.9	4.9	mA
I_{SD}	Supply Current, Hardware Shutdown	Current Out of V^-, V_{C12} = 43.2V, V^+ Floating (Note 8)	●		0.001	1	µA
	Discharge Switch-On Resistance	V_{CELL} > 3V (Note 3)	●	10		20	Ω
I_{OW}	Current Used for Open-Wire Detection		●	70	110	140	µA
	Thermal Shutdown Temperature				145		°C
	Thermal Shutdown Hysteresis				5		°C
Voltage Mode Timing Specifications							
t_{CYCLE}	Measurement Cycling	Time Required to Measure 12 Cells	●	11	13	15	ms
		Time Required to Measure 10 Cells	●	9	11	13	ms
		Time Required to Measure 3 Temperatures	●	2.8	3.4	4.1	ms
		Time Required to Measure 1 Cell or Temperature	●	1.0	1.2	1.4	ms
t_1	SDI Valid to SCKI Rising Setup		●	10			ns
t_2	SDI Valid to SCKI Rising Hold		●	250			ns
t_3	SCKI Low		●	400			ns
t_4	SCKI High		●	400			ns
t_5	CSBI Pulse Width		●	400			ns
t_6	CSBI Falling to SCKI Rising		●	100			ns
t_7	CSBI Falling to SDO Valid		●	100			ns
t_8	SCKI Falling to SDO Valid		●			250	ns
	Clock Frequency		●			1	MHz
	Watchdog Timer Timeout Period		●	1		2.5	Seconds
Timing Specifications							
t_{PD1}	CSBI to CSBO	C_{CSBO} = 150pF	●			600	ns
t_{PD2}	SCKI to SCKO	C_{SCKO} = 150pF	●			300	ns
t_{PD3}	SDI to SDOI Write Delay	C_{SDOI} = 150pF	●			300	ns
t_{PD4}	SDI to SDOI Read Delay	C_{SDO} = 150pF	●			300	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 43.2V, V^- = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Mode Digital I/O							
V_{IH}	Digital Input Voltage High	Pins SCKI, SDI and CSBI	●	2			V
V_{IL}	Digital Input Voltage Low	Pins SCKI, SDI and CSBI	●			0.8	V
V_{OL}	Digital Output Voltage Low	Pin SDO, Sinking 500µA	●			0.3	V
I_{IN}	Digital Input Current	V_{MODE}, TOS, SCKI, SDI, CSBI	●			10	µA
Current Mode Digital I/O							
I_{IH1}	Digital Input Current High	Pins CSBI, SCKI, SDI (Write, Pin Sourcing)	●		3	10	µA
I_{IL1}	Digital Input Current Low	CSBI, SCKI, SDI (Write, Pin Sourcing)	●	1000			µA
I_{IH2}	Digital Input Current High	SDOI (Read, Pin Sinking)	●	1000			µA
I_{IL2}	Digital Input Current Low	SDOI (Read, Pin Sinking)	●			10	µA
I_{OH1}	Digital Output Current High	CSBO, SCKO, SDOI (Write, Pin Sinking)	●		3	10	µA
I_{OL1}	Digital Output Current Low	CSBO, SCKO, SDOI(Write, Pin Sinking)	●	1000	1300	1600	µA
I_{OH2}	Digital Output Current High	SDI (Read, Pin Sourcing)	●	1000	1300	1600	µA
I_{OL2}	Digital Output Current Low	SDI (Read, Pin Sourcing)	●		3	10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ADC specifications are guaranteed by the Total Measurement Error (V_{ERR}) specification.

Note 3: Due to the contact resistance of the production tester, this specification is tested to relaxed limits. The 20Ω limit is guaranteed by design.

Note 4: V_{CELL} refers to the voltage applied across C*n* to C*n* – 1 for *n* = 1 to 12. V_{TEMP} refers to the voltage applied from V_{TEMP1} or V_{TEMP2} to V^-.

Note 5: These absolute maximum ratings apply provided that the voltage between inputs do not exceed the absolute maximum ratings.

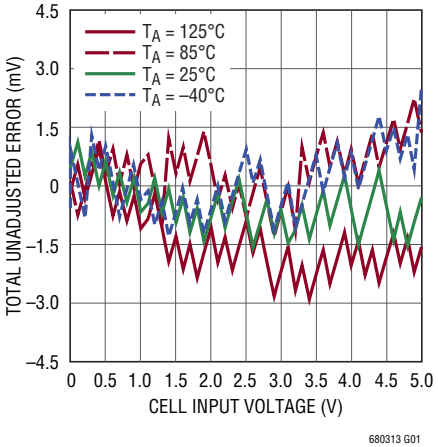
Note 6: Supply current is tested during continuous measuring. The supply current during periodic measuring (130ms, 500ms, 2s) is guaranteed by design.

Note 7: The CDC = 5, 6 and 7 supply currents are not measured. They are guaranteed by the CDC = 2 supply current measurement.

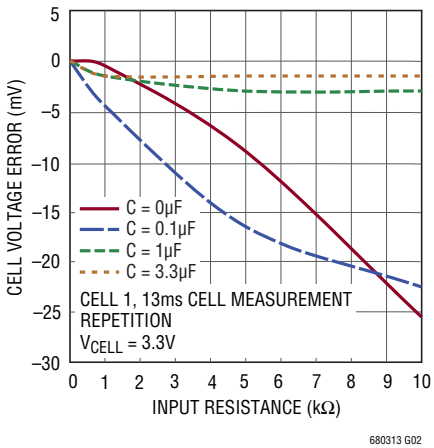
Note 8: Limit is determined by high speed automated test capability.

TYPICAL PERFORMANCE CHARACTERISTICS

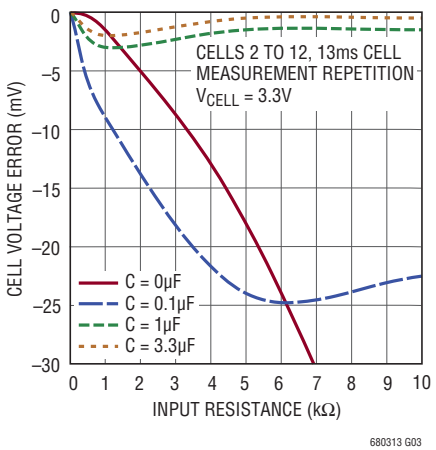
Cell Measurement Error vs Cell Input Voltage



Cell Measurement Error vs Input RC Values

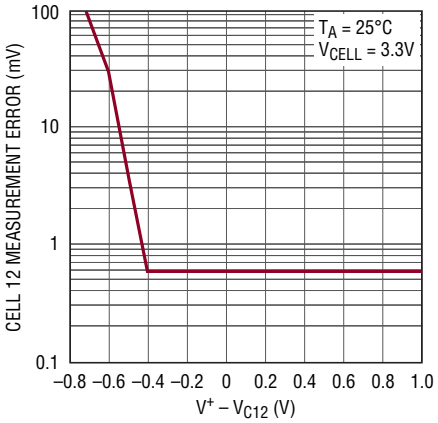


Cell Measurement Error vs Input RC Values



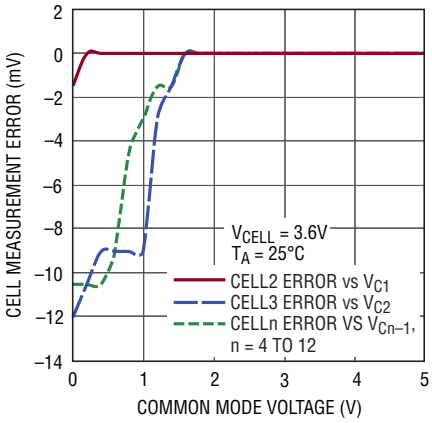
TYPICAL PERFORMANCE CHARACTERISTICS

Cell 12 Measurement Error vs V+



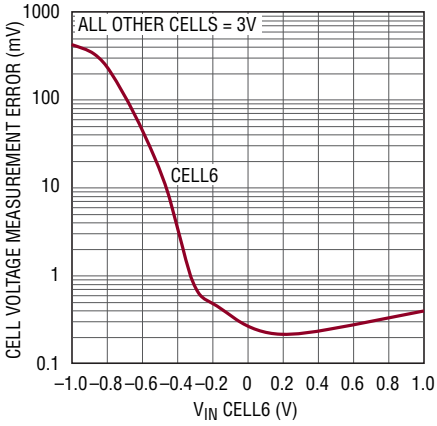
680313 G04

Cell Voltage Measurement Error vs Common Mode Voltage



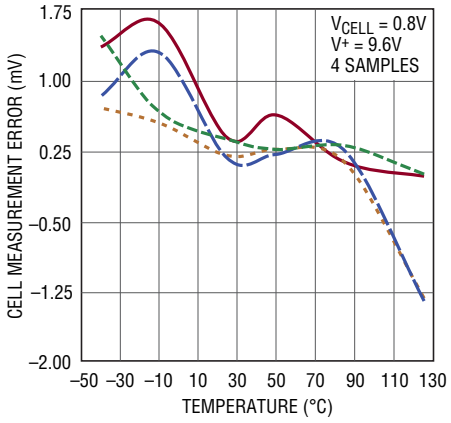
680313 G05

Cell Measurement Error vs Cell Voltage



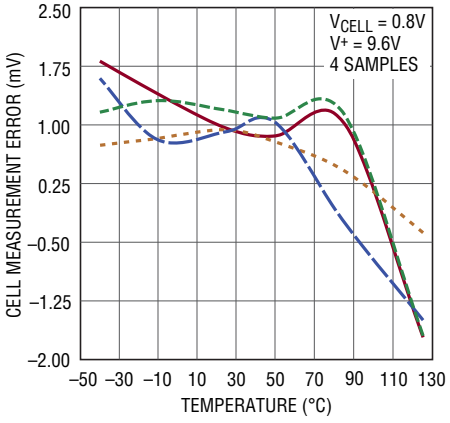
680313 G06

Cell 1 Voltage Measurement Error vs Temperature



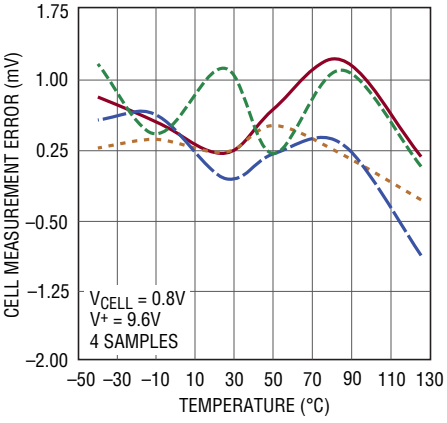
680313 G07

Cell 2 Voltage Measurement Error vs Temperature



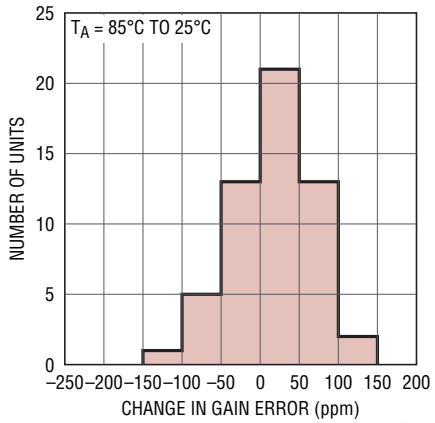
680313 G08

Cell 3 to Cell 12 Voltage Measurement Error vs Temperature



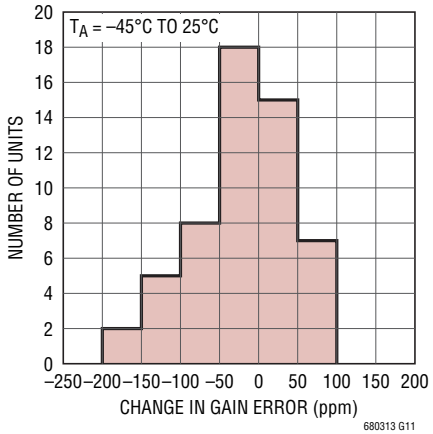
680313 G09

Measurement Gain Error Hysteresis



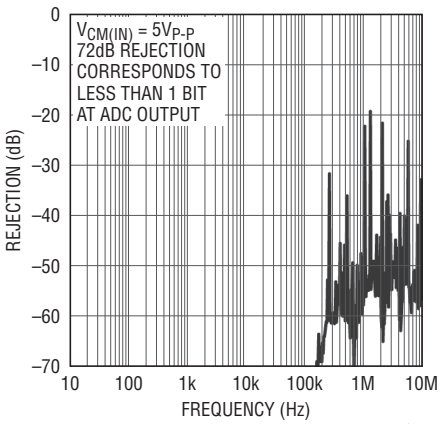
680313 G10

Measurement Gain Error Hysteresis



680313 G11

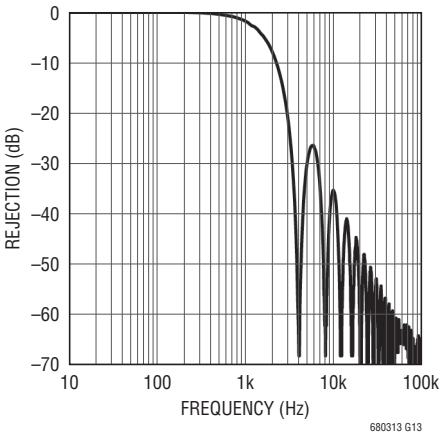
Cell Measurement Common Mode Rejection



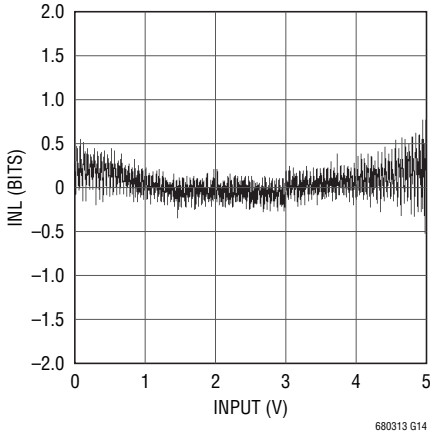
680313 G12

TYPICAL PERFORMANCE CHARACTERISTICS

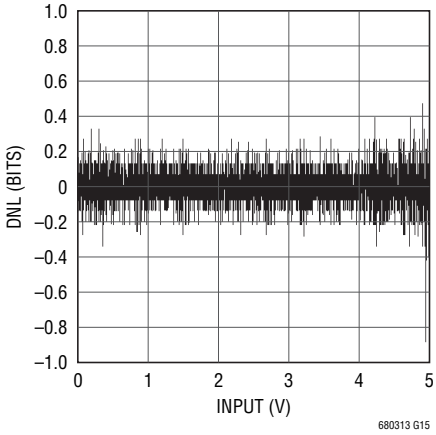
ADC Normal Mode Rejection vs Frequency



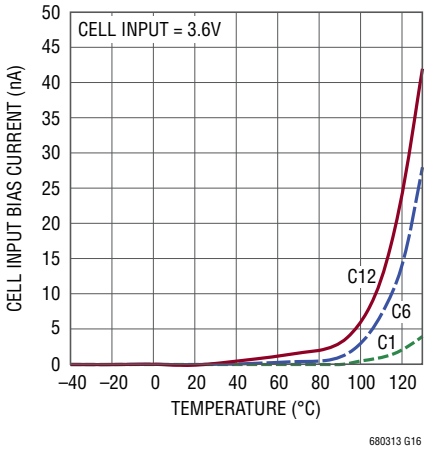
ADC INL



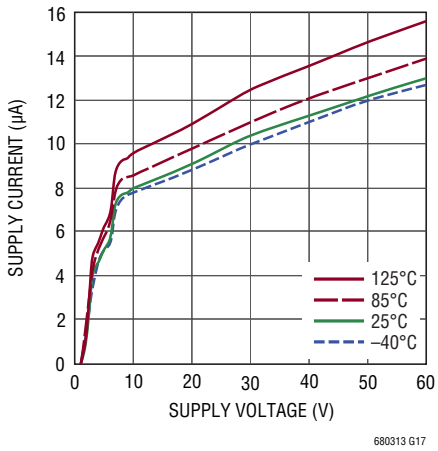
ADC DNL



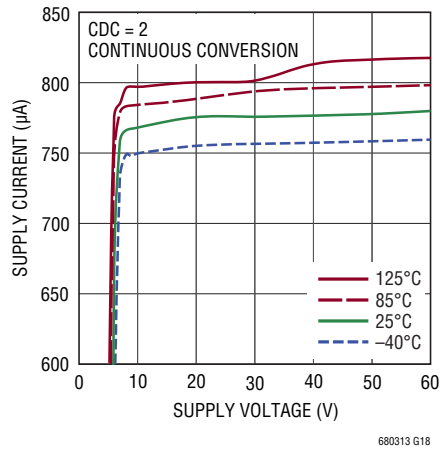
Cell Input Bias Current During Standby and Hardware Shutdown



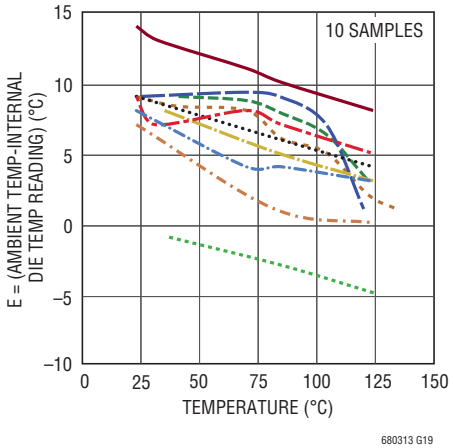
Standby Supply Current vs Supply Voltage



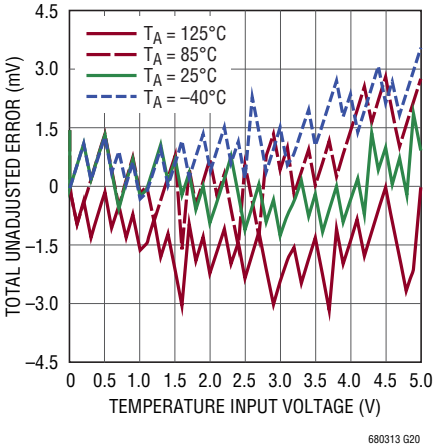
Supply Current vs Supply Voltage During Continuous Conversions



Internal Die Temperature Measurement Error Using an 8mV/°K Scale Factor

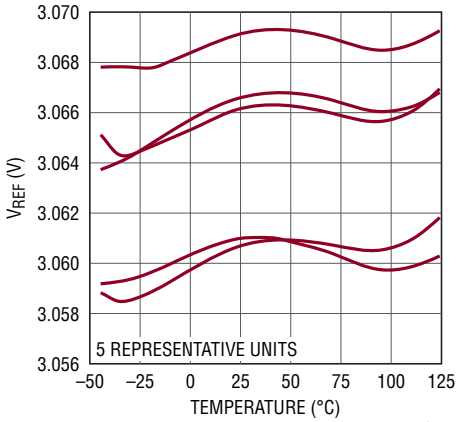


External Temperature Measurement Total Unadjusted Error vs Input

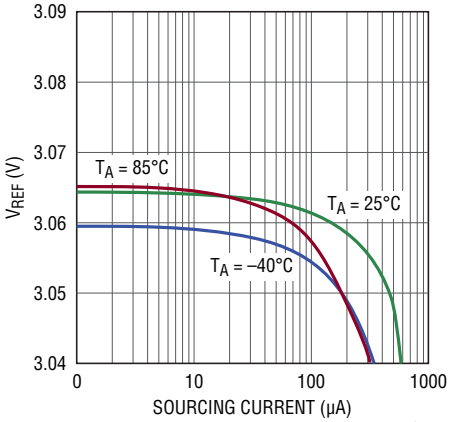


TYPICAL PERFORMANCE CHARACTERISTICS

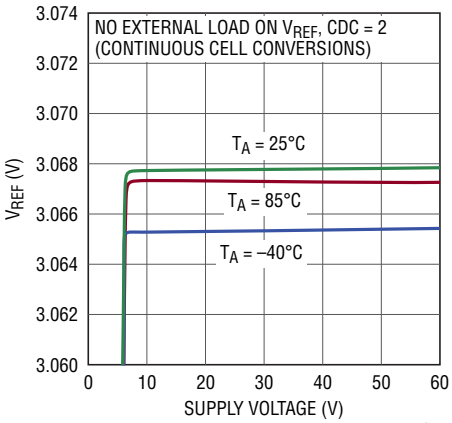
V_{REF} Output Voltage vs Temperature



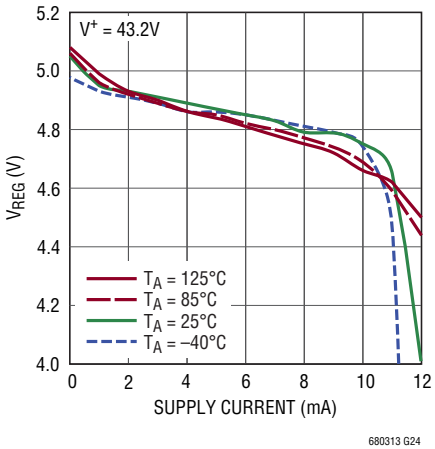
V_{REF} Load Regulation



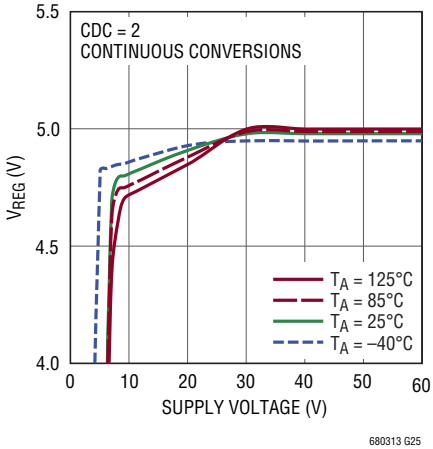
V_{REF} Line Regulation



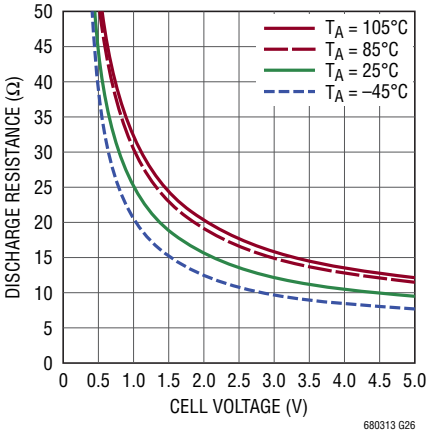
V_{REG} Load Regulation



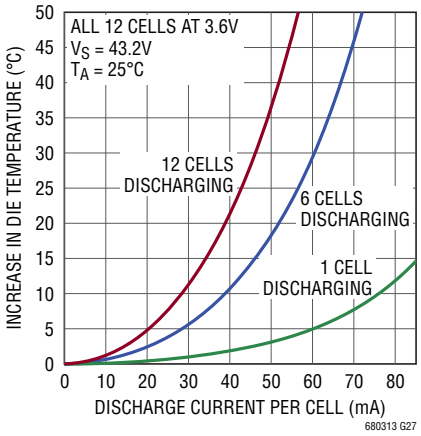
V_{REG} Line Regulation



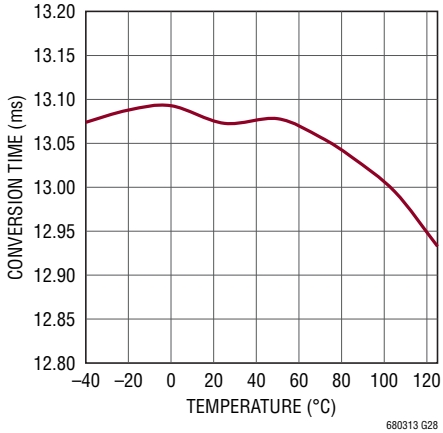
Internal Discharge Resistance vs Cell Voltage



Die Temperature Increase vs Discharge Current in Internal FET



Cell Conversion Time



PIN FUNCTIONS

To ensure pin compatibility with the LTC6802-1, the LTC6803-1 is configured such that the bottom cell input (C0) is connected internally to the negative supply voltage (V^-). The LTC6803-3 offers a unique pinout with an input for the bottom cell (C0). This simple functional difference offers the possibility for enhanced cell 1 measurement accuracy, enhanced SPI noise tolerance and simplified wiring. More information is provided in the applications section entitled Advantages of Kelvin Connections for C0.

CSBO (Pin 1): Chip Select Output (Active Low). CSBO is a buffered version of the chip select input, CSBI. CSBO drives the next IC in the daisy chain. See Serial Port in the Applications Information section.

SDOI (Pin 2): Serial Data I/O Pin. SDOI transfers data to and from the next IC in the daisy chain. See Serial Port in the Applications Information section.

SCKO (Pin 3): Serial Clock Output. SCKO is a buffered version of SCKI. SCKO drives the next IC in the daisy chain. See Serial Port in the Applications Information section.

V^+ (Pin 4): Positive Power Supply. Pin 4 can be tied to the most positive potential in the battery stack or an isolated power supply. V^+ must be greater than the most positive potential in the battery stack under normal operation. With an isolated power supply, LTC6803 can be turned off by simply shutting down V^+.

C12, C11, C10, C9, C8, C7, C6, C5, C4, C3, C2, C1 (Pins 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27): C1 through C12 are the inputs for monitoring battery cell voltages. The negative terminal of the bottom cell is tied to pin V^- for LTC6803-1, pin C0 for LTC6803-3 . The next lowest potential is tied to C1 and so forth. See the figures in the Applications Information section for more details on connecting batteries to the LTC6803-1 and LTC6803-3. The LTC6803 can monitor a series connection of up to 12 cells. Each cell in a series connection must have a common mode voltage that is greater than or equal to the cells below it. 100mV negative voltages are permitted.

S12, S11, S10, S9, S8, S7, S6, S5, S4, S3, S2, S1 (Pins 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28): S1 though S12 pins are used to balance battery cells. If one cell in a series becomes overcharged, an S output can be used to discharge the cell. Each S output has an internal N-channel MOSFET for discharging. See the Block Diagram. The NMOS has a maximum on resistance of 20Ω. An external resistor should be connected in series with the NMOS to dissipate heat outside of the LTC6803 package. When using the internal MOSFETs to discharge cells, the die temperature should be monitored. See Power Dissipation and Thermal Shutdown in the Applications Information section. The S pins also feature an internal pull-up PMOS. This allows the S pins to be used to drive the gates of external MOSFETs for higher discharge capability.

C0 (Pin 29 on LTC6803-3): Negative Terminal of the Bottom Battery Cell. C0 and V^- form Kelvin connections to eliminate effect of voltage drop at the V^- trace.

V^- (Pin 29 on LTC6803-1/ Pin 30 on LTC6803-3): Connect V^- to the most negative potential in the series of cells.

NC (Pin 30 on LTC6803-1/Pin 31 on LTC6803-3): This pin is not used and is internally connected to V^- through 10Ω. It can be left unconnected or connected to V^- on the PCB.

V_{TEMP1}, V_{TEMP2} (Pins 31, 32 on LTC6803-1/ Pins 32, 33 on LTC6803-3): Temperature Sensor Inputs. The ADC measures the voltage on V_{TEMPn} with respect to V^- and stores the result in the TMP registers. The ADC measurements are relative to the V_{REF} pin voltage. Therefore a simple thermistor and resistor combination connected to the V_{REF} pin can be used to monitor temperature. The V_{TEMP} inputs can also be general purpose ADC inputs. Any voltage from 0V to 5.125V referenced to V^- can be measured.

V_{REF} (Pin 33 on LTC6803-1/ Pin 34 on LTC6803-3): 3.065V Voltage Reference Output. This pin should be bypassed with a 1µF capacitor. The V_{REF} pin can drive a 100k resistive load connected to V^-. Larger loads should be buffered with an LT6003 op amp, or similar device.

PIN FUNCTIONS

V_{REG} (Pin 34 on LTC6803-1/Pin 35 on LTC6803-3): Linear Voltage Regulator Output. This pin should be bypassed with a 1µF capacitor. The V_{REG} pin is capable of supplying up to 4mA to an external load. The V_{REG} pin does not sink current.

TOS (Pin 35 on LTC6803-1/Pin 36 on LTC6803-3): Top of Stack Input. Tie TOS to V_{REG} when the LTC6803-1 or LTC6803-3 is the top device in a daisy chain. Tie TOS to V^- otherwise. When TOS is tied to V_{REG}, the LTC6803-1 or LTC6803-3 ignores the SDOI input and SCKO, CSBO are turned off. When TOS is tied to V^-, the LTC6803-1 or LTC6803-3 expects data to be passed to and from the SDOI pin.

NC (Pin 36 on LTC6803-1): No Connection.

WDTB (Pin 37): Watchdog Timer Output (Active Low). If there is no valid command received for 1 to 2.5 seconds, the WDTB output is asserted. The WDTB pin is an open-drain NMOS output. When asserted it pulls the output down to V^- and resets the configuration register to its default state.

GPIO1, GPIO2 (Pins 38, 39): General Purpose Input/Output. By writing a "0" to a GPIO configuration register bit, the open-drain output is activated and the pin is pulled to V^-. By writing logic "1" to the configuration register bit, the corresponding GPIO pin is high impedance. An external resistor is required to pull the pin up to V_{REG}. By reading the configuration register locations GPIO1 and GPIO2, the state of the pins can be determined. For example, if a "0" is written to register bit GPIO1, a "0" is always read back because the output N-channel MOSFET pulls Pin 38 to V^-. If a "1" is written to register bit GPIO1, the pin becomes high impedance. Either a "1" or a "0" is read back, depending on the voltage present at Pin 38. The GPIOs makes it possible to turn on/off circuitry around the LTC6803, or read logic values from a circuit around the LTC6803. The GPIO pins should be connected to V^- if not used.

V_{MODE} (Pin 40): Voltage Mode Input. When V_{MODE} is tied to V_{REG}, the SCKI, SDI, SDO and CSBI pins are configured as voltage inputs and outputs. This means these pins accept standard TTL logic levels. Connect V_{MODE} to V_{REG} when the LTC6803-1 or LTC6803-3 is the bottom device in a daisy chain. When V_{MODE} is connected to V^-, the SCKI, SDI and CSBI pins are configured as current inputs and outputs, and SDO is unused. Connect V_{MODE} to V^- when the LTC6803-1 or LTC6803-3 is being driven by another LTC6803-1 or LTC6803-3 in a daisy chain.

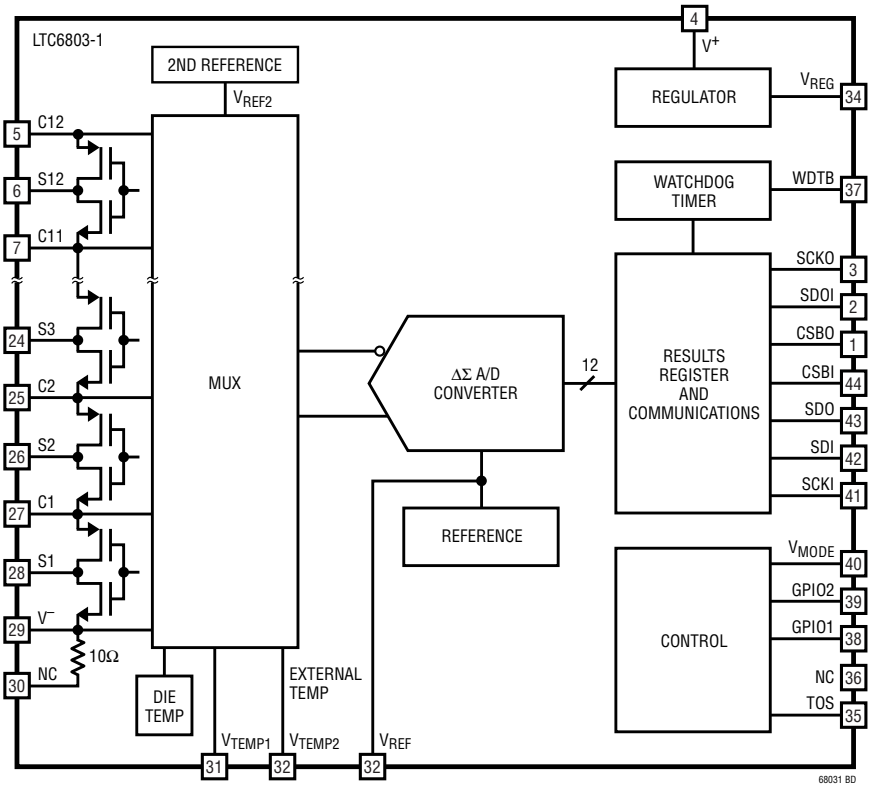
SCKI (Pin 41): Serial Clock Input. The SCKI pin interfaces to any logic gate (TTL levels) if V_{MODE} is tied to V_{REG}. SCKI must be driven by the SCKO pin of another LTC6803-1 or LTC6803-3 if V_{MODE} is tied to V^-. See Serial Port in the Applications Information Section.

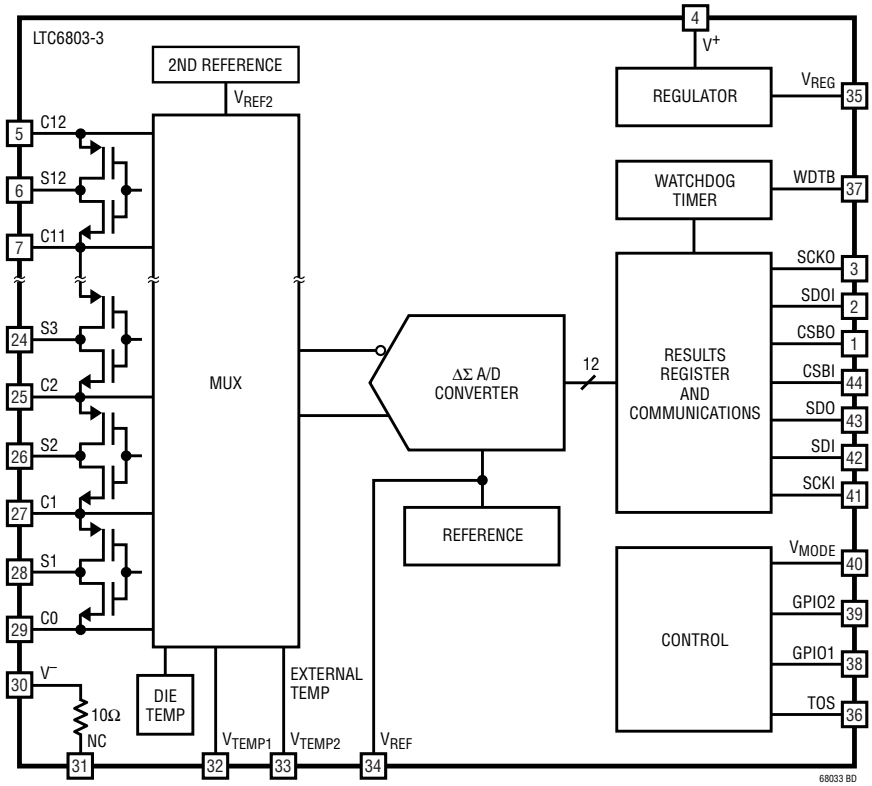
SDI (Pin 42): Serial Data Input. The SDI pin interfaces to any logic gate (TTL levels) if V_{MODE} is tied to V_{REG}. SDI must be driven by the SDOI pin of another LTC6803-1 or LTC6803-3 if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

SDO (Pin 43): Serial Data Output. The SDO pin is an NMOS open-drain output if V_{MODE} is tied to V_{REG}. A pull-up resistor is needed on SDO. SDO is not used if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

CSBI (Pin 44): Chip Select (Active Low) Input. The CSBI pin interfaces to any logic gate (TTL levels) if V_{MODE} is tied to V_{REG}. CSBI must be driven by the CSBO pin of another LTC6803-1 or LTC6803-3 if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

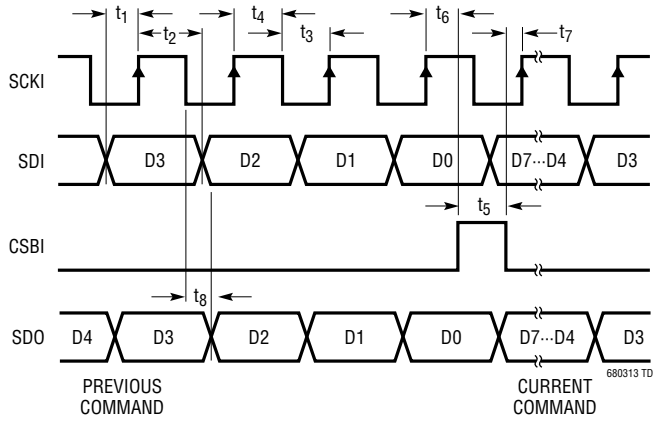
BLOCK DIAGRAMS





TIMING DIAGRAM

Timing Diagram of the Serial Interface



OPERATION

THEORY OF OPERATION

The LTC6803 is a data acquisition IC capable of measuring the voltage of 12 series connected battery cells. An input multiplexer connects the batteries to a 12-bit delta-sigma analog-to-digital converter (ADC). An internal 8ppm/°C voltage reference combined with the ADC give the LTC6803 its outstanding measurement accuracy. The inherent benefits of the delta-sigma ADC versus other types of ADCs (e.g., successive approximation) are explained in Advantages of Delta-Sigma ADCs in the Applications Information section.

Communication between the LTC6803 and a host processor is handled by an SPI compatible serial interface. As shown in Figure 1, the LTC6803-1s or LTC6803-3s can pass data up and down a stack of devices using simple diodes for isolation. This operation is described in Serial Port in the Applications Information section.

The LTC6803 also contains circuitry to balance cell voltages. Internal MOSFETs can be used to discharge cells. These internal MOSFETs can also be used to control external balancing circuits. Figure 1 illustrates cell balancing by internal discharge. Figure 12 shows the S pin controlling an external balancing circuit. It is important to note that the LTC6803 makes no decisions about turning on/off the internal MOSFETs. This is completely controlled by the host processor. The host processor writes values to a configuration register inside the LTC6803 to control the switches. The watchdog timer inside the LTC6803 will turn off the discharge switches if communication with the host processor is interrupted.

The LTC6803 has three modes of operation: hardware shutdown, standby and measure. Hardware shutdown is a true zero power mode. Standby mode is a power saving state where all circuits except the serial interface are turned off. In measure mode, the LTC6803 is used to measure cell voltages and store the results in memory. Measure mode will also monitor each cell voltage for overvoltage (OV) and undervoltage (UV) conditions.

HARDWARE SHUTDOWN MODE

The V^+ pin can be disconnected from the C pins and the battery pack. If the V^+ supply pin is 0V, the LTC6803 will typically draw less than 1nA from the battery cells. All circuits inside the IC are off. It is not possible to communicate with the IC when V^+ = 0V. See the Applications Information section for hardware shutdown circuits.

STANDBY MODE

The LTC6803 defaults (powers up) to standby mode. Standby mode is the lowest supply current state with a supply connected. Standby current is typically 12µA

OPERATION

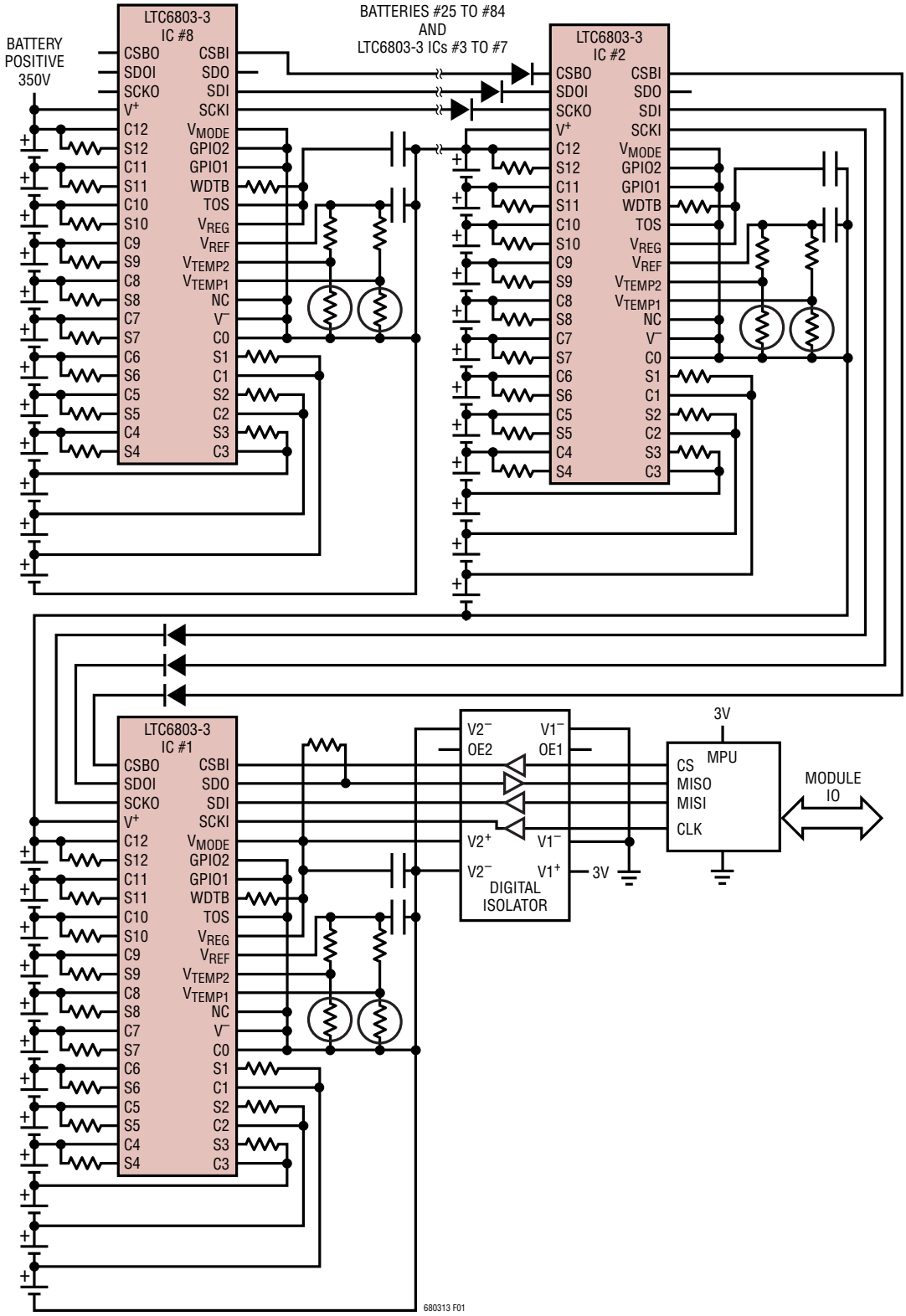


Figure 1. 96-Cell Battery Stack, Daisy-Chain Interface. This is a Simplified Schematic Showing the Basic Multi-IC Architecture

OPERATION

when V^+ = 44V. All circuits are turned off except the serial interface and the voltage regulator. For the lowest possible standby current consumption all SPI logic inputs should be set to logic 1 level. The LTC6803 can be programmed for standby mode by setting the comparator duty cycle configuration bits, CDC[2:0], to 0. If the part is put into standby mode while ADC measurements are in progress, the measurements will be interrupted and the cell voltage registers will be in an indeterminate state. To exit standby mode, the CDC bits must be written to a value other than 0.

MEASURE MODE

The LTC6803 is in measure mode when the CDC bits are programmed with a value from 1 to 7. When CDC = 1 the LTC6803 is on and waiting for a start ADC conversion command. When CDC is 2 through 7 the IC monitors each cell voltage and produces an interrupt signal on the SDO pin indicating all cell voltages are within the UV and OV limits. The value of the CDC bits determines how often the cells are monitored, and how much average supply current is consumed.

There are two methods for indicating the UV/OV interrupt status: toggle polling (using a 1kHz output signal) and level polling (using a high or low output signal). The polling methods are described in the Serial Port section. The UV/OV limits are set by the V_{UV} and V_{OV} values in the configuration registers. When a cell voltage exceeds the UV/OV limits a bit is set in the flag register. The UV and OV flag status for each cell can be determined using the *Read Flag Register Group*.

An ADC measurement can be requested at any time when the IC is in measure mode. To initiate cell voltage measurements while in measure mode, a Start A/D Conversion is sent. After the command has been sent, the LTC6803 will indicate the A/D converter status via toggle polling or level polling (as described in the Serial Port section). During cell voltage measurement commands, the UV and OV flags (within the flag register group) are also updated. When the measurements are complete, the part will continue monitoring UV and OV conditions at the rate designated by the CDC bits. Note that there is a 5µs window during each UV/OV comparison cycle where an ADC measurement request may be missed. This is an unlikely event. For example, the comparison cycle is 2 seconds when CDC = 7. Use the CLEAR command to detect missing ADC commands.

Operating with Less than 12 Cells

If fewer than 12 cells are connected to the LTC6803, the unused input channels must be masked. The MCxI bits in the configuration registers are used to mask channels. In addition, the LTC6803 can be configured to automatically bypass the measurements of the top 2 cells, reducing power consumption and measurement time. If the CELL10 bit is high, the inputs for cell 11 and cell 12 are masked and only the bottom 10 cell voltages will be measured. By default, the CELL10 bit is low, enabling measurement of all 12 cell voltages. Additional information regarding operation with less than 12 cells is provided in the applications section.

ADC RANGE AND OUTPUT FORMAT

The ADC outputs a 12-bit code with an offset of 0x200 (512 decimal). The input voltage can be calculated as:

$$V_{IN} = (D_{OUT} - 512) \bullet V_{LSB};\ V_{LSB} = 1.5mV$$

where D_{OUT} is a decimal integer.

For example, a 0V input will have an output reading of 0x200. An ADC reading of 0x000 means the input was –0.768V. The absolute ADC measurement range is –0.768V to 5.376V. The resolution is V_{LSB} = 1.5mV = (5.376 + 0.768)/2^{12}. The useful range is –0.3V to 5V. This range allows monitoring super capacitors, which could have small negative voltage. Inputs below –0.3V exceed the absolute maximum rating of the C pins. If all inputs are negative then the ADC range is reduced to –0.1V. Inputs above 5V will have noisy ADC readings (see Typical Performance Characteristics curves).

ADC MEASUREMENTS DURING CELL BALANCING

The primary cell voltage ADC measurement commands (STCVAD and STOWAD) automatically turn off a cell's discharge switch while its voltage is being measured. The discharge switches for the cell above and the cell below will also be turned off during the measurement. For example, discharge switches S4, S5 and S6 will be off while cell 5 is being measured. The UV/OV comparison conversions in

OPERATION

CDC modes 2 through 7 also cause a momentary turn-off of the discharge switch. For example, switches S4, S5 and S6 will be off while cell 5 is checked for a UV/OV condition.

In some systems it may be desirable to allow discharging to continue during cell voltage measurements. The cell voltage ADC conversion commands STCVDC and STOWDC allow the discharge switches to remain on during cell voltage measurements. This feature allows the system to perform a self test to verify the discharge functionality.

ADC REGISTER CLEAR COMMAND

The clear command can be used to clear the cell voltage registers and temperature registers. The clear command will set all registers to 0xFFF. This command is used to make sure conversions are being made. When cell voltages are stable, ADC results could stay the same. If a start ADC conversion command is sent to the LTC6803 but the PEC fails to match then the command is ignored and the voltage register contents also will not change. Sending a *clear* command then reading back register contents is a way to make sure LTC6803 is accepting commands and performing new measurements. The clear command takes 1ms to execute.

ADC CONVERTER SELF TEST

Two self-test commands can be used to verify the functionality of the digital portions of the ADC. The self tests also verify the cell voltage registers and temperature monitoring registers. During these self tests a test signal is applied to the ADC. If the circuitry is working properly all cell voltage and temperature registers will contain 0x555 or 0xAAA. The time required for the self-test function is the same as required to measure all cell voltages or all temperature sensors.

MULTIPLEXER AND REFERENCE SELF TEST

The LTC6803 uses a multiplexer to measure the 12 battery cell inputs, as well as the temperature signals. A diagnostic command is used to validate the function of the multiplexer, the temperature sensor, and the precision reference circuit. Diagnostic registers will be updated after each diagnostic test. The *muxfail* bit of the registers will be 1 if the multiplexer self test fails.

A constant voltage generated by the 2nd reference circuit will be measured by the ADC and the results written to the diagnostic register. The voltage reading should be 2.5V ±16%. Readings outside this range indicate a failure of the temperature sensor circuit, the precision reference circuit, or the analog portion of the ADC. The DAGN command executes in 16.4ms, which is the sum of the 12-cell t_{CYCLE} and 3 temperature t_{CYCLE}. The diagnostic read command can be used to read the registers.

USING THE GENERAL PURPOSE INPUTS/OUTPUTS (GPIO1, GPIO2)

The LTC6803 has two general purpose digital input/output pins. By writing a GPIO configuration register bit to a logic low, the open-drain output can be activated. The GPIOs give the user the ability to turn on/off circuitry around the LTC6803. One example might be a circuit to verify the operation of the system.

When a GPIO configuration bit is written to a logic high, the corresponding GPIO pin may be used as an input. The read back value of that bit will be the logic level that appears at the GPIO pin.

WATCHDOG TIMER CIRCUIT

The LTC6803 includes a watchdog timer circuit. The watchdog timer is on for all modes except CDC = 0. The watchdog timer times out if no valid command is received for 1 to 2.5 seconds. When the watchdog timer circuit times out, the WDTB open-drain output is asserted low and the configuration register bits are reset to their default (power-up) state. In the power-up state, CDC is 0, the S outputs are off and the IC is in the low power standby mode. The WDTB pin remains low until a valid command is received. The watchdog timer provides a means to turn off cell discharging should communications to the MPU be interrupted. There is no need for the watchdog timer at CDC = 0 since discharging is off. The open-drain WDTB output can be wire ORd with other external open-drain signals. Pulling the WDTB signal low will not initiate a

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watchdog event, but the CNFGO bit 7 will reflect the state of this signal. Therefore, the WDTB pin can be used to monitor external digital events if desired.

SERIAL PORT

Overview

The LTC6803 has an SPI bus compatible serial port. Several devices can be daisy chained in series. There are two sets of serial port pins, designated as low side and high side. The low side and high side ports enable devices to be daisy chained even when they operate at different power supply potentials. In a typical configuration, the positive power supply of the first, bottom device is connected to the negative power supply of the second, top device, as shown in Figure 1. When devices are stacked in this manner, they can be daisy chained by connecting the high side port of the bottom device to the low side port of the top device. With this arrangement, the master writes to or reads from the cascaded devices as if they formed one long shift register. The LTC6803-1/LTC6803-3 translate the voltage level of the signals between the low side and high side ports to pass data up and down the battery stack.

Physical Layer

On the LTC6803-1/LTC6803-3, seven pins comprise the low side and high side ports. The low side pins are CSBI, SCKI, SDI and SDO. The high side pins are CSBO, SCKO and SDOI. CSBI and SCKI are always inputs, driven by the master or by the next lower device in a stack. CSBO and SCKO are always outputs that can drive the next higher device in a stack. SDI is a data input when writing to a stack of devices. For devices not at the bottom of a stack, SDI is a data output when reading from the stack. SDOI is a data output when writing to and a data input when reading from a stack of devices. SDO is an open-drain output that is only used on the bottom device of a stack, where it may be tied with SDI, if desired, to form a single, bi-directional port. The SDO pin on the bottom device of a stack requires a pull-up resistor. For devices up in the stack, SDO should be tied to the local V^- or left floating.

To communicate between daisy-chained devices, the high side port pins of a lower device (CSBO, SCKO and SDOI) should be connected through high voltage diodes to the respective low side port pins of the next higher device (CSBI, SCKI and SDI). In this configuration, the devices communicate using current rather than voltage. To signal a logic high from the lower device to the higher device, the lower device sinks a smaller current from the higher device pin. To signal a logic low, the lower device sinks a larger current. Likewise, to signal a logic high from the higher device to the lower device, the higher device sources a larger current to the lower device pin. To signal a logic low, the higher device sources a smaller current. See Figure 2. Since CSBO, SCKO and SDOI voltages are close to the V^- of high side device, the V^- of the high side device must be at least 5V higher than that of the low side device to guarantee current flows of the current mode interface. It is recommended that high voltage diodes be placed in series with the SPI daisy-chain signals as shown if Figure 1. These diodes prevent reverse voltage stress on the IC if a battery group bus bar is removed. See Battery Interconnection Integrity for additional information.

Standby current consumed in the current mode serial interface is minimized when CSBI, SCKI and SDI are all high.

The voltage mode pin (V_{MODE}) determines whether the low side serial port is configured as voltage mode or current mode. For the bottom device in a daisy-chain stack, this pin must be pulled high (tied to V_{REG}). The other devices in the daisy chain must have this pin pulled low (tied to V^-) to designate current mode communication. To designate the top-of-stack device for polling commands, the TOS

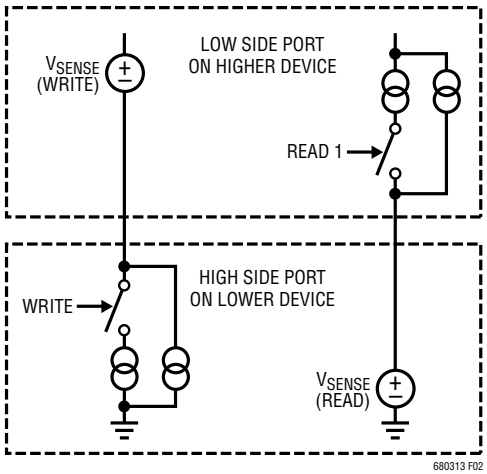

Figure 2. Current Mode Interface

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pin on the top device of a daisy chain must be tied high. The other devices in the stack must have TOS tied low. See Figure 1.

Data Link Layer

Clock Phase And Polarity: The LTC6803 SPI compatible interface is configured to operate in a system using CPHA = 1 and CPOL = 1. Consequently, data on SDI must be stable during the rising edge of SCKI.

Data Transfers: Every byte consists of 8 bits. Bytes are transferred with the most significant bit (MSB) first. On a write, the data value on SDI is latched into the device on the rising edge of SCKI (Figure 3). Similarly, on a read, the data value output on SDO is valid during the rising edge of SCKI and transitions on the falling edge of SCKI (Figure 4).

CSBI must remain low for the entire duration of a command sequence, including between a command byte and subsequent data. On a write command, data is latched in on the rising edge of CSBI.

Network Layer

PEC Byte: The packet error code (PEC) byte is a cyclic redundancy check (CRC) value calculated for all of the bits in a register group in the order they are passed, using the initial PEC value of 01000001 (0x41) and the following characteristic polynomial:

$$x^8 + x^2 + x + 1$$

To calculate the 8-bit PEC value, a simple procedure can be established:

1. Initialize the PEC to 0100 0001.
2. For each bit DIN coming into the register group, set IN0 = DIN XOR PEC[7], then IN1=PEC[0] XOR IN0, IN2 = PEC[1] XOR IN0.
3. Update the 8-bit PEC as PEC[7] = PEC[6], PEC[6] = PEC[5],.....PEC[3] = PEC[2], PEC[2] = IN2, PEC[1] = IN1, PEC[0] = IN0.
4. Go back to step 2 until all data are shifted. The 8-bit result is the final PEC byte.

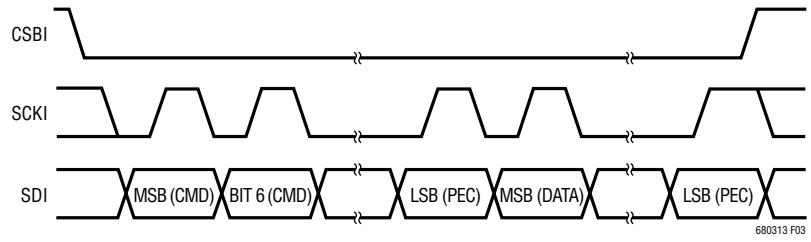

Figure 3. Transmission Format (Write)

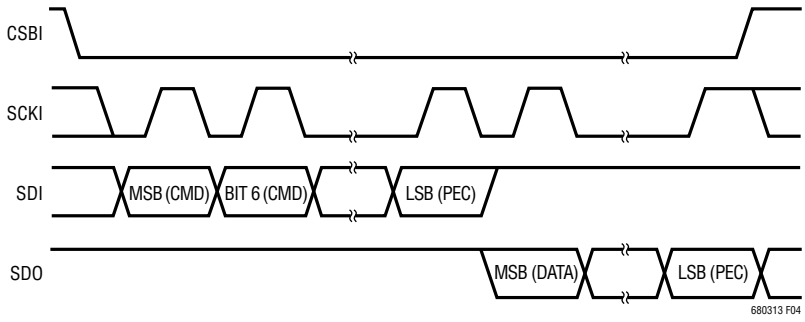

Figure 4. Transmission Format (Read)

OPERATION

An example to calculate the PEC is listed in Table 1 and Figure 5. The PEC of the 1 byte data 0x01 is computed as 0xC7 after the last bit of the byte clocked in. For multiple byte data, the PEC is valid at the end (LSB) of the last byte.

LTC6803 calculates PEC byte for any command or data received and compares it with the PEC byte following the command or data. The command or data is regarded as valid only if the PEC bytes match. LTC6803 also attaches the calculated PEC byte at the end of the data it shifts out.

For daisy-chained LTC6803-1/LTC6803-3, each device computes the PEC byte based on the data it sends out or receives for itself. The data passing through for other devices do affect its PEC. On a read command, each device shifts its data out with, and then shifts out the PEC byte it computed, MSB first. For example, when reading the flag registers from two stacked devices (bottom device A and top device B), the data will be output in the following order:

FLGR0(A), FLGR1(A), FLGR2(A), PEC(A), FLGR0(B), FLGR1(B), FLGR2(B), PEC(B)

On a write command, each device receives its data and then the PEC byte, MSB first. For example, when writing configuration registers to two stacked devices (bottom device A and top device B), the data will be input in the following order:

CFGRR0(B), CFGR1(B),……, CFGR5(B), PEC(B), CFGR0(A), CFGR1(A),……, CFGR5(A), PEC(A)

Broadcast Commands: A broadcast command is one to which all devices on the bus will respond, regardless of device address. See the Bus Protocols and Commands sections.

In daisy-chained configurations, all devices in the chain receive the command bytes simultaneously. For example, to initiate ADC conversions in a stack of devices, a single STCVAD command is sent, and all devices will start conversions at the same time. For read and write commands, a single command is sent, and then the stacked devices effectively turn into a cascaded shift register, in which data is shifted through each device to the next higher (on a write) or the next lower (on a read) device in the stack. See the Serial Command Examples section.

Polling Methods: For ADC conversions, three methods can be used to determine ADC completion. First, a controller can start an ADC conversion and wait for the specified conversion time to pass before reading the results. The second method is to hold CSBI low after an ADC start command has been sent. The ADC conversion status will be output on SDO (Figure 6). A problem with the second method is that the controller is not free to do other serial communication while waiting for ADC conversions to complete. The third method overcomes this limitation. The controller can send an ADC start command, perform other tasks, and then send a poll ADC converter status (PLADC) command to determine the status of the ADC conversions (Figure 7). For OV/UV interrupt status, the poll interrupt status (PLINT) command can be used to quickly determine whether any cell in a stack is in an overvoltage or undervoltage condition (Figure 7).

Table 1. Procedure to Calculate PEC Byte

CLOCK CYCLE	DIN	IN0	IN1	IN2	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]
0	0	0	1	0	0	1	0	0	0	0	0	1
1	0	1	1	0	1	0	0	0	0	0	1	0
2	0	0	1	1	0	0	0	0	0	0	1	1
3	0	0	0	1	0	0	0	0	0	1	1	0
4	0	0	0	0	0	0	0	0	1	1	0	0
5	0	0	0	0	0	0	0	1	1	0	0	0
6	0	0	0	0	0	0	1	1	0	0	0	0
7	1	1	1	1	0	1	1	0	0	0	0	0
8					1	1	0	0	0	1	1	1

OPERATION

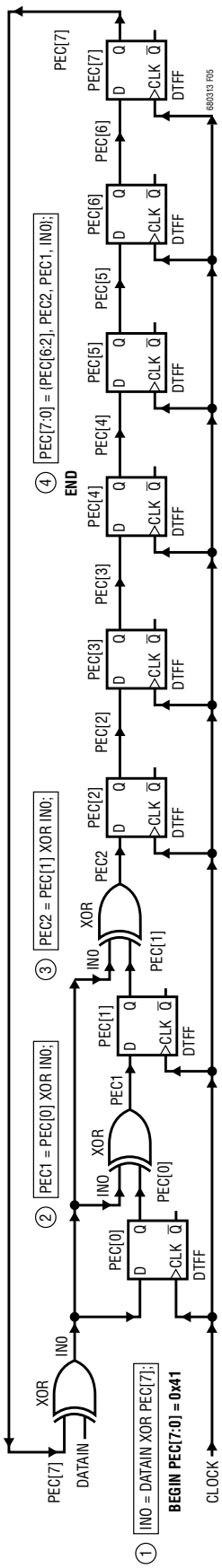

Figure 5

OPERATION

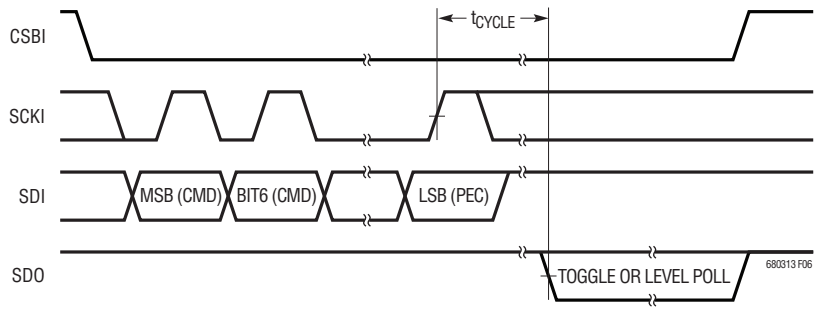

Figure 6. Transmission Format (ADC Conversion and Poll)

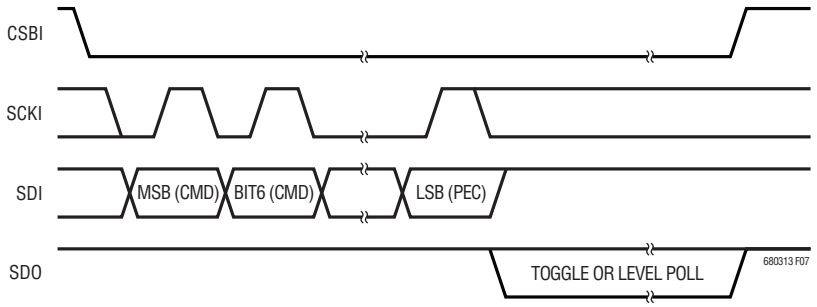

Figure 7. Transmission Format (PLADC Conversion or PLINT)

Toggle Polling: Toggle polling allows a robust determination both of device states and of the integrity of the connections between the devices in a stack. Toggle polling is enabled when the LVLPL bit is low. After entering a polling command, the data out line will be driven by the slave devices based on their status. When polling for the ADC converter status, data out will be low when any device is busy performing an ADC conversion and will toggle at 1kHz when no device is busy. Similarly, when polling for interrupt status, the output will be low when any device has an interrupt condition and will toggle at 1kHz when none has an interrupt condition.

Toggle Polling—Daisy-Chained Broadcast Polling: The SDO pin (bottom device) or SDI pin (stacked devices) will be low if a device is busy/in interrupt. If it is not busy/not in interrupt, the device will pass the signal from the SDOI input to data out (if not the top-of-stack device) or toggle the data out line at 1kHz (if the top-of-stack device). The master pulls CSBI high to exit polling.

Level Polling: Level polling is enabled when the LVLPL bit is high. After entering a polling command, the data out line will be driven by the slave devices based on their status. When polling for the ADC converter status, data out will be low when any device is busy performing an ADC conversion and will be high when no device is busy. Similarly, when polling for interrupt status, the output will be low when any device has an interrupt condition and will be high when none has an interrupt condition.

Level Polling—Daisy-Chained Broadcast Polling: The SDO pin (bottom device) or SDI pin (stacked devices) will be low if a device is busy/in interrupt. If it is not busy/not in interrupt, the device will pass the level from the SDOI input to data out (if not the top-of-stack device) or hold the data out line high (if the top-of-stack device). Therefore, if any device in the chain is busy or in interrupt, the SDO signal at the bottom of the stack will be low. If all devices are not busy/not in interrupt, the SDO signal at the bottom of the stack will be high. The master pulls CSBI high to exit polling.

OPERATION

Table 2. Protocol Key

PEC		Packet Error Code			Master-to-Slave
N		Number of Bits			Slave-to-Master
...		Continuation of Protocol			Complete Byte of Data

Table 3. Broadcast Poll Command

8	8	
Command	PEC	Poll Data

Revision Code: The diagnostic register group contains a 2-bit revision code. If software detection of device revision is necessary, then contact the factory for details. Otherwise, the code can be ignored. In all cases, however, the values of all bits must be used when calculating the packet error code (PEC) byte on data reads.

Bus Protocols: There are 3 different protocol formats, depicted in Table 3 through Table 5. Table 2 is the key for reading the protocol diagrams.

Table 4. Broadcast Read

8	8	8	…	8	8	8	…	8
Command	PEC	Data Byte Low	…	Data Byte High	PEC	Shift Byte 1	…	Shift Byte N

Table 5. Broadcast Write

8	8	8	…	8	8	8	…	8
Command	PEC	Data Byte Low	…	Data Byte High	PEC	Shift Byte 1	…	Shift Byte N

See Serial Command examples.

Table 6. Command Codes and PEC Bytes

COMMAND DESCRIPTION	NAME		CODE	PEC
Write Configuration Register Group	WRCFG		01	C7
Read Configuration Register Group	RDCFG		02	CE
Read All Cell Voltage Group	RDCV		04	DC
Read Cell Voltages 1-4	RDCVA		06	D2
Read Cell Voltages 5-8	RDCVB		08	F8
Read Cell Voltages 9-12	RDCVC		0A	F6
Read Flag Register Group	RDFLG		0C	E4
Read Temperature Register Group	RDTMP		0E	EA
Start Cell Voltage ADC Conversions and Poll Status	STCVAD	All Cell 1 Cell 2 Cell 3 Cell 4 Cell 5 Cell 6 Cell 7 Cell 8 Cell 9 Cell 10 Cell 11 Cell 12 Clear (FF) Self Test1 Self Test2	10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F	B0 B7 BE B9 AC AB A2 A5 88 8F 86 81 94 93 9A 9D

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Table 6. Command Codes and PEC Bytes (continued)

COMMAND DESCRIPTION	NAME		CODE	PEC
Start Open-Wire ADC Conversions and Poll Status	STOWAD	All	20	20
		Cell 1	21	27
		Cell 2	22	2E
		Cell 3	23	29
		Cell 4	24	3C
		Cell 5	25	3B
		Cell 6	26	32
		Cell 7	27	35
		Cell 8	28	18
		Cell 9	29	1F
		Cell 10	2A	16
		Cell 11	2B	11
		Cell 12	2C	04
Start Temperature ADC Conversions and Poll Status	STTMPAD	All	30	50
		External1	31	57
		External2	32	5E
		Internal	33	59
		Self Test 1	3E	7A
		Self Test 2	3F	7D
Poll ADC Converter Status	PLADC		40	07
Poll Interrupt Status	PLINT		50	77
Start Diagnose and Poll Status	DAGN		52	79
Read Diagnostic Register	RDDGNR		54	6B
Start Cell Voltage ADC Conversions and Poll Status, with Discharge Permitted	STCVDC	All	60	E7
		Cell 1	61	E0
		Cell 2	62	E9
		Cell 3	63	EE
		Cell 4	64	FB
		Cell 5	65	FC
		Cell 6	66	F5
		Cell 7	67	F2
		Cell 8	68	DF
		Cell 9	69	D8
		Cell 10	6A	D1
		Cell 11	6B	D6
		Cell 12	6C	C3
Start Open-Wire ADC Conversions and Poll Status, with Discharge Permitted	STOWDC	All	70	97
		Cell 1	71	90
		Cell 2	72	99
		Cell 3	73	9E
		Cell 4	74	8B
		Cell 5	75	8C
		Cell 6	76	85
		Cell 7	77	82
		Cell 8	78	AF
		Cell 9	79	A8
		Cell 10	7A	A1
		Cell 11	7B	A6
		Cell 12	7C	B3

OPERATION

Table 7. Configuration (CFG) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGR0	RD/WR	WDT	GPIO2	GPIO1	LVLPL	CELL10	CDC[2]	CDC[1]	CDC[0]
CFGR1	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGR2	RD/WR	MC4I	MC3I	MC2I	MC1I	DCC12	DCC11	DCC10	DCC9
CFGR3	RD/WR	MC12I	MC11I	MC10I	MC9I	MC8I	MC7I	MC6I	MC5I
CFGR4	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGR5	RD/WR	VOV[7]	VOV[6]	VOV[5]	VOV[4]	VOV[3]	VOV[2]	VOV[1]	VOV[0]

Table 8. Cell Voltage (CV) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVR00	RD	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
CVR01	RD	C2V[3]	C2V[2]	C2V[1]	C2V[0]	C1V[11]	C1V[10]	C1V[9]	C1V[8]
CVR02	RD	C2V[11]	C2V[10]	C2V[9]	C2V[8]	C2V[7]	C2V[6]	C2V[5]	C2V[4]
CVR03	RD	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
CVR04	RD	C4V[3]	C4V[2]	C4V[1]	C4V[0]	C3V[11]	C3V[10]	C3V[9]	C3V[8]
CVR05	RD	C4V[11]	C4V[10]	C4V[9]	C4V[8]	C4V[7]	C4V[6]	C4V[5]	C4V[4]
CVR06	RD	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
CVR07	RD	C6V[3]	C6V[2]	C6V[1]	C6V[0]	C5V[11]	C5V[10]	C5V[9]	C5V[8]
CVR08	RD	C6V[11]	C6V[10]	C6V[9]	C6V[8]	C6V[7]	C6V[6]	C6V[5]	C6V[4]
CVR09	RD	C7V[7]	C7V[6]	C7V[5]	C7V[4]	C7V[3]	C7V[2]	C7V[1]	C7V[0]
CVR10	RD	C8V[3]	C8V[2]	C8V[1]	C8V[0]	C7V[11]	C7V[10]	C7V[9]	C7V[8]
CVR11	RD	C8V[11]	C8V[10]	C8V[9]	C8V[8]	C8V[7]	C8V[6]	C8V[5]	C8V[4]
CVR12	RD	C9V[7]	C9V[6]	C9V[5]	C9V[4]	C9V[3]	C9V[2]	C9V[1]	C9V[0]
CVR13	RD	C10V[3]	C10V[2]	C10V[1]	C10V[0]	C9V[11]	C9V[10]	C9V[9]	C9V[8]
CVR14	RD	C10V[11]	C10V[10]	C10V[9]	C10V[8]	C10V[7]	C10V[6]	C10V[5]	C10V[4]
CVR15*	RD	C11V[7]	C11V[6]	C11V[5]	C11V[4]	C11V[3]	C11V[2]	C11V[1]	C11V[0]
CVR16*	RD	C12V[3]	C12V[2]	C12V[1]	C12V[0]	C11V[11]	C11V[10]	C11V[9]	C11V[8]
CVR17*	RD	C12V[11]	C12V[10]	C12V[9]	C12V[8]	C12V[7]	C12V[6]	C12V[5]	C12V[4]

*Registers CVR15, CVR16, and CVR17 can only be read if the CELL10 bit in register CFGR0 is low

Table 9. Flag (FLG) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLGR0	RD	C4OV	C4UV	C3OV	C3UV	C2OV	C2UV	C1OV	C1UV
FLGR1	RD	C8OV	C8UV	C7OV	C7UV	C6OV	C6UV	C5OV	C5UV
FLGR2	RD	C12OV*	C12UV*	C11OV*	C11UV*	C10OV	C10UV	C9OV	C9UV

* Bits C11UV, C12UV, C11OV and C12OV are always low if the CELL10 bit in register CFGR0 is high

OPERATION

Table 10. Temperature (TMP) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMPR0	RD	ETMP1[7]	ETMP1[6]	ETMP1[5]	ETMP1[4]	ETMP1[3]	ETMP1[2]	ETMP1[1]	ETMP1[0]
TMPR1	RD	ETMP2[3]	ETMP2[2]	ETMP2[1]	ETMP2[0]	ETMP1[11]	ETMP1[10]	ETMP1[9]	ETMP1[8]
TMPR2	RD	ETMP2[11]	ETMP2[10]	ETMP2[9]	ETMP2[8]	ETMP2[7]	ETMP2[6]	ETMP2[5]	ETMP2[4]
TMPR3	RD	ITMP[7]	ITMP[6]	ITMP[5]	ITMP[4]	ITMP[3]	ITMP[2]	ITMP[1]	ITMP[0]
TMPR4	RD	NA	NA	NA	THSD	ITMP[11]	ITMP[10]	ITMP[9]	ITMP[8]

Table 11. Packet Error Code (PEC)

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PEC	RD	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]

Table 12. Diagnostic Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DGNR0	RD	REF[7]	REF[6]	REF[5]	REF[4]	REF[3]	REF[2]	REF[1]	REF[0]
DGNR1	RD	REV[1]	REV[0]	MUXFAIL	NA	REF[11]	REF[10]	REF[9]	REF[8]

Table 13. Memory Bit Descriptions

NAME	DESCRIPTION	VALUES			
		CDC	UV/OV COMPARATOR PERIOD	V_{REF} POWERED DOWN BETWEEN MEASUREMENTS	CELL VOLTAGE MEASUREMENT TIME
CDC	Comparator Duty Cycle	0 (default)	N/A (Comparator Off) Standby Mode	Yes	N/A
		1	N/A (Comparator Off)	No	13ms
		2	13ms	No	13ms
		3	130ms	No	13ms
		4	500ms	No	13ms
		5	130ms	Yes	21ms
		6	500ms	Yes	21ms
		7	2000ms	Yes	21ms
CELL10	10-Cell Mode	0 = 12-cell mode (default); 1 = 10-cell mode			
LVLPL	Level Polling Mode	0 = toggle polling (default); 1 = level polling			
GPIO1	GPIO1 Pin Control	Write: 0 = GPIO1 pin pull-down on; 1 = GPIO1 pin pull-down off (default) Read: 0 = GPIO1 pin at logic '0'; 1 = GPIO1 pin at logic '1'			
GPIO2	GPIO2 Pin Control	Write: 0 = GPIO2 pin pull-down on; 1 = GPIO2 pin pull-down off (default) Read: 0 = GPIO2 pin at logic '0'; 1 = GPIO2 pin at logic '1'			
WDT	Watchdog Timer	Read: 0 = WDT pin at logic '0'; 1 = WDT pin at logic '1'			
DCCx	Discharge Cell x	x = 1..12 0 = turn off shorting switch for cell 'x' (default); 1 = turn on shorting switch			
V_{UV}	Undervoltage Comparison Voltage*	Comparison voltage = (V_{UV} – 31) • 16 • 1.5mV			
V_{OV}	Overvoltage Comparison Voltage*	Comparison voltage = (V_{OV} – 32) • 16 • 1.5mV			
MUXFAIL	Multiplexer Self Test Result	Read: 0 = test passed; 1 = test failed			

OPERATION

Table 13. Memory Bit Descriptions (continued)

NAME	DESCRIPTION	VALUES
MCxI	Mask Cell x Interrupts	x = 1..12 0 = enable interrupts for cell 'x' (default) 1 = turn off interrupts and clear flags for cell 'x'
CxV	Cell x Voltage*	x = 1..12 12-bit ADC measurement value for cell 'x' cell voltage for cell 'x' = (CxV – 512) • 1.5mV reads as 0xFFF while A/D conversion in progress
CxUV	Cell x Undervoltage Flag	x = 1..12 cell voltage compared to V_{UV} comparison voltage 0 = cell 'x' not flagged for undervoltage condition; 1 = cell 'x' flagged
CxOV	Cell x Overvoltage Flag	x = 1..12 cell voltage compared to V_{OV} comparison voltage 0 = cell 'x' not flagged for overvoltage condition; 1 = cell 'x' flagged
ETMPx	External Temperature Measurement*	Temperature measurement voltage = (ETMPx – 512) • 1.5mV
THSD	Thermal Shutdown Status	0 = thermal shutdown has not occurred; 1 = thermal shutdown has occurred Status cleared to '0' on read of Thermal Register Group
REV	Revision Code	Device revision code
ITMP	Internal Temperature Measurement*	Temperature measurement voltage = (ITMP – 512) • 1.5mV = 8mV * T(°K)
PEC	Packet Error Code	Cyclic redundancy check (CRC) value
REF	Reference Voltage for Diagnostics	This reference voltage = (REF – 512) • 1.5mV. Normal range is within 2.1V to 2.9V

*Voltage equations use the decimal value of the registers, 0 to 4095 for 12-bit and 0 to 255 for 8-bit registers

SERIAL COMMAND EXAMPLES

Examples below use a configuration of three stacked LTC6803-1 or LTC6803-3 devices: bottom (B), middle (M), and top (T)

Write Configuration Registers (Figure 8)

1. Pull CSBI low
2. Send WRCFG command and its PEC byte
3. Send CFGR0 byte for top device, then CFGR1 (T), …CFGR5 (T), PEC of CFGR0(T) to CFGR5(T)
4. Send CFGR0 byte for middle device, then CFGR1 (M) … CFGR5 (M)), PEC of CFGR0(M) to CFGR5(M)
5. Send CFGR0 byte for bottom device, then CFGR1 (B), … CFGR5 (B)), PEC of CFGR0(B) to CFGR5(B)
6. Pull CSBI high; data latched into all devices on rising edge of CSBI. S pins respond as data latched.

Calculation of serial interface time for sequence above:

Number of devices in stack = N
Number of bytes in sequence = B = 2 command byte and 7 data bytes per device = 2 + 7 • N
Serial port frequency per bit = F
Time = (1/F) • B • 8 bits/byte = (1/F) • (2 + 7 • N) • 8
Time for 3-cell example above, with 1MHz serial port = (1/1000000) • (2 + 7 • 3) • 8 = 184µs

OPERATION

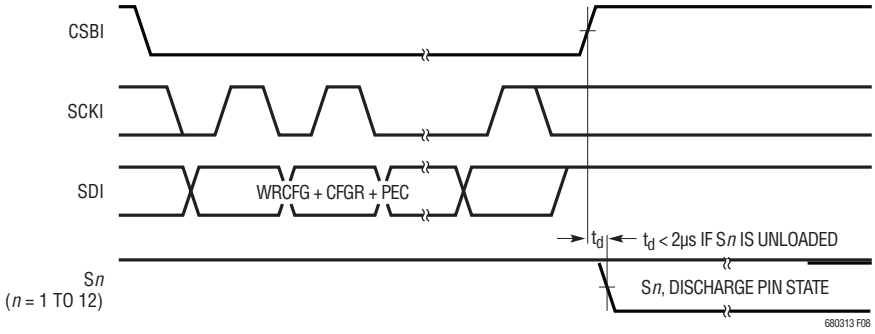

Figure 8. S Pin Action and SPI Transmission

Read Cell Voltage Registers (12 Cell Mode)

1. Pull CSBI low
2. Send RDCV command and PEC
3. Read CVR00 byte of bottom device, then CVR01 (B), CVR02 (B), … CVR17 (B), and then PEC (B)
4. Read CVR00 byte of middle device, then CVR01 (M), CVR02 (M), … CVR17 (M), and then PEC (M)
5. Read CVR00 byte for top device, then CVR01 (T), CVR02 (T), … CVR17 (T), and then PEC (T)
6. Pull CSBI high

Calculation of serial interface time for sequence above:

Number of devices in stack = N
Number of bytes in sequence = B = 2 command byte, and 18 data bytes plus 1 PEC byte per device = 2 + 19 • N
Serial port frequency per bit = F
Time = (1/F) • B • 8 bits/byte = (1/F) • (2 + 19 • N) • 8
Time for 3-cell example above, with 1MHz serial port = (1/1000000) • (2 + 19 • 3) • 8 = 472µs

Start Cell Voltage ADC Conversions and Poll Status (Toggle Polling)

1. Pull CSBI low
2. Send STCVAD command byte and PEC (all devices in stack start ADC conversions simultaneously)
3. SDO output from bottom device pulled low for approximately 12ms
4. SDO output toggles at 1kHz rate, indicating conversions complete for all devices in daisy chain
5. Pull CSBI high to exit polling

Start Cell Voltage ADC Conversions and Poll Status (Broadcast Command with Toggle Polling)

1. Pull CSBI low
2. Send STCVAD command and PEC (all devices in stack start ADC conversions simultaneously)
3. SDO output of all devices in parallel pulled low for approximately 12ms
4. SDO output toggles at 1kHz rate, indicating conversions complete for all devices in the daisy chain
5. Pull CSBI high to exit polling

Poll Interrupt Status (Level Polling)

1. Pull CSBI low
2. Send PLINT command and PEC
3. SDO output from bottom device pulled low if any device has an interrupt condition; otherwise, SDO high
4. Pull CSBI high to exit polling

APPLICATIONS INFORMATION

DIFFERENCE BETWEEN THE LTC6803-1 AND LTC6803-3

The **only** difference between the LTC6803-1 and the LTC6803-3 is the bonding of the V^- and C0 pins. The V^- and C0 are separate signals on every LTC6803 die. In the LTC6803-1 package, the V^- and C0 signals are shorted together by bonding these signals to the same pin. In the LTC6803-3 package, V^- and C0 are separate pins. Therefore, the LTC6803-1 is pin compatible with the LTC6802-1. For new designs the LTC6803-3 pinout allows a Kelvin connection to C0 (Figure 24).

CELL VOLTAGE FILTERING

The LTC6803 employs a sampling system to perform its analog-to-digital conversions and provides a conversion result that is essentially an average over the 0.5ms conversion window, provided there isn't noise aliasing with respect to the delta-sigma modulator rate of 512kHz. This indicates that a lowpass filter with 30dB attenuation at 500kHz may be beneficial. Since the delta-sigma integration bandwidth is about 1kHz, the filter corner need not be lower than this to assure accurate conversions.

Series resistors of 100Ω may be inserted in the input paths without introducing meaningful measurement error. Shunt capacitors may be added from the cell inputs to V^-, creating RC filtering as shown in Figure 9. The cell balancing MOSFET in Figure 12 can cause a small transient when it switches on and off. Keeping the cutoff frequency of the RC filter relatively high will allow adequate settling prior to the actual conversion. A delay of about 500µs is provided in the ADC timing, so a 16kHz LPF is optimal (100Ω, 0.1µF) and offers 30dB of noise rejection.

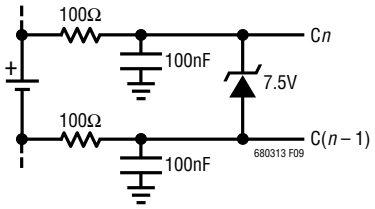

Figure 9. Adding RC Filtering to the Cell Inputs (One Cell Connection Shown)

Larger series resistors and shunt capacitors can be used to lower the filter bandwidth. The measurement error due to the larger component values is a complex function of the component values. The error also depends on how often measurements are made. Table 14 is an example. In each example a 3.6V cell is being measured and the error is displayed in millivolts. There is a RC filter in series with inputs C1 through C12 for the LTC6803-1. There is an RC filter in series with inputs C0 through C12 for the LTC6803-3.

Table 14. Cell Measurement Errors vs Input RC Values

	R = 100Ω, C = 0.1µF	R = 1k, C = 0.1µF	R = 1k, C = 1µF	R = 10k, C = 3.3µF
Cell 1 Error (mV, LTC6803-1)	0.5	4.5	1.5	1.5
Cell 2 to Cell 12 (mV)	1	9	3	0.5

For the LTC6803-1, no resistor should be placed in series with the V^- pin. Because the supply current flows from the V^- pin, any resistance on this pin could generate a significant conversion error for cell 1, and the error of cell 1 caused by the RC filter differs from errors of cell 2 to cell 12.

OPEN CONNECTION DETECTION

When a cell input (C pin) is open, it affects two cell measurements. Figure 10 shows an open connection to C3, in an application without external filtering between the C pins and the cells. During normal ADC conversions (that is, using the STCVAD command), the LTC6803 will give near zero readings for B3 and B4 when C3 is open. The zero reading for B3 occurs because during the measurement of B3, the ADC input resistance will pull C3 to the C2 potential. Similarly, during the measurement of B4, the ADC input resistance pulls C3 to the C4 potential.

Figure 11 shows an open connection at the same point in the cell stack as Figure 10, but this time there is an external filtering network still connected to C3. Depending on the value of the capacitor remaining on C3, a normal measurement of B3 and B4 may not give near-zero readings, since the C3 pin is not truly open. In fact, with a large external capacitance on C3, the C3 voltage will be charged midway

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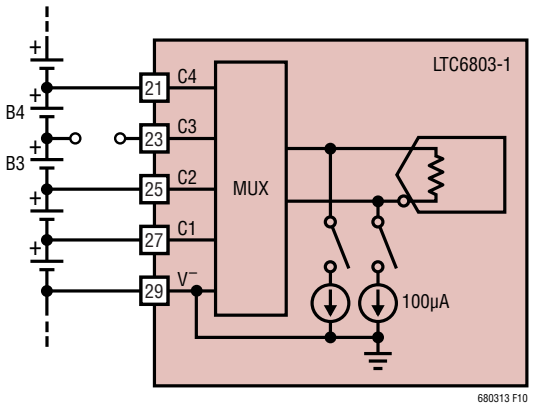

Figure 10. Open Connection

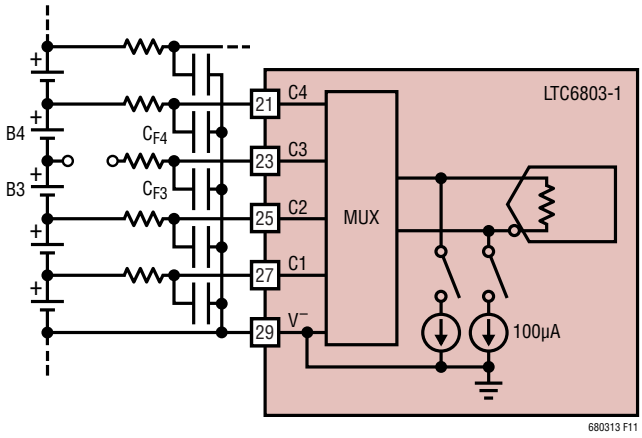

Figure 11. Open Connection with RC Filtering

between C2 and C4 after several cycles of measuring cells B3 and B4. Thus the measurements for B3 and B4 may indicate a valid cell voltage when in fact the exact state of B3 and B4 is unknown.

To reliably detect an open connection, the command STOWAD is provided. With this command, two 100µA current sources are connected to the ADC inputs and turned on during all cell conversions. Referring again to Figure 11, with the STOWAD command, the C3 pin will be pulled down by the 100µA current source during the B3 cell measurement *and* during the B4 cell measurement. This will tend to decrease the B3 measurement result and increase the B4 measurement result relative to the normal STCVAD command. The biggest change is observed in the B4 measurement when C3 is open. So, the best method to detect an open wire at input C3 is to look for an increase in the value of battery connected between inputs C3 and C4 (battery B4).

The following algorithm can be used to detect an open connection to cell pin C*n*:

1. Issue a STOWAD command (with 100µA sources connected).
2. Issue a RDCV command and store all cell measurements into array CELLA(*n*).
3. Issue the 2nd STOWAD command (with 100µA sources connected).
4. Issue the 2nd RDCV command and store all cell measurements into array CELLB(*n*).
5. For battery cells, if CELLA(1) < 0 or CELLB(1) < 0, V^- must be open.

   If CELLA(12) < 0 or CELLB(12) < 0, C12 must be open.

   For *n* = 2 to 11, if CELLB(*n*+1) – CELLA(*n*+1) > 200mV, or CELLB(n+1) reaches the full scale of 5.375V, then C*n* is open.

The 200mV threshold is chosen to provide tolerance for measurement errors. For a system with the capacitor connected to C*n* larger than 0.5µF, repeating step 3 several times will discharge the external capacitor enough to meet the criteria.

If the top C pin is open yet V^+ is still connected, then the best way to detect an open connection to the top C pin is by comparing the sum of all cell measurements using the STCVAD command to an auxiliary measurement of the sum of all the cells, using a method similar to that shown in Figure 21. A significantly lower result for the sum of all 12 cells suggests an open connection to the top C pin, provided it was already determined that no other C pin is open.

USING THE S PINS AS DIGITAL OUTPUTS OR GATE DRIVERS

The S outputs include an internal pull-up PMOS. Therefore the S pins will behave as a digital output when loaded with a high impedance, e.g., the gate of an external MOSFET. For applications requiring high battery discharge currents, connect a discrete PMOS switch device and suitable

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discharge resistor to the cell, and the gate terminal to the S output pin, as illustrated in Figure 12.

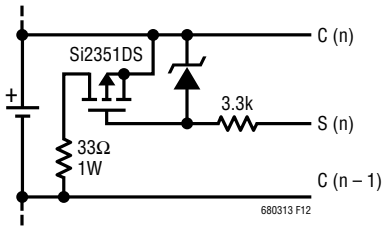

Figure 12. External Discharge FET Connection (One Cell Shown)

POWER DISSIPATION AND THERMAL SHUTDOWN

The MOSFETs connected to the pins S1 through S12 can be used to discharge battery cells. An external resistor should be used to limit the power dissipated by the MOSFETs. The maximum power dissipation in the MOSFETs is limited by the amount of heat that can be tolerated by the LTC6803. Excessive heat results in elevated die temperatures. The electrical characteristics for the LTC6803 I-grade are guaranteed for die temperatures up to 85°C. Little or no degradation will be observed in the measurement accuracy for die temperatures up to 105°C. Damage may occur above 150°C, therefore the recommended maximum die temperature is 125°C.

To protect the LTC6803 from damage due to overheating, a thermal shutdown circuit is included. Overheating of the device can occur when dissipating significant power in the cell discharge switches. The problem is exacerbated when the thermal conductivity of the system is poor.

The thermal shutdown circuit is enabled whenever the device is not in standby mode (see Modes of Operation). It will also be enabled when any current mode input or output is sinking or sourcing current. If the temperature detected on the device goes above approximately 145°C, the configuration registers will be reset to default states, turning off all discharge switches and disabling ADC conversions. When a thermal shutdown has occurred, the THSD bit in the temperature register group will go high. The bit is cleared by performing a read of the temperature registers (RDTMP command).

Since thermal shutdown interrupts normal operation, the internal temperature monitor should be used to determine when the device temperature is approaching unacceptable levels.

USING THE LTC6803 WITH LESS THAN 12 CELLS

If the LTC6803 is powered by the stacked cells, the minimum number of cells is governed by the supply voltage requirements of the LTC6803. The sum of the cell voltages must be 10V to guarantee that all electrical specifications are met.

Figure 13 shows an example of the LTC6803 when used to monitor seven cells. The lowest C inputs connect to the seven cells and the upper C inputs connect to C12. Other configurations, e.g., 9 cells, would be configured in the same way: the lowest C inputs connected to the battery cells and the unused C inputs connected to C12. The unused inputs will result in a reading of 0V for those channels.

The ADC can also be commanded to measure a stack of 10 or 12 cells, depending on the state of the CELL10 bit in the control register. The ADC can also be commanded to measure any individual cell voltage.

FAULT PROTECTION

Care should always be taken when using high energy sources such as batteries. There are numerous ways that systems can be misconfigured when considering the assembly and service procedures that might affect a battery system during its useful lifespan. Table 15 shows the various situations that should be considered when planning protection circuitry. The first five scenarios are to be anticipated during production and appropriate protection is included within the LTC6803-1/LTC6803-3 device itself.

BATTERY INTERCONNECTION INTEGRITY

The FMEA scenarios involving a break in the stack of battery cells are potentially the most damaging. In the case where the battery stack has a discontinuity between groupings of cells monitored by LTC6803 ICs, any load will force a large reverse potential on the daisy-chain connection. This

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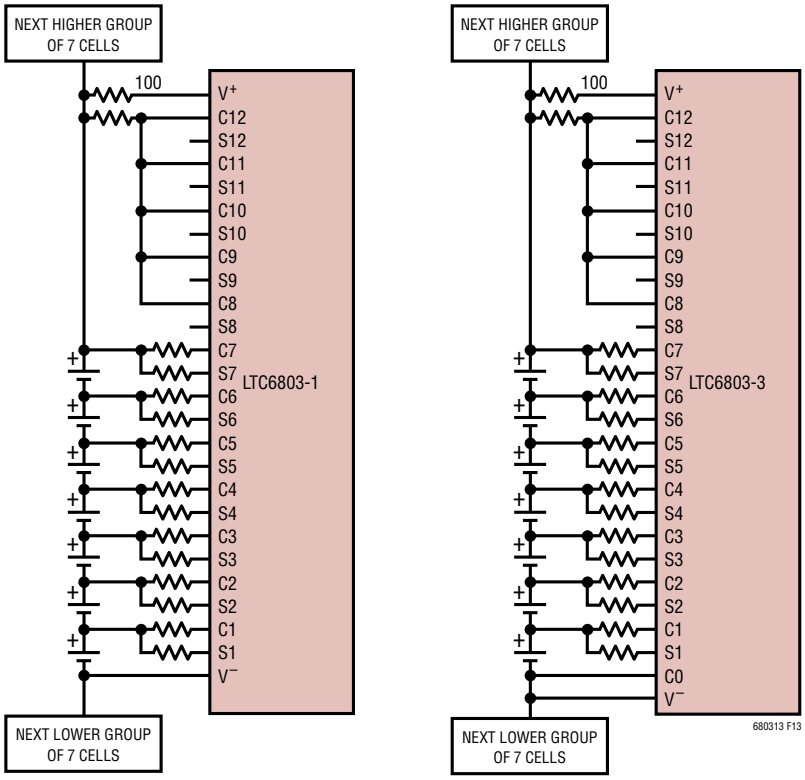

Figure 13. Monitoring 7 Cells with the LTC6803-1/LTC6803-3

Table 15. LTC6803-1/LTC6803-3 Failure Mechanism Effect Analysis

SCENARIO	EFFECT	DESIGN MITIGATION
Cell input open-circuit (random).	Power-up sequence at IC inputs.	Clamp diodes at each pin to V^+ and V^- (within IC) provide alternate power path.
Cell input open-circuit (random).	Differential input voltage overstress.	Zener diodes across each cell voltage input pair (within IC) limits stress.
Disconnection of a harness between a group of battery cells and the IC (in a system of stacked groups).	Loss of supply connection to the IC.	Separate power may be supplied by a local supply.
Data link disconnection between stacked LTC6803 units.	Break of "daisy-chain" communication (no stress to ICs). Communication will be lost to devices above the disconnection. The devices below the disconnection are still able to communicate and perform all functions, however, the polling feature is disabled.	All units above the disconnection will enter standby mode within 2 seconds of disconnect. Discharge switches are disabled in standby mode.
Cell-pack integrity, break between stacked units.	Daisy-chain voltage reversal up to full stack potential during pack discharge.	Use series protection diodes with top-port I/O connections (RS07J for up to 600V). Use isolated data link at bottom-most data port.
Cell-pack integrity, break between stacked units.	Daisy-chain positive overstress during charging.	Add redundant current path link. See Figure 14.
Cell-pack integrity, break within stacked unit.	Cell input reverse overstress during discharge.	Add parallel Schottky diodes across each cell for load-path redundancy. Diode and connections must handle full operating current of stack, will limit stress on IC.
Cell-pack integrity, break within stacked unit.	Cell input positive overstress during charge.	Add SCR across each cell for charge-path redundancy. SCR and connections must handle full charging current of stack, will limit stress on IC by selection of trigger Zener.

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situation might occur in a modular battery system during initial installation or a service procedure. The daisy-chain ports are protected from the reverse potential in this scenario by external series high voltage diodes required in the upper port data connections as shown in Figure 14.

During the charging phase of operation, this fault would lead to forward biasing of daisy-chain ESD clamps that would also lead to part damage. An alternative connection to carry current during this scenario will avoid this stress from being applied (Figure 14).

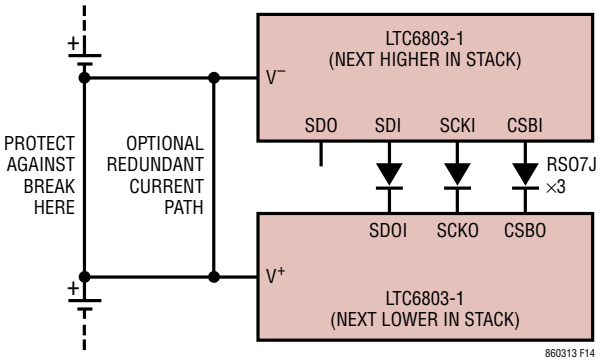
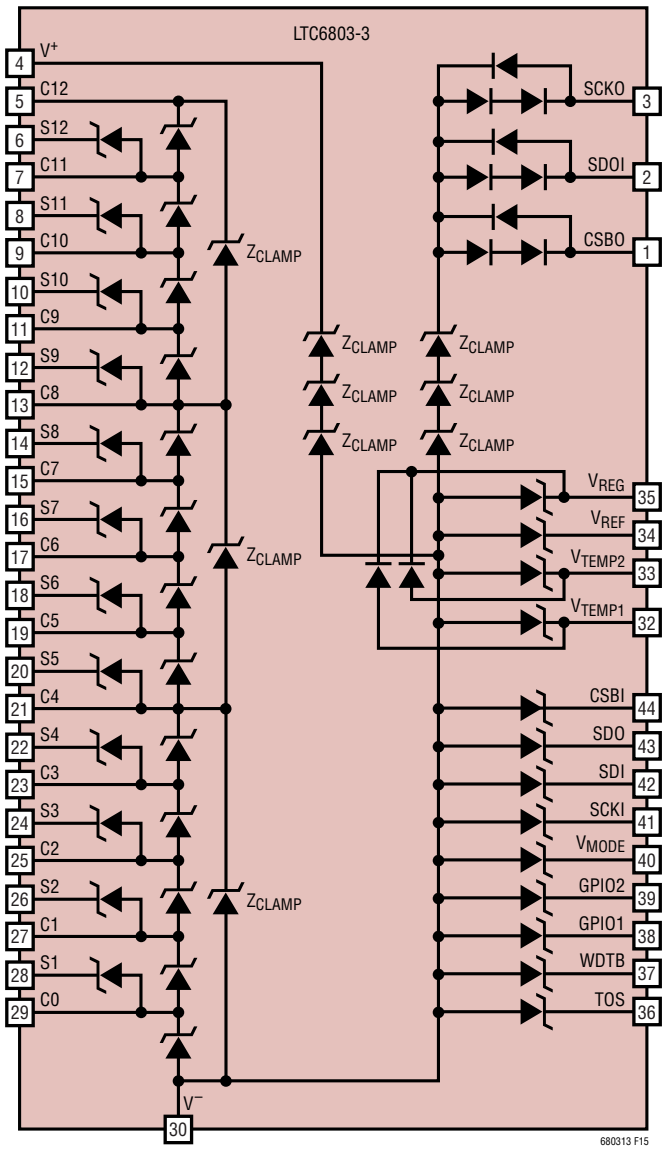


Figure 14. Reverse-Voltage Protection for the Daisy Chain (One Link Connection Shown)

Internal Protection Diodes

Each pin of the LTC6803 has protection diodes to help prevent damage to the internal device structures caused by external application of voltages beyond the supply rails as shown in Figure 15. The diodes shown are conventional silicon diodes with a forward breakdown voltage of 0.5V. The unlabeled Zener diode structures have a reverse-breakdown characteristic which initially breaks down at 12V then snaps back to a 7V clamping potential. The Zener diodes labeled Z_{CLAMP} are higher voltage devices with an initial reverse breakdown of 30V snapping back to 25V. The forward voltage drop of all Zeners is 0.5V. Refer to Figure 15 in the event of unpredictable voltage clamping or current flow. Limiting the current flow at any pin to ±10mA will prevent damage to the IC.



NOTE: NOT SHOWN ARE PN DIODES TO ALL OTHER PINS FROM PIN 30

Figure 15. Internal Protection Diodes

READING EXTERNAL TEMPERATURE PROBES

The LTC6803 includes two channels of ADC input, V_{TEMP1} and V_{TEMP2}, that are intended to monitor thermistors (tempco about –4%/°C generally) or diodes (–2.2mV/°C typical) located within the cell array. Sensors can be powered directly from V_{REF} as shown in Figure 16 (up to 60µA total).

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For sensors that require higher drive currents, a buffer op amp may be used as shown in Figure 17. Power for the sensor is actually sourced indirectly from the V_{REG} pin in this case. Probe loads up to about 1mA maximum are supported in this configuration. Since V_{REF} is shutdown during the LTC6803 idle and shutdown modes, the thermistor drive is also shut off and thus power dissipation minimized. Since V_{REG} remains always on, the buffer op amp (LTC6000 shown) is selected for its ultralow power consumption (12µA).

Expanding Probe Count

As shown Figure 18, a dual 4:1 multiplexer is used to expand the general purpose V_{TEMP1} and V_{TEMP2} ADC inputs to accept 8 different probe signals. The channel is selected by setting the general purpose digital outputs GPIO1 and GPIO2 and the resultant signals are buffered by sections of the LT6004 micropower dual operational amplifier. The probe excitation circuitry will vary with probe type and is not shown here.

Another method of multiple sensor support is possible without the use of any GPIO pins. If the sensors are PN diodes and several used in parallel, then the hottest diode will produce the lowest forward voltage and effectively establish the input signal to the V_{TEMP} input(s). The hottest diode will therefore dominate the readout from the V_{TEMP} inputs that the diodes are connected to. In this scenario, the specific location or distribution of heat is not known, but such information may not be important in practice. Figure 19 shows the basic concept. In any of the sensor configurations shown, a full-scale cold readout would be an indication of a failed open-sensor connection to the LTC6803.

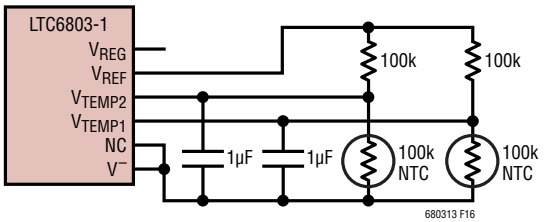

Figure 16. Driving Thermistors Directly from V_{REF}

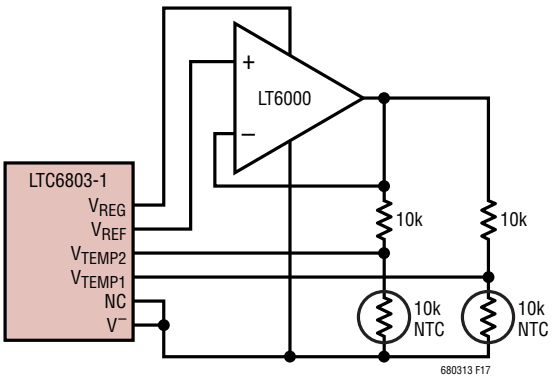

Figure 17. Buffering V_{REF} for Higher Current Sensors

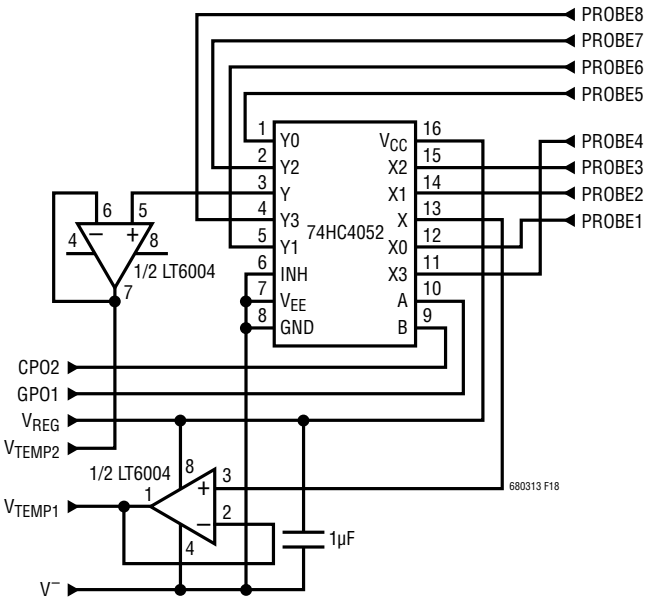

Figure 18. Expanding Sensor Count with Multiplexing

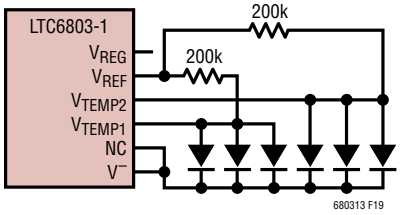

Figure 19. Using Diode Sensors as Hot Spot Detectors

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ADDING CALIBRATION AND FULL-STACK MEASUREMENTS

The general purpose V_{TEMP} ADC inputs may be used to digitize any signals from 0V to 4V with accuracy corresponding closely with that of the cell 1 ADC input. One useful signal to provide is a high accuracy voltage reference, such as 3.300V from an LTC6655-3.3. From periodic readings of this signal, the host software can provide correction of the LTC6803 readings to improve the accuracy over that of the internal LTC6803 reference and/or validate ADC operation. Figure 20 shows a means of selectively powering an LTC6655-3.3 from the battery stack, under the control of the GPIO1 output of the LTC6803-1. Since the operational power of the reference IC would add significant thermal loading to the LTC6803 if powered from V_{REG}, an external high voltage NPN pass transistor is used to form a local 4.4V (V_{be} below V_{REG}) from the battery stack. The GPIO1 signal controls a PMOS FET switch to activate the reference when calibration is to be performed. Since GPIO signals default to logic high in shutdown, the reference will automatically turn off during idle periods.

Another useful signal is a measure of the total stack potential. This provides a redundant operational measurement of the cells in the event of a malfunction in the normal acquisition process, or as a faster means of monitoring the entire stack potential. Figure 21 shows how a resistive divider is used to derive a scaled representation of a full cell group potential. A MOSFET is used to disconnect

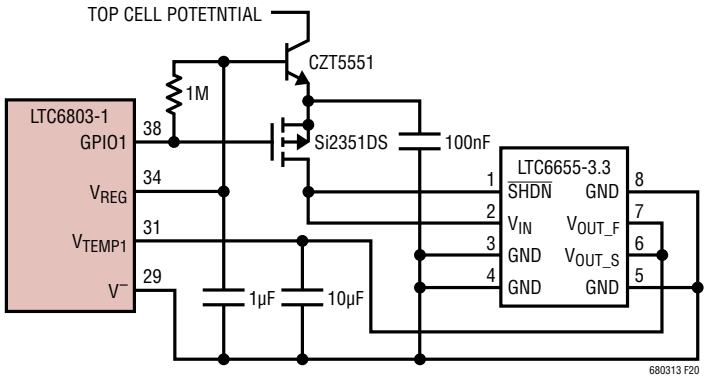

Figure 20. Providing Measurement of Calibration Reference

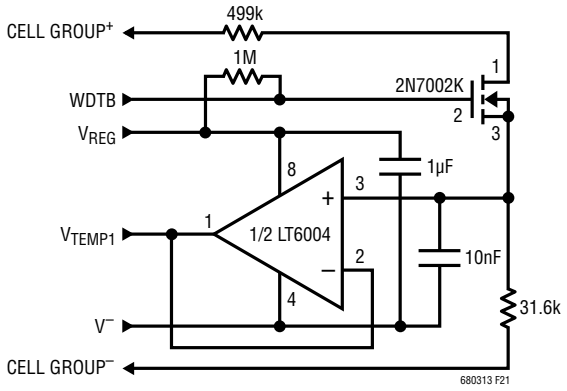

Figure 21. Using a V_{TEMP} Input for Full-Stack Readings

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the resistive loading on the cell group when the IC enters standby mode (i.e., when WDTB goes low). An LT6004 micropower operational amplifier section is shown for buffering the divider signal to preserve accuracy. This circuit has the virtue that it can be converted about four times more frequently than the entire battery array, thus offering a higher sample rate option at the expense of some precision/accuracy, reserving the high resolution cell readings for calibration and balancing data.

PROVIDING HIGH SPEED ISOLATION OF THE SPI DATA PORT

Isolation techniques that are capable of supporting the 1Mbps data rate of the LTC6803 require more power on the isolated (battery) side than can be furnished by the V_{REG} output of the LTC6803. To keep battery drain minimal, this means that a DC/DC function must be implemented along with a suitable data isolation circuit, such as shown in Figure 22. A quad (3 + 1) data isolator Si8441AB-C-IS is used to provide non-galvanic SPI signal connections between a host microprocessor and an LTC6803. An inexpensive isolated DC/DC converter provides powering of the isolator function completely from the host 5V power supply. A quad three-state buffer is used to allow SPI inputs at the LTC6803 to rise to logic high level when the isolator circuitry powers down, assuring the lowest power consumption in the standby condition. The pull-ups to V_{REG} are selected to match the internal loading on V_{REG} by ICs operating with a current mode SPI interface, thus balancing the current in all cells during operation. The additional pull-up on the SDO line (1k resistor and Schottky diode) is to improve rise time, in lower data-rate applications this may not be needed.

SUPPLY DECOUPLING IF BATTERY-STACK POWERED

As shown in Figure 23, the LTC6803-3 can have filtering on both V^+ and V^-, so differential bypassing to the cell group potentials is recommended. The Zener suppresses overvoltages from reaching the IC supply pins. A small ferrite-bead inductor provides protection for the Zener, particularly from energetic ESD strikes. Since the LTC6803-1 cannot have a series resistance to V^-, additional Schottky diodes are needed to prevent ESD-induced reverse-supply (substrate) currents to flow.

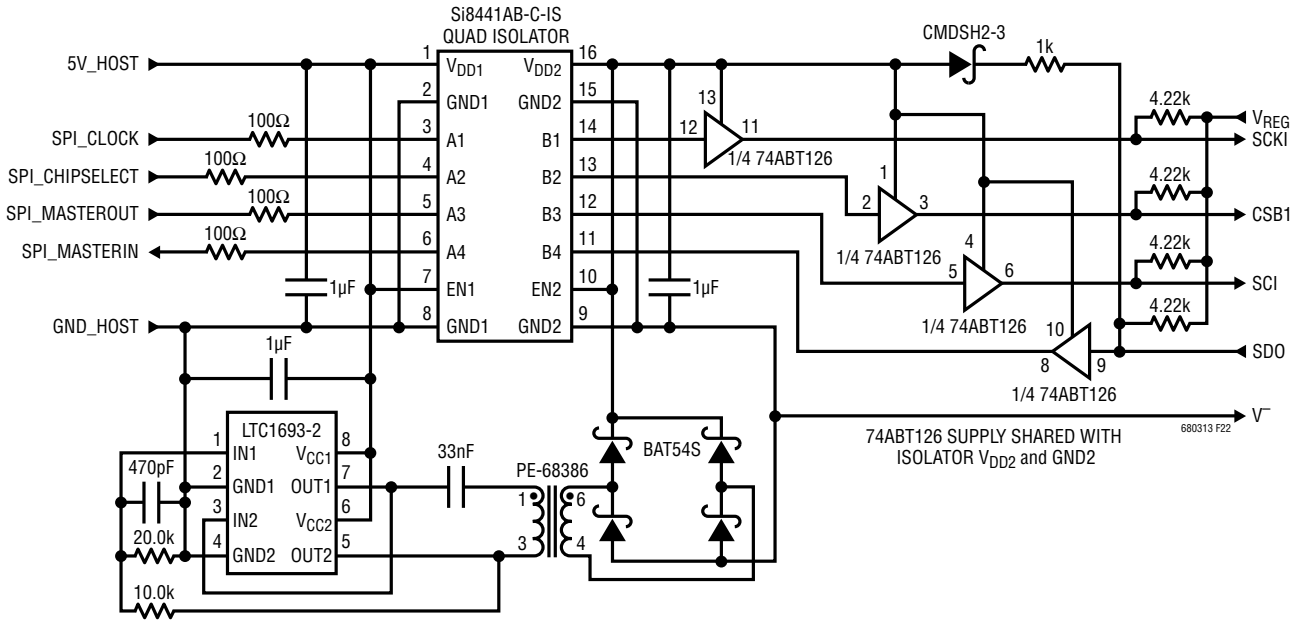

Figure 22. Providing an Isolated High Speed Data Interface

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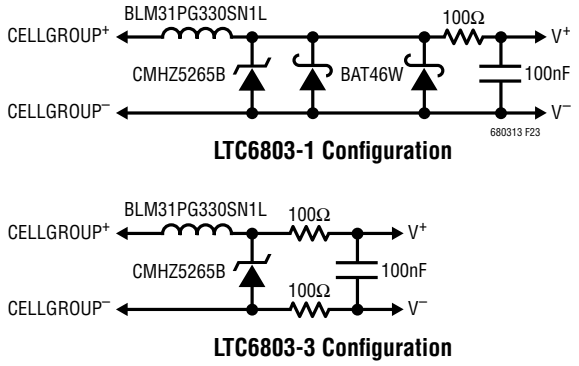

Figure 23. Supply Decoupling

ADVANTAGES OF KELVIN CONNECTION ON C0

The V^- trace resistance can cause an observable voltage drop between the negative end of the bottom battery cell and V^- pin of LTC6803. This voltage drop will add to the measurement error of the bottom cell voltage for LTC6803-1. The LTC6803-3 separates C0 from V^-, allowing Kelvin connection on C0 as shown in Figure 24. Any voltage drop on V^- trace will not affect the bottom cell voltage measurement. The Kelvin connection will also allow RC filtering on V^- as shown in Figure 23.

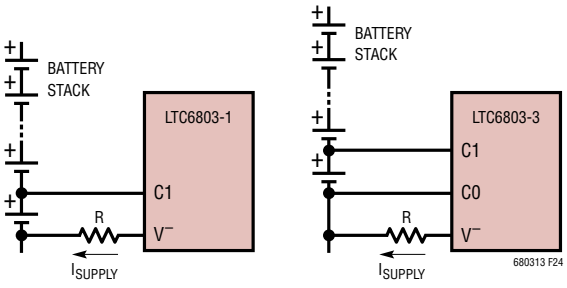

Figure 24. Kelvin Connection on C0 Improving Bottom Cell Voltage Measurement Accuracy

HARDWARE SHUTDOWN

To completely shut down the LTC6803 a PMOS switch can be connected to V^+, or V^+ can be driven from an isolated power supply. Figure 25 shows an example of a switched

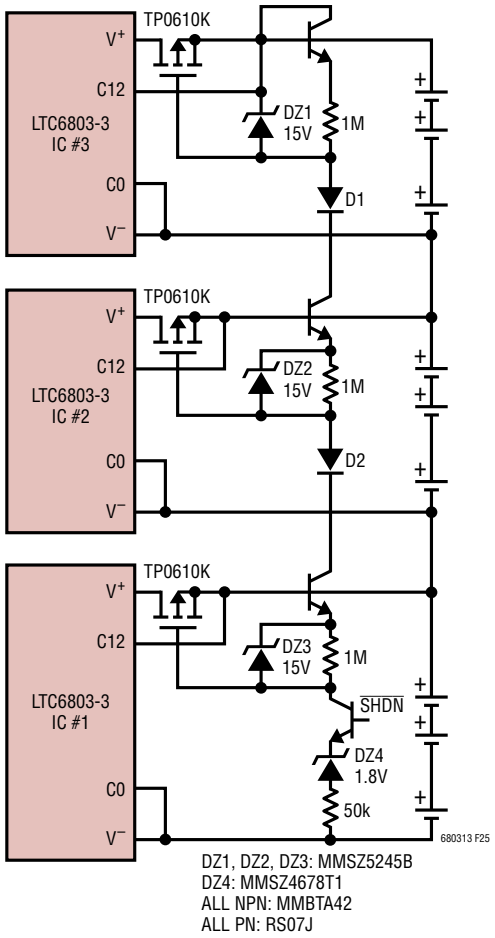

Figure 25. Hardware Shutdown Circuit Reduces Total Supply Current of LTC6803 to Less Than 1nA

V^+. The breakdown voltage of DZ4 is about 1.8V. If $\overline{SHDN}$ < 1.8V, no current will flow through the stacked MMBTA42s and the 1M resistors. TP0610Ks will be completely shut off. If $\overline{SHDN}$ > 2.5V, M7 will be turned on and all TP0610Ks will be turned on.

Figure 26 is an example of isolated power supply. This circuit provides power for two LTC6803s used to monitor 24 series connected battery cells. When 5V is removed, the LTC6803s will draw 1nA from the battery cells. Note that use of an external V^+ supply will not protect daisy-chain SPI operation at low total stack potentials (below 5V).

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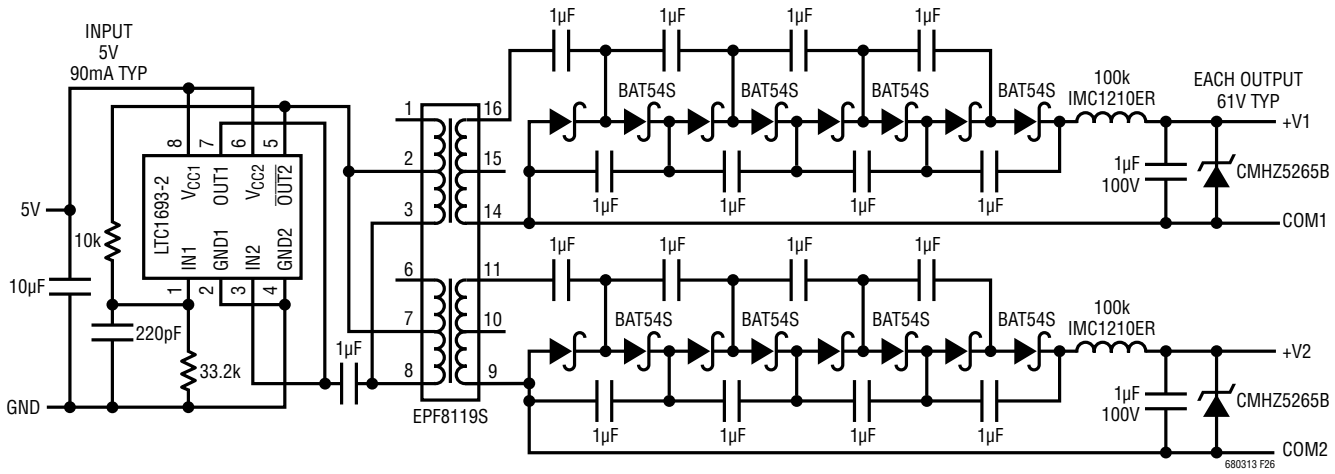

Figure 26. LTC6803 Powered by Isolated Power Supplies

PCB LAYOUT CONSIDERATIONS

The V_{REG} and V_{REF} pins should be bypassed with a 1µF capacitor for best performance. The LTC6803 is capable of operation with as much as 55V between V^+ and V^-. Care should be taken on the PCB layout to maintain physical separation of traces at different potentials. The pinout of the LTC6803-1 and LTC6803-3 were chosen to facilitate this physical separation. There is no more than 5.5V between any two adjacent pins. The package body is used to separate the highest voltage (e. g., 43.2V) from the lowest voltage (0V). As an example, Figure 27 shows the DC voltage on each pin with respect to V^- when twelve 3.6V battery cells are connected to the LTC6803-3.

ADVANTAGES OF DELTA-SIGMA ADCS

The LTC6803 employs a delta-sigma analog-to-digital converter for voltage measurement. The architecture of delta sigma converters can vary considerably, but the common characteristic is that the input is sampled many times over the course of a conversion and then filtered or averaged to produce the digital output code. In contrast, a SAR converter takes a single snapshot of the input voltage and then performs the conversion on this single sample. For measurements in a noisy environment, a delta sigma converter provides distinct advantages over a SAR converter.

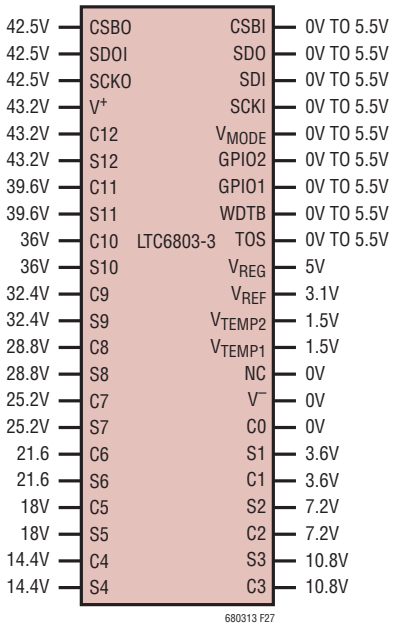

Figure 27. Typical Pin Voltages for Twelve 3.6V Cells

While SAR converters can have high sample rates, the full-power bandwidth of a SAR converter is often greater than 1MHz, which means the converter is sensitive to noise out to this frequency. And many SAR converters have much higher bandwidths—up to 50MHz and beyond. It is possible to filter the input, but if the converter is multiplexed to measure several input channels a separate filter will be

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required for each channel. A low frequency filter cannot reside between a multiplexer and an ADC and achieve a high scan rate across multiple channels. Another consequence of filtering a SAR ADC is that any noise reduction gained by filtering the input cancels the benefit of having a high sample rate in the first place, since the filter will take many conversion cycles to settle.

For a given sample rate, a delta-sigma converter can achieve excellent noise rejection while settling completely in a single conversion—something that a filtered SAR converter cannot do. Noise rejection is particularly important in high voltage switching controllers, where switching noise will invariably be present in the measured voltage. Other advantages of delta-sigma converters are that they are inherently monotonic, meaning they have no missing codes, and they have excellent DC specifications.

Converter Details

The LTC6803's ADC has a second order delta-sigma modulator followed by a SINC2, finite impulse response (FIR) digital filter. The front-end sample rate is 512ksps, which greatly reduces input filtering requirements. A simple 16kHz, 1-pole filter composed of a 100Ω resistor and a 0.1µF capacitor at each input will provide adequate filtering for most applications. These component values will not degrade the DC accuracy of the ADC.

Each conversion consists of two phases—an autozero phase and a measurement phase. The ADC is autozeroed at each conversion, greatly improving CMRR. The second half of the conversion is the actual measurement.

Noise Rejection

Figure 28 shows the frequency response of the ADC. The roll-off follows a SINC2 response, with the first notch at 4kHz. Also shown is the response of a 1-pole, 850Hz filter (187µs time constant) which has the same integrated response to wideband noise as the LTC6803's ADC, which

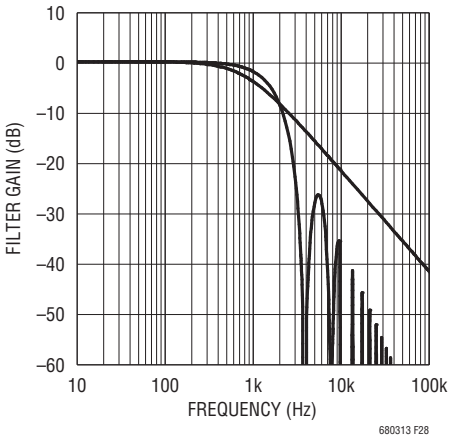


Figure 28. Noise Filtering of the LTC6803 ADC

is about 1350Hz. This means that if wideband noise is applied to the LTC6803 input, the increase in noise seen at the digital output will be the same as an ADC with a wide bandwidth (such as a SAR) preceded by a perfect 1350Hz brick wall lowpass filter.

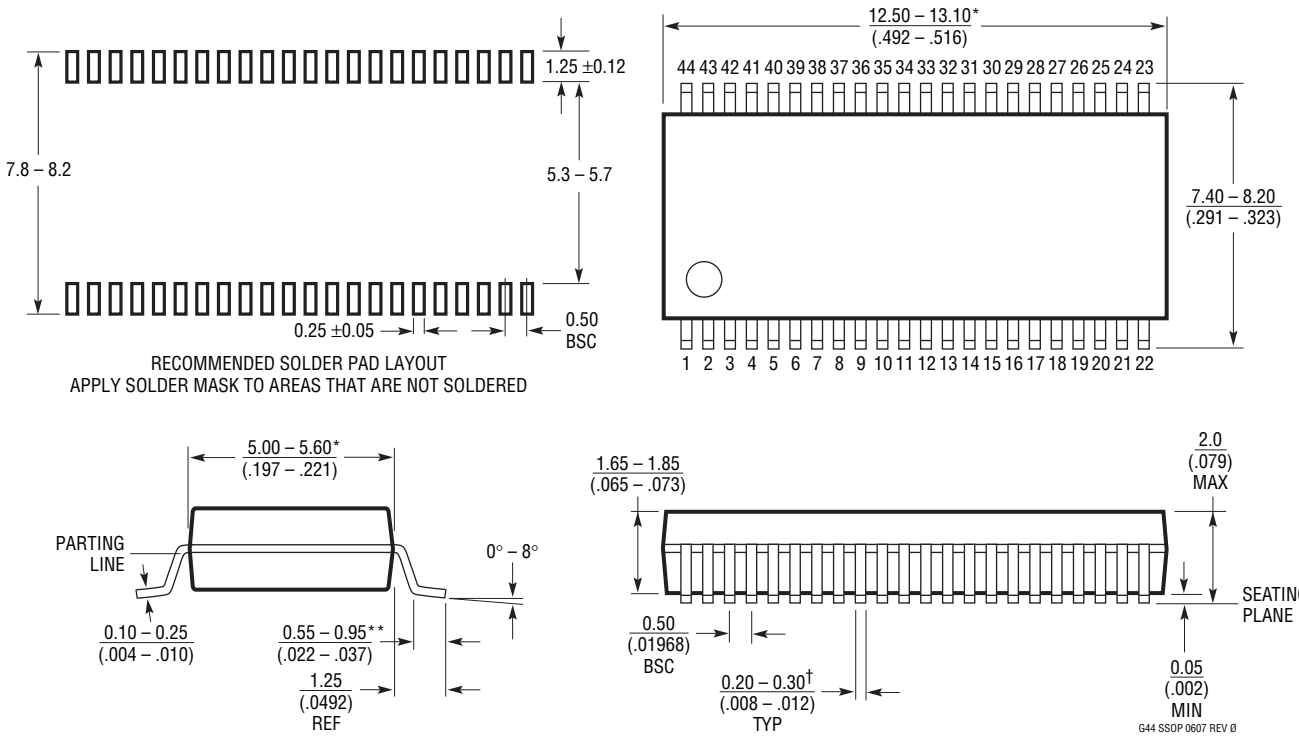
Thus if an analog filter is placed in front of a SAR converter to achieve the same noise rejection as the LTC6803 ADC, the SAR will have a slower response to input signals. For example, a step input applied to the input of the 850Hz filter will take 1.55ms to settle to 12 bits of precision, while the LTC6803 ADC settles in a single 1ms conversion cycle. This also means that very high sample rates do not provide any additional information because the analog filter limits the frequency response.

While higher order active filters may provide some improvement, their complexity makes them impractical for high channel count measurements as a single filter would be required for each input.

Also note that the SINC2 response has a 2nd order roll-off envelope, providing an additional benefit over a single pole analog filter.

PACKAGE DESCRIPTION

G Package
44-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1754 Rev Ø)



NOTE:
1.DRAWING IS NOT A JEDEC OUTLINE
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
4. DRAWING NOT TO SCALE
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH SHALL NOT EXCEED .15mm PER SIDE

**LENGTH OF LEAD FOR SOLDERRING TO A SUBSTRATE

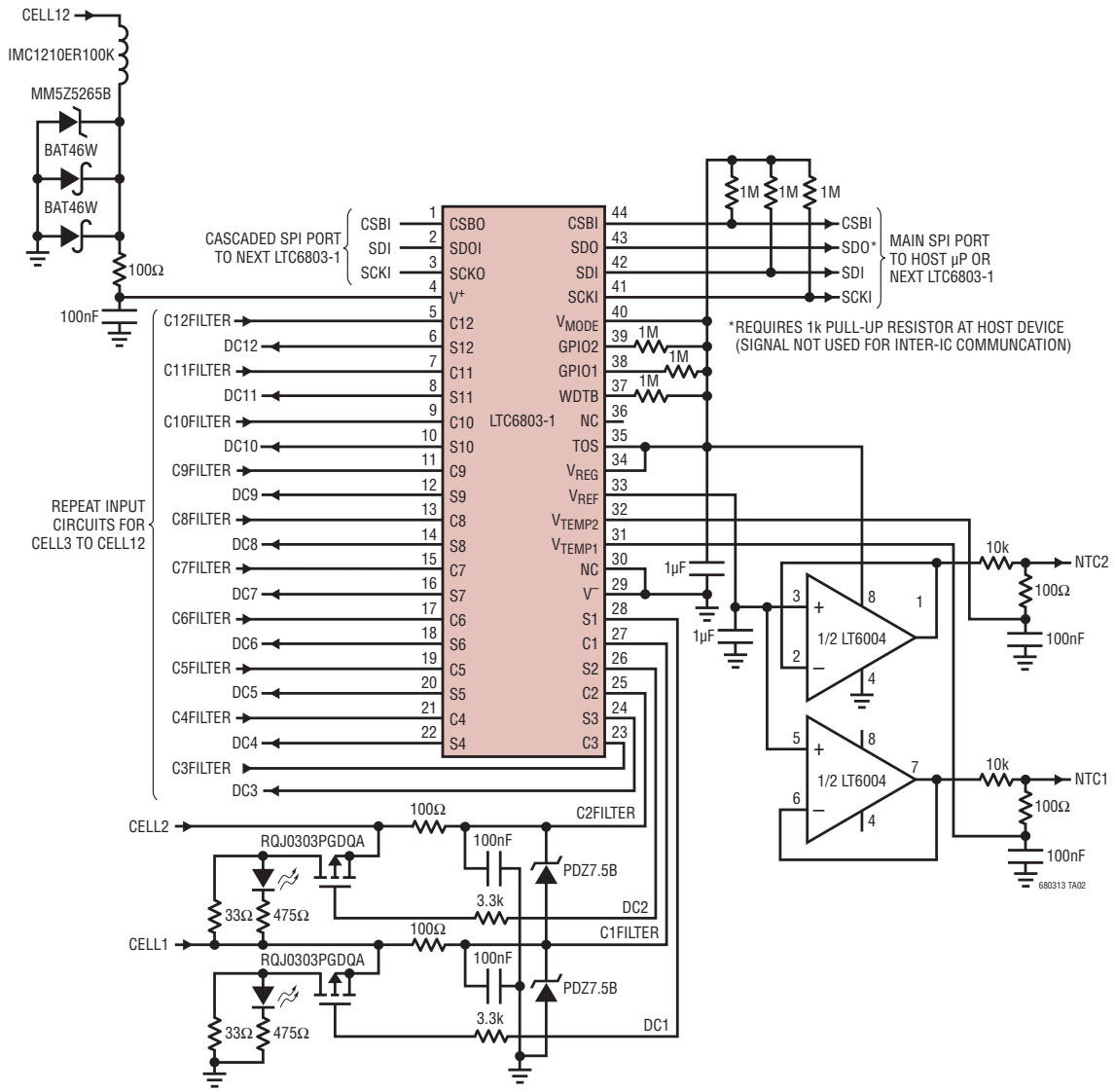
†THE MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS DO NOT EXCEED 0.13mm PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/12	Clarification to UV/OV Operation	14, 15
		Correction to 12-Cell Li-Ion Application Circuit	40

TYPICAL APPLICATION

Cascadable 12-Cell Li-Ion Battery Monitor



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6801	Independent Multicell Battery Stack Fault Monitor	Monitors Up to 12 Series-Connected Battery Cells for Undervoltage or Overvoltage. Companion to LTC6802 and LTC6803 Family
LTC6802-1	Multicell Battery Stack Monitor with Parallel Addressed Serial Interface	Functionally Equivalent to the LTC6803-1 and LTC6803-3, Pin Compatible with the LTC6803-1
LTC6802-2	Multicell Battery Stack Monitor with an Individually Addressable Serial Interface	Functionally Equivalent to LTC6803-2/LTC6803-4, Pin Compatible with the LTC6803-2
LTC6803-2/ LTC6803-4	Multicell Battery Stack Monitor with an Individually Addressable Serial Interface	Functionality Equivalent to LTC6803-1/LTC6803-3, Allows for Parallel Communication Battery Stack Topologies

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