THE DATASHEET OF

XRD5412AID-F

XRD5408/10/12

5V, Low Power, Voltage Output Serial 8/10/12-Bit DAC Family

May 2000-2

FEATURES

- 8/10/12-Bit Resolution
- Operates from a Single 5V Supply
- Buffered Voltage Output: 13μs Typical Settling Time
- 240μW Total Power Consumption (typ)
- Guaranteed Monotonic Over Temperature
- Flexible Output Range: 0V to V_{DD}
- 8 Lead SOIC and PDIP Package
- Power On Reset
- Serial Data Output for Daisy Chaining

APPLICATIONS

- Digital Calibration
- Battery Operated Instruments
- Remote Industrial Devices
- Cellular Telephones
- Motion Control

GENERAL DESCRIPTION

The XRD5408/10/12 are low power, voltage output digital-to-analog converters (DAC) for +3V power supply operation. The parts draw only 70μA of quiescent current and are available in both an 8-lead PDIP and SOIC package.

The XRD5408/10/12 have a 3 wire serial port with an output allowing the user to daisy chain several of them together. The serial port will support both Microwire™, SPI™, and QSPI™ standards.

The outputs of the XRD5408/10/12 are set at a gain of +2. The output short circuit current is 7mA typical.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRD5408AID	8 Lead 150 Mil JEDEC SOIC	-40°C to +85°C
XRD5408AIP	8 Lead 300 Mil PDIP	-40°C to +85°C
XRD5410AID	8 Lead 150 Mil JEDEC SOIC	-40°C to +85°C
XRD5410AIP	8 Lead 300 Mil PDIP	-40°C to +85°C
XRD5412AID	8 Lead 150 Mil JEDEC SOIC	-40°C to +85°C
XRD5412AIP	8 Lead 300 Mil PDIP	-40°C to +85°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ (510) 668-7017

BLOCK DIAGRAM

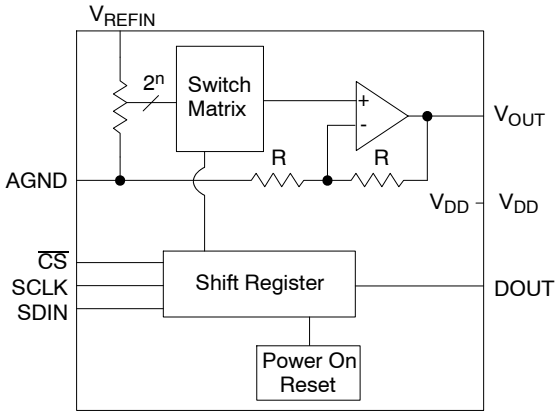
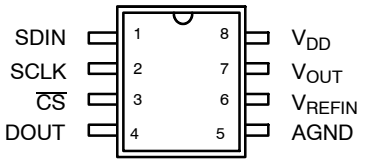
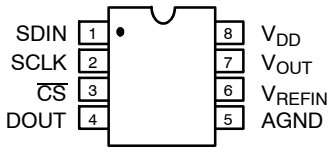


Figure 1. Block Diagram

PIN CONFIGURATION



8 Lead SOIC (Jedec, 0.150")



8 Lead PDIP (0.300")

PIN DESCRIPTION

Pin #	Symbol	Description
1	SDIN	Serial Data Input
2	SCLK	Serial Data Clock
3	$\overline{CS}$	Chip Select (Active High)
4	DOUT	Serial Data Output
5	AGND	Analog Ground
6	V_{REFIN}	Voltage Reference Input
7	V_{OUT}	DAC Output
8	V_{DD}	Supply Voltage

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD}= 5V, GND= 0V, REFIN= 2.048V (External), R_L= 10kΩ, C_L= 100pF, T_A= T_{MIN} to T_{MAX}, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Static Performance XRD5408						
N	Resolution	8			Bits	
INL	Relative Accuracy		0.25	0.5	LSB	
DNL	Differential Nonlinearity		0.25	0.5	` LSB	Guaranteed Monotonic
V_{OS}	Offset Error	0	3	8	mV	
TCV_{OS}	Offset Tempco		2		ppm/°C	
PSRR	Offset-Error Power-Supply Rejection Ratio		0.5	1	mV	$4.5V \leq V_{DD} \leq 5.5V$
GE	Gain Error		0.1	0.4	%FS	
TCGE	Gain-Error Tempco		10		ppm/°C	
PSRR	Power-Supply Rejection Ratio		0.1	1.25	mV	$4.5V \leq V_{DD} \leq 5.5V$, Measured at FS
Static Performance XRD5410						
N	Resolution	10			Bits	
INL	Relative Accuracy		0.5	1	LSB	
DNL	Differential Nonlinearity		0.25	0.5	` LSB	Guaranteed Monotonic
V_{OS}	Offset Error	0	3	8	mV	
TCV_{OS}	Offset Tempco		2		ppm/°C	
PSRR	Offset-Error Power-Supply Rejection Ratio		0.5	1	mV	$4.5V \leq V_{DD} \leq 5.5V$
GE	Gain Error		0.1	0.4	%FS	
TCGE	Gain-Error Tempco		10		ppm/°C	
PSRR	Power-Supply Rejection Ratio		0.1	1.25	mV	$4.5V \leq V_{DD} \leq 5.5V$, Measured at FS
Static Performance XRD5412						
N	Resolution	12			Bits	
INL	Relative Accuracy		2	4	LSB	
DNL	Differential Nonlinearity		0.5	-1	LSB	Guaranteed Monotonic
				+1.25	LSB	
V_{OS}	Offset Error	0	3	8	mV	
TCV_{OS}	Offset Tempco		2		ppm/°C	
PSRR	Offset-Error Power-Supply Rejection Ratio		0.5	1	mV	$4.5V \leq V_{DD} \leq 5.5V$
GE	Gain Error		0.1	0.4	%FS	
TCGE	Gain-Error Tempco		10		ppm/°C	
PSRR	Power-Supply Rejection Ratio		0.1	1.25	mV	$4.5V \leq V_{DD} \leq 5.5V$, Measured at FS

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: V_{DD}= 5V, GND= 0V, REFIN= 2.048V (External), R_L= 10kΩ, C_L= 100pF, T_A= T_{MIN} to T_{MAX}, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Voltage Output (V_{OUT}) XRD5408/10/12						
V_O	Output Voltage Range	0		V_{DD}–0.4	V	
V_{REG}	Output Load Regulation		2	4	mV	V_{OUT} = 2V, R_L=2kΩ
$+I_{SC}$	Short-Circuit Current, Sink		13		mA	V_{OUT} = V_{DD}
$-I_{SC}$	Short-Circuit Current, Source		7		mA	V_{OUT} = GND
Voltage Reference Input (V_{REFIN}) XRD5408/10/12						
V_{REFIN}	Voltage Range	0		V_{DD}	V	Output Swing Limited, Not Code Dependent
R_{IN}	Input Resistance	40	65		kΩ	
TCR_{IN}	Input Resistance Tempco		1500		ppm/°C	
C_{IN}	Input Capacitance		32	40	pF	Not Code Dependent
AC_{FT}	AC Feedthrough		-80		dB	REFIN = 1kHz, 2Vp-p, SD_{IN}=000h
Digital Inputs (SDIN, SCLK, $\overline{CS}$) XRD5408/10/12						
V_{IH}	Input High	3.5			V	
V_{IL}	Input Low			1	V	
I_{IN}	Input Current			` 1	µA	V_{IN}=0V or V_{DD}
C_{IN}	Input Capacitance		10		pF	
Digital Output (DOUT) XRD5408/10/12						
V_{OH}	Output High	V_{DD}-1			V	I_{SOURCE}=4mA
V_{OL}	Output Low			0.4	V	I_{SINK}=4mA
Dynamic Performance XRD5408/10/12						
SR	Voltage-Output Slew Rate	0.13	0.21		V/µs	T_A=+25°C
t_s	Voltage-Output Settling Time		13	15	µs	` 1/2LSB, V_{OUT}=2V
D_{FT}	Digital Feedthrough		1		nV-s	$\overline{CS}$=V_{DD}, SDIN=SCLK=100kHz
SINAD	Signal-to-Noise Plus Distortion		68		dB	V_{REFIN}=1kHz, 2Vp-p F.S., SDIN=Full Scale, –3dB BW=250kHz
Power Supply XRD5408/10/12						
V_{DD}	Positive Supply Voltage	4.5		5.5	V	
I_{DD}	Power Supply Current		35	60	µA	All Inputs=0V or V_{DD}, Output=No Load, I_{REF} Not Included, V_O=0V (Note [1])
Switching Characteristics XRD5408/10/12						
t_{CSS}	$\overline{CS}$ Setup Time	10	20		ns	
t_{CSH0}	SCLK Fall to $\overline{CS}$ Fall Hold Time	5			ns	
t_{CSH1}	SCLK Fall to $\overline{CS}$ Rise Hold TIme	0			ns	
t_{CH}	SCLK High Width	20	35		ns	
t_{CL}	SCLK Low Width	20	35		ns	

Notes:

[1] Total supply current consumption = I_{DD} + I_{REF} + (V_O / 70K.)

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: V_{DD}= 5V, GND= 0V, REFIN= 2.048V (External), R_L= 10kΩ, C_L= 100pF, T_A= T_{MIN} to T_{MAX}, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{DS}	D_{IN} Setup Time	10	45		ns	
t_{DH}	D_{IN} Hold Time	0			ns	
t_{DO}	D_{OUT} Valid Propagation Delay		8	15	ns	C_L= 50pF
t_{CSW}	$\overline{CS}$ High Pulse Width	20	40		ns	
t_{CS1}	$\overline{CS}$ Rise to SCLK Rise Setup Time	10	20		ns	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +7V
Digital Input Voltage to GND ..... -0.3V, V_{DD} +0.3V
V_{REFIN} ..... -0.3V, V_{DD} +0.3V
V_{OUT}[1] ..... V_{DD}, GND
Continuous Current, Any Pin ..... -20mA, +20mA

Package Power Dissipation Ratings (T_A= +70°C)
PDIP (derate 9mW/°C above +70°C) 117mW
SOIC (derate 6mW/°C above +70°C) ... 155mW
Operating Temperature Range ..... -40°C to + 85°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Notes

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2] Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes *which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.*

TIMING

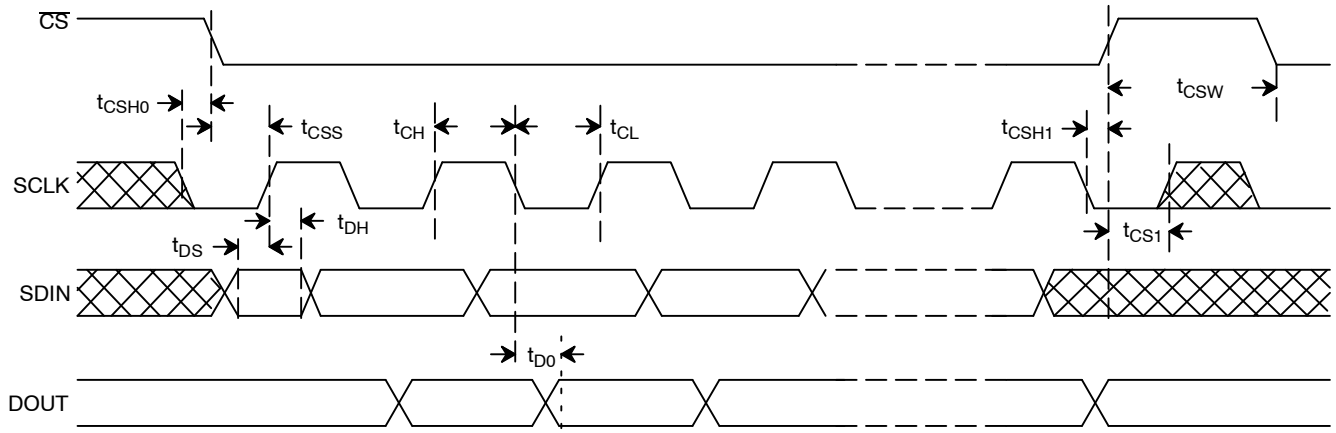


Figure 2. Timing Diagram

Input			Output
1111	1111	(0000)	$+ 2 (V_{REFIN}) \frac{255}{256}$
1000	0001	(0000)	$+ 2 (V_{REFIN}) \frac{129}{256}$
1000	0000	(0000)	$+ 2 (V_{REFIN}) \frac{128}{256} = + V_{REFIN}$
0111	1111	(0000)	$+ 2 (V_{REFIN}) \frac{127}{256}$
0000	0001	(0000)	$+ 2 (V_{REFIN}) \frac{1}{256}$
0000	0000	(0000)	0V

Note:
Write 8-bit data words with four sub-LSB 0s because the DAC input latch is 12 bits wide.

Table 1. Binary Code Table

THEORY OF OPERATION

XRD5408/10/12 Description

The XRD5408/10/12 are micro-power, voltage output, serial daisy-chain programmable DACs operating from a single 5V power supply. The DACs are built on a 0.6 micron CMOS process. The features of these DACs make it well suited for industrial control, low distortion audio, battery operated devices and cost sensitive designs that want to minimize pin count on ICs.

Resistor String DAC

A resistor string architecture converts digital data using a switch matrix to an analog signal as shown in *Figure 3.*

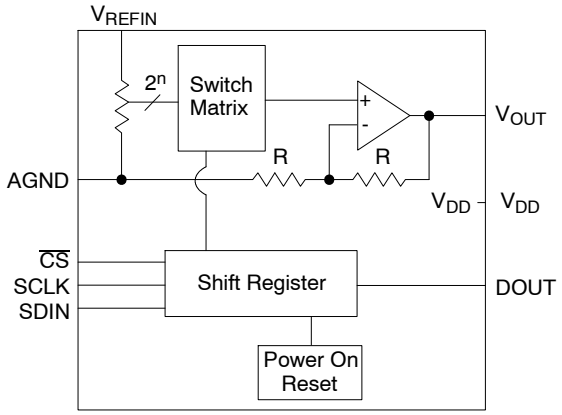


Figure 3. XRD5408/10/12 DAC Architecture

The resistor string architecture provides a non-inverted output voltage (V_{OUT}) of the reference input (V_{REFIN}) for single supply operation while maintaining a constant input resistance. Unlike inverted R-2R architectures the reference input resistance will remain constant independent of code. This greatly simplifies the analog driving source requirements for the reference voltage and minimizes distortion. Similarly input capacitance varies only approximately 4pF over all codes.

Fixed Gain +2 Voltage Output Amplifier

A high open-loop gain operational amplifier buffers the resistor string with a stable, fixed gain of +2. The voltage output will settle within 13□s. The output is short circuit protected and can regulate an output load of 2V into 2k□ within 2mV at 25°C.

While the reference input will accept a voltage from rail-to-rail, the linear input voltage range is constrained by the output swing of the fixed +2 closed-loop gain amplifier. Full scale output swing is achieved with an external reference of approximately 1/2 V_{DD}. The reference voltage must be positive because the XRD5408/10/12 DAC is non-inverting.

Serial Daisy-Chainable Digital Interface

The three wire serial interface includes a DOUT to enable daisy-chaining of several DACs. This minimizes pin count necessary of digital asics or controllers to address multiple DACS. The serial interface is designed for CMOS logic levels. Timing is shown in *Figure 2*. The binary coding table (*Table 1)* shows the DAC transfer function.

A power on reset circuit forces the DAC to reset to all “0”s on power up.

APPLICATION NOTES

Serial Interface

The XRD5408/10/12 family has a three wire serial interface that is compatible with Microwire™, SPI™ and QSPI™ standards. Typical configurations are shown in *Figure 4 and Figure 5*. Maximum serial port clock rate is limited by the minimum pulse width of t_{CH} and t_{CL}. Feedthrough noise from the serial port to the analog output (V_{OUT}) is minimized by lowering the frequency of the serial port and holding the digital edges to >5ns.

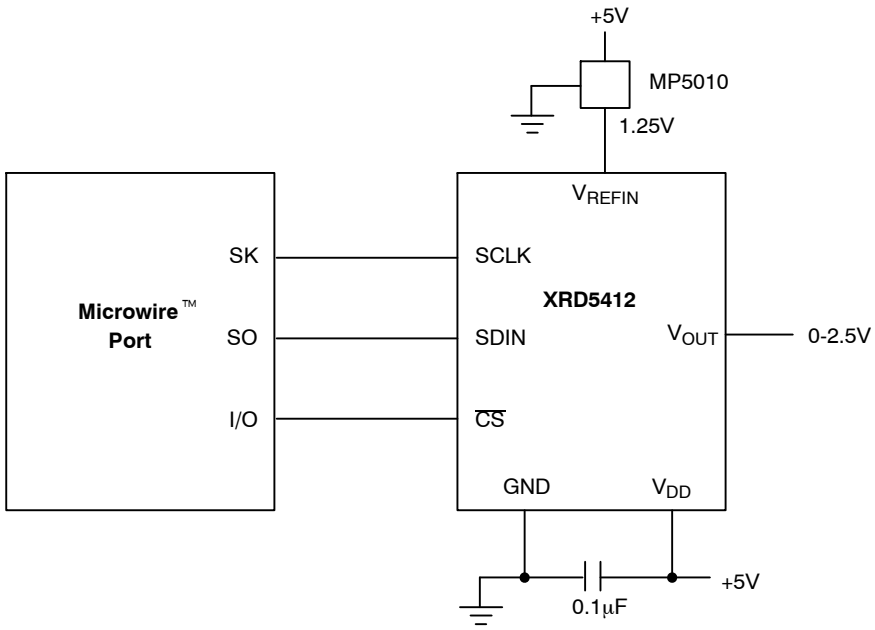


Figure 4. Typical Microwire™ Application Circuit

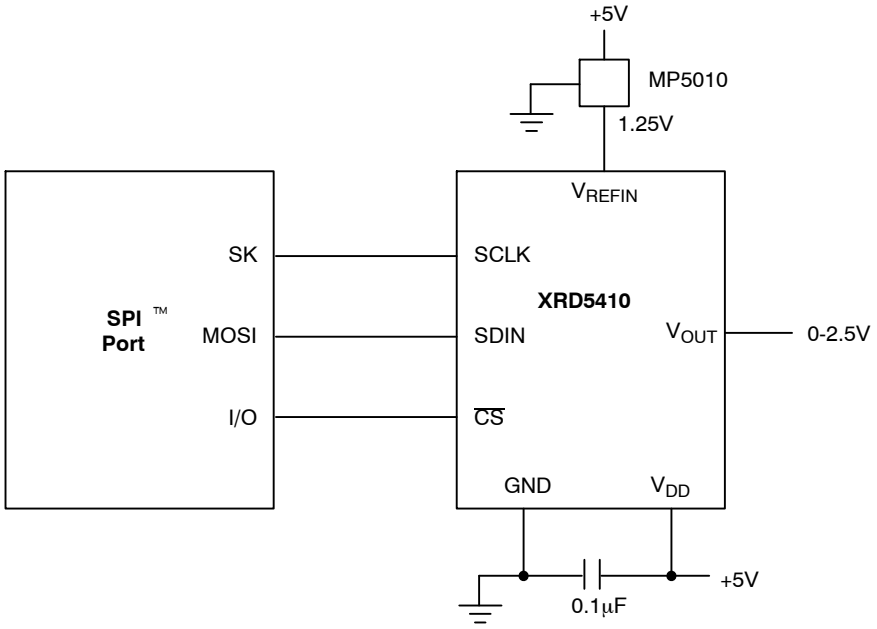


Figure 5. Typical SPI™ Application Circuit

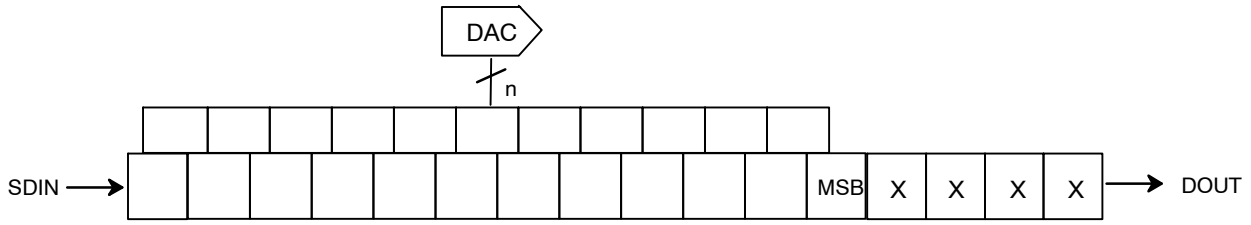


Figure 6. Shift Register Format

The DACs are programmed by a 16 bit word of serial data. The format of the serial input register is shown in Figure 6. The leading 4 bits are not used to update the DAC. If the DAC is not daisy-chained then only a 12 bit serial word is needed to program the DAC. The next 8, 10 or 12 bits after the 4 leading bits are data bits. The XRD5408's first 8 bits are valid data and the trailing 4 bits must be set to 0. *Figure 7* demonstrates the 16 bit digital word for the 8, 10,12 bit DACs.

Part	Leading Unused Bits	Data Bits MSB LSB	Trailing "0" Bits
XRD5412	XXXX	XXXXXXXX	None
XRD5410	XXXX	XXXXXXXX	00
XRD5408	XXXX	XXXXXXXX	0000

Table 2. 16-Bit Digital Word Register for XRD5408, XRD5410, XRD5412.

SCLK should be held low when $\overline{CS}$ transitions low. Data is clocked in on the rising edge of SCLK when $\overline{CS}$ is low. SDIN data is held in a 16 bit serial shift register. The DAC is updated with the data bits on the rising edge of $\overline{CS}$. When $\overline{CS}$ is high data is not shifted into the XRD5408/10/12.

Daisy-Chaining

The digital output port (DOUT) has a 4mA drive for greater fan-out capability when daisy-chaining. DOUT allows cascading of multiple DACs with the same serial data stream. The data at SDIN appears at DOUT after 16 clock cycles plus one clock width (t_{CH}) and a propagation delay (t_{DO}). DOUT remains in the state of the last data bit when $\overline{CS}$ is high. DOUT changes on the falling edge of SCLK when $\overline{CS}$ is low.

Any number of DACs can be connected in this way by connecting DOUT of one DAC to SDIN of the next DAC.

AC_{FT} Feedthrough (DAC Code = 0)

AC Feedthrough from V_{REFIN} to V_{OUT} is minimized with low impedance grounding as shown in *Figure 7*. If the DAC data is set to all "0"s then V_{OUT} is a function of the divider between the DAC string impedance and ground impedance. See the Power Supply and Grounding section for recommendations. The typical AC feedthrough for a 1kHz 2Vpp signal with code = 0 is -80dB.

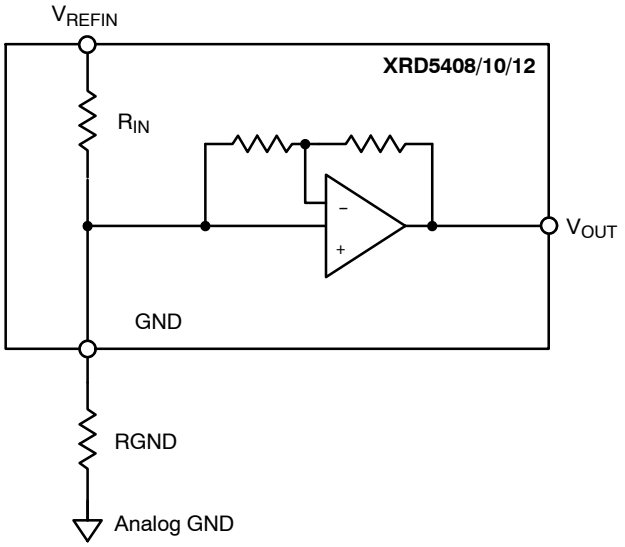


Figure 7. AC_{FT} Feedthrough Equivalent Circuit, DAC Code =0

Compatible with MAX515 & MAX539

The XRD5408/10/12 family of DACs are functionally campatible with the MAX515 & MAX539 while providing significant improvements. The XRD5408/10/12 DACs have lower power, faster serial ports, and a constant reference impedance to minimize the reference driving requirements and maximize system linearity. The DOUT

port also has 4mA driving capability for greater fan-out when daisy-chaning to other digital inputs.

Monotonicity

The XRD5408/10/12 family of DACs are monotonic over the entire temperature range.

Micro-Power Operation

The XRD5408 is the lowest power in their class. The quiescent current rating does not include the reference ladder current. Power can be saved when the part is not in use by setting the DAC code to all “0”s assuming the output load is referenced to ground. This minimizes the DAC output load current. An analog switch placed in series with the reference ladder can toggle the reference voltage off when the circuit is inactive to minimize power consumption.

Power Supply and Grounding

Best parametric results are obtained by powering the XRD5408/10/12 family of DACs from an analog +5V power supply and analog ground. Digital power supplies and grounds should be separated or connected to the analog supplies and grounds only at the low-impedance power-supply source. This is best accomplished on a multilayer PCB with dedicated planes to ground and power. The DACs should be locally bypassed with both 0.1 □F and 2.2 □F capacitors mounted as close as possible to the power supply pin (V_{DD}). Surface mount ceramic capacitors are recommended for low impedance, wide band power supply bypass. If only one +5V power supply is available for both analog and digital circuity isolate the analog power supply to the XRD5408/10/12 DAC with an inductor or ferrite bead before the local bypass capacitors.

PERFORMANCE CHARACTERISTICS

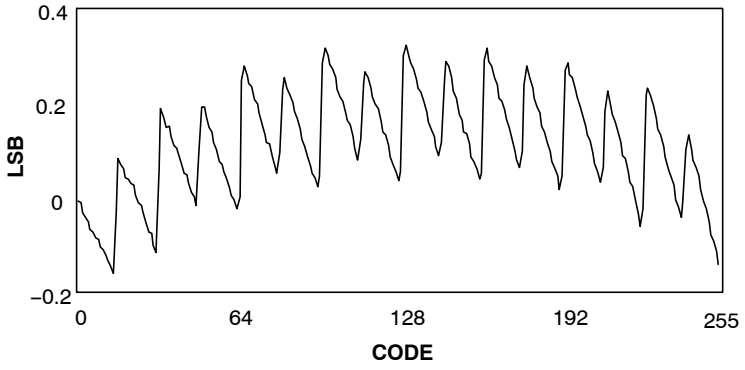


Figure 8. XRD5408 INL

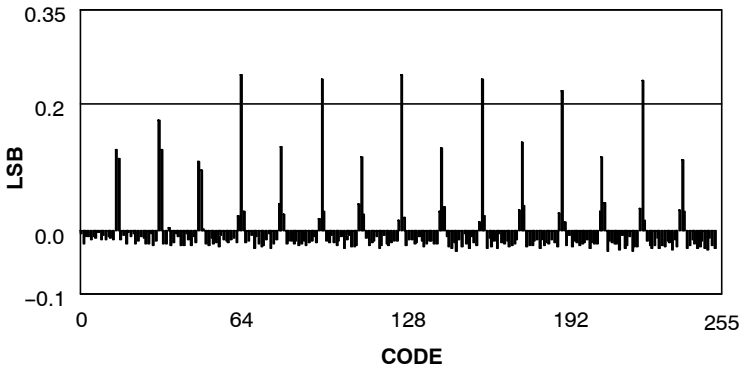


Figure 9. XRD5408 DNL

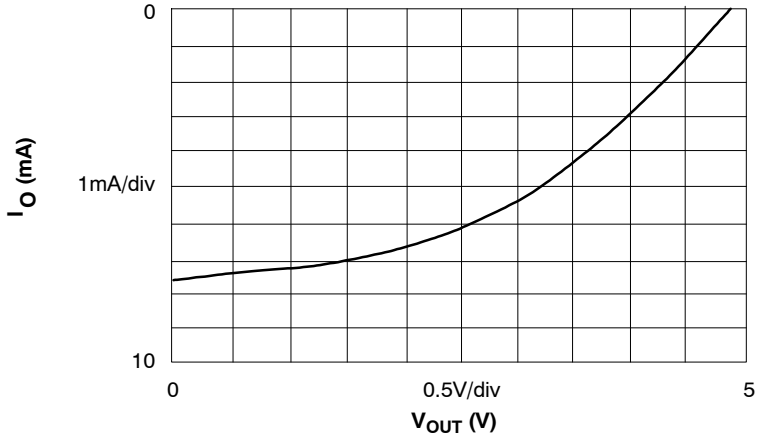


Figure 10. Output Source Current vs. Output Voltage

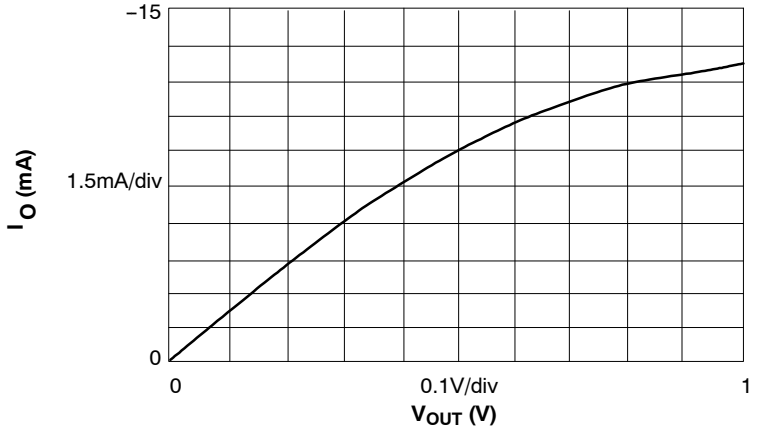


Figure 11. Output Sink Current vs. Output Voltage

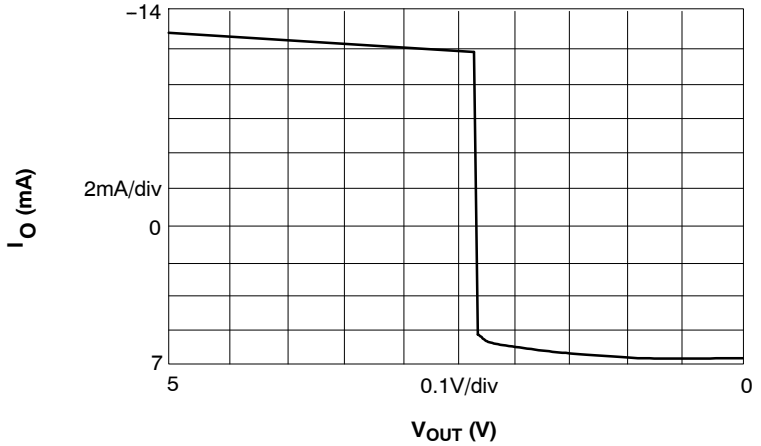


Figure 12. Output Sink and Source Current vs. Output Volatge

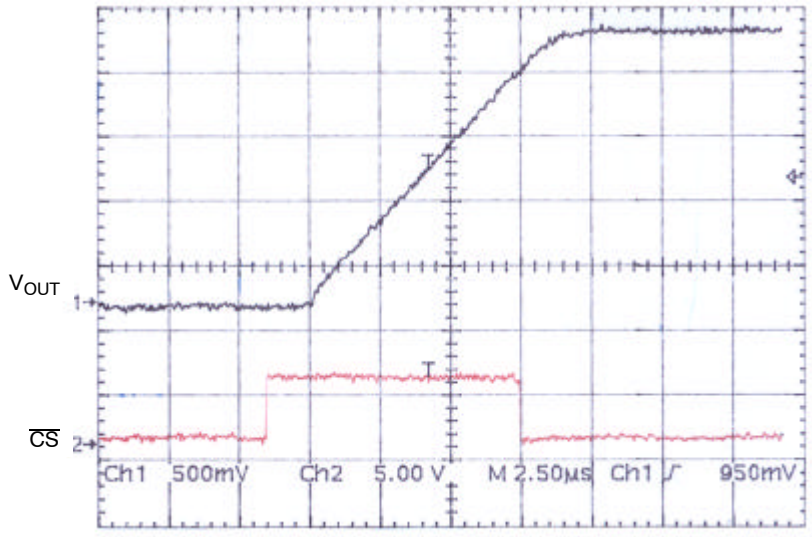


Figure 13. Voltage Output Settling Time (t_S), V_{DD} = 5V, V_{REFIN} = 1V, No Load

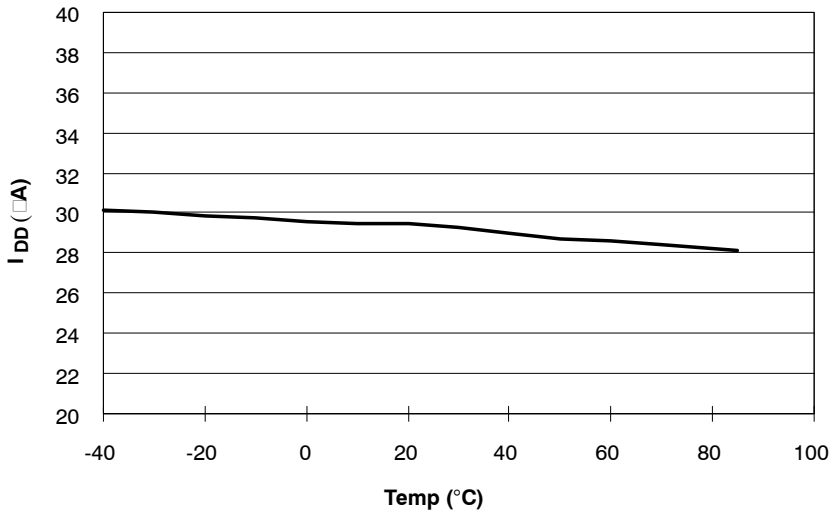


Figure 14. I_{DD} vs. Temperature

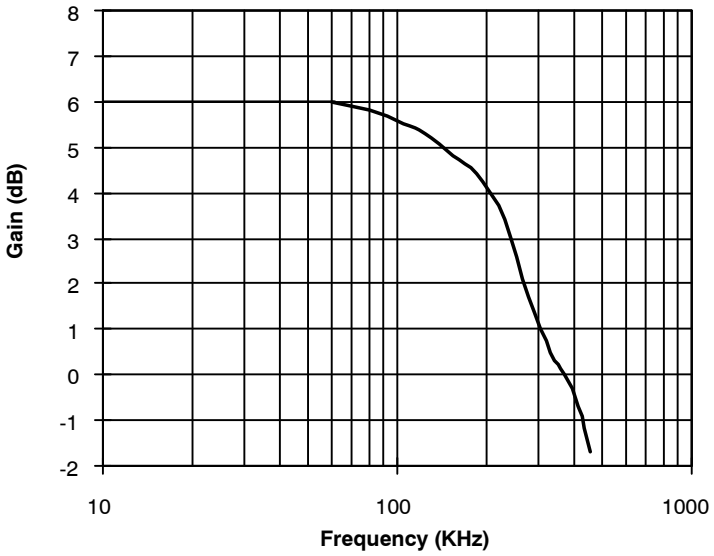


Figure 15. Closed Loop Gain vs. Frequency

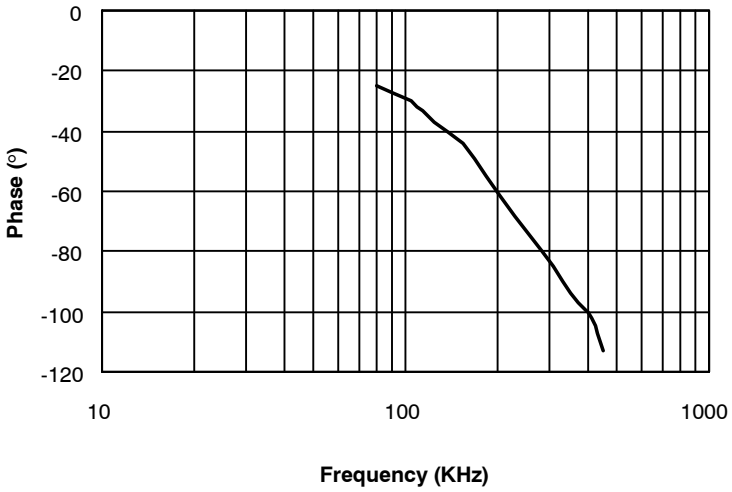


Figure 16. Closed Loop Phase vs. Frequency

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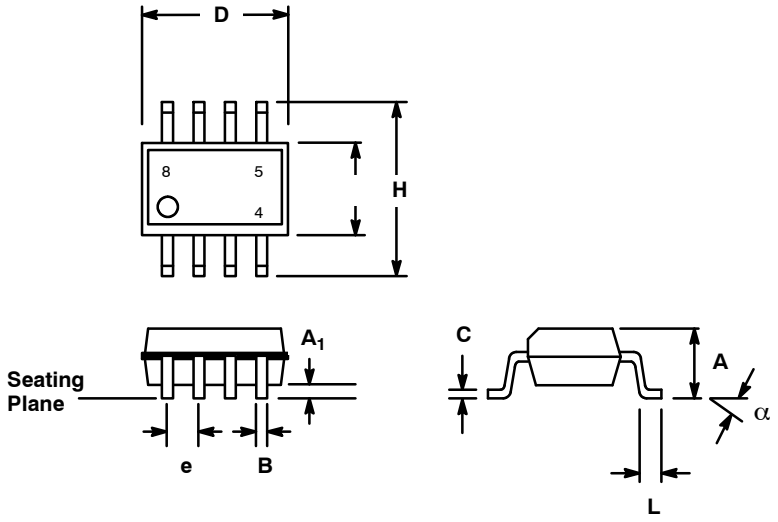
SPI™ and **QSPI**™ are trademarks of Motorola Corporation.

8 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)

Rev. 1.00

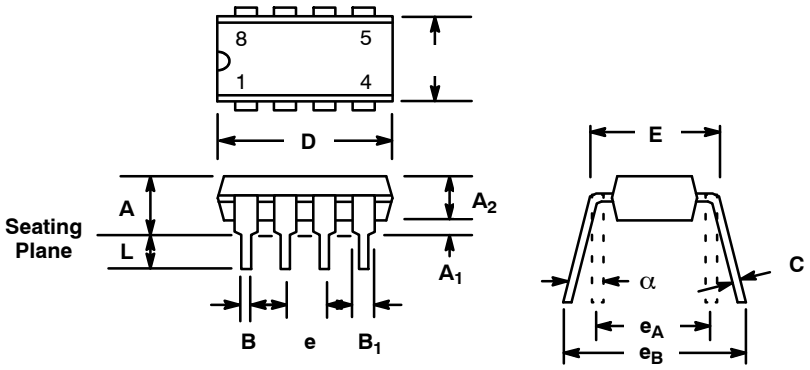


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A_1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

8 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 2.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.348	0.430	8.84	10.92
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

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Datasheet May 2000

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