TEF6862

Car Radio Enhanced Selectivity Tuner (CREST)

Rev. 01 — 14 September 2006 Product data sheet

1. General description

The TEF6862 is a single-chip car radio tuner for AM, FM and weather band reception providing AM double conversion for LW, MW and full range SW (11 m to 120 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz.

FM double conversion to IF1 = 10.7 MHz and IF2 = 450 kHz with integrated image rejection for both IF1 and IF2; integrated IF filter with variable bandwidth and automatic bandwidth control algorithm with flexibility via the I^2C-bus; capable of US FM, Europe FM, Japan FM, East Europe FM and weather band reception; all FM bands can be selected using high injection LO or low injection LO in the FM mixer 1.

Tuning system including crystal oscillator, VCO, PLL synthesizer and state machine for timing uncritical control of search, preset change and AF check via microcontroller.

2. Features

- High dynamic range FM front-end mixer for conversion of FM RF (65 MHz to 108 MHz and USA weather band) to an IF frequency of 10.7 MHz; mixer provides inherent image rejection which can be switched from low injection LO to high injection LO via the I^2C-bus
- FM front-end AGC PIN diode drive circuit; AGC detection at the FM font-end mixer input and the IF filter input; AGC threshold for detection at the mixer input is programmable and keyed AGC function can be selected via the I^2C-bus; the AGC PIN diode drive can be activated by the I^2C-bus for a search tuning in local mode; in AM mode the AGC PIN diode drive can be activated by the I^2C-bus if required; information on amount of PIN diode AGC is available via the I^2C-bus
- FM front-end mixer includes +6 dB gain setting via the I^2C-bus
- FM second mixer for conversion of IF1 10.7 MHz to IF2 450 kHz including inherent image rejection; the gain can be controlled via the I^2C-bus
- Integrated FM channel selection filter with continuous variable bandwidth providing simultaneous low distortion and high selectivity with only one external ceramic filter; improved sensitivity with dynamic threshold extension can be enabled via the I^2C-bus
- Fully integrated FM demodulator with very low distortion
- Digital bandwidth control algorithm with detection on adjacent channel information, deviation, detuning and level with customer flexibility via the I^2C-bus
- Digital alignment circuit for bus controlled adjustment of oscillator tuning voltage to two FM antenna tank circuit tuning voltages; AM and FM level start and slope alignment; IF filter and demodulator center frequency alignment
- AM and FM level detection (signal strength indication)
- Separate RF input to FM front-end mixer for weather band
- Flag or voltage output indicators for actual IF bandwidth information

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- AM front-end mixer for conversion of AM RF to an IF frequency of 10.7 MHz
- AM RF AGC circuit for external cascode AGC and PIN diode AGC
- AM noise blanker with detection at IF1 and blanking at IF2
- AM second mixer for conversion of IF1 10.7 MHz to IF2 450 kHz; IF2 AGC amplifier and AM demodulator with low distortion
- For AM stereo applications the gain controlled AM IF2 output voltage can be switched to MPXAM output pin via the I^2C-bus
- Crystal oscillator providing frequency for second conversion, references for synthesizer PLL and analog signal processor and timing for tuning action
- LC tuning oscillator with low phase noise and oscillator dividers with selectable divider ratios for worldwide tuner reception without band switching in application
- Fast synthesizer PLL tuning system with dynamically adapting loop parameters combining fast PLL frequency jumps for inaudible RDS updating with low spurious responses for large signal-to-noise ratios
- Sequential state machine for preset change, search and inaudible AFU allowing a timing uncritical microcontroller operation; the state machine generates timing signals for the internal inaudible tuning mute and analog or digital signal processor
- An alternative frequency check can be initiated by the signal processor for audio correlation algorithms directly without involvement of the microcontroller
- Audio soft slope tuning mute circuit allowing inaudible AFU
- Two hardware programmable I^2C-bus addresses
- Two software controlled flag outputs
- Several test modes for fast IC and system tests

3. Quick reference data

Table 1. Quick reference data

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_{CCA}	analog supply voltage	on pins VCC, VCCPLL, VCCVCO, VCCRF, AMMIX2OUT1, AMMIX2OUT2, MIX1OUT1 and MIX1OUT2	8	8.5	9	V
Current in FM mode						
$I_{CC(tot)}$	total supply current		-	101.9	-	mA
Current in AM mode						
$I_{CC(tot)}$	total supply current		-	84.4	-	mA
Tuning system; see Table 37, Table 38 and Table 39						
Timings						
t_{tune}	tuning time	Europe FM and US FM band; f_{ref} = 100 kHz; f_{RF} = 87.5 MHz to 108 MHz	-	0.75	1	ms
		AM MW band; f_{ref} = 20 kHz; f_{RF} = 0.53 MHz to 1.7 MHz	-	-	10	ms
$t_{upd(AF)}$	AF update time	cycle time for inaudible AF update including 1 ms mute start and 1 ms mute release time	-	6	6.5	ms

Table 1. Quick reference data *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM overall system parameters[1]						
$f_{i(RF)}$	RF input frequency	LW	144	-	288	kHz
		MW	522	-	1710	kHz
		SW	2.3	-	26.1	MHz
V_{sens}	sensitivity voltage	(S+N)/N = 26 dB	-	45	-	µV
(S+N)/N	signal plus noise-to-noise ratio		54	58	-	dB
THD	total harmonic distortion	200 µV < $V_{i(RF)}$ < 1 V; m = 0.8	-	0.5	1	%
IP3	third-order intercept point		-	130	-	dBµV
FM overall system parameters[2]						
$f_{i(RF)}$	RF input frequency		65	-	108	MHz
V_{sens}	sensitivity voltage	(S+N)/N = 26 dB				
		IF bandwidth wide	-	2	-	µV
		IF bandwidth dynamic; threshold extension off	-	1.8	-	µV
		IF bandwidth dynamic; threshold extension on	-	1.6	-	µV
(S+N)/N	signal plus noise-to-noise ratio	V_i = 3 mV; IF bandwidth wide	-	63	-	dB
THD	total harmonic distortion	Δf = 75 kHz	-	0.2	0.7	%
IP3	third-order intercept point		-	123	-	dBµV
Weatherband overall system parameters[2]; see Figure 27						
$f_{i(RF)}$	RF input frequency		162.4	-	162.55	MHz
(S+N)/N	signal plus noise-to-noise ratio	Δf = 1.5 kHz; $V_{i(RF)}$ = 10 mV; de-emphasis = 120 µs	-	45	-	dB
THD	total harmonic distortion	Δf = 5 kHz	-	0.7	-	%

[1] Based on 15 pF/60 pF dummy aerial, voltages at dummy aerial input, f_{mod} = 400 Hz, 2.15 kHz audio bandwidth, $f_{i(RF)}$ = 990 kHz, m = 0.3, unless otherwise specified.

[2] Based on 75 Ω dummy aerial, voltages at dummy aerial input, f_{mod} = 1 kHz, de-emphasis = 50 µs, B = 300 Hz to 22 kHz, Δf = 22.5 kHz, unless otherwise specified.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEF6862HL	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

5. Block diagram

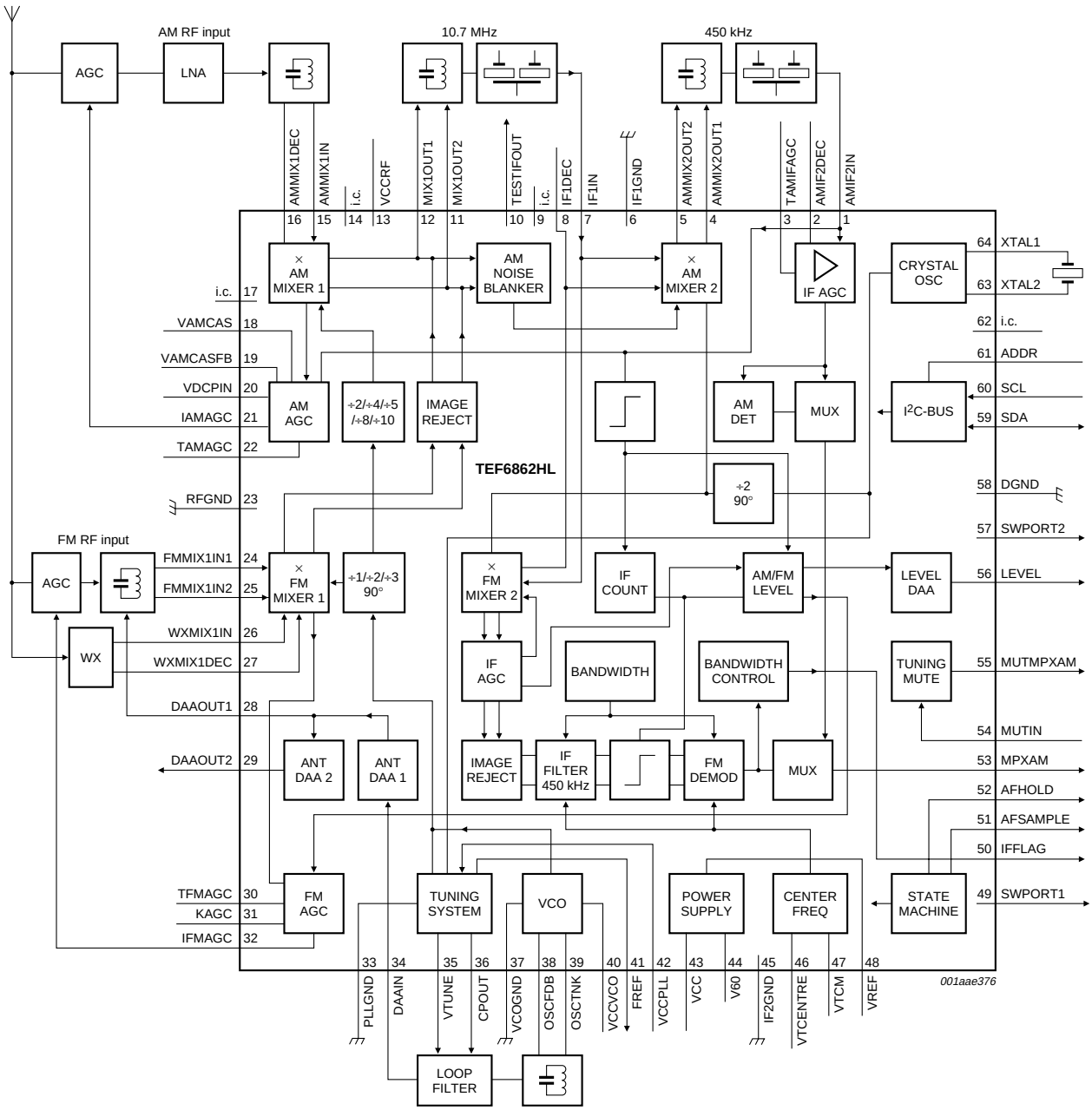


Fig 1. Block diagram of TEF6862HL

6. Pinning information

6.1 Pinning

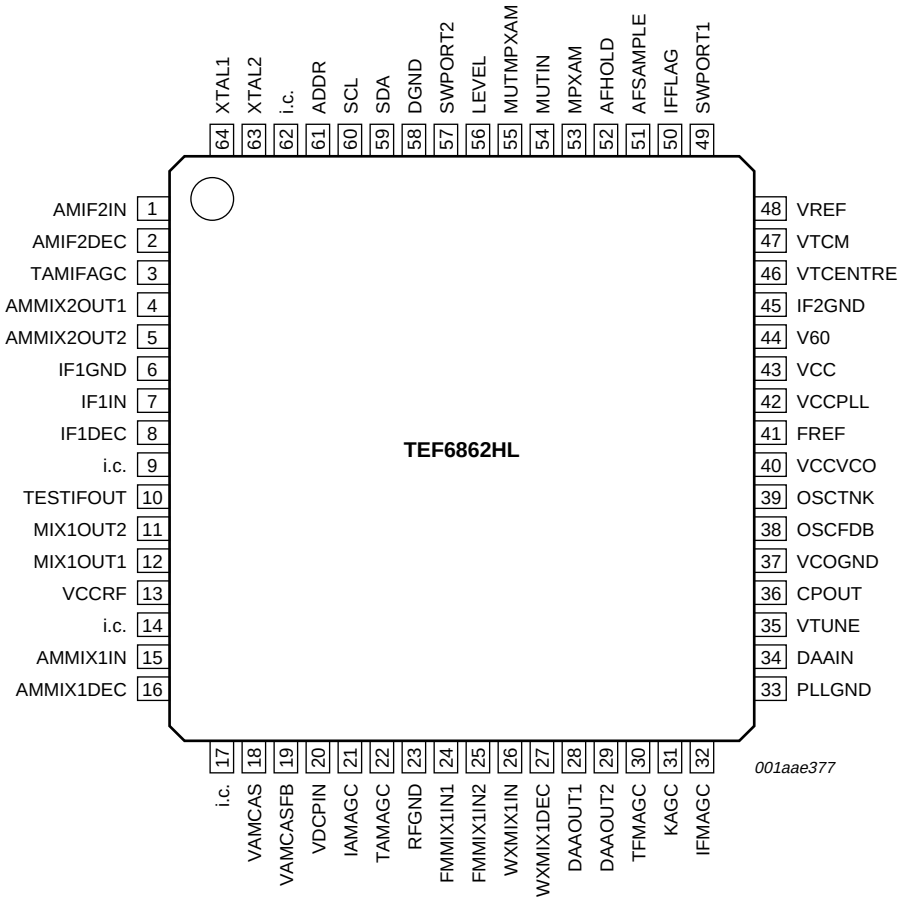


Fig 2. Pin configuration for LQFP64

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
AMIF2IN	1	AM IF2 input
AMIF2DEC	2	decoupling for AM IF2 input
TAMIFAGC	3	time constant of AM IF AGC
AMMIX2OUT1	4	AM mixer 2 output 1
AMMIX2OUT2	5	AM mixer 2 output 2
IF1GND	6	IF1 ground
IF1IN	7	AM and FM mixer 2 input
IF1DEC	8	AM and FM mixer 2 decoupling
i.c.	9	internally connected; leave open

Table 3. Pin description *…continued*

Symbol	Pin	Description
TESTIFOUT	10	test pin IF filter output
MIX1OUT2	11	AM and FM mixer 1 output 2 at IF1
MIX1OUT1	12	AM and FM mixer 1 output 1 at IF1
VCCRF	13	supply voltage for AM and FM RF
i.c.	14	internally connected; leave open
AMMIX1IN	15	AM mixer 1 input
AMMIX1DEC	16	AM mixer 1 decoupling
i.c.	17	internally connected; leave open
VAMCAS	18	cascode AM AGC
VAMCASFB	19	feedback for cascode AM AGC
VDCPIN	20	5 V bias voltage for AM PIN diode
IAMAGC	21	AGC current for AM PIN diode
TAMAGC	22	time constant of AM RF AGC
RFGND	23	RF ground
FMMIX1IN1	24	FM mixer 1 input 1
FMMIX1IN2	25	FM mixer 1 input 2
WXMIX1IN	26	weather band mixer input
WXMIX1DEC	27	weather band mixer decoupling
DAAOUT1	28	antenna DAA output 1
DAAOUT2	29	antenna DAA output 2
TFMAGC	30	time constant of FM RF AGC
KAGC	31	time constant of keyed FM front-end AGC
IFMAGC	32	PIN diode drive current output of FM front-end AGC
PLLGND	33	ground for tuning PLL
DAAIN	34	input of DAA circuit for antenna tank circuit
VTUNE	35	tuning voltage; 3 mA charge pump output
CPOUT	36	charge pump output
VCOGND	37	VCO ground
OSCFDB	38	VCO feedback
OSCTNK	39	VCO tank circuit
VCCVCO	40	VCO supply voltage
FREF	41	reference frequency output
VCCPLL	42	supply voltage for tuning PLL
VCC	43	supply voltage (8.5 V)
V60	44	input for FM filter and demodulator supply current
IF2GND	45	FM IF2 ground
VTCENTRE	46	filtering of tuning voltage of center frequency
VTCM	47	reference for filtering of tuning voltage of center frequency
VREF	48	reference voltage for noise decoupling
SWPORT1	49	software port output 1
IFFLAG	50	FM IF2 bandwidth voltage flag

Table 3. Pin description *...continued*

Symbol	Pin	Description
AFSAMPLE	51	AF sample flag output
AFHOLD	52	AF hold flag output and input
MPXAM	53	not muted FM or AM demodulator output and IF output for AM stereo
MUTIN	54	input of tuning mute circuit
MUTMPXAM	55	FM MPX output or AM output from tuning mute
LEVEL	56	level voltage output for AM and FM
SWPORT2	57	software port output 2
DGND	58	digital ground
SDA	59	I^2C-bus data line input and output
SCL	60	I^2C-bus clock line input
ADDR	61	address select
i.c.	62	internally connected
XTAL2	63	crystal oscillator 2
XTAL1	64	crystal oscillator 1

7. Functional description

7.1 FM mixer 1

The FM quadrature mixer converts FM RF (65 MHz to 108 MHz and 162.4 MHz to 162.55 MHz) to an IF of 10.7 MHz. The FM mixer provides inherent image rejection and a large dynamic range. The image rejection can be switched from low injection LO to high injection LO via the I^2C-bus independently of the band selection. The gain can be increased by 6 dB via the I^2C-bus.

7.2 FM RF AGC

AGC detection at the FM front-end mixer input with programmable threshold. When the threshold is exceeded, the PIN diode drive circuit sources a current to an external PIN diode circuit, keeping the mixer input signal level constant.

Keyed AGC function is selectable via the I^2C-bus and uses the in-band level information derived from the limiter level detector.

The AGC PIN diode drive circuit can be forced via the I^2C-bus to deliver a fixed current as a local function for search tuning. In AM mode, the AGC PIN diode drive circuit can also be forced via the I^2C-bus to deliver the maximum source current into the external FM PIN diode circuitry. AGC information is available via the I^2C-bus.

7.3 FM mixer 2

The FM quadrature mixer converts 10.7 MHz FM IF1 to 450 kHz FM IF2 and includes inherent image rejection. The gain can be selected via I^2C-bus to compensate for different ceramic filter insertion loss.

7.4 FM IF2 channel filter

The order and dynamic range of the filter is designed for operation with only one external ceramic filter in the application. The filter characteristic is optimized to combine high selectivity with low distortion from maximum to minimum IF bandwidth settings. The bandwidth of the filter can be selected directly with 5 bits via the I^2C-bus or automatically via the bandwidth control algorithm. When the automatic mode is selected the bandwidth depends on the signal conditions: the amount of adjacent channel, the deviation of the desired signal, detuning and signal strength.

The filter center frequency is I^2C-bus aligned with 6 bits.

7.5 FM limiter and level detection

The limiter amplifies the IF filter output signal, removes AM modulations from the IF signal and supplies a well defined signal for the FM demodulator. From the limiter also the RSSI is derived which is converted to a suitable level voltage with minimum temperature drift.

7.6 FM demodulator

The fully integrated FM demodulator converts the IF signal from the limiter to the FM MPX output signal with very low distortion. The center frequency of the filter in the demodulator is aligned together with the IF2 filter center frequency.

7.7 Audio output buffer

The output buffer for AM and FM amplifies the demodulated signal and includes low-pass filtering to attenuate any IF residual signals. The gain is increased in weather band reception to compensate for the low frequency deviation.

7.8 Tuning mute

The audio soft slope tuning mute circuit is controlled by the sequential machine for different tuning actions to eliminate audible effects. Control signals are generated to control the muting and the weak signal processing in the signal processor.

7.9 Weather band input

A separate RF input to the FM front-end mixer for weather band makes the weather band application easier.

7.10 IF filter and demodulator tuning

The center frequency as well as the bandwidth of both the IF filter and demodulator are coupled to the stable crystal reference frequency. Fine adjustment is achieved with a 6-bit DAA.

7.11 VCO and dividers

The varactor tuned LC oscillator together with the dividers provides the local oscillator signal for both AM and FM front-end mixers. The VCO has an operating frequency of approximately 160 MHz to 256 MHz. In FM mode the LO frequency is divided by 1, 2 or 3.

These dividers generate in-phase and quadrature-phase output signals used in the FM front-end mixer for image rejection. In AM mode the LO frequency is divided by 6, 8, 10, 16 or 20 depending on the selected AM band.

7.12 Crystal oscillator

The linear crystal oscillator provides a 20.5 MHz signal. A divider-by-two generates in-phase and quadrature-phase mixer frequencies for the conversion from IF1 to IF2 including image rejection. The reference divider generates from the crystal frequency various reference frequencies for the tuning PLL. Also the different timing signals for the sequential machine as well as the analog signal processor reference frequency are derived from the crystal reference.

7.13 Tuning PLL

The tuning PLL locks the VCO frequency divided by the programmable divider ratio to the reference frequency. Due to the combination of different charge pump signals in the PLL loop filter, the loop parameters are adapted dynamically. Tuning to different radio frequencies is done by changing the programmable divider ratio. The tuning step size is selected with the reference frequency divider setting.

7.14 Antenna DAA

The antenna DAA measures the VCO tuning voltage and multiplies it with a factor defined by the 7-bit DAA1 setting to generate a tuning voltage for the FM antenna tank circuit. A second tuning voltage (DAA output 2) for an optional second FM tank circuit is derived from the first tuning voltage with 4 bits.

7.15 AM RF AGC

The AM front-end is designed for the application of an external JFET low noise amplifier with cascode AGC and PIN diode AGC both controlled by an integrated AGC circuit. Four AGC thresholds of the detector at the first mixer input are selectable via I^2C-bus. A further detector at the IF AGC input prevents undesired overload (see Figure 21). AGC information can be read out via I^2C-bus. The PIN diode current drive circuit includes a pull-up current source for reverse biasing of the PIN diode, when the AGC is not active to achieve a low parasitic capacitance.

7.16 AM mixer

The large dynamic range AM mixer converts AM RF (144 kHz to 26.1 MHz) to an IF of 10.7 MHz.

7.17 AM IF noise blanker

The spike detection for the AM noise blanker is at the output of the AM front-end mixer. Blanking is realized at the output of the second AM mixer. The sensitivity of the noise blanker can be set in three settings and switched off via I^2C-bus.

7.18 AM IF AGC amplifier and demodulator

The 450 kHz IF2 signal after the ceramic channel selection filter is amplified by the IF AGC amplifier and demodulated. Instead of the demodulated AM audio signal, also the IF2 signal can be selected on the MPXAM output pin. This IF2 signal can be used for an external AM stereo decoder. To avoid overdrive of the input stage a detector at the input drives the RF AGC.

7.19 AM level detection

The IF2 signal used for AM IF AGC and demodulation is also used in the limiter circuit for in-band level detection to generate a level voltage.

7.20 AM and FM level DAA

The start and slope of the level detector output are programmable with 5 bits and 3 bits respectively to achieve level information independent on gain variations in the signal channel.

7.21 AM and FM IF counter

The output signal from the limiters is used for IF counting in both AM and FM. The IF count time is automatically controlled to achieve the optimum counting accuracy. The minimum count time is 2 ms.

8. I²C-bus protocol

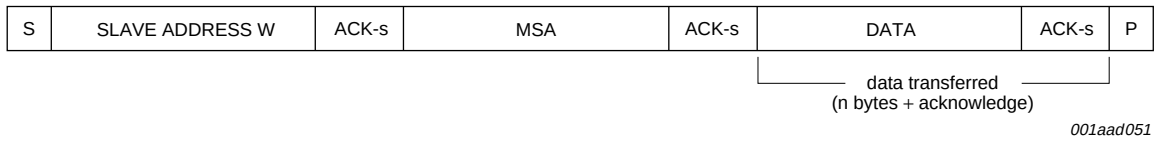


Fig 3. Write mode

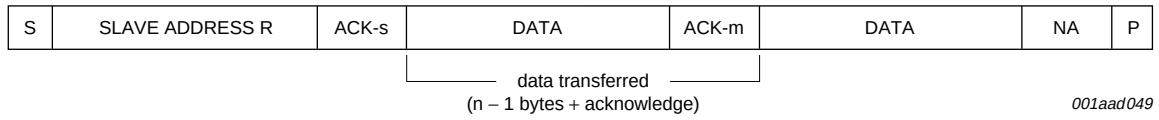


Fig 4. Read mode

Table 4. Description of I²C-bus format

Code	Description
S	START condition
Slave address W	1100 0000b for pin ADDR grounded
	1100 0010b for pin ADDR floating
Slave address R	1100 0001b for pin ADDR grounded
	1100 0011b for pin ADDR floating

Table 4. Description of I²C-bus format *…continued*

Code	Description
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
NA	not acknowledge
MSA	mode and subaddress byte
Data	data byte
P	STOP condition

8.1 Read mode

Read data is loaded into the output register at the preceding acknowledge clock pulse.

Table 5. Read register overview

Data byte	Name	Reference
0h	IFCOUNTER	Section 8.1.1
1h	TUNER	Section 8.1.2
2h	ACDREAD	Section 8.1.3
3h	LEVEL	Section 8.1.4
4h	ID	Section 8.1.5
5h	TEMP	Section 8.1.6

8.1.1 Read mode: data byte IFCOUNTER

Table 6. IFCOUNTER - data byte 0h bit allocation

7	6	5	4	3	2	1	0
IFCM1	IFCM0	IFCS	IFCA	IFC3	IFC2	IFC1	IFC0

Table 7. IFCOUNTER - data byte 0h bit description

Bit	Symbol	Description
7 and 6	IFCM[1:0]	IF counter mode
		00 = no new counter result available (IF counter value is last result or reset state)
		01 = new counter result available (IF counter value is new result)
		10 = counter result from AFU (IF counter value is AF result)
		11 = POR is detected, the I²C-bus data is reset to POR state
5	IFCS	IF counter sign
		0 = the IF counter result indicates a positive **RF** frequency
		1 = the IF counter result indicates a negative **RF** frequency
4	IFCA	IF counter accuracy
		0 = IF counter result with 1 kHz resolution in FM mode and 0.5 kHz resolution in AM mode
		1 = IF counter result with 8 kHz resolution in FM mode and 4 kHz resolution in AM mode
3 to 0	IFC[3:0]	IF counter result; see Table 8

Table 8. IF counter result

IFC3	IFC2	IFC1	IFC0	FM deviation from nominal value		AM deviation from nominal value	
				IFCA = 0	IFCA = 1	IFCA = 0	IFCA = 1
0	0	0	0	0 kHz to 1 kHz	reset state	0 kHz to 0.5 kHz	reset state
0	0	0	1	1 kHz to 2 kHz	-	0.5 kHz to 1 kHz	-
0	0	1	0	2 kHz to 3 kHz	16 kHz to 24 kHz	1 kHz to 1.5 kHz	8 kHz to 12 kHz
0	0	1	1	3 kHz to 4 kHz	24 kHz to 32 kHz	1.5 kHz to 2 kHz	12 kHz to 16 kHz
0	1	0	0	4 kHz to 5 kHz	32 kHz to 40 kHz	2 kHz to 2.5 kHz	16 kHz to 20 kHz
0	1	0	1	5 kHz to 6 kHz	40 kHz to 48 kHz	2.5 kHz to 3 kHz	20 kHz to 24 kHz
0	1	1	0	6 kHz to 7 kHz	48 kHz to 56 kHz	3 kHz to 3.5 kHz	24 kHz to 28 kHz
0	1	1	1	7 kHz to 8 kHz	56 kHz to 64 kHz	3.5 kHz to 4 kHz	28 kHz to 32 kHz
1	0	0	0	8 kHz to 9 kHz	64 kHz to 72 kHz	4 kHz to 4.5 kHz	32 kHz to 36 kHz
1	0	0	1	9 kHz to 10 kHz	72 kHz to 80 kHz	4.5 kHz to 5 kHz	36 kHz to 40 kHz
1	0	1	0	10 kHz to 11 kHz	80 kHz to 88 kHz	5 kHz to 5.5 kHz	40 kHz to 44 kHz
1	0	1	1	11 kHz to 12 kHz	88 kHz to 96 kHz	5.5 kHz to 6 kHz	44 kHz to 48 kHz
1	1	0	0	12 kHz to 13 kHz	96 kHz to 104 kHz	6 kHz to 6.5 kHz	48 kHz to 52 kHz
1	1	0	1	13 kHz to 14 kHz	104 kHz to 112 kHz	6.5 kHz to 7 kHz	52 kHz to 56 kHz
1	1	1	0	14 kHz to 15 kHz	112 kHz to 120 kHz	7 kHz to 7.5 kHz	56 kHz to 60 kHz
1	1	1	1	15 kHz to 16 kHz	≥ 120 kHz	7.5 kHz to 8 kHz	≥ 60 kHz

After a tuning action, which is activated by the state machine, the IF counter is reset at that moment when tuning is established (PLL in-lock). Reset is also possible via bit IFCR. The first counter result is available from 2 ms after reset. For FM further results can be obtained from 4 ms, 8 ms, 16 ms and 32 ms after reset, the increasing count time attenuates influence of FM modulation on the counter result. After this, the counter continues at the maximum count time of 32 ms (see Figure 5).

After AFU sampling the IF counter read value is held (IFCM = 10); see Figure 6, Figure 14 and Figure 15. The counter itself remains active in the background in raw mode (2 ms count time). The IF counter hold is disabled after I^2C-bus read.

For AM mode the count time is fixed to 2 ms and results are available every 2 ms.

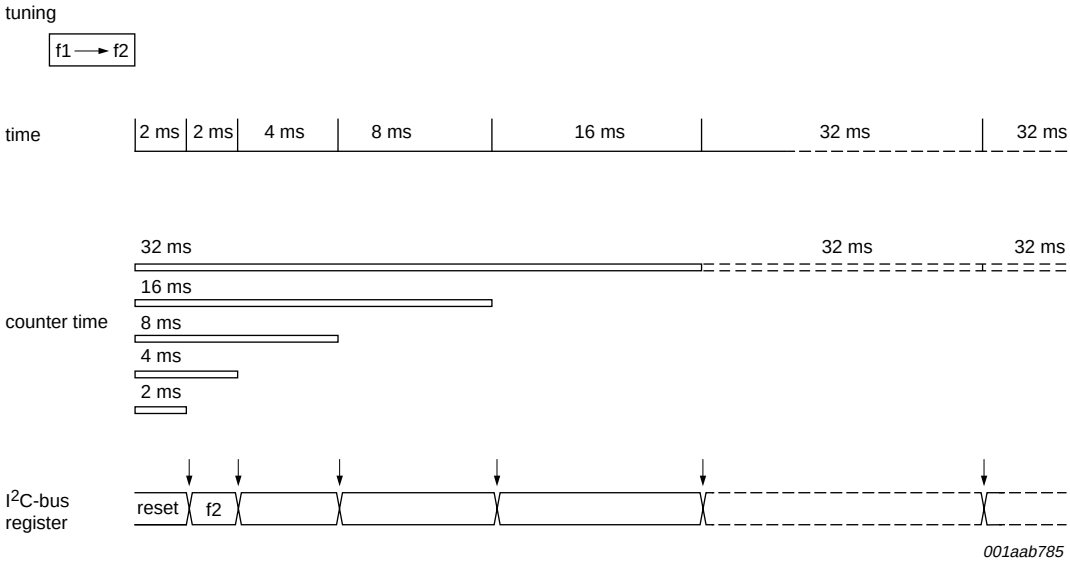


Fig 5. IF counter in FM mode after tuning

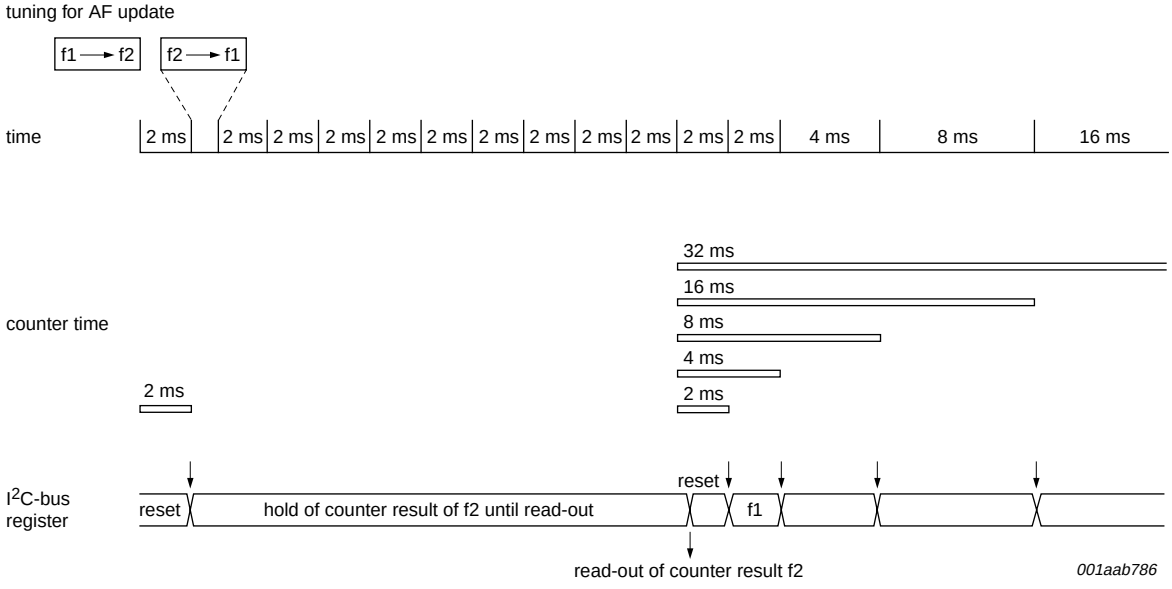


Fig 6. IF counter in FM mode during and after AF update

8.1.2 Read mode: data byte TUNER

Table 9. TUNER - data byte 1h bit allocation

7	6	5	4	3	2	1	0
RAGC1	RAGC0	-	IFBW4	IFBW3	IFBW2	IFBW1	IFBW0

Table 10. TUNER - data byte 1h bit description

Bit	Symbol	Description
7 and 6	RAGC[1:0]	RF AGC attenuation indicator, PIN diode current on pins IAMAGC or IFMAGC
		00 = < 0.1 mA
		01 = 0.1 mA to 0.5 mA
		10 = 0.5 mA to 2.5 mA
		11 = > 2.5 mA
5	-	not used
4 to 0	IFBW[4:0]	FM IF filter bandwidth control 45 kHz to 130 kHz

8.1.3 Read mode: data byte ACDREAD

Table 11. ACDREAD - data byte 2h bit allocation

7	6	5	4	3	2	1	0
ACD2	ACD1	ACD0	MOD2	MOD1	MOD0	OFFS	WAM

Table 12. ACDREAD - data byte 2h bit description

Bit	Symbol	Description
7 to 5	ACD[2:0]	adjacent channel detector value
4 to 2	MOD[2:0]	modulation detector value
1	OFFS	offset detector result
		0 = no offset detected
		1 = offset detected (adjacent channel breakthrough)
0	WAM	wideband AM detector result
		0 = no WAM detected
		1 = WAM detected (multipath or co-channel)

After AFU sampling the content of the byte ACDREAD is held until the next I^2C-bus read. The values ACD and MOD and the WAM bit can be used as quality indicators of the alternate frequency. The OFFS bit cannot be used because of too slow attack time. See Figure 14 and Figure 15.

8.1.4 Read mode: data byte LEVEL

Table 13. LEVEL - data byte 3h bit allocation

7	6	5	4	3	2	1	0
LEV7	LEV6	LEV5	LEV4	LEV3	LEV2	LEV1	LEV0

Table 14. LEVEL - data byte 3h bit description

Bit	Symbol	Description
7 to 0	LEV[7:0]	level detector output value V_{level} [V] = $\frac{1}{64}$LEV[7:0] + 0.25

8.1.5 Read mode: data byte ID

Table 15. ID - data byte 4h bit allocation

7	6	5	4	3	2	1	0
IFCAPG	-	-	-	-	ID2	ID1	ID0

Table 16. ID - data byte 4h bit description

Bit	Symbol	Description
7	IFCAPG	IF filter gear; value is used for IFCAP adjustment (byte IFCAP); see Table 47 and Table 48
6 to 3	-	not used
2 to 0	ID[2:0]	device type identification 010 = TEF6862

8.1.6 Read mode: data byte TEMP

Table 17. TEMP - data byte 5h bit allocation

7	6	5	4	3	2	1	0
TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0

Table 18. TEMP - data byte 5h bit description

Bit	Symbol	Description
7 to 0	TEMP[7:0]	chip temperature; 1 step ≈ 1 K; relative indication

8.2 Write mode

The tuner is controlled by the I^{2}C-bus. After the IC address the MSA byte contains the control of the tuning action via the bits MODE[2:0] and REGC and subaddressing via bits SA[3:0] (see Figure 7).

The tuner circuit is controlled by the CONTROL register. Any data change in the CONTROL register has immediate effect and will change the operation of the tuner circuit accordingly. The subaddress range 00h to 05h includes data that may lead to audible disturbance when changed. Therefore the subaddress range 00h to 05h is not loaded in the CONTROL register directly but loaded in a BUFFER register instead. This allows the IC to take care of tuning actions and mute control, freeing the microcontroller from cumbersome controls and timings. The subaddress range of 06h to 0Fh does not contain such critical data. I^{2}C-bus information in the range 06h to 0Fh will be loaded in the CONTROL register directly (at acknowledge of each byte).

Controlled by a state machine the BUFFER data will be loaded in the CONTROL register for new settings. However at the same time the CONTROL data is loaded in the BUFFER register. This register swap action allows a fast return to the previous setting because the previous data remains available in the BUFFER register (see Figure 8 and Figure 9).

Via MODE several operational modes can be selected for the state machine. MODE offers all standard tuning actions as well as generic control for flexibility. The state machine controls the tuner by controlling I^{2}C-bus data and internal circuits like the IF counter and mute. Action progress is monitored by the accompanying signal processor via the AFSAMPLE and AFHOLD lines, this way functions like weak signal processing can be controlled complementary to the tuner action.

The state machine operation starts at the end of transmission (P = STOP). In case a previous action is still active this is ignored and the new action defined by MODE is started immediately. When only the address byte is transmitted no action is started however (device presence test).

To minimize the I^2C-bus transmission time only bytes that include data changes need to be written. Following the MSA byte the transmission can start at any given data byte defined by the subaddress (SA) bits.

Furthermore when writing the buffered range either the current BUFFER data or the current CONTROL data can be used as default, controlled by the REGC bit: with REGC = 0 any BUFFER data that is not newly written via I^2C-bus remains unchanged. In general the BUFFER register will contain the previous tuner setting so this becomes default for the new setting. When only the MSA byte is transmitted defining a tuning MODE with REGC = 0 the tuner will return to its previous settings (see Figure 8). Instead with REGC = 1 the BUFFER register is loaded with data from the CONTROL register first, this way not written BUFFER data equals the CONTROL data. Since the CONTROL register contains the current tuner setting with REGC = 1 the current tuner setting is default for the new setting. When a tuning MODE action is defined with REGC = 1 the tuner will keep its current settings (CONTROL = current) for all data that is not newly written during the transmission (see Figure 9).

After power-on reset, all registers are in their default settings. The tuning mute circuit is muted. The control signals for the signal processors are set to AFSAMPLE = HIGH and AFHOLD = HIGH. An action of the state machine de-mutes the circuit.

Table 19. Write mode subaddress overview

Subaddress	Name	Default	Reference
0h	BANDWIDTH	1111 1110b	Section 8.2.2
1h	PLLM	0000 1000b	Section 8.2.3
2h	PLLL	0111 1110b	Section 8.2.4
3h	DAA	0100 0000b	Section 8.2.5
4h	AGC	1000 0000b	Section 8.2.6
5h	BAND	0010 0000b	Section 8.2.7
6h	CONTROL	1001 1000b	Section 8.2.8
7h	LEVEL	1000 0100b	Section 8.2.9
8h	IFCF	0010 0000b	Section 8.2.10
9h	IFCAP	0000 1000b	Section 8.2.11
Ah	ACD	0100 1010b	Section 8.2.12
Fh	TEST	0000 0000b	Section 8.2.13

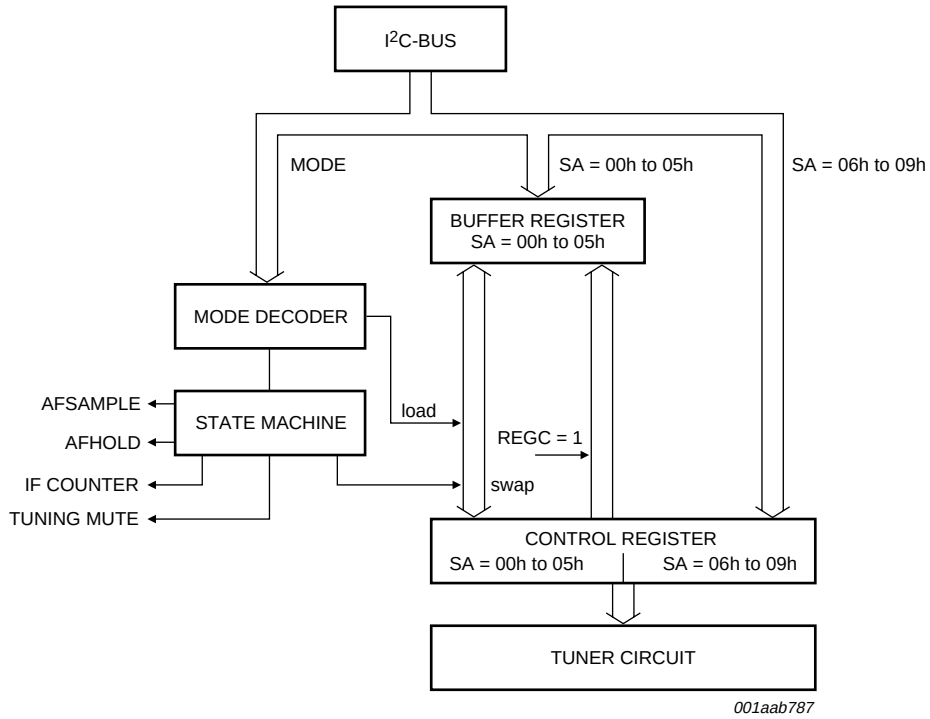


Fig 7. I²C-bus control

Fig 8. Write to CONTROL register with swap, REGC = 0

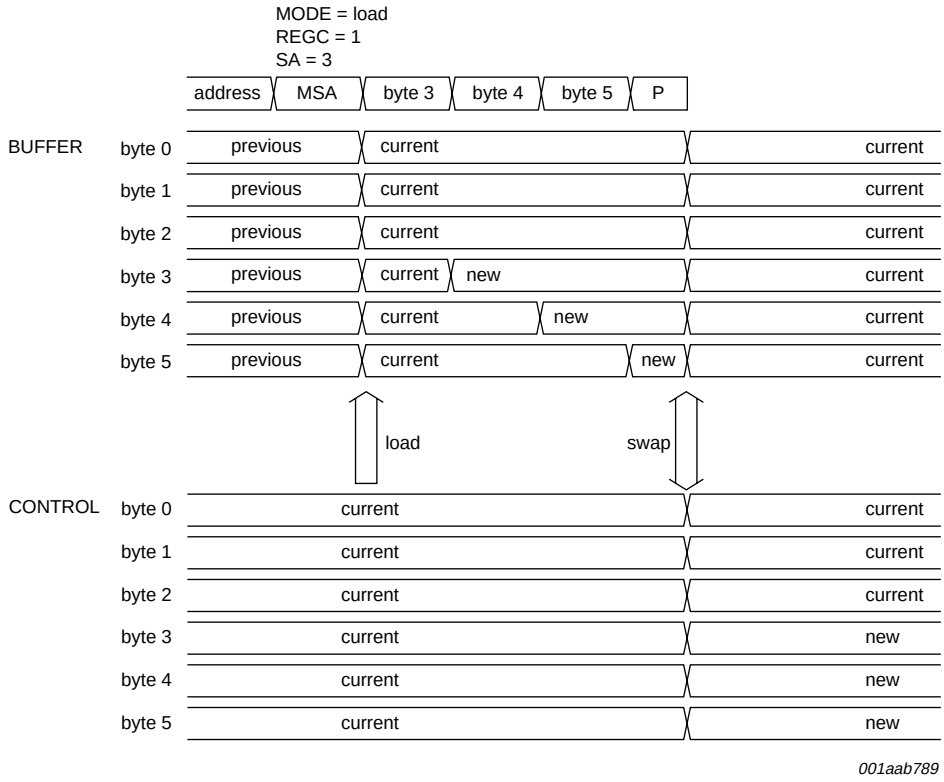


Fig 9. Write to CONTROL register with swap, REGC = 1

8.2.1 Mode and subaddress byte for write

Table 20. MSA - mode and subaddress byte bit allocation

7	6	5	4	3	2	1	0
MODE2	MODE1	MODE0	REGC	SA3	SA2	SA1	SA0

Table 21. MSA - mode and subaddress byte bit description

Bit	Symbol	Description
7 to 5	MODE[2:0]	mode; see Table 22
4	REGC	register mode
		0 = buffer mode or back mode: previous tuning data is default for new I²C-bus write (data of the BUFFER register is not changed before I²C-bus write); see Figure 8
		1 = control mode or current mode: current tuning data is default for new I²C-bus write (the BUFFER register is loaded with CONTROL register data before I²C-bus write); see Figure 9
3 to 0	SA[3:0]	subaddress; write data byte subaddress 0 to 15. The subaddress value is auto-incremented and will revert from SA = 15 to SA = 0. The auto-increment function cannot be switched off.

Table 22. Tuning action modes[1]

MODE2	MODE1	MODE0	Symbol	Description
0	0	0	buffer	write BUFFER register, no state machine action, no swap
0	0	1	preset	tune to new program with 60 ms mute control; swap[2]; see Figure 10 and Figure 11
0	1	0	search	tune to new program and stay muted (for release use end mode); swap[2]; see Figure 12 and Figure 13
0	1	1	AF update	tune to AF program; check AF quality and tune back to main program; two swap operations[3]; see Figure 14 and Figure 15
1	0	0	jump	tune to AF program in minimum time; swap; see Figure 16 and Figure 17
1	0	1	check	tune to AF program and stay muted (for release use end mode); swap; see Figure 18 and Figure 19
1	1	0	load	write CONTROL register via BUFFER; no state machine action; immediate swap; see Figure 8 and Figure 9
1	1	1	end	end action; release mute; no swap; see Figure 20

[1] When the write transmission of a state machine command starts during a mute state of the state machine, the sequences of the state machine start immediately with the actions which follow the mute period in the standard sequence (see Figure 11, Figure 13, Figure 15, Figure 17 and Figure 19).

[2] In the modes preset and search the AM AGC time constant is set to fast during the period of complete mute.

[3] The AF update sequence can also be started by pulling the AFHOLD pin LOW. In this case the AF information should be loaded into the BUFFER before. LOW period for a correct AF update timing: $t_{LOW} > 20\ \mu s$. Between the end of the I²C-bus transmission and the falling edge of the AFHOLD pulse a delay of $\geq 20\ \mu s$ is necessary.

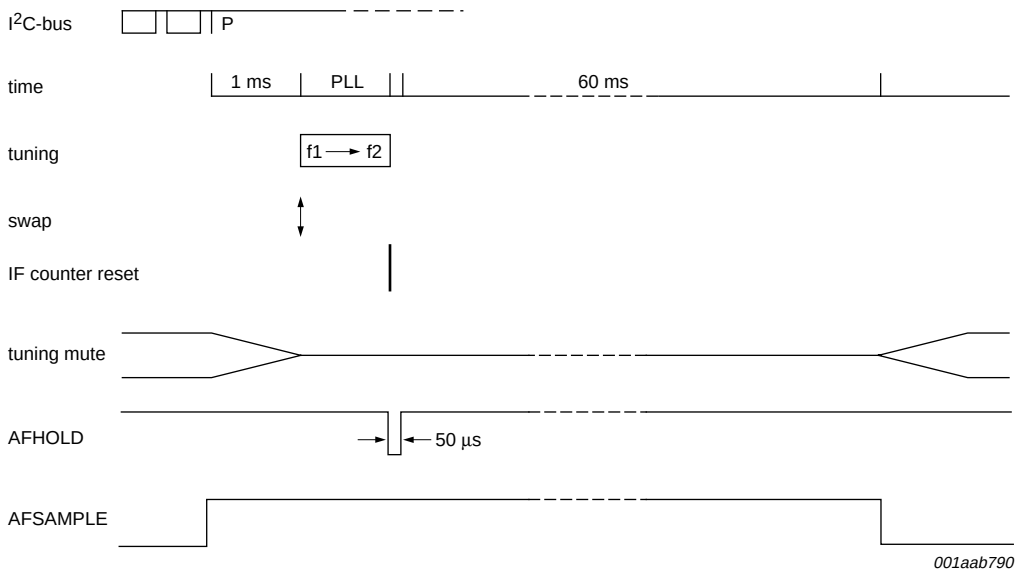


Fig 10. Preset mode

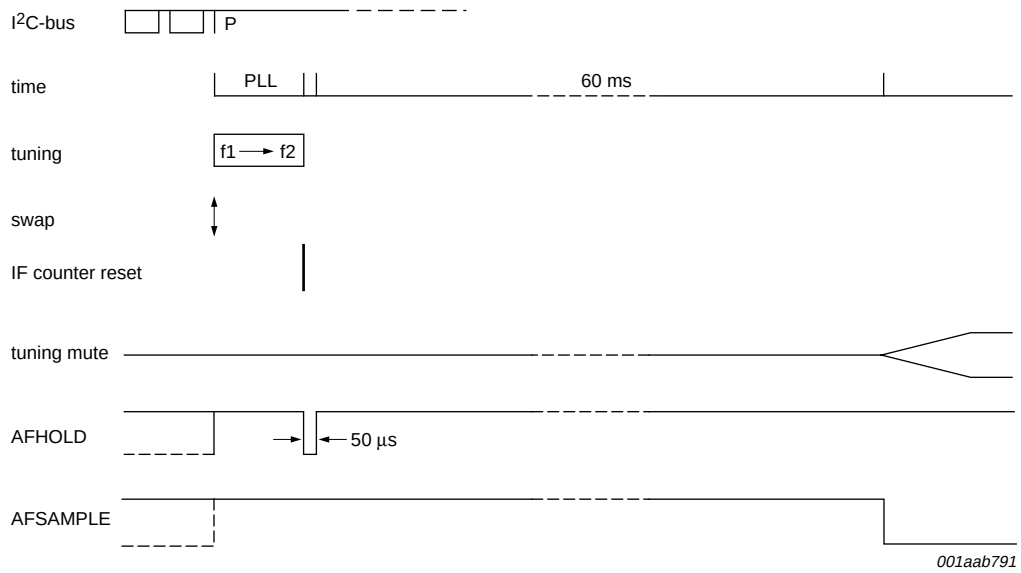


Fig 11. Preset mode, started during mute

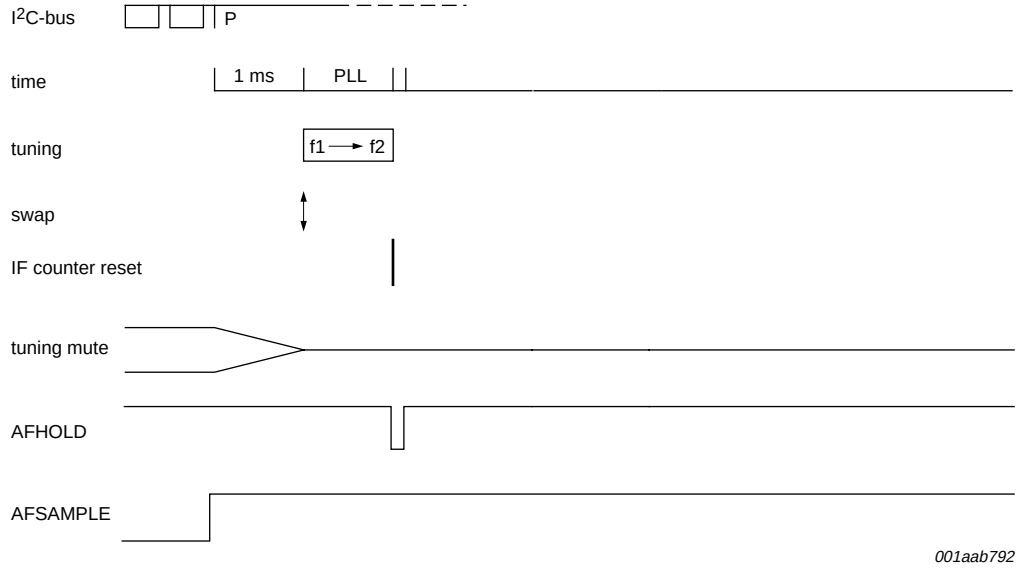


Fig 12. Search mode

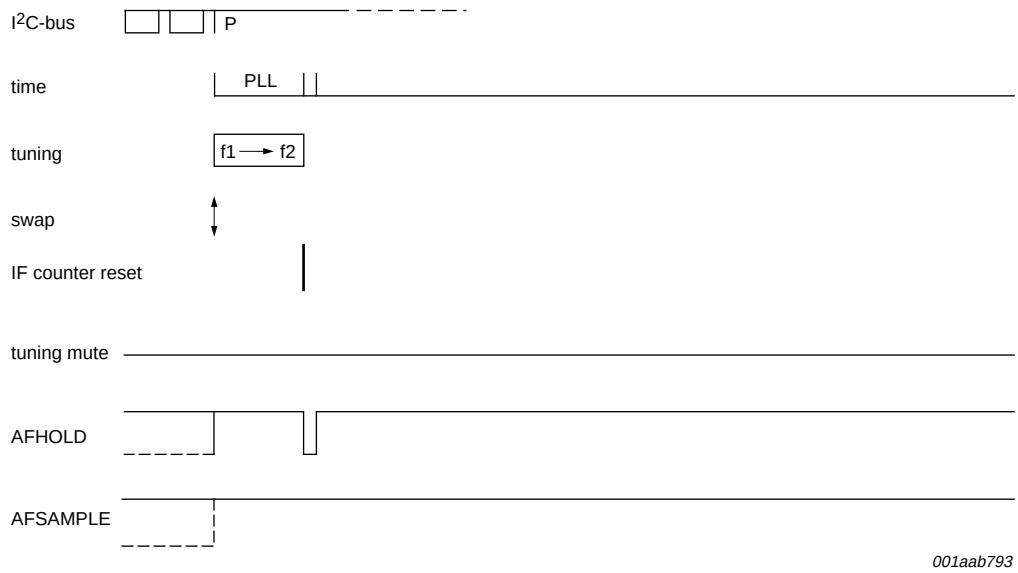


Fig 13. Search mode, started during mute

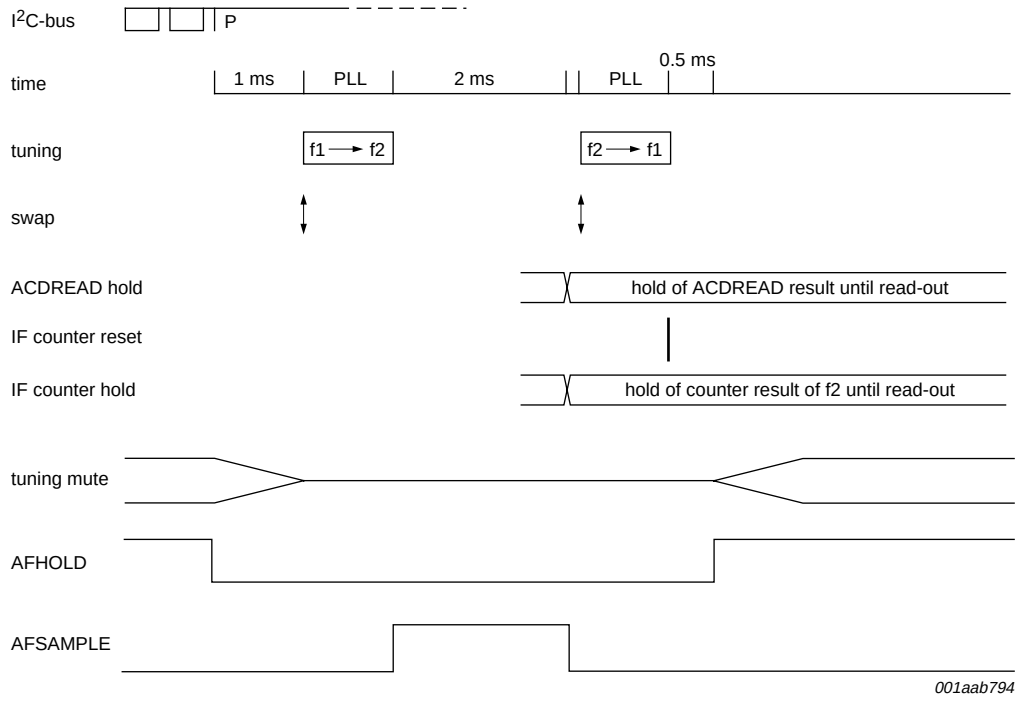


Fig 14. AF update mode

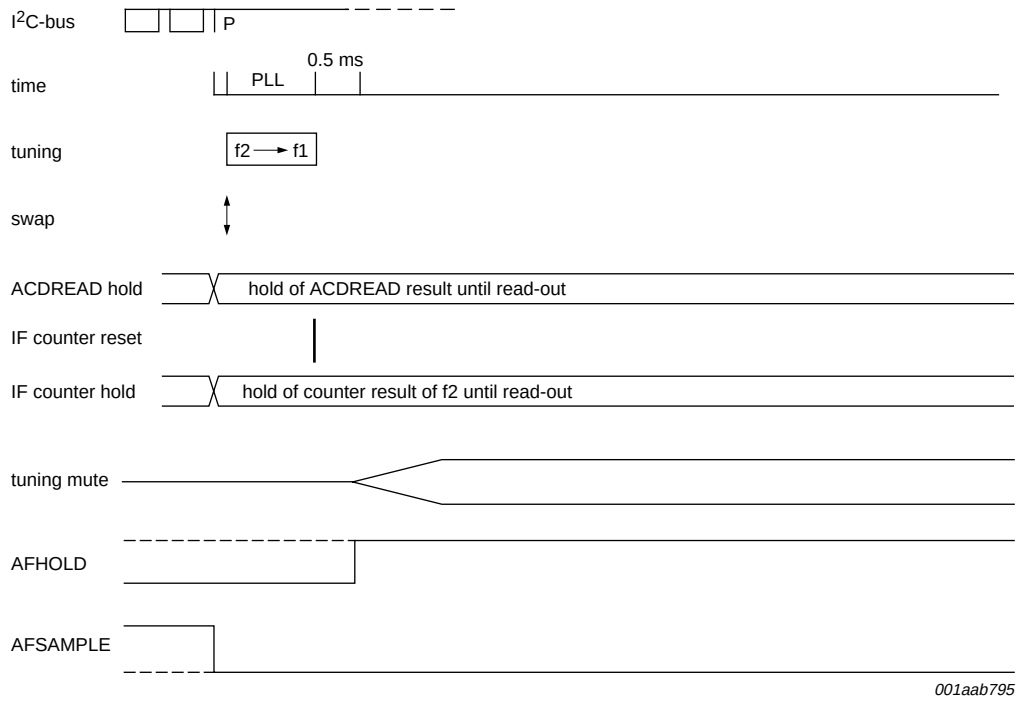


Fig 15. AF update mode, started during mute

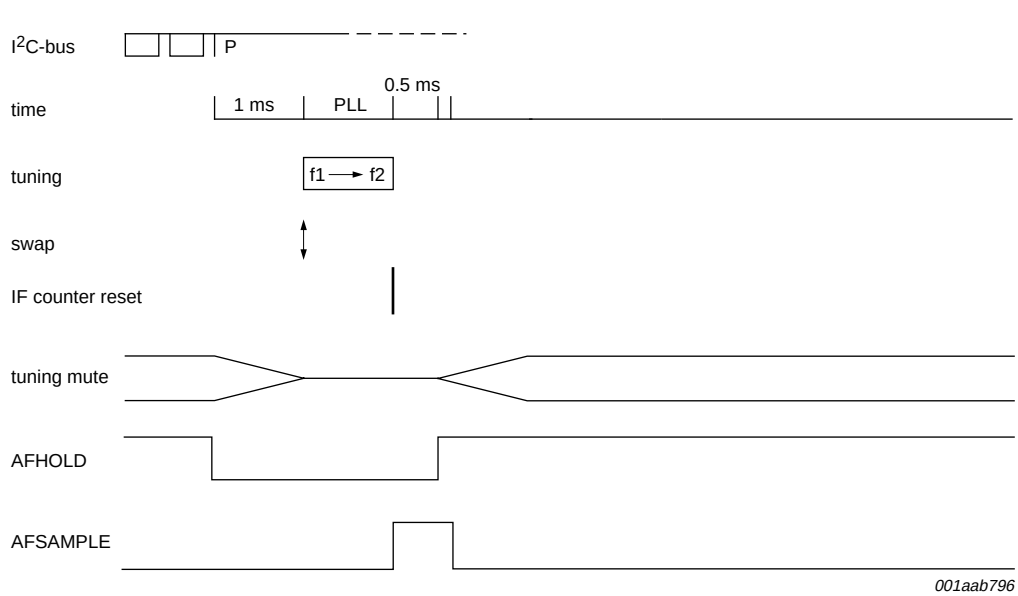


Fig 16. Jump mode

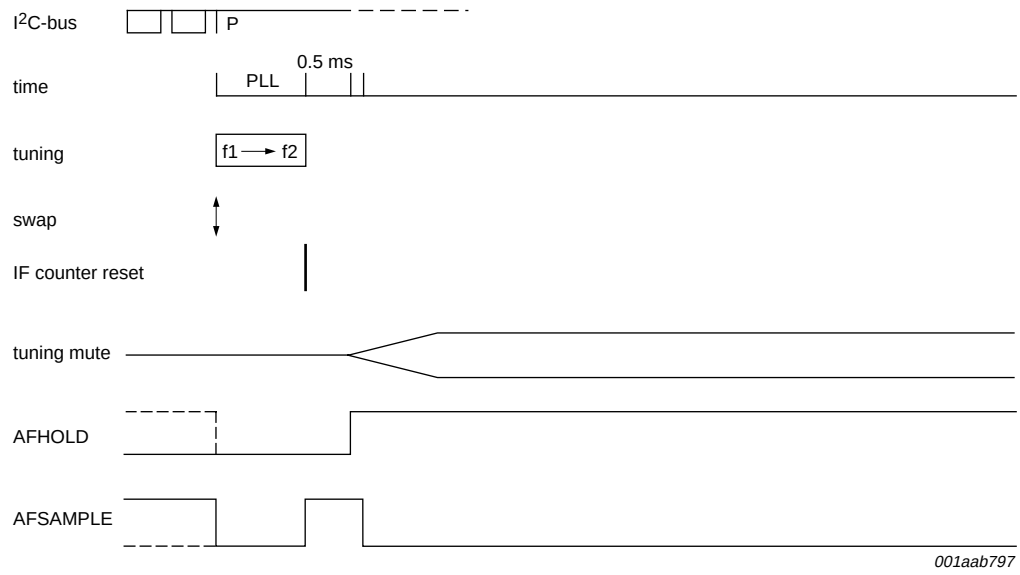


Fig 17. Jump mode, started during mute

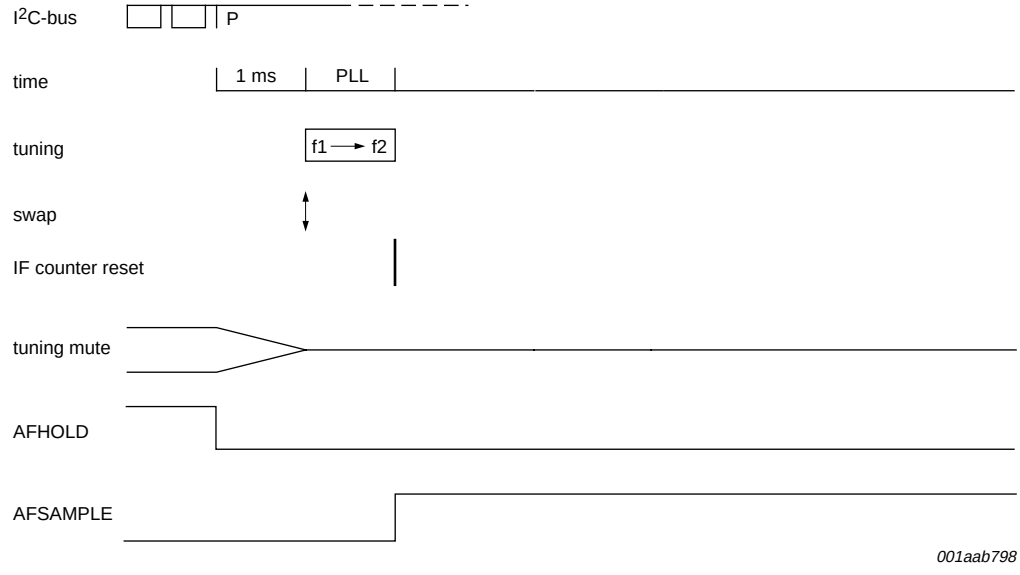


Fig 18. Check mode

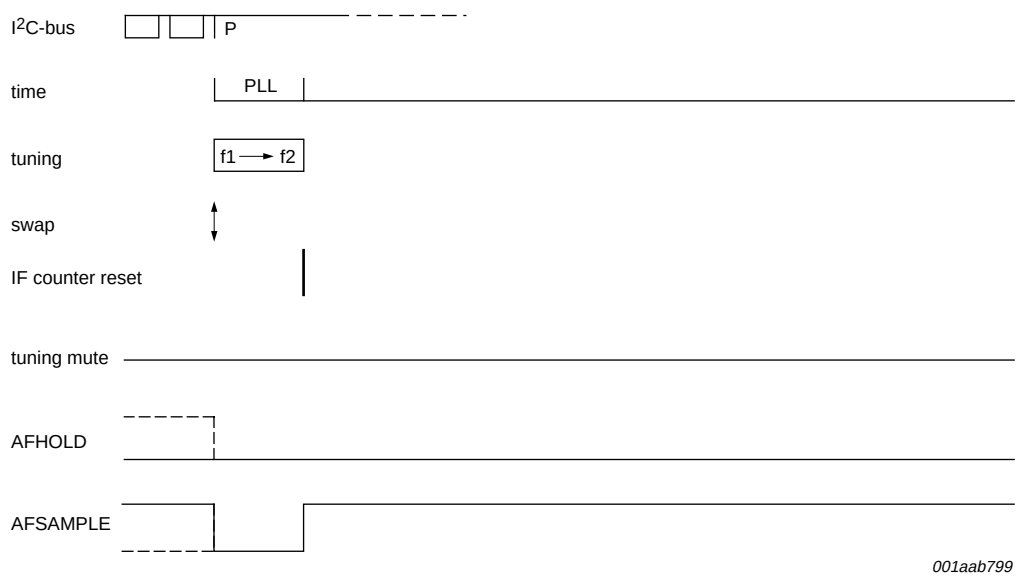


Fig 19. Check mode, started during mute

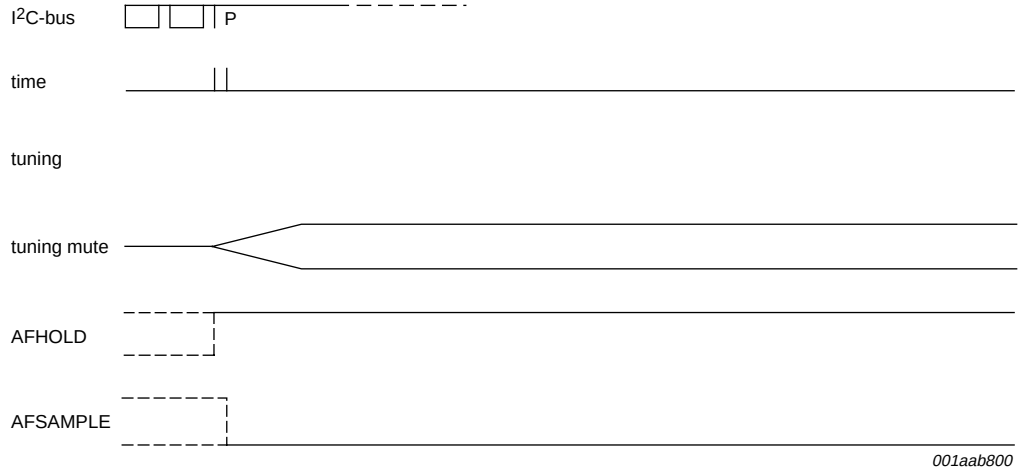


Fig 20. End mode

8.2.2 Write mode: data byte BANDWIDTH

Table 23. BANDWIDTH - data byte 0h bit allocation with default setting (buffered)

7	6	5	4	3	2	1	0
DYN	BW4	BW3	BW2	BW1	BW0	TE1	FLAG
1	1	1	1	1	1	1	0

Table 24. BANDWIDTH - data byte 0h bit description

Bit	Symbol	Description
7	DYN	dynamic bandwidth
		0 = FM IF bandwidth set by BW[4:0]
		1 = FM IF bandwidth dynamically controlled
6 to 2	BW[4:0]	FM IF bandwidth: if DYN = 0: 0 to 31: FM fixed IF bandwidth 45 kHz to 130 kHz; if DYN = 1: 0 to 15: upper limit of dynamic range is 130 kHz and lower limit is 45 kHz to 86 kHz; 16 to 31: upper limit of dynamic range is 89 kHz to 130 kHz and lower limit is 45 kHz
1	TE1	threshold extension; the control is combined with bit TE0 of data byte ACD; see Table 49
0	FLAG	software programmable flag
		0 = SWPORT1 pin inactive (high-impedance)
		1 = SWPORT1 pin active (pull-down to ground)

8.2.3 Write mode: data byte PLLM

Table 25. PLLM - data byte 1h bit allocation with default setting (buffered)

7	6	5	4	3	2	1	0
RFGAIN	PLL14	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8
0	0	0	0	1	0	0	0

Table 26. PLLM - data byte 1h bit description

Bit	Symbol	Description
7	RFGAIN	RF gain setting in FM mode
		0 = FM standard RF gain
		1 = +6 dB additional RF gain at FM mixer 1
6 to 0	PLL[14:8]	upper byte of PLL divider word

8.2.4 Write mode: data byte PLLL

Table 27. PLLL - data byte 2h bit allocation with default setting (buffered)

7	6	5	4	3	2	1	0
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0
0	1	1	1	1	1	1	0

Table 28. PLLL - data byte 2h bit description

Bit	Symbol	Description
7 to 0	PLL[7:0]	lower byte of PLL divider word; PLL[14:0] is the divider ratio N of the VCO programmable divider; N = 1024 to 32767

8.2.5 Write mode: data byte DAA

Table 29. DAA - data byte 3h bit allocation with default setting (buffered)

7	6	5	4	3	2	1	0
AGCSW	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0
0	1	0	0	0	0	0	0

Table 30. DAA - data byte 3h bit description

Bit	Symbol	Description
7	AGCSW	RF AGC switch
		0 = no control of unused RF AGC
		1 = unused PIN diode supplied with constant current
6 to 0	DAA[6:0]	alignment of antenna circuit tuning voltage ($0.1V_{DAAIN}$ to $2.0V_{DAAIN}$)

8.2.6 Write mode: data byte AGC

Table 31. AGC - data byte 4h bit allocation with default setting (buffered)

7	6	5	4	3	2	1	0
SDAA3	SDAA2	SDAA1	SDAA0	AGC1	AGC0	KAGC	LODX
1	0	0	0	0	0	0	0

Table 32. AGC - data byte 4h bit description

Bit	Symbol	Description
7 to 4	SDAA[3:0]	alignment of second antenna circuit tuning voltage ($0.7V_{DAAOUT1}$ to $1.35V_{DAAOUT1}$)
3 and 2	AGC[1:0]	setting of RF AGC threshold voltage; for AM, see Table 33 and for FM, see Table 34
1	KAGC	keyed AGC
		FM mode
		0 = keyed AGC off
		1 = keyed AGC on; the AGC start level is shifted to a value 10 dB above the standard AGC start level, when the level voltage of the wanted RF signal is below the threshold level voltage for narrow-band AGC
		AM mode
		0 = cascode RF AGC active, PIN diode AGC active
		1 = cascode RF AGC disabled, PIN diode AGC active
0	LODX	local switch
		0 = standard operation (DX)
		1 = forced FM RF AGC attenuation (LOCAL)

Table 33. Setting of RF AGC threshold voltage for AM

AGC1	AGC0	AM mixer 1 input voltage (peak-to-peak value)
0	0	1000 mV
0	1	700 mV
1	0	500 mV
1	1	350 mV

Table 34. Setting of RF AGC threshold voltage for FM

AGC1	AGC0	FM mixer 1 input voltage (RMS value)
0	0	24 mV

Table 34. Setting of RF AGC threshold voltage for FM *...continued*

AGC1	AGC0	FM mixer 1 input voltage (RMS value)
0	1	17 mV
1	0	12 mV
1	1	9 mV

8.2.7 Write mode: data byte BAND

Table 35. BAND - data byte 5h bit allocation with default setting (buffered)

7	6	5	4	3	2	1	0
BAND2	BAND1	BAND0	FREF2	FREF1	FREF0	LOINJ	AMST
0	0	1	0	0	0	0	0

Table 36. BAND - data byte 5h bit description

Bit	Symbol	Description
7 to 5	BAND[2:0]	divider ratio M; see Table 37 for BAND[2:0] = 000 the IF bandwidth is set to 20 kHz and the weather band input is active
4 to 2	FREF[2:0]	PLL reference frequency; see Table 38
1	LOINJ	0 = high injection image suppression
		1 = low injection image suppression
0	AMST	AM stereo
		0 = standard operation
		1 = the AM IF signal is available at pin MPXAM

Table 37. Decoding of BAND bits

BAND2	BAND1	BAND0	Divider ratio M	Receiver band
0	0	0	1	WB
0	0	1	2	FM
0	1	0	3	FM
0	1	1	6	AM
1	0	0	8	AM
1	0	1	10	AM
1	1	0	16	AM
1	1	1	20	AM

Table 38. Reference frequencies

FREF2	FREF1	FREF0	f_{ref}
0	0	0	100 kHz
0	0	1	50 kHz
0	1	0	25 kHz
0	1	1	20 kHz
1	0	0	10 kHz
1	0	1	reserved
1	1	0	reserved
1	1	1	reserved

The correct charge pump current for each reference frequency is selected automatically, see Table 39.

Table 39. Charge pump source[1]

FREF2	FREF1	FREF0	LOINJ	Charge pump current	f_{ref}
0	0	0	X	CP1	100 kHz
0	0	1	X	CP2	50 kHz
0	1	0	X	CP3	25 kHz
0	1	1	1	CP3	20 kHz
0	1	1	0	CP4	20 kHz
1	0	0	X	CP5	10 kHz

[1] X = don't care.

8.2.7.1 Tuning overview

High injection LO (Europe FM, US FM and AM):

$N = \frac{(f_{RF} + 10.7\ MHz) \times M}{f_{ref}}$ with LOINJ = 0 to achieve full image suppression in FM.

Low injection LO (Japan FM and OIRT):

$N = \frac{(f_{RF} - 10.7\ MHz) \times M}{f_{ref}}$ with LOINJ = 1 to achieve full image suppression in FM.

$tuning\ step = \frac{f_{ref}}{M}$

where: M is the divider ratio of the VCO frequency for AM mixer 1 and FM mixer 1 $M = \frac{f_{VCO}}{f_{mixer\ 1}}$.

When in AM mode the tuner settings $N = \frac{(f_{RF} - 10.7\ MHz) \times M}{f_{ref}}$ or $N = \frac{(10.7\ MHz - f_{RF}) \times M}{f_{ref}}$ are selected, the correct IF counter sign is achieved with LOINJ = 1.

Table 40. Standard tuner settings

Broadcast band	BAND2	BAND1	BAND0	M	FREF2	FREF1	FREF0	f_{ref}	LOINJ	Tuning step
Europe FM and US FM	0	0	1	2	0	0	0	100 kHz	0	50 kHz
Japan FM	0	1	0	3	0	0	0	100 kHz	1	33.3 kHz
East Europe FM (OIRT FM)	0	1	0	3	0	1	1	20 kHz	1	6.67 kHz
WB FM	0	0	0	1	0	1	0	25 kHz	0	25 kHz
AM MW and LW	1	1	1	20	0	1	1	20 kHz	0	1 kHz
AM SW 120 m to 60 m	1	1	0	16	1	0	0	10 kHz	0	0.625 kHz

Table 40. Standard tuner settings *…continued*

Broadcast band	BAND2	BAND1	BAND0	M	FREF2	FREF1	FREF0	f_{ref}	LOINJ	Tuning step
AM SW 49 m to 22 m	1	0	1	10	1	0	0	10 kHz	0	1 kHz
AM SW 25 m to 15 m	1	0	0	8	1	0	0	10 kHz	0	1.25 kHz
AM SW 16 m to 11 m	0	1	1	6	1	0	0	10 kHz	0	1.67 kHz

8.2.8 Write mode: data byte CONTROL

Table 41. CONTROL - data byte 6h bit allocation with default setting (buffered)

7	6	5	4	3	2	1	0
1	IFGAIN	INS1	INS0	0	STBY	IFCR	SFLAG
	0	0	1		0	0	0

Table 42. CONTROL - data byte 0h bit description

Bit	Symbol	Description
7	-	not used, must be set to logic 1
6	IFGAIN	IF gain
		0 = IF gain for low loss 10.7 MHz filter
		1 = increased IF gain (6 dB) for high loss 10.7 MHz filter
5 and 4	INS[1:0]	IF noise blanker sensitivity (threshold)[1]
		00 = noise blanker off
		01 = noise blanker sensitivity low
		10 = noise blanker sensitivity medium
		11 = noise blanker sensitivity high
3	-	not used, must be set to logic 0
2	STBY	0 = operation
		1 = standby mode
1	IFCR	IF counter reset
		0 = standard operation (reset at tuning)
		1 = forced reset of IF counter (IFCR returns to logic 0)
0	SFLAG	second flag output
		0 = SWPORT2 pin inactive (high-impedance)
		1 = SWPORT2 pin active (pull-down to ground)

[1] Noise blanker test condition: pulse repetition rate = 100 Hz; pulse duration = 5 ns; rise and fall time < 1 ns; measured at dummy aerial input (15 pF/60 pF).

8.2.9 Write mode: data byte LEVEL

Table 43. LEVEL - data byte 7h bit allocation with default setting

7	6	5	4	3	2	1	0
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0
1	0	0	0	0	1	0	0

Table 44. LEVEL - data byte 7h bit description

Bit	Symbol	Description
7 to 3	LST[4:0]	level start voltage alignment
2 to 0	LSL[2:0]	level slope alignment

8.2.10 Write mode: data byte IFCF

Table 45. IFCF - data byte 8h bit allocation with default setting

7	6	5	4	3	2	1	0
IFCFA	IFWB	IFCF5	IFCF4	IFCF3	IFCF2	IFCF1	IFCF0
0	0	1	0	0	0	0	0

Table 46. IFCF - data byte 8h bit description

Bit	Symbol	Description
7	IFCFA	FM IF filter alignment
		0 = standard operation
		1 = alignment mode: fast settling of IF filter (decoupling of the time constant capacitor at VTCENTRE), IFCAP auto-correction disabled and reset
6	IFWB	FM IF filter narrow
		0 = standard operation
		1 = alignment mode: FM IF filter at 20 kHz bandwidth
5 to 0	IFCF[5:0]	FM IF filter center frequency alignment

8.2.11 Write mode: data byte IFCAP

Table 47. IFCAP - data byte 9h bit allocation with default setting

7	6	5	4	3	2	1	0
IFCAPA	0	0	0	IFCAP3	IFCAP2	IFCAP1	IFCAP0
0				1	0	0	0

Table 48. IFCAP - data byte 9h bit description

Bit	Symbol	Description
7	IFCAPA	FM IF filter capacitor alignment enable
		0 = standard operation
		1 = alignment and initialization mode: IFCAP auto-correction disabled and reset
6 to 4	-	not used, must be set to logic 0
3 to 0	IFCAP[3:0]	alignment of FM IF filter capacitor value (use read bit IFCAPG)

The fully integrated IF2 filter of the TEF6862 has to be aligned in order to achieve the optimum performance at all ambient conditions. The following procedure is used for a correct factory alignment.

8.2.11.1 Factory alignment of IFCAP

FM IF filter operation point alignment (data byte IFCAP): a single alignment of the FM IF filter operation range secures an accurate and continuous frequency setting over the full temperature range and all FM bands.

1. Set bit IFCAPA = 1 to disable internal IFCAP control
2. Increase bit IFCAP from 0 upwards until I^2C-bus read bit IFCAPG (read data byte 4, ID) changes from logic 0 to logic 1
3. Save this IFCAP setting as alignment value
4. Set bit IFCAPA = 0 to return to normal operation

8.2.11.2 Initialization of the radio

During radio initialization bit IFCAPA = 1 is used for writing the stored IFCAP alignment value. Afterwards bit IFCAPA = 0. After the initialization repeated writing of the IFCAP byte with the identical IFCAP alignment value is only allowed with bit IFCAPA = 0.

8.2.11.3 Factory alignment of IFCF

FM IF filter center frequency alignment (data byte IFCF): to correct IF frequency errors caused by an error in the crystal frequency the alignment is preferably performed for every FM band in use. A test frequency in the center of the band is preferred. An accurate alignment result is realized by testing for symmetrical filter attenuation.

1. Set RF generator level V_{RF} = 200 µV
2. Set bit IFWB = 1 for better accuracy (20 kHz bandwidth)
3. Set bit IFCFA = 1 to enable fast settling of the filter frequency
4. Test high side of filter curve: tune to f_{RF} – 50 kHz (Europe/USA) or f_{RF} + 33.3 kHz (Japan/OIRT)
5. Change IFCF[5:0] from 0 to 63 and note the read result LEV[7:0] (level voltages)
6. Test low side of filter curve: tune to f_{RF} + 50 kHz (Europe/USA) or f_{RF} – 33.3 kHz (Japan/OIRT)
7. Change IFCF[5:0] from 0 to 63 and note the level voltages
8. Find the IFCF[5:0] value where both level curves cross (lowest difference) and save this IFCF[5:0] value
9. Set bit IFWB = 0 to return to normal operation
10. Set bit IFCFA = 0 to return to normal operation

8.2.12 Write mode: data byte ACD

Table 49. ACD - data byte Ah bit allocation with default setting

7	6	5	4	3	2	1	0
TE0	LAP1	LAP0	BAL1	BAL0	WAM1	WAM0	BWFLAG
0	1	0	0	1	0	1	0

Table 50. IFCF - data byte Ah bit description

Bit	Symbol	Description
7	TE0	threshold extension; additional control towards narrow bandwidth at low RF levels; control is combined with bit TE1 of data byte BANDWIDTH
		TE[1:0] = 00 = threshold extension control is off
		TE[1:0] = 01 = threshold extension control is low
		TE[1:0] = 10 = threshold extension control is standard
		TE[1:0] = 11 = threshold extension control is high
6 and 5	LAP[1:0]	latch protection; additional wide bandwidth control at low RF and high modulation to avoid distortion
		00 = latch protection control is off
		01 = latch protection control is low
		10 = latch protection control is standard
		11 = latch protection control is high
4 and 3	BAL[1:0]	control balance of adjacent channel detector and modulation detector; focus of bandwidth control between adjacent channel suppression (avoid breakthrough) and modulation handling (avoid overmodulation distortion)
		00 = control is biased towards adjacent channel breakthrough protection
		01 = standard control
		10 = control is biased towards modulation handling
		11 = control is biased further towards modulation handling
2 and 1	WAM[1:0]	wideband AM threshold; control towards narrow bandwidth is reduced when multipath is detected
		00 = off
		01 = low sensitivity; high threshold
		10 = medium sensitivity; medium threshold
		11 = high sensitivity; low threshold
0	BWFLAG	bandwidth flag output pin
		0 = analog control voltage at IFFLAG pin
		1 = control flag at IFFLAG pin (IFFLAG = HIGH for bandwidth > 56 kHz)

8.2.13 Write mode: data byte TEST

Table 51. TEST - data byte Fh bit allocation with default setting[1]

7	6	5	4	3	2	1	0
0	0	0	TEST4	TEST3	TEST2	TEST1	TEST0
			0	0	0	0	0

[1] The test control byte is for internal use only.

9. Limiting values

Table 52. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage	on pins VCC, VCCPLL, VCCVCO, VCCRF, AMMIX2OUT1, AMMIX2OUT2, MIX1OUT1 and MIX1OUT2		–0.3	+10	V
V_{V60}	voltage on pin V60		[1]	–0.3	V_{CCA} + 0.3	V
ΔV_{CCAn}	voltage difference between any analog supply pins			–0.3	+0.3	V
V_{SCL}	voltage on pin SCL			–0.3	+5.5	V
V_{SDA}	voltage on pin SDA			–0.3	+5.5	V
V_i	input voltage	on pin ADDR		–0.3	+5.5	V
V_o	output voltage	on pins AFHOLD and AFSAMPLE		–0.3	+5.5	V
		on pins SWPORT1 and SWPORT2	[1]	–0.3	V_{CCA} + 0.3	V
V_n	voltage on any other pin		[1]	–0.3	V_{CCA} + 0.3	V
T_{stg}	storage temperature			–40	+150	°C
T_{amb}	ambient temperature	subjective functionality	[2]	–40	+105	°C
		full functionality		–40	+85	°C
V_{esd}	electrostatic discharge voltage	human body model	[3][4]	–2000	+2000	V
		machine model	[4][5]	–200	+200	V

[1] The maximum voltage must be less than 10 V.

[2] The IC is functional; parameter values are not guaranteed. Operation at maximum temperature will affect lifetime performance.

[3] Class 2 according to JESD22-A114C.01.

[4] All VCC pins and all GND pins connected to tester ground; all other pins tested versus tester ground.

[5] Class B according to EIA/JESD22-A115-A.

10. Thermal characteristics

Table 53. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	60	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		10	K/W

11. Static characteristics

Table 54. Static characteristics

V_{CCA} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_{CCA}	analog supply voltage	on pins VCC, VCCPLL, VCCVCO, VCCRF, AMMIX2OUT1, AMMIX2OUT2, MIX1OUT1 and MIX1OUT2	8	8.5	9	V
V_{V60}	voltage on pin V60		5.5	6.5	-	V
Current in FM mode						
I_{CC}	supply current	T_{amb} = –40 °C	22	27.6	-	mA
		T_{amb} = 25 °C	21.5	26	31.2	mA
		T_{amb} = 85 °C	-	25	30	mA
$I_{CC(PLL)}$	PLL supply current	T_{amb} = –40 °C	-	5.9	-	mA
		T_{amb} = 25 °C	4.1	5.5	7.1	mA
		T_{amb} = 85 °C	-	5.1	6.6	mA
$I_{CC(VCO)}$	VCO supply current	T_{amb} = –40 °C	-	1.8	-	mA
		T_{amb} = 25 °C	0.9	1.7	2.5	mA
		T_{amb} = 85 °C	-	1.6	2.35	mA
$I_{CC(RF)}$	RF supply current	T_{amb} = –40 °C	-	13.9	18.2	mA
		T_{amb} = 25 °C	11.8	15.3	20	mA
		T_{amb} = 85 °C	-	16	20.8	mA
$I_{PIN(AM)}$	AM PIN diode current	data byte DAA bit AGCSW = 1	-	1	-	mA
$I_{I(V60)}$	input current on pin V60	T_{amb} = –40 °C	-	44.5	53.4	mA
		T_{amb} = 25 °C	35	42	50	mA
		T_{amb} = 85 °C	-	39	47	mA
$I_{MIX1OUT1}$	current on pin MIX1OUT1	T_{amb} = –40 °C	-	5.3	-	mA
		T_{amb} = 25 °C	4.3	5.7	7.5	mA
		T_{amb} = 85 °C	-	6.0	8.0	mA
$I_{MIX1OUT2}$	current on pin MIX1OUT2	T_{amb} = –40 °C	-	5.3	-	mA
		T_{amb} = 25 °C	4.3	5.7	7.5	mA
		T_{amb} = 85 °C	-	6.0	8.0	mA
$I_{CC(tot)}$	total supply current		-	101.9	-	mA
Current in AM mode						
I_{CC}	supply current	T_{amb} = –40 °C	-	37.5	-	mA
		T_{amb} = 25 °C	30	36	43	mA
		T_{amb} = 85 °C	-	34	40	mA
$I_{CC(PLL)}$	PLL supply current	T_{amb} = –40 °C	-	5.9	-	mA
		T_{amb} = 25 °C	4.1	5.5	7.1	mA
		T_{amb} = 85 °C	-	5.1	6.6	mA

Table 54. Static characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC(VCO)}$	VCO supply current	T_{amb} = –40 °C	-	1.8	-	mA
		T_{amb} = 25 °C	0.9	1.7	2.5	mA
		T_{amb} = 85 °C	-	1.6	2.35	mA
$I_{CC(RF)}$	RF supply current	T_{amb} = –40 °C	-	7.56	-	mA
		T_{amb} = 25 °C	5.25	7.5	11.25	mA
		T_{amb} = 85 °C	-	7.43	11.2	mA
$I_{PIN(FM)}$	FM PIN diode current	data byte DAA bit AGCSW = 1	–15	–10	–7	mA
$I_{I(V60)}$	input current on pin V60	T_{amb} = –40 °C	-	13	16.6	mA
		T_{amb} = 25 °C	9.5	13	16.6	mA
		T_{amb} = 85 °C	-	13	16.6	mA
$I_{MIX1OUT1}$	current on pin MIX1OUT1	T_{amb} = –40 °C	-	6	-	mA
		T_{amb} = 25 °C	4.5	5.75	7	mA
		T_{amb} = 85 °C	-	5.4	6.5	mA
$I_{MIX1OUT2}$	current on pin MIX1OUT2	T_{amb} = –40 °C	-	6	-	mA
		T_{amb} = 25 °C	4.5	5.75	7	mA
		T_{amb} = 85 °C	-	5.4	6.5	mA
$I_{AMMIX2OUT1}$	current on pin AMMIX2OUT1	T_{amb} = –40 °C	-	5.5	-	mA
		T_{amb} = 25 °C	3.7	4.6	5.5	mA
		T_{amb} = 85 °C	-	3.7	4.5	mA
$I_{AMMIX2OUT2}$	current on pin AMMIX2OUT2	T_{amb} = –40 °C	-	5.5	-	mA
		T_{amb} = 25 °C	3.7	4.6	5.5	mA
		T_{amb} = 85 °C	-	3.7	4.5	mA
$I_{CC(tot)}$	total supply current		-	84.4	-	mA

12. Dynamic characteristics

Table 55. Dynamic characteristics

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Crystal oscillator						
f_{xtal}	crystal frequency		-	20.5	-	MHz
C/N	carrier-to-noise ratio	f_{xtal} = 20.5 MHz; Δf = 10 kHz	112	-	-	dBc/√Hz
Circuit inputs: pins XTAL1 and XTAL2[1]						
$V_{o(xtal)}$	crystal output voltage		80	100	160	mV
R_i	input resistance	$V_{XTAL1-XTAL2}$ = 1 mV	-	–500	–250	Ω
C_i	input capacitance		6	8	11	pF

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tuning system; see Table 37, Table 38 and Table 39						
Voltage controlled oscillator						
$f_{VCO(min)}$	minimum VCO frequency		-	-	153.6	MHz
$f_{VCO(max)}$	maximum VCO frequency		256	-	-	MHz
C/N	carrier-to-noise ratio	f_{VCO} = 200 MHz; Δf = 10 kHz; Q ≥ 30	-	98	-	dBc/√Hz
α_{ripple}	ripple rejection	$V_{CC(ripple)}/V_{o(MPXAM)}$; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 50 mV; f_{VCO} = 200 MHz; FM mode	44	50	-	dB
Charge pump: pin CPOUT; see Table 39						
$V_{tune(min)}$	minimum tuning voltage	charge pump CP1				
		T_{amb} = 25 °C	-	-	0.5	V
		T_{amb} = −40 °C	-	-	0.5	V
		charge pump CP4				
		T_{amb} = 25 °C	-	-	0.7	V
		T_{amb} = −40 °C	-	-	0.7	V
$V_{tune(max)}$	maximum tuning voltage	charge pump CP1				
		T_{amb} = 25 °C	$V_{CC(PLL)}$ − 1.3	-	-	V
		T_{amb} = −40 °C	$V_{CC(PLL)}$ − 1.3	-	-	V
		charge pump CP4				
		T_{amb} = 25 °C	$V_{CC(PLL)}$ − 0.7	-	-	V
		T_{amb} = −40 °C	$V_{CC(PLL)}$ − 0.7	-	-	V
$I_{sink(CP1)}$	CP1 sink current	f_{ref} = 100 kHz; V_{CPOUT} = 0.5 V to $V_{CC(PLL)}$ − 1.3 V; $f_{VCO} > f_{ref} \times$ divider ratio	-	180	-	µA
$I_{source(CP1)}$	CP1 source current	f_{ref} = 100 kHz; V_{CPOUT} = 0.5 V to $V_{CC(PLL)}$ − 1.3 V; $f_{VCO} < f_{ref} \times$ divider ratio	-	−180	-	µA
$I_{sink(CP2)}$	CP2 sink current	f_{ref} = 50 kHz; V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 1.5 V; $f_{VCO} > f_{ref} \times$ divider ratio	-	360	-	µA
$I_{source(CP2)}$	CP2 source current	f_{ref} = 50 kHz; V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 1.5 V; $f_{VCO} < f_{ref} \times$ divider ratio	-	−360	-	µA
$I_{sink(CP3)}$	CP3 sink current	f_{ref} = 20 kHz or 25 kHz; V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V; $f_{VCO} > f_{ref} \times$ divider ratio	-	780	-	µA

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{source(CP3)}$	CP3 source current	f_{ref} = 20 kHz or 25 kHz; V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V; $f_{VCO} < f_{ref} \times$ divider ratio	-	−780	-	µA
$I_{sink(CP4)}$	CP4 sink current	f_{ref} = 20 kHz; V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V; $f_{VCO} > f_{ref} \times$ divider ratio	-	1400	-	µA
$I_{source(CP4)}$	CP4 source current	f_{ref} = 20 kHz; V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V; $f_{VCO} < f_{ref} \times$ divider ratio	-	−1400	-	µA
$I_{sink(CP5)}$	CP5 sink current	f_{ref} = 10 kHz; V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V; $f_{VCO} > f_{ref} \times$ divider ratio	-	2200	-	µA
$I_{source(CP5)}$	CP5 source current	f_{ref} = 10 kHz; V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V; $f_{VCO} < f_{ref} \times$ divider ratio	-	−2200	-	µA
Charge pump: pin VTUNE						
$V_{tune(min)}$	minimum tuning voltage	T_{amb} = 25 °C	-	-	0.8	V
		T_{amb} = −40 °C	-	-	0.8	V
$V_{tune(max)}$	maximum tuning voltage	T_{amb} = 25 °C	$V_{CC(PLL)}$ − 0.7	-	-	V
		T_{amb} = −40 °C	$V_{CC(PLL)}$ − 0.7	-	-	V
$I_{o(sink)}$	output sink current	V_{tune} = 0.8 V to $V_{CC(PLL)}$ − 0.7 V; $f_{VCO} > f_{ref} \times$ divider ratio	-	2800	-	µA
$I_{o(source)}$	output source current	V_{tune} = 0.8 V to $V_{CC(PLL)}$ − 0.7 V; $f_{VCO} < f_{ref} \times$ divider ratio	-	−2800	-	µA
Timings						
t_{tune}	tuning time	Europe FM and US FM band; f_{ref} = 100 kHz; f_{RF} = 87.5 MHz to 108 MHz	-	0.75	1	ms
		AM MW band; f_{ref} = 20 kHz; f_{RF} = 0.53 MHz to 1.7 MHz	-	-	10	ms
$t_{upd(AF)}$	AF update time	cycle time for inaudible AF update including 1 ms mute start and 1 ms mute release time	-	6	6.5	ms
Reference frequency for car signal processor IC; output: pin FREF						
f_{ref}	reference frequency	$f_{ref} = f_{xtal}/272$; f_{xtal} = 20.5 MHz	-	75.368	-	kHz
$V_{o(p-p)}$	peak-to-peak output voltage	R_L unloaded	70	140	-	mV
V_O	output voltage		3.2	3.5	3.8	V
R_o	output resistance		-	-	50	kΩ

Table 55. Dynamic characteristics *…continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Antenna Digital Auto Alignment (DAA)						
DAA input: pin DAAIN						
I_{LI}	input leakage current	V_{DAAIN} = 0.4 V to 8 V	–10	-	+10	nA
V_i	input voltage		0	-	8.5	V
DAA output 1: pin DAAOUT1[2]						
V_o	output voltage	FM mode				
		minimum value; data byte DAA bits DAA[6:0] = 000 0000; V_{tune} = 0.5 V	-	-	0.5	V
		maximum value; data byte DAA bits DAA[6:0] = 111 1111; V_{tune} = 4.25 V	$V_{CC(PLL)}$ – 0.5	-	-	V
		V_{tune} = 4 V				
		data byte DAA bits DAA[6:0] = 000 0000	-	-	0.5	V
		data byte DAA bits DAA[6:0] = 100 0000	4.1	4.23	4.4	V
		V_{tune} = 2 V				
		data byte DAA bits DAA[6:0] = 101 0101	2.6	2.74	2.9	V
		data byte DAA bits DAA[6:0] = 010 1010	1.3	1.46	1.5	V
		AM mode; independent of tuning voltage				
		minimum value; data byte DAA bits DAA[6:0] = 000 0000	-	-	0.6	V
		maximum value; data byte DAA bits DAA[6:0] = 111 1111	$V_{CC(PLL)}$ – 0.5	-	-	V
$V_{n(o)}$	output noise voltage	data byte DAA bits DAA[6:0] = 100 0000; FM mode; V_{tune} = 4 V with frequency range from 300 Hz to 22 kHz	-	30	100	µV
$\Delta V_{o(T)}$	output voltage deviation over temperature	T_{amb} = –40 °C to +85 °C; data byte DAA bits DAA[6:0] = 100 0000	–30	-	+30	mV
$\Delta V_{o(step)}$	step output voltage tolerance	n = 0 to 127; FM mode; V_{tune} = 4 V	$-0.5V_{LSB}$	0	$+0.5V_{LSB}$	
ΔV_o	output voltage deviation	V_{tune} = 4 V; I_{load} = 50 µA	$-V_{LSB}$	-	$+V_{LSB}$	
		V_{tune} = 4 V; I_{load} = –50 µA	$-V_{LSB}$	-	$+V_{LSB}$	

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{s(o)}$	output settling time	$V_{DAAOUT1}$ = 0.2 V to 8.25 V; C_L = 270 pF	-	30	60	µs
α_{ripple}	ripple rejection	$V_{CC(ripple)}/V_o$; data byte DAA bits DAA[6:0] = 101 0101; FM mode; V_{tune} = 4 V; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 100 mV	-	40	-	dB
C_L	load capacitance		-	-	270	pF
DAA2: pin DAAOUT2[3]						
V_o	output voltage	AM mode and FM mode				
		minimum value; data byte AGC bits SDAA[3:0] = 0000; $V_{DAAOUT1}$ = 0.5 V	-	-	0.5	V
		maximum value; data byte AGC bits SDAA[3:0] = 1111; $V_{DAAOUT1}$ = 6.3 V	$V_{CC(PLL)}$ – 0.5	-	-	V
		$V_{DAAOUT1}$ = 4 V				
		data byte AGC bits SDAA[3:0] = 0000	2.6	2.8	3.0	V
		data byte AGC bits SDAA[3:0] = 1000	3.99	4.19	4.39	V
		$V_{DAAOUT1}$ = 2 V				
		data byte AGC bits SDAA[3:0] = 1010	2.07	2.27	2.47	V
		data byte AGC bits SDAA[3:0] = 0101	1.63	1.83	2.03	V
$V_{n(o)}$	output noise voltage	data byte AGC bits SDAA[3:0] = 1000; FM mode; $V_{DAAOUT1}$ = 4 V with frequency range from 300 Hz to 22 kHz	-	30	100	µV
$\Delta V_{o(T)}$	output voltage deviation over temperature	T_{amb} = –40 °C to +85 °C; data byte AGC bits SDAA[3:0] = 1000	–30	-	+30	mV
$\Delta V_{o(step)}$	step output voltage tolerance	n = 0 to 15; FM mode; $V_{DAAOUT1}$ = 4 V	$-0.5V_{LSB}$	0	$+0.5V_{LSB}$	
ΔV_o	output voltage deviation	$V_{DAAOUT1}$ = 4 V; I_{load} = 50 µA	$-V_{LSB}$	-	$+V_{LSB}$	
		$V_{DAAOUT1}$ = 4 V; I_{load} = –50 µA	$-V_{LSB}$	-	$+V_{LSB}$	
$t_{s(o)}$	output settling time	$V_{DAAOUT2}$ = 0.2 V to 8.25 V; C_L = 270 pF	-	20	30	µs

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{ripple}	ripple rejection	$V_{CC(ripple)}/V_{DAAOUT2}$; data byte AGC bits SDAA[3:0] = 1010; FM mode; $V_{DAAOUT1}$ = 4 V; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 100 mV	-	50	-	dB
C_L	load capacitance		-	-	270	pF
AM channel						
AM RF AGC detector A (peak detector): pin AMMIX1IN; see Figure 21						
$V_{i(RF)(p-p)}$	peak-to-peak RF input voltage	start level of wideband AGC; m = 1; data byte AGC bits AGC[1:0] = 00 (standard setting); see Table 33	700	1000	1400	mV
AM RF AGC detector B: pin AMIF2IN; see Figure 21						
$V_{i(IF)(p-p)}$	peak-to-peak IF input voltage	start level of AGC; peak-to-peak value of modulated signal; m = 1	175	250	350	mV
RF cascode AGC						
$\alpha_{cr(AGC)}$	AGC control range		-	10	-	dB
V_{VAMCAS}	voltage on pin VAMCAS	cascode base DC voltage at maximum gain at cascode AGC	-	5	-	V
R_{VAMCAS}	resistance on pin VAMCAS	cascode base source resistance	-	1	-	kΩ
$I_{sourceVAMCASmax}$	maximum source current on pin VAMCAS	cascode base source current drive capability	100	-	-	µA
$I_{sink(VAMCAS)}$	sink current on pin VAMCAS	cascode base sink current drive capability	-	0	-	µA
$V_{VAMCASFB}$	voltage on pin VAMCASFB	cascode emitter DC voltage at minimum gain at cascode AGC	-	260	-	mV
		cascode AGC disabled; data byte AGC bit KAGC = 1	-	800	-	mV
$I_{VAMCASFB}$	current on pin VAMCASFB	cascode feedback current	-	-	1	µA
AM RF PIN diode AGC current generator output						
Pin IAMAGC						
$\alpha_{cr(AGC)}$	AGC control range	f_{RF} = 999 kHz; dummy aerial 15 pF/60 pF	-	50	-	dB
V_{IAMAGC}	voltage on pin IAMAGC	PIN diode drive DC voltage	1	-	-	V
$I_{sink(max)}$	maximum sink current	V_{IAMAGC} = 1 V	10	-	-	mA
I_{source}	source current	AGC not active	-	–2.5	-	µA

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{sink}	sink current	FM mode; data byte DAA bit AGCSW = 1		0.5	1	-	mA
		FM mode; data byte DAA bit AGCSW = 0		-	-	100	nA
$C_{o(IAMAGC)}$	output capacitance on pin IAMAGC			-	3	-	pF
Pin VDCPIN							
$V_{o(VDCPIN)}$	output voltage on pin VDCPIN	bias voltage for AM PIN diode	[4]	4.5	5	5.5	V
$R_{source(VDCPIN)}$	source resistance on pin VDCPIN	bias source resistance		-	150	-	Ω
$I_{source(max)}$	maximum source current	maximum bias source current		-	-	–20	mA
$I_{sink(max)}$	maximum sink current	maximum bias sink current capability		30	-	-	µA
AM mixer 1 (IF1 = 10.7 MHz)							
Mixer input: pins AMMIX1IN and AMMIX1DEC							
R_i	input resistance		[5]	40	-	-	kΩ
C_i	input capacitance		[5]	1.5	3	4.5	pF
$V_{i(max)}$	maximum input voltage	on pin AMMIX1IN; 1 dB compression point of $V_{MIX1OUT}$; m = 0		500	-	-	mV
Mixer output: pins MIX1OUT1 and MIX1OUT2							
R_o	output resistance		[6]	100	-	-	kΩ
C_o	output capacitance		[6]	-	4	7	pF
$V_{o(p-p)(max)}$	maximum peak-to-peak output voltage			12	15	-	V
$G_{m(conv)}$	conversion transconductance gain	I_o/V_i		1.79	2.44	3.2	mA/V
$\Delta G_{m(conv)(T)}$	conversion transconductance gain deviation over temperature	$\Delta G_{m(conv)}/(G_{m(conv)} \times \Delta T)$		-	-0.75×10^{-3}	-	K^{-1}
IP3	third-order intercept point	R_L = 2.6 kΩ (AC load between output pins); Δf = 300 kHz		135	138	-	dBµV
IP2	second-order intercept point	R_L = 2.6 kΩ (AC load between output pins)		-	170	-	dBµV
$V_{n(i)(eq)}$	equivalent input noise voltage	band limited noise; R_{source} = 330 Ω; noise of R_{source} included; R_L = 2.6 kΩ (AC load between output pins)		-	5.8	8	nV/√Hz
NF	noise figure			-	4.5	7.1	dB

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AM mixer 2 (IF2 = 450 kHz)							
Mixer input: pins IF1IN and IF1DEC							
R_i	input resistance		[5]	-	330	-	Ω
C_i	input capacitance		[5]	1.5	3	4.5	pF
$V_{i(max)(M)}$	peak maximum input voltage	on pin IF1IN; 1 dB compression point of $V_{AMMIX2OUT}$		1.1	1.4	-	V
Mixer output: pins AMMIX2OUT1 and AMMIX2OUT2							
R_o	output resistance		[8]	50	-	-	kΩ
C_o	output capacitance		[8]	1.5	3	4.5	pF
$V_{o(p-p)(max)}$	maximum peak-to-peak output voltage	$V_{AMMIX2OUT1}$ = 8.5 V; $V_{AMMIX2OUT2}$ = 8.5 V		12	15	-	V
I_{LO}	output leakage current	FM mode; T_{amb} = −40 °C to +85 °C		-	-	10	µA
$G_{m(conv)}$	conversion transconductance gain	I_o/V_i		1.79	2.44	3.2	mA/V
$\Delta G_{m(conv)(T)}$	conversion transconductance gain deviation over temperature	$\Delta G_{m(conv)}/(G_{m(conv)} \times \Delta T)$		-	-0.8×10^{-3}	-	K^{-1}
IP3	third-order intercept point	R_L = 1.5 kΩ (AC load between output pins); Δf = 300 kHz		134	137	-	dBµV
IP2	second-order intercept point	R_L = 1.5 kΩ (AC load between output pins)		-	170	-	dBµV
$V_{n(i)(eq)}$	equivalent input noise voltage	R_{source} = 330 Ω; noise of R_{source} included; R_L = 1.5 kΩ (AC load between output pins)		-	15	22	nV/√Hz
NF	noise figure			-	16	19.5	dB
AM IF2 AGC stage: pins AMIF2IN and AMIF2DEC							
R_i	input resistance		[9]	1.6	2	2.4	kΩ
C_i	input capacitance		[9]	-	5	-	pF
V_i	input voltage	for α = −10 dB audio attenuation	[9]	-	10	20	µV
$V_{stop(AGC)}$	AGC stop voltage	input carrier voltage		100	-	-	mV
AM demodulator output: pin MPXAM; input pins AMIF2IN and AMIF2DEC							
V_{sens}	sensitivity voltage	m = 0.3; f_{mod} = 400 Hz; B_{AF} = 2.15 kHz; R_{source} = 2 kΩ					
		(S+N)/N = 26 dB		-	60	90	µV
		(S+N)/N = 46 dB		-	600	900	µV

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
(S+N)/N	signal plus noise-to-noise ratio	m = 0.3; f_{mod} = 400 Hz; B_{AF} = 2.15 kHz; R_{source} = 2 kΩ	54	60	-	dB
V_o	output voltage	AM mono; m = 0.3; data byte BAND bit AMST = 0; f_{mod} = 400 Hz; V_i = 100 µV to 100 mV	230	290	350	mV
THD	total harmonic distortion	m = 0.8; f_{mod} = 400 Hz; B_{AF} = 2.15 kHz; V_i = 100 µV to 100 mV	-	0.5	1	%
$t_{sw(FM-AM)}$	FM to AM switching time	V_i = 100 µV	-	1000	1500	ms
t_s	settling time	AM AGC				
		V_i = 100 µV to 100 mV	-	400	600	ms
		V_i = 100 mV to 100 µV	-	600	900	ms
V_o	output voltage	IF2 output voltage at AM stereo; m = 0; data byte BAND bit AMST = 1	130	180	230	mV
R_o	output resistance		-	-	500	Ω
C_o	output capacitance		-	3	-	pF
Z_L	load impedance		10	-	-	kΩ
α_{ripple}	ripple rejection	$V_{CC(ripple)}/V_{o(MPXAM)}$; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 50 mV; V_i = 10 mV	20	26	-	dB
AM level detector output: pin LEVEL; see Figure 22; input pins AMIF2IN and AMIF2DEC						
LSL	level slope alignment position	level slope measured from V_i = 0.5 mV to 5 mV; level slope aligned to (800 ± 50) mV/20 dB	0	-	7	
ΔV_{slope}	step size for adjustment of level slope	V_i = 1.4 mV	40	60	80	mV/20 dB
LST	level start alignment position	V_i = 1.4 mV; level slope aligned to (800 ± 50) mV/20 dB; level start aligned to $V_{O(levdet)}$ = 2.1 V ± 0.05 V	4	-	27	
ΔV_{start}	step size for adjustment of level starting point	LSL aligned to 800 mV/20 dB	-	40	72	mV
$V_{start(levdet)}$	level detection start voltage	corner of level curve; LSL[2:0] = 100; LST[4:0] = 1 0000	-	25	42	µV
$\Delta V_{LEVEL(T)}$	voltage variation over temperature on pin LEVEL	T_{amb} = –40 °C to +85 °C	-	0.07	-	dB/K

Table 55. Dynamic characteristics *…continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
B_{levdet}	level detector bandwidth	V_i = 15 mV; default setting of level DAA; T_{amb} = −40 °C to +85 °C	60	90	-	kHz
R_o	output resistance		-	-	500	Ω
R_L	load resistance		25	-	-	kΩ
$C_{L(max)}$	maximum load capacitance		25	-	-	pF
α_{ripple}	ripple rejection	$V_{CC(ripple)}/V_{o(levdet)(AC)}$; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 50 mV; V_i = 10 mV	-	24	-	dB
AM noise blanker						
t_{sup}	suppression time		4	7	11	µs
V_{th}	threshold voltage	detection threshold of noise pulses at RF input (*"CISPR 16-1"*); repetition rate = 100 Hz; pulse duration = 5 ns; rise and fall time < 1 ns; noise pulse combined with an unmodulated RF input signal of $V_{i(RF)}$ = 1 mV; pulse and RF input signal measured at dummy aerial input (15 pF/60 pF); data byte CONTROL bits INS[1:0] = 11	-	1000	-	mV
ΔV_{th}	threshold voltage difference	reference: INS = 11; data byte CONTROL bits INS[1:0] = 10	-	3	-	dB
		reference: INS = 11; data byte CONTROL bits INS[1:0] = 01	-	6	-	dB
FM channel						
FM RF AGC (FM distance mode; data byte AGC bit LODX = 0)						
Input: pins FMMIXIN1 and FMMIXIN2[10]						
$V_{i(RF)AGC(start)}$	start AGC RF input voltage	data byte AGC bits AGC[1:0] = 11	-	9	-	mV
		data byte AGC bits AGC[1:0] = 10	-	12	-	mV
		data byte AGC bits AGC[1:0] = 01	-	17	-	mV
		data byte AGC bits AGC[1:0] = 00	-	24	-	mV

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PIN diode drive output: pin IFMAGC						
$I_{source(max)}$	maximum source current	$V_{TFMAGC} = V_{O(ref)} + 0.5$ V; data byte AGC bit KAGC = 0; $V_i > V_{i(RF)AGC(start)}$	–15	–10	–7	mA
$I_{sink(max)}$	maximum sink current	at AGC decay; $V_{TFMAGC} = V_{O(ref)} - 0.5$ V; data byte AGC bit KAGC = 0	7	10	15	mA
I_{source}	source current	AM mode; data byte DAA bit AGCSW = 1	–15	–10	–7	mA
		AM mode; data byte DAA bit AGCSW = 0	-	0	-	mA
		data byte AGC bit LODX = 1 (FM local)	–0.75	–0.5	–0.35	mA
Threshold voltage for narrow-band AGC: pin LEVEL						
V_{th}	threshold voltage	data byte AGC bit KAGC = 1; see Table 32	500	950	1400	mV
FM mixer 1 (IF1 = 10.7 MHz)						
Mixer input: pins FMMIXIN1 and FMMIXIN2[10]						
$V_{i(RF)(max)}$	maximum RF input voltage	1 dB compression point of FM mixer output voltage	75	100	-	mV
$V_{n(i)(eq)}$	equivalent input noise voltage	R_{source} = 200 Ω; noise of R_{source} included; R_L = 2.6 kΩ	-	2.7	3.2	nV/√Hz
R_i	input resistance	RFGAIN = 0	3	3.8	4.7	kΩ
		RFGAIN = 1	1.6	2.0	2.5	kΩ
C_i	input capacitance		-	2	4	pF
$G_{m(conv)}$	conversion transconductance gain	I_o/V_i; data byte PLLM bit RFGAIN = 0	12	18	25	mA/V
		I_o/V_i; data byte PLLM bit RFGAIN = 1	24	36	50	mA/V
$\Delta G_{m(conv)(T)}$	conversion transconductance gain deviation over temperature	$\Delta G_{m(conv)}/(G_{m(conv)} \times \Delta T)$	-	-0.2×10^{-3}	-	K^{-1}
NF	noise figure	R_{source} = 300 Ω				
		T_{amb} = –40 °C	-	2.8	4.2	dB
		T_{amb} = 25 °C	-	3.1	4.6	dB
		T_{amb} = 85 °C	-	3.5	5.2	dB
$R_{gen(recom)}$	recommended generator resistance		-	200	-	Ω
IP3	third-order intercept point	Δf_{RF} = 800 kHz	117	123	-	dBμV
IRR	image rejection ratio	$V_{o(wanted)}/V_{o(image)}$; $f_{RF(wanted)}$ = 87.5 MHz; $f_{RF(image)}$ = 108.9 MHz	25	35	-	dB

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mixer output: pins MIX1OUT1 and MIX1OUT2[6]						
R_o	output resistance		100	-	-	kΩ
C_o	output capacitance		-	4	6	pF
$V_{o(p-p)(max)}$	maximum peak-to-peak output voltage		4.5	5.6	-	V
FM weather band mixer input: pins WXMIXIN and WXMIXDEC[11]						
R_i	input resistance		-	5.1	-	kΩ
C_i	input capacitance		-	2	4	pF
$G_{m(conv)}$	conversion transconductance gain	I_o/V_i; data byte PLLM bit RFGAIN = 0	10	15	21	mA/V
$\Delta G_{m(conv)(T)}$	conversion transconductance gain deviation over temperature	$\Delta G_{m(conv)}/(G_{m(conv)} \times \Delta T)$	-	-1×10^{-3}	-	K^{-1}
NF	noise figure	R_{source} = 300 Ω	-	3.5	5	dB
$R_{gen(recom)}$	recommended generator resistance		-	200	-	Ω
IP3	third-order intercept point		-	116	-	dBμV
IRR	image rejection ratio	$V_{o(wanted)}/V_{o(image)}$; $f_{RF(wanted)}$ = 162.475 MHz; $f_{RF(image)}$ = 183.875 MHz	20	27	-	dB
FM filter and demodulator						
Tunable filter						
B_{max}	maximum bandwidth	data byte BANDWIDTH bit DYN = 1; dynamic mode	-	130	-	kHz
		data byte BANDWIDTH bits BW[4:0] = 1 1111; fixed mode	-	130	-	kHz
B_{min}	minimum bandwidth	data byte BANDWIDTH bit DYN = 1; dynamic mode	-	45	-	kHz
		data byte BANDWIDTH bits BW[4:0] = 0 0000; fixed mode	-	45	-	kHz
$B_{IF(WX)}$	IF bandwidth (weather band mode)		-	20	-	kHz
$\Delta f_{c(IF2)}$	IF2 center frequency step size		-	2	-	kHz
$f_{c(IF2)(T)}$	IF2 center frequency over temperature		–40	-	+40	Hz/K

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bandwidth indicator: pin IFFLAG						
V_o	output voltage	monitor output voltage for IF2 bandwidth; data byte ACD bit BWFLAG = 0				
		data byte BANDWIDTH bits BW[4:0] = 0 0000	-	2	-	V
		data byte BANDWIDTH bits BW[4:0] = 1 0000	-	1.25	-	V
		data byte BANDWIDTH bits BW[4:0] = 1 1111	-	0.525	-	V
R_o	output resistance		-	5	-	kΩ
B_{th}	threshold bandwidth	data byte ACD bit BWFLAG = 1	-	56	-	kHz
FM demodulator						
FM mixer 2 input: pins IF1IN and IF1DEC[7]						
$V_{i(max)}$	maximum input voltage		200	280	-	mV
$V_{i(start)(lim)}$	limiter start input voltage	α = –3 dB at MPX voltage	-	4	-	μV
$V_{i(sens)}$	input sensitivity voltage	Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 50 μs; R_{source} = 330 Ω				
		(S+N)/N = 26 dB	-	10	-	μV
		(S+N)/N = 46 dB	-	72	-	μV
R_i	input resistance		275	330	400	Ω
C_i	input capacitance		1.5	3	4.5	pF
FM demodulator output: pin MPXAM						
(S+N)/N	signal plus noise-to-noise ratio	FM mode; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 50 μs; V_i = 3 mV; B = 300 Hz to 22 kHz	70	73	-	dB
		weather band mode; Δf = 1.5 kHz; f_{mod} = 1 kHz; de-emphasis = 120 μs; V_i = 10 mV	-	45	-	dB
THD	total harmonic distortion	FM mode; f_{mod} = 1 kHz; V_i = 10 mV				
		Δf = 75 kHz	-	0.2	0.7	%
		Δf = 150 kHz	-	1.5	5.0	%
		weather band mode; f_{mod} = 1 kHz; V_i = 10 mV; Δf = 5 kHz	-	0.7	-	%

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{AM}	AM suppression	$V_{o(FM)}/V_{o(AM)}$; FM mode: Δf = 22.5 kHz; f_{mod} = 1 kHz; AM mode: m = 0.3; f_{mod} = 1 kHz; de-emphasis = 50 µs; V_i = 3 mV	40	60	-	dB
α_{ripple}	ripple rejection	$V_{CC(ripple)}/V_{o(MPXAM)}$; f_{ripple} = 100 Hz to 20 kHz; $V_{CC(ripple)}$ = 50 mV	-	50	-	dB
V_o	output voltage	V_i = 20 µV to 1 V [7]				
		Δf = 1.2 kHz; f_{mod} = 57 kHz	-	7	-	mV
		Δf = 22.5 kHz; f_{mod} = 1 kHz	190	225	265	mV
R_o	output resistance		-	-	500	Ω
R_L	load resistance		20	-	-	kΩ
C_L	load capacitance		20	-	-	pF
f_{-3dB}	cut-off frequency	C_L = 0 pF; R_L > 20 kΩ	-	280	-	kHz
Tuning mute and MPX; input pin: MUTIN and output pin: MUTMPXAM						
α_{mute}	mute attenuation		60	75	-	dB
t_{att}	attack time	soft mute	-	1	-	ms
t_{decay}	decay time	soft mute	-	1	-	ms
G	gain	AM mode and FM mode	–1	0	+1	dB
		weather band mode	22.5	23.5	24.5	dB
R_o	output resistance		-	-	100	Ω
R_L	load resistance		5	-	-	kΩ
C_L	load capacitance		20	-	-	pF
α_{ripple}	ripple rejection	$V_{CC(ripple)}/V_{o(MUTMPXAM)}$; f_{ripple} = 100 Hz to 20 kHz; $V_{CC(ripple)}$ = 50 mV	-	50	-	dB
FM level detector output: pin LEVEL[7]; input: pin IF1IN						
LSL	level slope alignment position	level slope measured from V_i = 0.5 mV to 5 mV; level slope aligned to (800 ± 50) mV/20 dB	0	-	7	
ΔV_{slope}	step size for adjustment of level slope	V_i = 1 mV	40	60	80	mV/20 dB
LST	level start alignment position	V_i = 1 mV; level slope aligned to (800 ± 50) mV/20 dB; level start aligned to $V_{O(levdet)}$ = 2.1 V ± 0.05 V	4	-	27	
ΔV_{start}	step size for adjustment of level starting point	data byte LEVEL bits LSL[2:0] = 100	-	40	72	mV

Table 55. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{start(levdet)}$	level detection start voltage	corner of level curve; LSL[2:0] = 100; LST[4:0] = 1 0000	-	8	20	µV
$\Delta V_{LEVEL(T)}$	voltage variation over temperature on pin LEVEL	T_{amb} = –40 °C to +85 °C; V_i = 1 mV	-	0.06	-	dB/K
f_{-3dB}	cut-off frequency	V_i = 10 mV; default setting of level DAA	100	150	-	kHz
R_o	output resistance		-	-	500	Ω
R_L	load resistance		25	-	-	kΩ
C_L	load capacitance		25	-	-	pF
α_{ripple}	ripple rejection	$V_{CC(ripple)}/V_{o(levdet)(AC)}$; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 50 mV	-	26	-	dB
IF counter (FM IF2 or AM IF2 counter); see Table 8						
Pins IF1IN and IF1DEC[7]						
$V_{i(sens)}$	input sensitivity voltage	FM mode	-	30	100	µV
Pins AMIF2IN and AMIF2DEC[9]						
$V_{i(sens)}$	input sensitivity voltage	AM mode; m = 0	-	150	300	µV
Digital outputs						
Pin AFHOLD						
$I_{sink(max)}$	maximum sink current	AFHOLD = LOW; V_o = 0.4 V	1.0	-	-	mA
Pin AFSAMPLE						
$I_{sink(max)}$	maximum sink current	AFSAMPLE = LOW; V_o = 0.4 V	1.0	-	-	mA
Pin SWPORT1						
$I_{sink(max)}$	maximum sink current	SWPORT1 = LOW; data byte BANDWIDTH bit FLAG = 1; V_o = 0.4 V	1.0	-	-	mA
Pin SWPORT2						
$I_{sink(max)}$	maximum sink current	SWPORT2 = LOW; data byte CONTROL bit SFLAG = 1; V_o = 0.4 V	1.0	-	-	mA

[1] Measured between pins XTAL1 and XTAL2.

[2] Conversion gain formula of DAA output 1: $V_{DAAOUT1} = \left(1.915 \times \frac{n}{128} + 0.1\right) \times V_{tune}$ where n = 0 to 127.

[3] Conversion gain formula of DAA output 2: $V_{DAAOUT2} = \left(0.693 \times \frac{n}{16} + 0.7\right) \times V_{DAAOUT1}$ where n = 0 to 15.

[4] The PIN diode BAP70AM should not be supplied by the internal source at pin VDCPIN, but by an external source.

[5] Input parameters of AM mixer 1 measured between pins AMMIX1IN and AMMIX1DEC.

[6] Output parameters of AM and FM mixer 1 measured between pins MIX1OUT1 and MIX1OUT2.

[7] Input parameters of FM mixer 2 measured between pins IF1IN and IF1DEC.

[8] Output parameters of AM mixer 2 measured between pins AMMIX2OUT1 and AMMIX2OUT2.

[9] Input parameters of AM mixer 2 measured between pins AMIF2IN and AMIF2DEC.

[10] Input parameters of FM mixer 1 measured between pins FMIFAGCIN2 and IFAGCDEC.

[11] Input parameters of FM mixer 1 measured between pins WXMIX1IN and WXMIX1DEC.

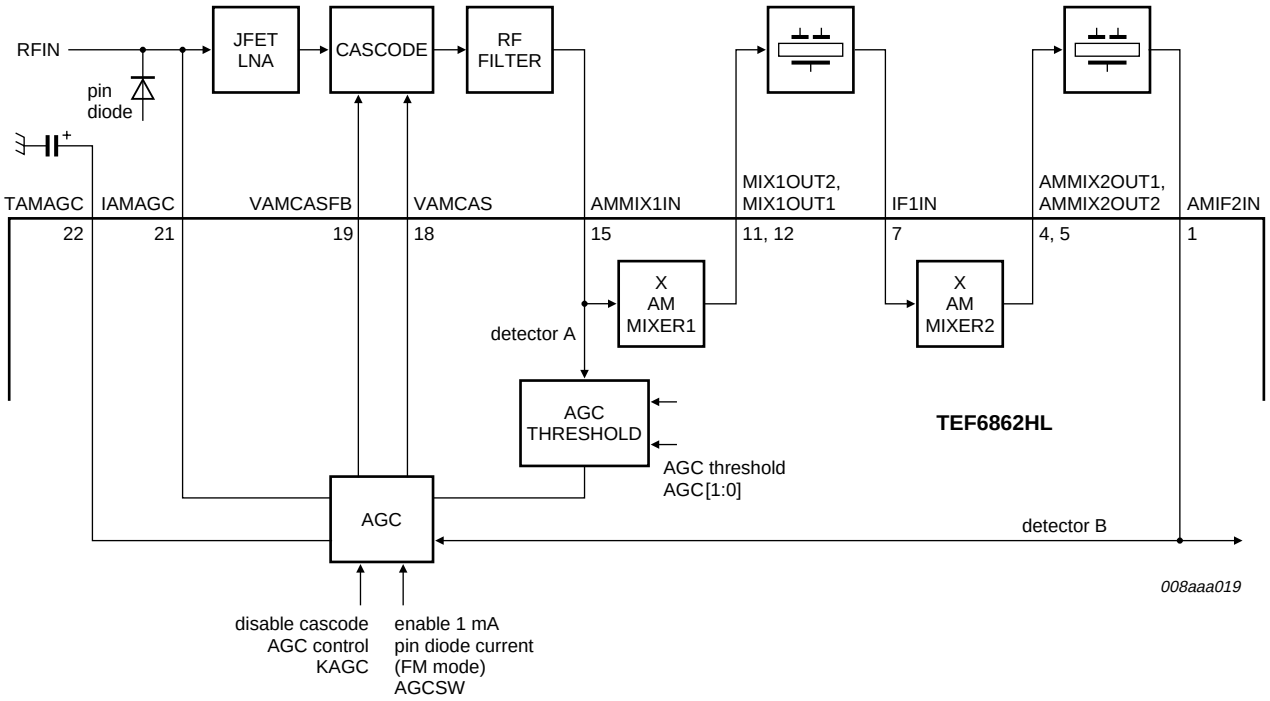
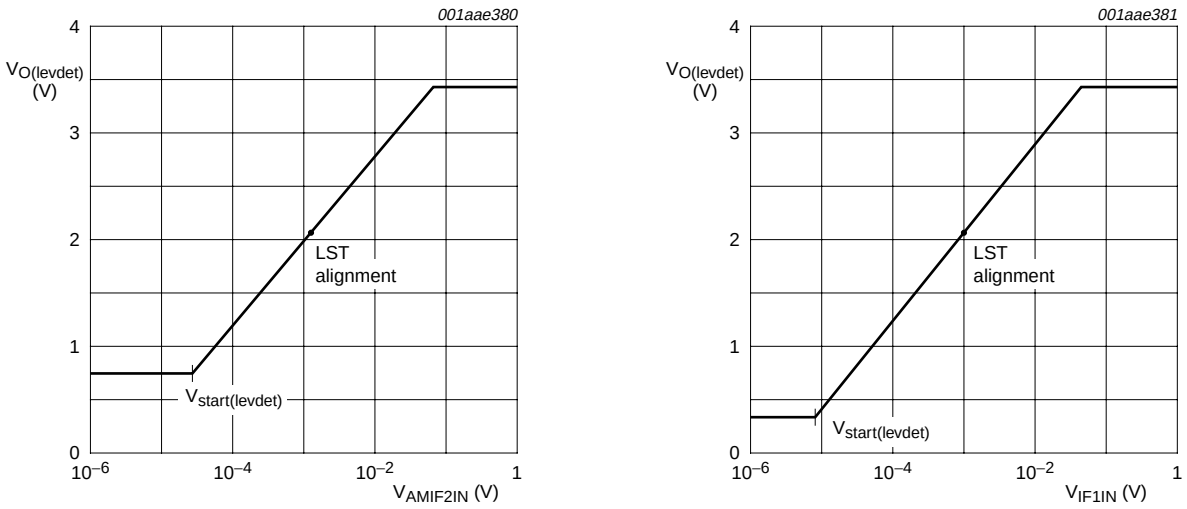


Fig 21. AM AGC circuit



a. AM level curve.

b. FM level curve.

Fig 22. Level detector function

13. I²C-bus characteristics

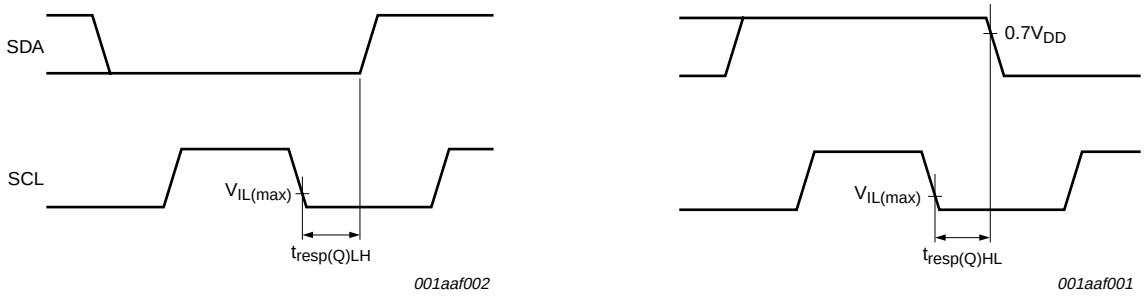
The maximum I²C-bus communication speed is 400 kbit/s. The TEF6862HL is compatible with the autogate function of the TEF689xH. SDA and SCL HIGH and LOW internal thresholds are specified according to an I²C-bus voltage range from 2.5 V to 3.3 V including I²C-bus voltage tolerances of ±10 %. The I²C-bus interface tolerates also SDA and SCL signals from a 5 V bus. Restrictions for V_{IL} in a 5 V application can be derived from Table 56.

Table 56. I²C-bus parameters

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage			-	-	1.09	V
V_{IH}	HIGH-level input voltage			1.56	-	-	V
C_i	capacitance for each I/O pin	pin SDA		-	4	6	pF
		pin SCL		-	3	5	pF
$t_{resp(Q)HL}$	HIGH-to-LOW data output response time	acknowledge and read data; see Figure 23					
		V_{DD} = 5 V; I = 3 mA; C_b = 400 pF		-	700	863	ns
		V_{DD} = 3.3 V; R_p = 1.8 kΩ; C_b = 400 pF		-	570	668	ns
		V_{DD} = 2.5 V; R_p = 35 kΩ; C_b = 10 pF		-	520	593	ns
$t_{resp(Q)LH}$	LOW-to-HIGH data output response time	read data; see Figure 23		-	450	488	ns
t_{of}	output fall time from V_{IHmin} to V_{ILmax}	C_b = 10 pF to 120 pF; see Figure 24	[1]	20 + 0.1C_b	10 × V_{DD}	-	ns
		C_b ≥ 120 pF; see Figure 24	[1][2]	20 + 0.1C_b	-	250	ns

[1] Minimum value of t_{of}; C_b = total capacitance of one I²C-bus line [pF].

[2] Typical value of t_{of}; the output fall time t_{of} [ns] depends on the total load capacitance C_b [pF] and the I²C-bus voltage V_{DD} [V]: $t_{of} = {}^{1}/_{12} \times V_{DD} \times C_b$.



a. Data change from LOW to HIGH

b. Data change from HIGH to LOW

Fig 23. Data output response time of the IC

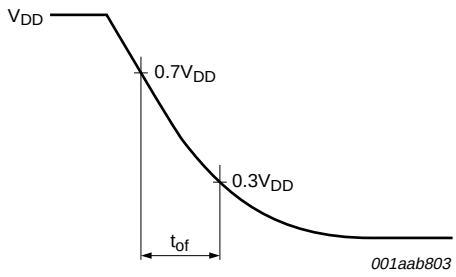


Fig 24. Definition of the fall time of the output signal

14. Overall system parameters

Table 57. Overall system parameters

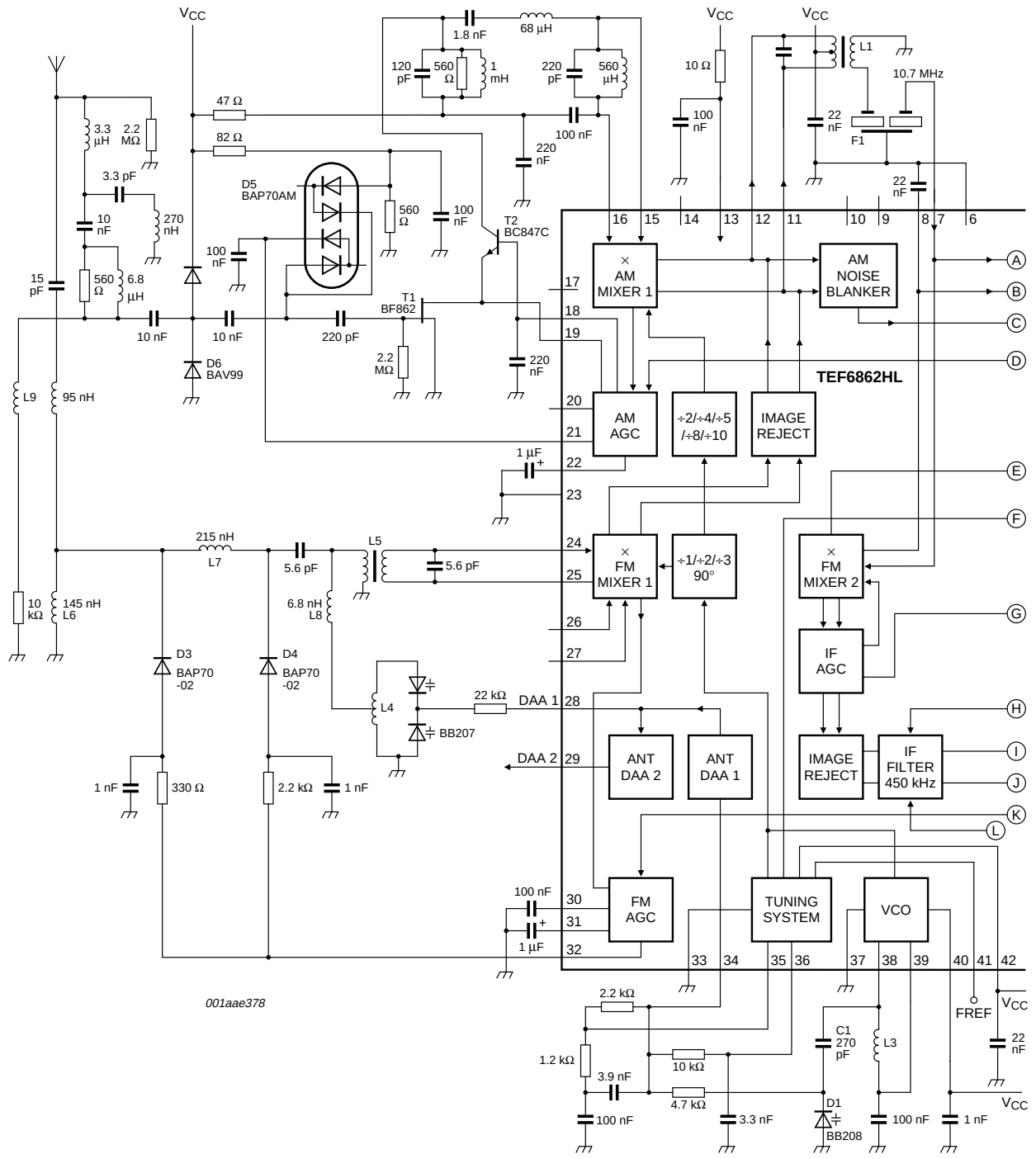
V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM overall system parameters[1]						
$f_{i(RF)}$	RF input frequency	LW	144	-	288	kHz
		MW	522	-	1710	kHz
		SW	2.3	-	26.1	MHz
V_{sens}	sensitivity voltage	(S+N)/N = 26 dB	-	45	-	µV
(S+N)/N	signal plus noise-to-noise ratio		54	58	-	dB
THD	total harmonic distortion	200 µV < $V_{i(RF)}$ < 1 V; m = 0.8	-	0.5	1	%
IP3	third-order intercept point		-	130	-	dBµV
FM overall system parameters[2]						
$f_{i(RF)}$	RF input frequency		65	-	108	MHz
V_{sens}	sensitivity voltage	(S+N)/N = 26 dB				
		IF bandwidth wide	-	2	-	µV
		IF bandwidth dynamic; threshold extension off	-	1.8	-	µV
		IF bandwidth dynamic; threshold extension on	-	1.6	-	µV
(S+N)/N	signal plus noise-to-noise ratio	V_i = 3 mV; IF bandwidth wide	-	63	-	dB
THD	total harmonic distortion	Δf = 75 kHz	-	0.2	0.7	%
IP3	third-order intercept point		-	123	-	dBµV
Weatherband overall system parameters[2]; see Figure 27						
$f_{i(RF)}$	RF input frequency		162.4	-	162.55	MHz
(S+N)/N	signal plus noise-to-noise ratio	Δf = 1.5 kHz; $V_{i(RF)}$ = 10 mV; de-emphasis = 120 µs	-	45	-	dB
THD	total harmonic distortion	Δf = 5 kHz	-	0.7	-	%

[1] Based on 15 pF/60 pF dummy aerial, voltages at dummy aerial input, f_{mod} = 400 Hz, 2.15 kHz audio bandwidth, $f_{i(RF)}$ = 990 kHz, m = 0.3, unless otherwise specified.

[2] Based on 75 Ω dummy aerial, voltages at dummy aerial input, f_{mod} = 1 kHz, de-emphasis = 50 µs, B = 300 Hz to 22 kHz, Δf = 22.5 kHz, unless otherwise specified.

15. Application information



For list of components see Table 58.

Fig 25. Application diagram of TEF6862HL (continued in Figure 26)

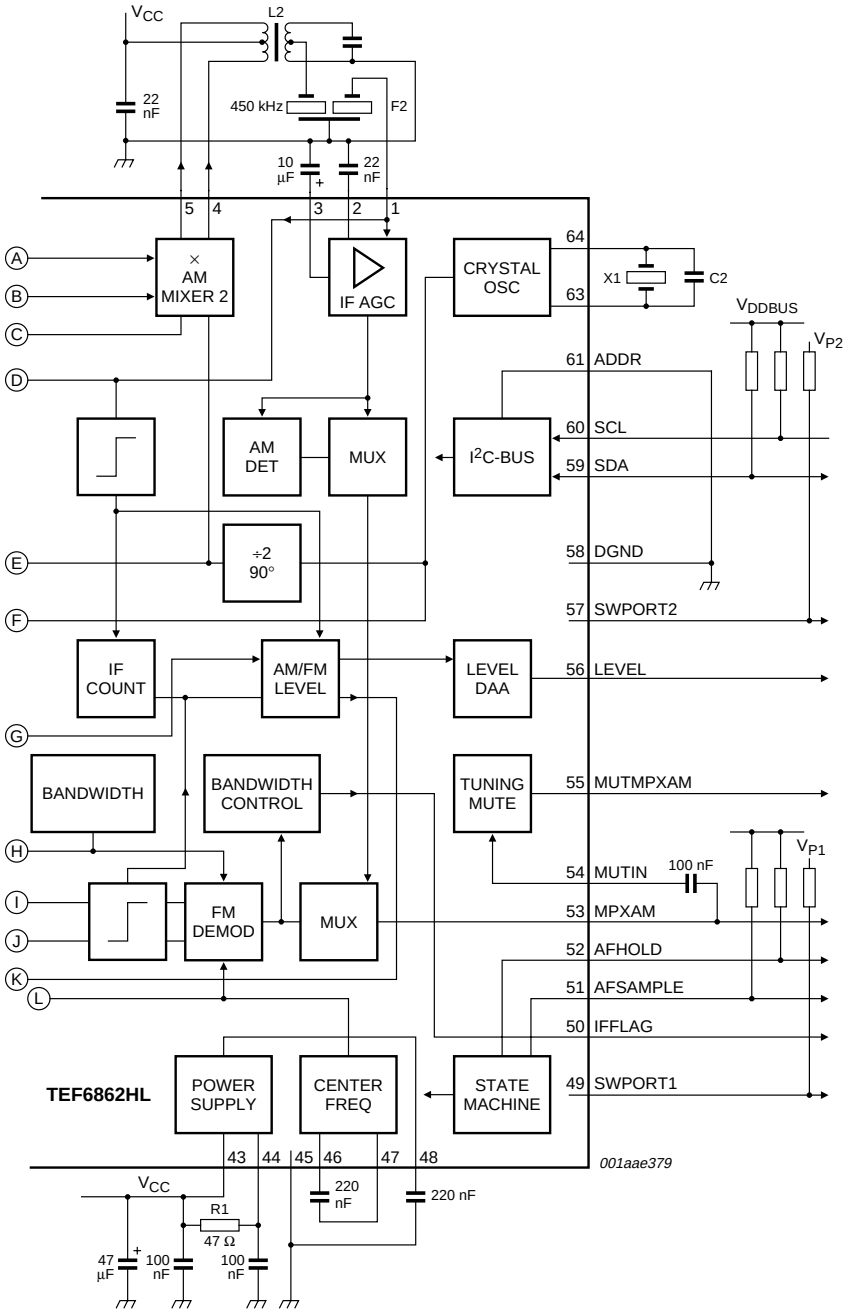


Fig 26. Application diagram of TEF6862HL (continued from Figure 25)

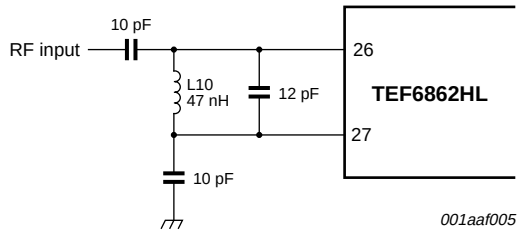


Fig 27. Weather band application

Table 58. List of components of Figure 25, Figure 26 and Figure 27

Symbol	Component	Type	Manufacturer
C1	capacitor for VCO tuning	270 pF; type NP0	-
C2	capacitor for frequency pulling	1.8 pF; type NP0[1]	-
R1	resistor for supply V_{V60}	47 Ω; 0.2 W	-
L1	10.7 MHz IF coil	PF670CCS-A065DX	TOKO
L2	450 kHz IF coil	P7PSGAE-A021YBY=S	TOKO
L3	oscillator coil	E543SNAS-02010	TOKO
L4	FM image rejection	611SNS-1066Y	TOKO
L5	FM input transformer	369INS-3076X	TOKO
L6	FM antenna coil	LQN1HR; 145 nH	MURATA
L7	PIN diode bias	LQN1HR; 215 nH	MURATA
L8	connection image reject	6.8 nH	-
L9	AM input	388BN-1211Z	TOKO
L10	weather band input coil	47 nH; LQW31H	MURATA
X1	crystal 20.5 MHz	LN-G102-587	NDK
D1	diode	BB208	Philips
D2	diode	BB207	Philips
D3	diode	BAP70-02	Philips
D4	diode	BAP70-02	Philips
D5	diode	BAP70AM	Philips
D6	diode	BAV99	Philips
T1	transistor	BF862	Philips
T2	transistor	BC847C	Philips
F1	ceramic filter	10.7 MHz; SFELA10M7HAA0-B0	MURATA
F2	ceramic filter	450 kHz; CFWLA450KGFA-B0	MURATA

[1] The capacitor is used to achieve a crystal frequency of 20.5 MHz together with the crystal type LN-G102-587.

Table 59. DC operating points

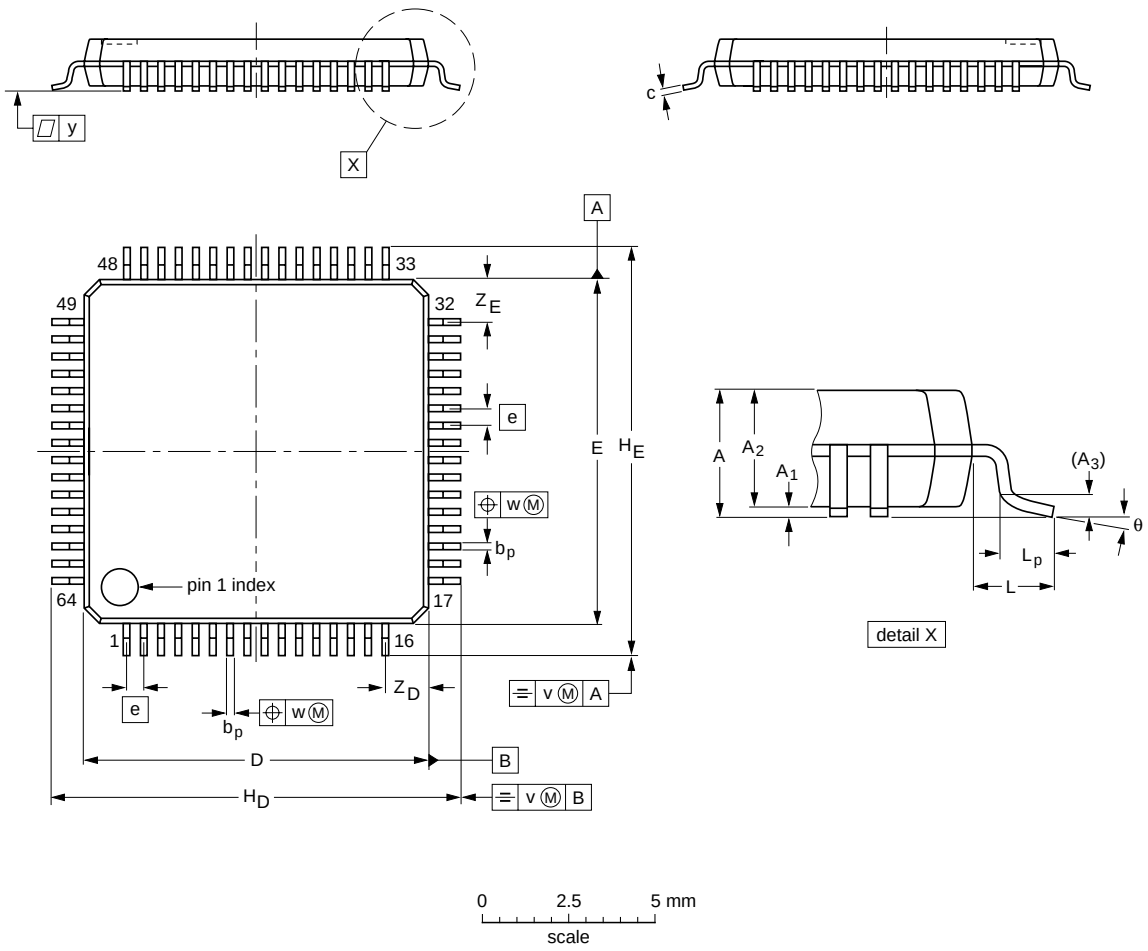
Symbol	Pin	Unloaded DC voltage (V)					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
AMIF2IN	1	-	2.8	-	floating		
AMIF2DEC	2	-	2.8	-	floating		
TAMIFAGC	3	-	4	-	floating		
AMMIX2OUT1	4	external 8.5			external 8.5		
AMMIX2OUT2	5	external 8.5			external 8.5		
IF1GND	6	external GND			external GND		
IF1IN	7	-	3.1	-	-	2.5	-
IF1DEC	8	-	3.1	-	-	2.5	-
i.c.	9	-	-	-	-	-	-
TESTIFOUT	10	-	8.35	-	-	test pin active: 7.6; test pin not active: 8.3	-
MIX1OUT2	11	external 8.5			external 8.5		
MIX1OUT1	12	external 8.5			external 8.5		
VCCRF	13	external 8.5			external 8.5		
i.c.	14	-	-	-	-	-	-
AMMIX1IN	15	-	4.4	-	floating		
AMMIX1DEC	16	-	4.4	-	floating		
i.c.	17	-	-	-	-	-	-
VAMCAS	18	-	5	-	-	0	-
VAMCASFB	19	-	4.3	-	-	0	-
VDCPIN	20	-	5	-	-	5	-
IAMAGC	21	external biasing			external biasing		
TAMAGC	22	-	1.4	-	floating		
RFGND	23	external GND			external GND		
FMMIX1IN1	24	-	0	-	FM: 2.0; WB: 0	FM: 2.8; WB: 0	FM: 3.0; WB: 0.5
FMMIX1IN2	25	-	0	-	FM: 2.0; WB: 0	FM: 2.8; WB: 0	FM: 3.0; WB: 0.5
WXMIX1IN	26	-	0	-	WB: 2.0; FM: 0	WB: 2.8; FM: 0	WB: 3.0; FM: 0.5
WXMIX1DEC	27	-	0	-	WB: 2.0; FM: 0	WB: 2.8; FM: 0	WB: 3.0; FM: 0.5
DAAOUT1	28	0	-	8.5	0	-	8.5
DAAOUT2	29	0	-	8.5	0	-	8.5
TFMAGC	30	-	0.8	-	-	0.8	-
KAGC	31	-	4.7	-	-	2.5	-
IFMAGC	32	-	0	-	external biasing		
PLLGND	33	external GND			external GND		
DAAIN	34	0	-	8.5	0	-	8.5

Table 59. DC operating points *…continued*

Symbol	Pin	Unloaded DC voltage (V)					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
VTUNE	35	0	-	8.5	0	-	8.5
CPOUT	36	0	-	8.5	0	-	8.5
VCOGND	37	external GND			external GND		
OSCFDB	38	-	7.4	-	-	7.4	-
OSCTNK	39	-	7.4	-	-	7.4	-
VCCVCO	40	external 8.5			external 8.5		
FREF	41	3.2	3.5	3.8	3.2	3.5	3.8
VCCPLL	42	external 8.5			external 8.5		
VCC	43	external 8.5			external 8.5		
V60	44	external > 5.5			external > 5.5		
IF2GND	45	external GND			external GND		
VTCENTRE	46	-	0	-	-	1.3	-
VTCM	47	-	0	-	-	4.2	-
VREF	48	4.1	4.3	4.5	4.1	4.3	4.5
SWPORT1	49	open-collector			open-collector		
IFFLAG	50	-	2	-	IFFLAG = 1: open-collector; IFFLAG = 0: 0.5 to 2		
AFSAMPLE	51	-	0	-	-	0	-
AFHOLD	52	-	5	-	-	5	-
MPXAM	53	4.2	-	5	-	4.3	-
MUTIN	54	-	4.3	-	-	4.3	-
MUTMPXAM	55	-	4.3	-	-	4.3	-
LEVEL	56	0	-	7	0	-	7
SWPORT2	57	open-collector			open-collector		
DGND	58	external GND			external GND		
SDA	59	external I^2C-bus voltage			external I^2C-bus voltage		
SCL	60	external I^2C-bus voltage			external I^2C-bus voltage		
ADDR	61	external			external		
i.c.	62	-	-	-	-	-	-
XTAL2	63	-	6	-	-	6	-
XTAL1	64	-	6	-	-	6	-

16. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 28. Package outline SOT314-2 (LQFP64)

17. Soldering

17.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 60. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 61. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

- larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

17.5 Package related soldering information

Table 62. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

18. Abbreviations

Table 63. Abbreviations

Acronym	Description
AF	Alternative Frequency
AFU	Alternative Frequency Updating
AGC	Automatic Gain Control
DAA	Digital Auto Alignment
DX	Distance
IC	Integrated Circuit
IF	Intermediate Frequency
JFET	Junction Field Effect Transistor
LO	Local Oscillator
MPX	Multiplex
LW	Long Wave
MW	Medium Wave
PLL	Phase-Locked Loop
POR	Power-On Reset
RDS	Radio Data System
RF	Radio Frequency
RSSI	Radio Signal Strength Information
SW	Short Wave
VCO	Voltage-Controlled Oscillator
WB	Weather Band

19. Revision history

Table 64. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEF6862_1	20060914	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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