THE DATASHEET OF

TL16C752BLPTREP

www.win-source.net 0086-755-83957316

3.3 V DUAL UART WITH 64-BYTE FIFO

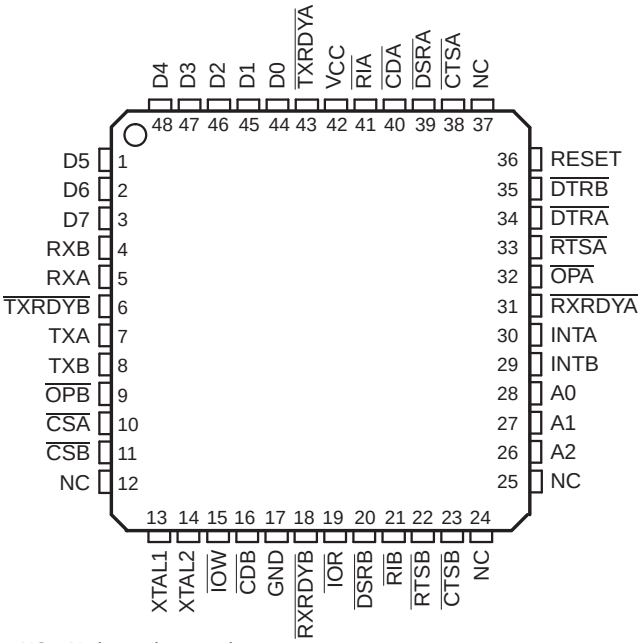
Check for Samples: TL16C752B-EP

FEATURES

- **Controlled Baseline**
  - **One Assembly Site**
  - **Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 110°C and –40°C to 105°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree** (1)
- **Pin Compatible With ST16C2550 With Additional Enhancements**
- **Up to 1.5-Mbps Baud Rate When Using Crystal (24-MHz Input Clock)**
- **Up to 3-Mbps Baud Rate When Using Oscillator or Clock Source (48-MHz Input Clock)**
- **64-Byte Transmit FIFO**
- **64-Byte Receive FIFO With Error Flags**
- **Programmable and Selectable Transmit and Receive FIFO Trigger Levels for DMA and Interrupt Generation**
- **Programmable Receive FIFO Trigger Levels for Software/Hardware Flow Control**
- **Software/Hardware Flow Control**
  - **Programmable Xon/Xoff Characters**
  - **Programmable Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$**
- **Optional Data Flow Resume by Xon Any Character**
- **DMA Signaling Capability for Both Received and Transmitted Data**
- **Supports 3.3-V Operation**
- **Software Selectable Baud Rate Generator**
- **Prescaler Provides Additional Divide By Four Function**
- **Fast Access Time 2 Clock Cycle $\overline{\text{IOR}}$/$\overline{\text{IOW}}$ Pulse Width**
- **Programmable Sleep Mode**
- **Programmable Serial Interface Characteristics**
  - **5-Bit, 6-Bit, 7-Bit, or 8-Bit Characters**
  - **Even, Odd, or No Parity Bit Generation and Detection**
  - **1, 1.5, or 2 Stop Bit Generation**
- **False Start Bit Detection**
- **Complete Status Reporting Capabilities in Both Normal and Sleep Mode**
- **Line Break Generation and Detection**
- **Internal Test and Loopback Capabilities**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, and $\overline{\text{CD}}$)**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PACKAGE
(TOP VIEW)



NC − No internal connection

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DESCRIPTION/ORDERING INFORMATION

The TL16C752B is a dual-universal asynchronous receiver/transmitter (UART) with 64-byte FIFOs, automatic hardware/software flow control, and data rates up to 3 Mbps. The TL16C752B offers enhanced features. It has a transmission control register (TCR) that stores receiver FIFO threshold levels to start/stop transmission during hardware and software flow control. With the FIFO RDY register, the software gets the status of TXRDY/RXRDY for all four ports in one access. On-chip status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows onboard diagnostics.The UART transmits data, sent to it over the peripheral 8-bit bus, on the TX signal and receives characters on the RX signal. Characters can be programmed to be 5, 6, 7, or 8 bits. The UART has a 64-byte receive FIFO and transmit FIFO and can be programmed to interrupt at different trigger levels. The UART generates its own desired baud rate based upon a programmable divisor and its input clock. It can transmit even, odd, or no parity and 1, 1.5, or 2 stop bits. The receiver can detect break, idle, or framing errors, FIFO overflow, and parity errors. The transmitter can detect FIFO underflow. The UART also contains a software interface for modem control operations, and has software flow control and hardware flow control capabilities.

The TL16C752B is available in a 48-pin PT (LQFP) package.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)
–40°C to 105°C	TL16C752BTPTREP
–55°C to 110°C	TL16C752BLPTREP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A0	28	I	Address 0 select bit. Internal registers address selection.
A1	27	I	Address 1 select bit. Internal registers address selection.
A2	26	I	Address 2 select bit. Internal registers address selection.
$\overline{CDA}$, $\overline{CDB}$	40, 16	I	Carrier detect (active low). These inputs are associated with individual UART channels A and B. A low on these pins indicates that a carrier has been detected by the modem for that channel. The state of these inputs is reflected in the modem status register (MSR).
$\overline{CSA}$, $\overline{CSB}$	10, 11	I	Chip select A and B (active low). These pins enable data transfers between the user CPU and the TL16C752B for the channel(s) addressed. Individual UART sections (A, B) are addressed by providing a low on the respective $\overline{CSA}$ and $\overline{CSB}$ pins.
$\overline{CTSA}$, $\overline{CTSB}$	38, 23	I	Clear to send (active low). These inputs are associated with individual UART channels A and B. A logic low on the CTS pins indicates the modem or data set is ready to accept transmit data from the TL16C752B. Status can be tested by reading MSR bit 4. These pins only affect the transmit and receive operations when auto CTS function is enabled through the enhanced feature register (EFR) bit 7, for hardware flow control operation.
D0–D4 D5–D7	44–48, 1–3	I/O	Data bus (bidirectional). These pins are the eight bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
$\overline{DSRA}$, $\overline{DSRB}$	39, 20	I	Data set ready (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem or data set is powered on and is ready for data exchange with the UART. The state of these inputs is reflected in the modem status register (MSR).
$\overline{DTRA}$, $\overline{DTRB}$	34, 35	O	Data terminal ready (active low). These outputs are associated with individual UART channels A and B. A logic low on these pins indicates that the TL16C752B is powered on and ready. These pins can be controlled through the modem control register. Writing a 1 to MCR bit 0 sets the $\overline{DTR}$ output to low, enabling the modem. The output of these pins is high after writing a 0 to MCR bit 0, or after a reset.
GND	17	Pwr	Signal and power ground
INTA, INTB	30, 29	O	Interrupt A and B (active high). These pins provide individual channel interrupts, INT A and B. INT A and B are enabled when MCR bit 3 is set to a logic 1, interrupt sources are enabled in the interrupt enable register (IER). Interrupt conditions include: receiver errors, available receiver buffer data, available transmit buffer space or when a modem status flag is detected. INTA-B are in the high-impedance state after reset.
$\overline{IOR}$	19	I	Read input (active low strobe). A high-to-low transition on $\overline{IOR}$ loads the contents of an internal register defined by address bits A0–A2 onto the TL16C752B data bus (D0–D7) for access by an external CPU.
$\overline{IOW}$	15	I	Write input (active low strobe). A low-to-high transition on $\overline{IOW}$ transfers the contents of the data bus (D0–D7) from the external CPU to an internal register that is defined by address bits A0–A2 and $\overline{CSA}$ and $\overline{CSB}$.
$\overline{OPA}$, $\overline{OPB}$	32, 9	O	User-defined outputs. This function is associated with individual channels A and B. The state of these pins is defined by the user through the software settings of the MCR register, bit 3. INTA-B are set to active mode and $\overline{OP}$ to a logic 0 when the MCR-3 is set to a logic 1. INTA-B are set to the 3-state mode and $\overline{OP}$ to a logic 1 when MCR-3 is set to a logic 0. See bit 3, modem control register (MCR bit 3). The output of these two pins is high after reset.
RESET	36	I	Reset. RESET resets the internal registers and all the outputs. The UART transmitter output and the receiver input is disabled during reset time. See TL16C752B external reset conditions for initialization details. RESET is an active-high input.
$\overline{RIA}$, $\overline{RIB}$	41, 21	I	Ring indicator (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem has received a ringing signal from the telephone line. A low-to-high transition on these input pins generates a modem status interrupt, if enabled. The state of these inputs is reflected in the modem status register (MSR).
$\overline{RTSA}$, $\overline{RTSB}$	33, 22	O	Request to send (active low). These outputs are associated with individual UART channels A and B. A low on the $\overline{RTS}$ pin indicates the transmitter has data ready and waiting to send. Writing a 1 in the modem control register (MCR bit 1) sets these pins to low, indicating data is available. After a reset, these pins are set to high. These pins only affect the transmit and receive operation when auto $\overline{RTS}$ function is enabled through the enhanced feature register (EFR) bit 6, for hardware flow control operation.
RXA, RXB	5, 4	I	Receive data input. These inputs are associated with individual serial channel data to the TL16C752B. During the local loopback mode, these RX input pins are disabled and TX data is internally connected to the UART RX input internally.
$\overline{RXRDYA}$, $\overline{RXRDYB}$	31, 18	O	Receive ready (active low). $\overline{RXRDY}$ A and B goes low when the trigger level has been reached or a timeout interrupt occurs. They go high when the RX FIFO is empty or there is an error in RX FIFO.

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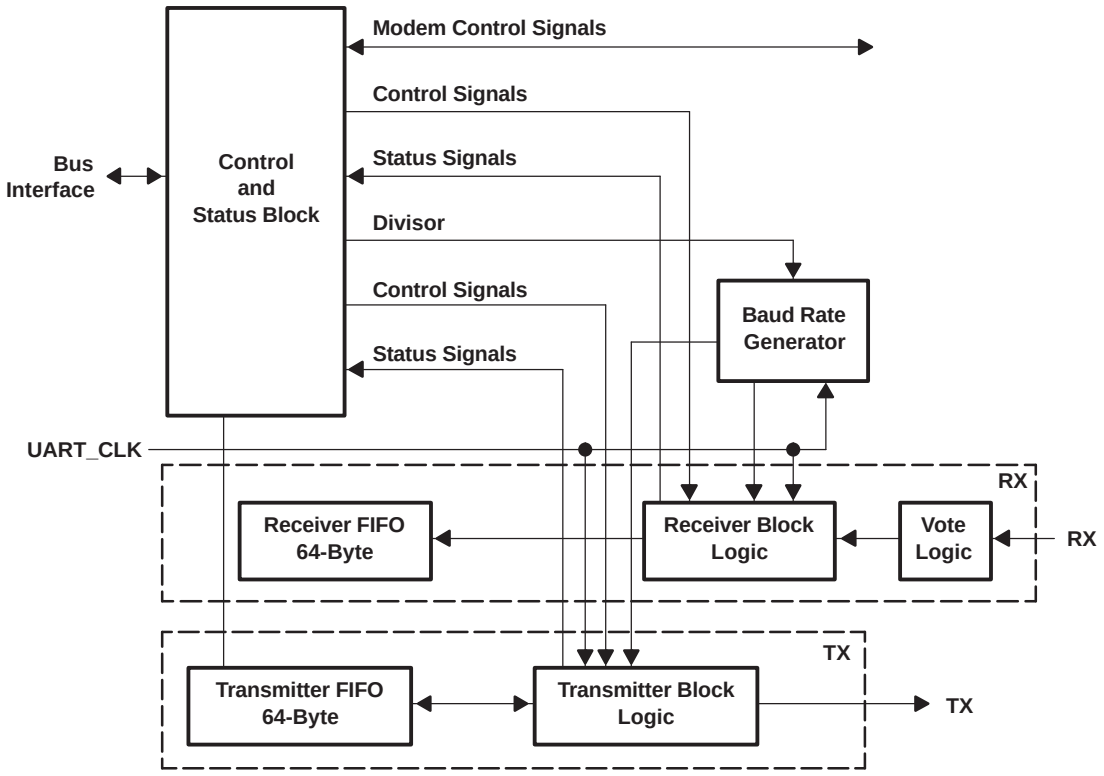
TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
TXA, TXB	7, 8	O	Transmit data. These outputs are associated with individual serial transmit channel data from the TL16C752B. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX input.
$\overline{\text{TXRDYA}}$, $\overline{\text{TXRDYB}}$	43, 6	O	Transmit ready (active low). $\overline{\text{TXRDY}}$ A and B go low when there are at least a trigger level numbers of spaces available. They go high when the TX buffer is full.
V_{CC}	42	I	Power supply inputs
XTAL1	13	I	Crystal or external clock input. XTAL1 functions as a crystal input or as an external clock input. A crystal can be connected between XTAL1 and XTAL2 to form an internal oscillator circuit (see Figure 10). Alternatively, an external clock can be connected to XTAL1 to provide custom data rates.
XTAL2	14	O	Output of the crystal oscillator or buffered clock. See also XTAL1. XTAL2 is used as a crystal oscillator output or buffered a clock output.

FUNCTIONAL BLOCK DIAGRAM



A. The vote logic determines whether the RX data is a logic 1 or 0. It takes three samples of the RX line and uses a majority vote to determine the logic level received. The vote logic operates on all bits received.

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FUNCTIONAL DESCRIPTION

The TL16C752B UART is pin-compatible with the ST16C2550 UART. It provides more enhanced features. All additional features are provided through a special enhanced feature register.

The UART performs a serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-parallel conversion on data characters transmitted by the processor. The complete status of each channel of the TL16C752B UART can be read at any time during functional operation by the processor.

The TL16C752B can be placed in an alternate mode (FIFO mode) relieving the processor of excessive software overhead by buffering received/transmitted characters. Both the receiver and transmitter FIFOs can store up to 64 bytes (including three additional bits of error status per byte for the receiver FIFO) and have selectable or programmable trigger levels. Primary outputs RXRDY and TXRDY allow signalling of DMA transfers.

The TL16C752B has selectable hardware flow control and software flow control. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the $\overline{\text{RTS}}$ output and $\overline{\text{CTS}}$ input signals. Software flow control automatically controls data flow by using programmable Xon/Xoff characters.

The UART includes a programmable baud rate generator that can divide the timing reference clock input by a divisor between 1 and (2^{16}–1).

Trigger Levels

The TL16C752B provides independent selectable and programmable trigger levels for both receiver and transmitter DMA and interrupt generation. After reset, both transmitter and receiver FIFOs are disabled and so, in effect, the trigger level is the default value of one byte. The selectable trigger levels are available via the FCR. The programmable trigger levels are available via the TLR.

Hardware Flow Control

Hardware flow control is comprised of auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$. Auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$ can be enabled/disabled independently by programming EFR[7:6].

With auto-$\overline{\text{CTS}}$, $\overline{\text{CTS}}$ must be active before the UART can transmit data.

Auto-$\overline{\text{RTS}}$ only activates the $\overline{\text{RTS}}$ output when there is enough room in the FIFO to receive data and deactivates the $\overline{\text{RTS}}$ output when the RX FIFO is sufficiently full. The halt and resume trigger levels in the TCR determine the levels at which $\overline{\text{RTS}}$ is activated/deactivated.

If both auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$ are enabled, when $\overline{\text{RTS}}$ is connected to CTS, data transmission does not occur unless the receiver FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If not enabled, overrun errors occur if the transmit data rate exceeds the receive FIFO servicing latency.

Auto-$\overline{\text{RTS}}$

Auto-$\overline{\text{RTS}}$ data flow control originates in the receiver block (see functional block diagram). **Figure 1** shows $\overline{\text{RTS}}$ functional timing. The receiver FIFO trigger levels used in auto-$\overline{\text{RTS}}$ are stored in the TCR. $\overline{\text{RTS}}$ is active if the RX FIFO level is below the halt trigger level in TCR[3:0]. When the receiver FIFO halt trigger level is reached, $\overline{\text{RTS}}$ is deasserted. The sending device (e.g., another UART) may send an additional byte after the trigger level is reached (assuming the sending UART has another byte to send), because it may not recognize the deassertion of $\overline{\text{RTS}}$ until it has begun sending the additional byte. $\overline{\text{RTS}}$ is automatically reasserted once the receiver FIFO reaches the resume trigger level programmed via TCR[7:4]. This reassertion allows the sending device to resume transmission.

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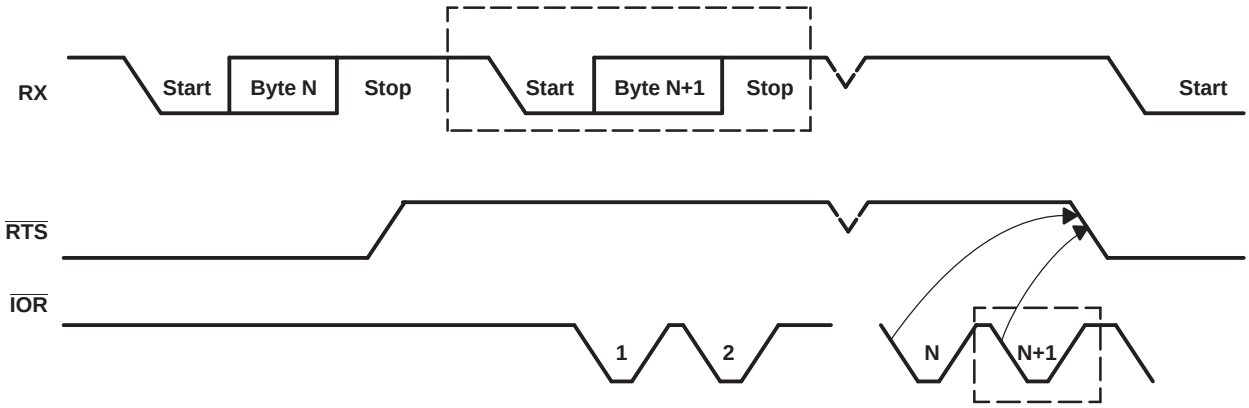


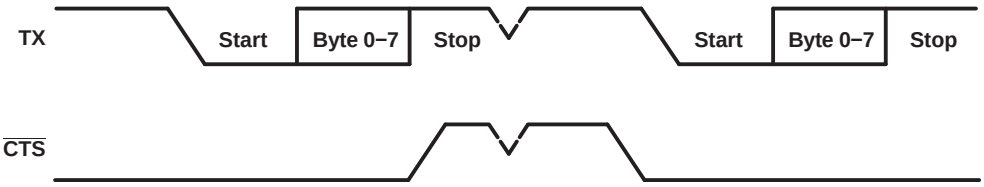
A. N = receiver FIFO trigger level 2.

B. The two blocks in dashed lines cover the case where an additional byte is sent as described in Auto-$\overline{\text{RTS}}$.

Figure 1. $\overline{\text{RTS}}$ Functional Timing

Auto-$\overline{\text{CTS}}$

The transmitter circuitry checks $\overline{\text{CTS}}$ before sending the next data byte. When $\overline{\text{CTS}}$ is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, $\overline{\text{CTS}}$ must be deasserted before the middle of the last stop bit that is currently being sent. The auto-$\overline{\text{CTS}}$ function reduces interrupts to the host system. When flow control is enabled, the $\overline{\text{CTS}}$ state changes and need not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{\text{CTS}}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result. **Figure 2** shows $\overline{\text{CTS}}$ functional timing, and **Figure 3** shows an example of autoflow control.



A. When $\overline{\text{CTS}}$ is low, the transmitter keeps sending serial data out

B. When $\overline{\text{CTS}}$ goes high before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte but it does not send the next byte.

C. When $\overline{\text{CTS}}$ goes from high to low, the transmitter begins sending data again.

Figure 2. $\overline{\text{CTS}}$ Functional Timing

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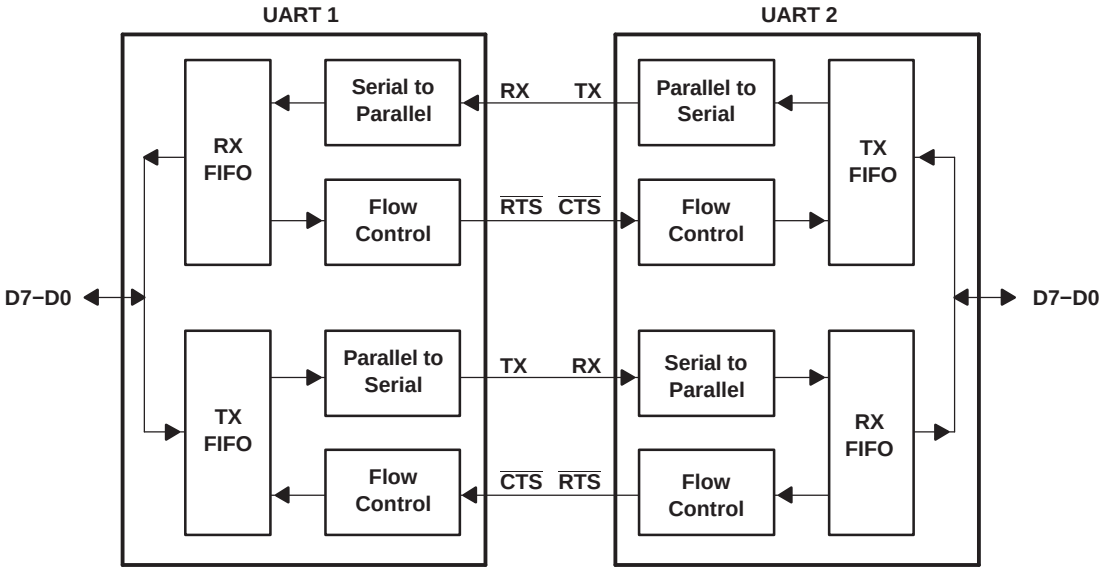

Figure 3. Autoflow Control (Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$) Example

Software Flow Control

Software flow control is enabled through the enhanced feature register and the modem control register. Different combinations of software flow control can be enabled by setting different combinations of EFR[3-0]. Table 1 shows software flow control options.

There are two other enhanced features relating to S/W flow control:

- **Xon Any Function [MCR(5)]:** Operation resumes after receiving any character after recognizing the Xoff character.

NOTE

It is possible that an Xon1 character is recognized as an Xon Any character which could cause an Xon2 character to be written to the RX FIFO.

- **Special Character [EFR(5)]:** Incoming data is compared to Xoff2. Detection of the special character sets the Xoff interrupt [IIR(4)] but does not halt transmission. The Xoff interrupt is cleared by a read of the IIR. The special character is transferred to the RX FIFO.

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Table 1. Software Flow Control Options EFR[0:3]

BIT 3	BIT 2	BIT 1	BIT 0	Tx, Rx SOFTWARE FLOW CONTROLS
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1, Xon2: Xoff1, Xoff2
X	X	0	X	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	0	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
1	1	1	1	Transmit Xon1, Xon2: Xoff1, Xoff2 Receiver compares Xon1 and Xon2: Xoff1 and Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2: Xoff1 and Xoff2

RX

When software flow control operation is enabled, the TL16C752B compares incoming data with Xoff1/2 programmed characters (in certain cases Xoff1 and Xoff2 must be received sequentially (1)). When the correct Xoff characters are received, transmission is halted after completing transmission of the current character. Xoff detection also sets IIR[4] (if enabled via IER[5]) and causes INT to go high.

To resume transmission an Xon1/2 character must be received (in certain cases Xon1 and Xon2 must be received sequentially). When the correct Xon characters are received IIR[4] is cleared and the Xoff interrupt disappears.

NOTE

If a parity, framing, or break error occurs while receiving a software flow control character, this character is treated as normal data and is written to the RCV FIFO.

TX

Xoff1/2 characters are transmitted when the RX FIFO has passed the HALT trigger level programmed in TCR[3:0].

Xon1/2 characters are transmitted when the RX FIFO reaches the RESUME trigger level programmed in TCR[7:4].

An important note here is that if, after an xoff character has been sent and software flow control is disabled, the UART transmits Xon characters automatically to enable normal transmission to proceed. A feature of the TL16C752B UART design is that if the software flow combination (EFR[3:0]) changes after an Xoff has been sent, the originally programmed Xon is automatically sent. If the RX FIFO is still above the trigger level, the newly programmed Xoff1/2 is transmitted.

The transmission of Xoff/Xon(s) follows the exact same protocol as transmission of an ordinary byte from the FIFO. This means that even if the word length is set to be 5, 6, or 7 characters then the 5, 6, or 7 least significant bits of Xoff1,2/Xon1,2 is transmitted. (Note that the transmission of 5, 6, or 7 bits of a character is seldom done, but this functionality is included to maintain compatibility with earlier designs.)

It is assumed that software flow control and hardware flow control are never enabled simultaneously. **Figure 4** shows an example of software flow control.

(1) When pairs of Xon/Xoff characters are programmed to occur sequentially, received Xon1/Xoff1 characters must be written to the Rx FIFO if the subsequent character is not Xon2/Xoff2.

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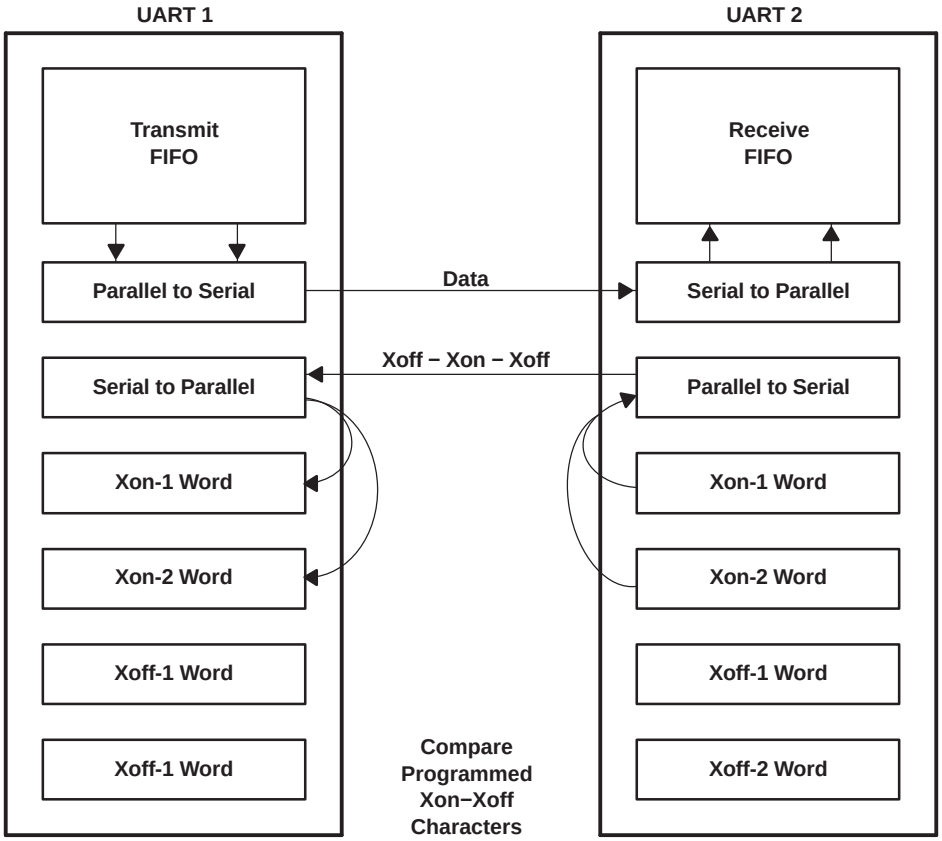

Figure 4. Software Flow Control Example

Software Flow Control Example

Assumptions: UART1 is transmitting a large text file to UART2. Both UARTs are using software flow control with single character Xoff (0F) and Xon (0D) tokens. Both have Xoff threshold (TCR [3:0]=F) set to 60 and Xon threshold (TCR[7:4]=8) set to 32. Both have the interrupt receive threshold (TLR[7:4]=D) set to 52.

UART1 begins transmission and sends 52 characters, at which point UART2 generates an interrupt to its processor to service the RCV FIFO, but assume the interrupt latency is fairly long. UART1 continues sending characters until a total of 60 characters have been sent. At this time UART2 transmits a 0F to UART1, informing UART1 to halt transmission. UART1 likely sends the 61st character, while UART2 is sending the Xoff character. UART2 is serviced and the processor reads enough data out of the RCV FIFO that the level drops to 32. UART2 now sends a 0D to UART1, informing UART1 to resume transmission.

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Reset

Table 2 summarizes the state of registers after reset.

Table 2. Register Reset Functions(1)

REGISTER	RESET CONTROL	RESET STATE
Interrupt enable register	RESET	All bits cleared
Interrupt identification register	RESET	Bits 0 is set. All other bits cleared.
FIFO control register	RESET	All bits cleared
Line control register	RESET	Reset to 00011101 (1D hex).
Modem control register	RESET	All bits cleared
Line status register	RESET	Bits 5 and 6 set. All other bits cleared
Modem status register	RESET	Bits 0–3 cleared. Bits 4–7 input signals.
Enhanced feature register	RESET	All bits cleared
Receiver holding register	RESET	Pointer logic cleared
Transmitter holding register	RESET	Pointer logic cleared
Transmission control register	RESET	All bits cleared
Trigger level register	RESET	All bits cleared

(1) Registers DLL, DLH, SPR, Xon1, Xon2, Xoff1, Xoff2 are not reset by the top-level reset signal RESET, i.e., they hold their initialization values during reset.

Table 3 summarizes the state of registers after reset.

Table 3. Signal Reset Functions

SIGNAL	RESET CONTROL	RESET STATE
TX	RESET	High
$\overline{\text{RTS}}$	RESET	High
$\overline{\text{DTR}}$	RESET	High
$\overline{\text{RXRDY}}$	RESET	High
$\overline{\text{TXRDY}}$	RESET	Low

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Interrupts

The TL16C752B has interrupt generation and prioritization (6 prioritized levels of interrupts) capability. The interrupt enable register (IER) enables each of the 6 types of interrupts and the INT signal in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0–3, 5–7. When an interrupt is generated, the IIR indicates that an interrupt is pending and provides the type of interrupt through IIR[5–0]. **Table 4** summarizes the interrupt control functions.

Table 4. Interrupt Control Functions

IIR[5–0]	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
000001	None	None	None	None
000110	1	Receiver line status	OE, FE, PE, or BI errors occur in characters in the RX FIFO	FE, PE, BI: All erroneous characters are read from the RX FIFO. OE: Read LSR
001100	2	RX timeout	Stale data in RX FIFO	Read RHR
000100	2	RHR interrupt	DRDY (data ready) (FIFO disable) RX FIFO above trigger level (FIFO enable)	Read RHR
000010	3	THR interrupt	TFE (THR empty)(FIFO disable)TX FIFO passes above trigger level (FIFO enable)	Read IIR OR a write to the THR
000000	4	Modem status	MSR[3:0] = 0	Read MSR
010000	5	Xoff interrupt	Receive Xoff character(s)/special character	Receive Xon character(s)/Read of IIR
100000	6	CTS, RTS	$\overline{RTS}$ pin or $\overline{CTS}$ pin change state from active (low) to inactive (high)	Read IIR

It is important to note that for the framing error, parity error, and break conditions, LSR[7] generates the interrupt. LSR[7] is set when there is an error anywhere in the RX FIFO and is cleared only when there are no more errors remaining in the FIFO. LSR[4–2] always represent the error status for the received character at the top of the RX FIFO. Reading the RX FIFO updates LSR[4–2] to the appropriate status for the new character at the top of the FIFO. If the RX FIFO is empty, then LSR[4–2] are all zeros.

For the Xoff interrupt, if an Xoff flow character detection caused the interrupt, the interrupt is cleared by an Xon flow character detection. If a special character detection caused the interrupt, the interrupt is cleared by a read of the LSR

Interrupt Mode Operation

In interrupt mode (if any bit of IER[3:0] is 1) the processor is informed of the status of the receiver and transmitter by an interrupt signal, INT. Therefore, it is not necessary to continuously poll the line stats register (LSR) to see if any interrupt needs to be serviced. **Figure 5** shows interrupt mode operation.

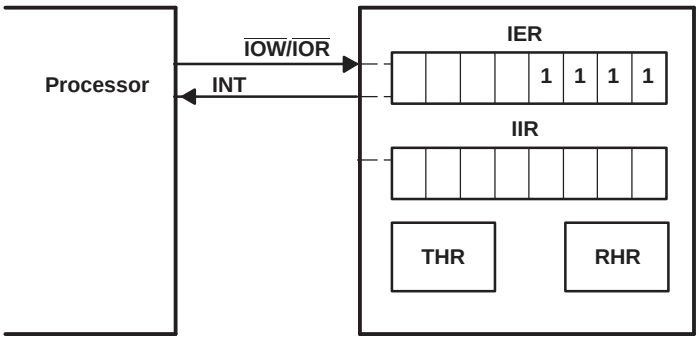

Figure 5. Interrupt Mode Operation

Polled Mode Operation

In polled mode (IER[3:0]=0000) the status of the receiver and transmitter can be checked by polling the line status register (LSR). This mode is an alternative to the FIFO interrupt mode of operation where the status of the receiver and transmitter is automatically known by means of interrupts sent to the CPU. **Figure 6** shows FIFO polled mode operation.

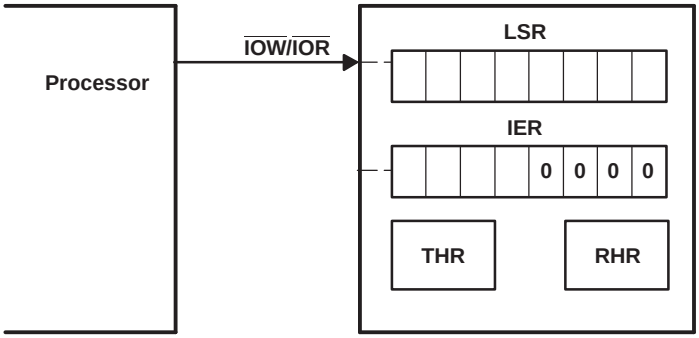

Figure 6. FIFO Polled Mode Operation

DMA Signalling

There are two modes of DMA operation: DMA mode 0 or 1, selected by FCR[3].

In DMA mode 0 or FIFO disable (FCR[0]=0) DMA occurs in single character transfers. In DMA mode 1 multi-character (or block) DMA transfers are managed to relieve the processor for longer periods of time.

Single DMA Transfers (DMA Mode0/FIFO Disable)

Transmitter: When empty, the $\overline{\text{TXRDY}}$ signal becomes active. $\overline{\text{TXRDY}}$ goes inactive after one character has been loaded into it.

Receiver: $\overline{\text{RXRDY}}$ is active when there is at least one character in the FIFO. It becomes inactive when the receiver is empty.

Figure 7 shows $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA mode0/FIFO disable.

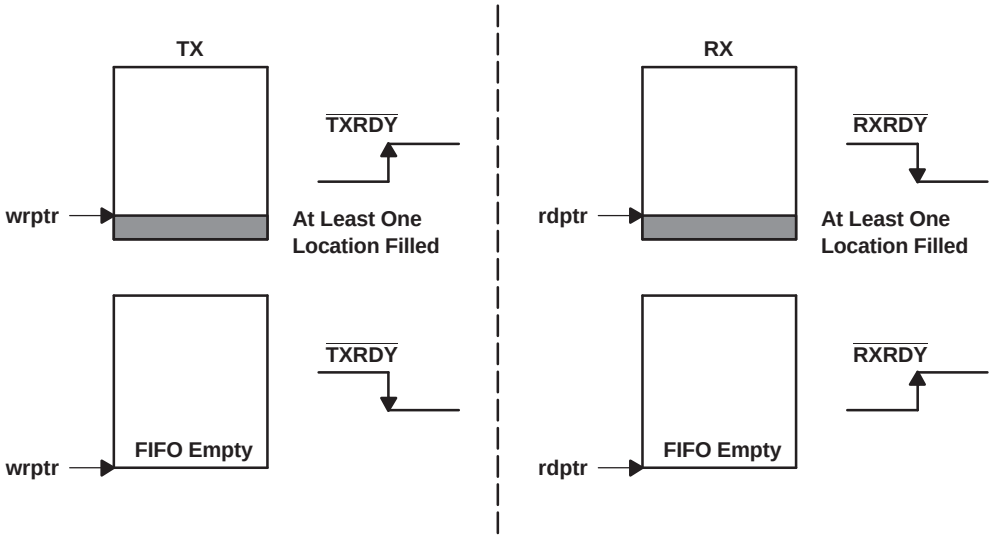

Figure 7. $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA Mode 0/FIFO Disable

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Block DMA Transfers (DMA Mode 1)

Transmitter: $\overline{\text{TXRDY}}$ is active when there is a trigger level number of spaces available. It becomes inactive when the FIFO is full.

Receiver: $\overline{\text{RXRDY}}$ becomes active when the trigger level has been reached or when a timeout interrupt occurs. It goes inactive when the FIFO is empty or an error in the RX FIFO is flagged by LSR(7)

Figure 8 shows $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA mode 1.

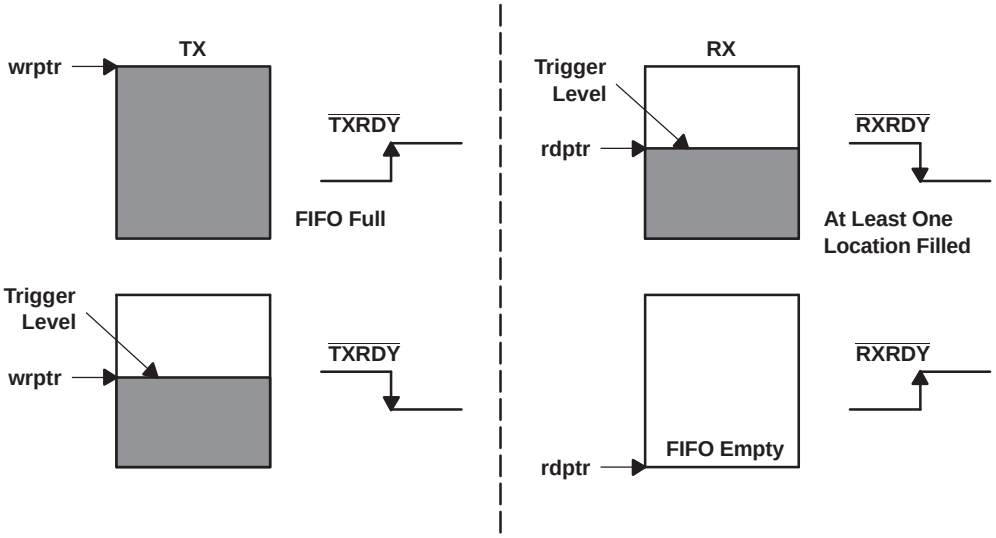

Figure 8. $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA Mode 1

Sleep Mode

Sleep mode is an enhanced feature of the TL16C752B UART. It is enabled when EFR[4], the enhanced functions bit, is set AND when IER[4] is set. Sleep mode is entered when:

- The serial data input line, RX, is idle (see break and time-out conditions).
- The TX FIFO and TX shift register are empty.
- There are no interrupts pending except THR and time-out interrupts.

NOTE

Sleep mode is not entered if there is data in the RX FIFO.

In sleep mode the UART clock and baud rate clock are stopped. Since most registers are clocked using these clocks, the power consumption is greatly reduced. The UART wakes up when any change is detected on the RX line, when there is any change in the state of the modem input pins, or if data is written to the TX FIFO.

NOTE

: Writing to the divisor latches, DLL and DLH, to set the baud clock, must not be done during sleep mode. Therefore it is advisable to disable sleep mode using IER[4] before writing to DLL or DLH.

Break and Timeout Conditions

An RX idle condition is detected when the receiver line, RX, has been high for a time equivalent to (4X programmed word length) +12 bits. The receiver line is sampled midway through each bit.

When a break condition occurs the TX line is pulled low. A break condition is activated by setting LCR[6].

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Programmable Baud Rate Generator

The TL16C752B UART contains a programmable baud generator that takes any clock input and divides it by a divisor in the range between 1 and (2^{16}–1). An additional divide-by-4 prescaler is also available and can be selected by MCR[7], as shown in **Figure 9** . The output frequency of the baud rate generator is 16× the baud rate. The formula for the divisor is:

divisor = (XTAL1 crystal input frequency/prescaler) / (desired baud rate × 16)

where:

$$\text{prescaler} = \begin{cases} 1, & \text{when MCR[7] is set to 0 after reset (divide-by-1 clock selected)} \\ 4, & \text{when MCR[7] is set to 1 after reset (divide-by-4 clock selected)} \end{cases} \quad (1)$$

NOTE

The default value of prescaler after reset is divide-by-1.

Figure 9 shows the internal prescaler and baud rate generator circuitry.

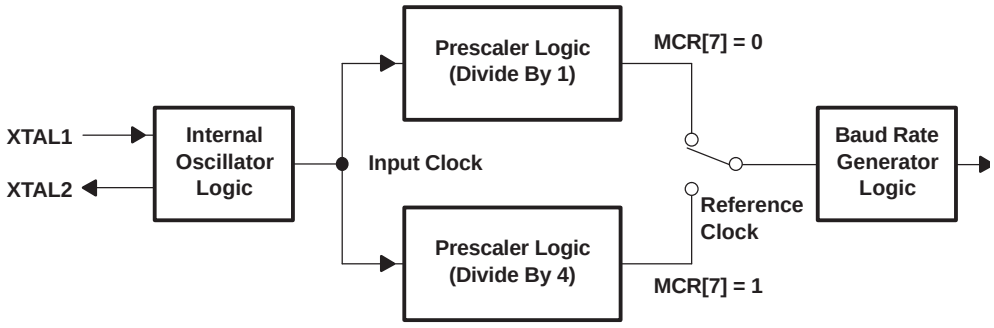

Figure 9. Prescaler and Baud Rate Generator Block Diagram

DLL and DLH must be written to in order to program the baud rate. DLL and DLH are the least significant and most significant byte of the baud rate divisor. If DLL and DLH value are both zero, the UART is effectively disabled, as no baud clock is generated.

NOTE

The programmable baud rate generator is provided to select both the transmit and receive clock rates.

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Table 5 and **Table 6** show the baud rate and divisor correlation for crystal with frequency 1.8432 MHz and 3.072 MHz respectively.

Figure 10 shows the crystal clock circuit reference.

Table 5. Baud Rates Using a 1.8432-MHz Crystal

DESIRED BAUD RATE	DIVISOR USEDTO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 6. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USEDTO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	1.23
3600	53	
4800	40	
7200	27	
9600	20	
19200	10	
38400	5	2.86

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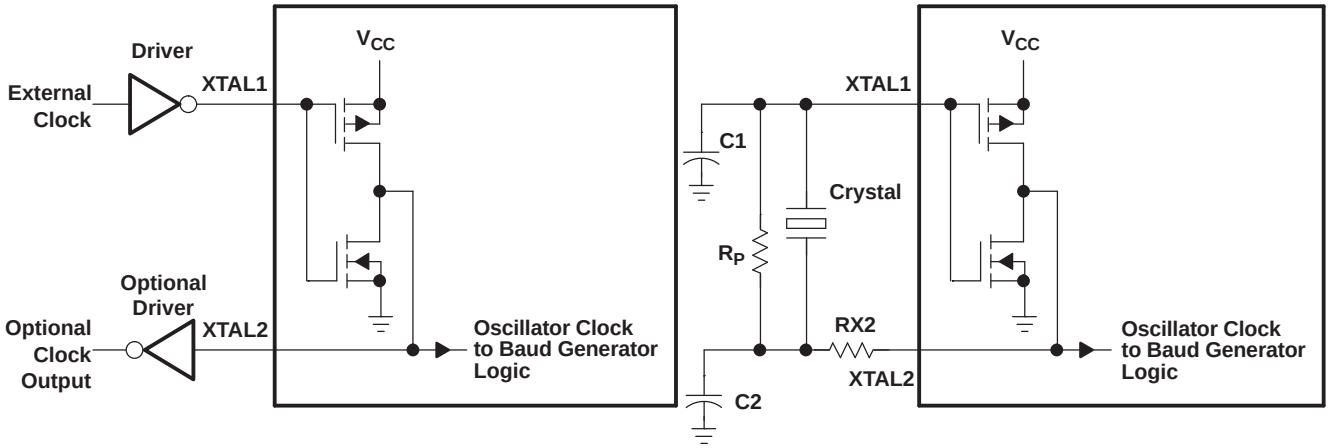

A. For crystal with fundamental frequency from 1 MHz to 24 MHz

B. For input clock frequency higher than 24 MHz, the crystal is not allowed and the oscillator must be used, since the TL16C752B internal oscillator cell can only support the crystal frequency up to 24 MHz.

TYPICAL CRYSTAL OSCILLATOR NETWORK				
CRYSTAL	**R_P**	**RX2**	**C1**	**C2**
3.072 MHz	1 MΩ	1.5 kΩ	10 pF–30 pF	40 pF–60 pF
1.8432 MHz	1 MΩ	1.5 kΩ	10 pF–30 pF	40 pF–60 pF

Figure 10. Typical Crystal Clock Circuits

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	3.6	V
V_I	Input voltage range	–0.5	V_{CC} + 0.5	V
V_O	Output voltage range	–0.5	V_{CC} + 0.5	V
T_A	Operating free-air temperature range (L device)	–55	110	°C
T_A	Operating free-air temperature range (T device)	–40	105	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

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RECOMMENDED OPERATING CONDITIONS

Low voltage (3.3 V nominal) (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	High-level input voltage(1)		0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage(1)				0.3 V_{CC}	V
V_O	Output voltage(2)		0		V_{CC}	V
V_{OH}	High-level output current	I_{OH} = –8 mA(3)	V_{CC} – 0.8			V
		I_{OH} = –4 mA(4)	V_{CC} – 0.8			
V_{OL}	Low-level output current	I_{OL} = –8 mA(3)			0.5	V
		I_{OL} = 4 mA(4)			0.5	
C_I	Input capacitance				18	pF
T_A	Operating free-air temperature range (L device)		-55	25	110	
T_A	Operating free-air temperature range (T device)		–40	25	105	°C
T_J	Virtual junction temperature range(5)			25	125	°C
	Oscillator/clock speed(6)				48	MHz
	Clock duty cycle			50%		
I_{CC}	Supply current(7)	36 MHz, 3.6 V		20		mA
		5 MHz, 3.6 V		6		
		Sleep mode, 3.6 V		1.2		

(1) Meets TTL levels, $V_{IO(min)}$ = 2 V and $V_{IH(max)}$ = 0.8 V on nonhysteresis inputs.
(2) Applies for external output buffers.
(3) These parameters apply for D7–D0.
(4) These parameters apply for $\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$, $\overline{\text{INIA}}$, $\overline{\text{INTB}}$, $\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$, $\overline{\text{RXRDYA}}$, $\overline{\text{RXRDYB}}$, $\overline{\text{TXRDYA}}$, $\overline{\text{TXRDYB}}$, TXA, TXB.
(5) These junction temperatures reflect simulated conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.
(6) The internal oscillator cell can only support up to 24 MHz clock frequency to make the crystal oscillating when crystal is used. If external oscillator or other on board clock source is used, the TL16C752B can work for input clock frequency up to 48 MHz.
(7) Measurement condition:
(a) Normal operation other than sleep mode: V_{CC} = 3.3 V, T_A = 25°C. Full duplex serial activity on all serial (UART) channels at the clock frequency specified in the recommended operating conditions with divisor of one.
(b) Sleep mode: V_{CC} = 3.3 V, T_A = 25°C. After enabling the sleep mode for all four channels, all serial and host activity is kept idle.

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TIMING REQUIREMENTS

T_A = –55°C to 110°C (L device) , –40°C to 105°C (T device) V_{CC} = 3.3 V + 10% (unless otherwise noted) (see **Figures 12** through **Figure 19**)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	IOR delay from chip select		0		ns
t_{d2}	Read cycle delay		$2t_{p(I)}$ (1)		ns
t_{d3}	Delay from IOR to data			28.5	ns
t_{d4}	Data disable time			15	ns
t_{d5}	$\overline{IOW}$ delay from chip select		10		ns
t_{d6}	Write cycle delay	100-pF load	$2t_{p(I)}$ (1)		ns
t_{d7}	Delay from IOW to output	100-pF load		50	ns
t_{d8}	Delay to set interrupt from MODEM input	100-pF load		70	ns
t_{d9}	Delay to reset interrupt from $\overline{IOR}$			70	ns
t_{d10}	Delay from stop to set interrupt	100-pF load		1_{Rclk}	
(2)t_{d11}	Delay from $\overline{IOR}$ to reset interrupt			70	ns
t_{d12}	Delay from stop to interrupt			100	ns
t_{d13}	Delay from initial INT reset to transmit start		8	24	(2)
t_{d14}	Delay from $\overline{IOW}$ to reset interrupt			70	ns
t_{d15}	Delay from stop to set $\overline{RXRDY}$			1	Clock
t_{d16}	Delay from IOR to reset $\overline{RXRDY}$			1	µm
t_{d17}	Delay from IOW to set $\overline{TXRDY}$			70	ns
t_{d18}	Delay from start to reset $\overline{TXRDY}$			16	(2)
t_{d19}	Delay between successive assertion of $\overline{IOW}$ and $\overline{IOR}$			4P(1)	(2)
t_{h1}	Chip select hold time from $\overline{IOR}$		0		ns
t_{h2}	Chip select hold time from $\overline{IOW}$		0		ns
t_{h3}	Data hold time		15		ns
th4	Address hold time		0		ns
t_{h5}	Hold time from XTAL1 clock↓ to $\overline{IOW}$ or $\overline{IOR}$ release		20		ns
t_{p1}, t_{p2}	Clock cycle period		20		ns
t_{p3}	Oscillator/clock speed	V_{CC} = 3 V		48	MHz
$t_{(RESET)}$	Reset pulse width		200		ns
t_{su1}	Address setup time		0		ns
t_{su2}	Data setup time		16		ns
t_{su3}	Setup time from $\overline{IOW}$ or $\overline{IOR}$ assertion to XTAL1 clock↑		20		ns
t_{w1}	$\overline{IOR}$ strobe width		$2t_{p(I)}$ (1)		ns
t_{w2}	$\overline{IOW}$ strobe width		$2t_{p(I)}$ (1)		ns

(1) $t_{p(I)}$ = input clock period
(2) Baud rate

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TYPICAL CHARACTERISTICS

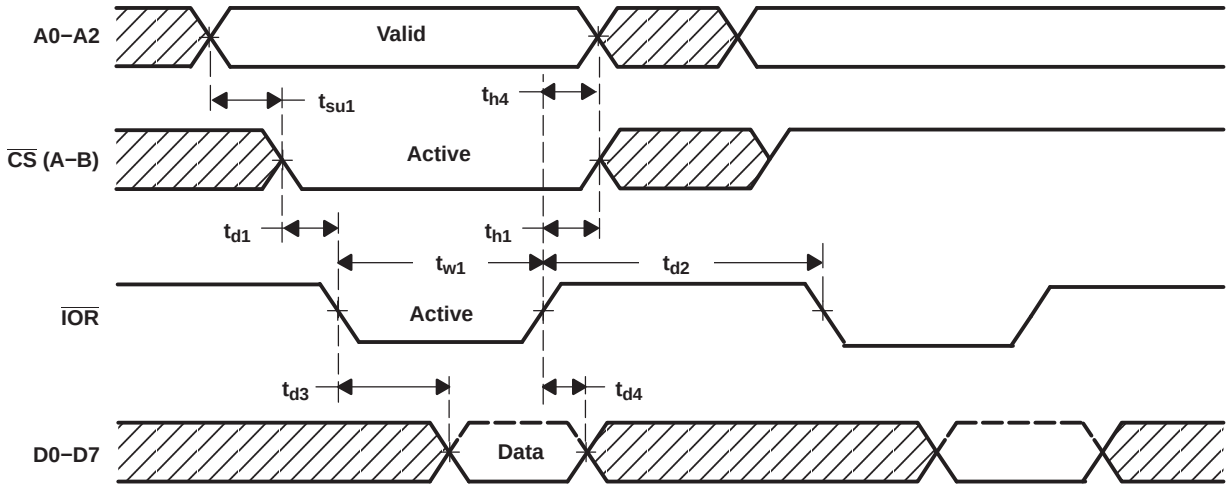

Figure 11. General Read Timing

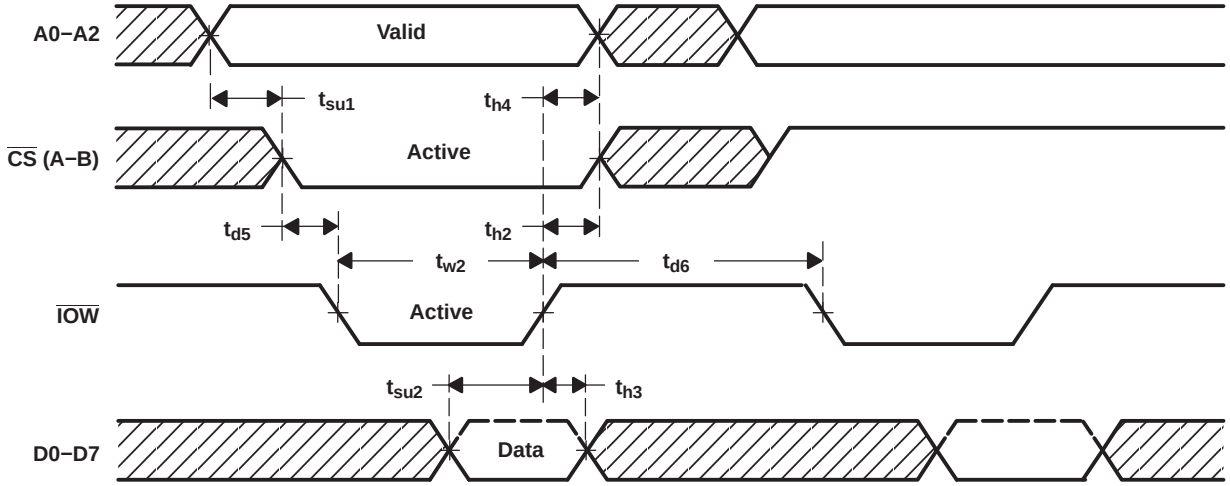

Figure 12. General Write Timing

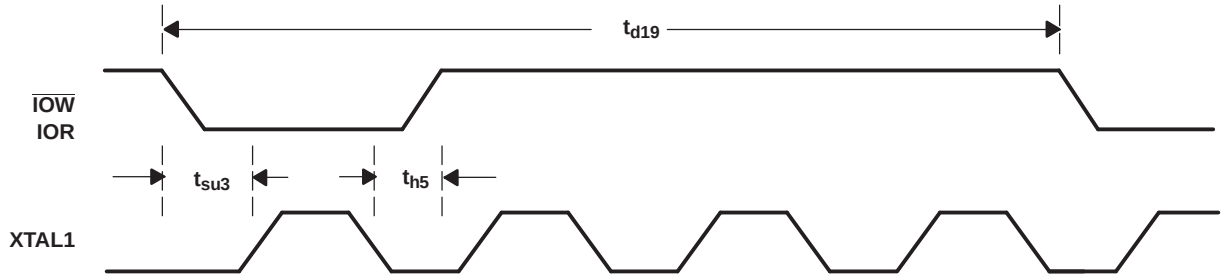

Figure 13. Alternate Read/Write Strobe Timing

TYPICAL CHARACTERISTICS (continued)

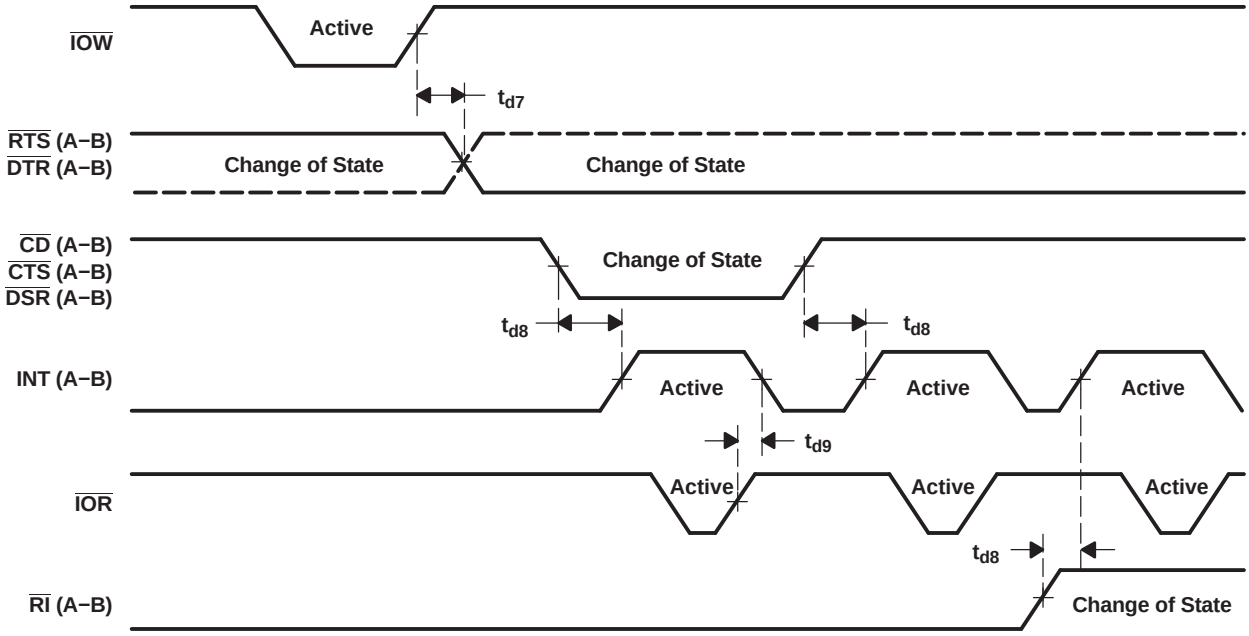

Figure 14. Modem Input/Output Timing

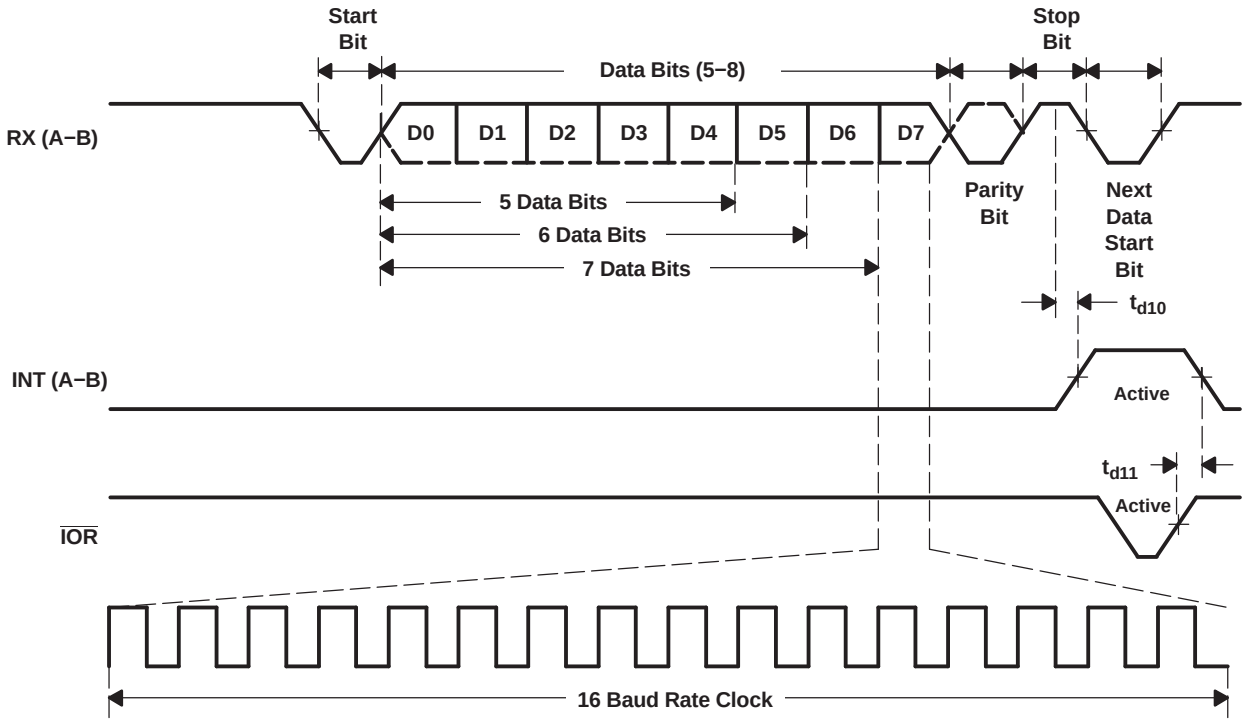

Figure 15. Receive Timing

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TYPICAL CHARACTERISTICS (continued)

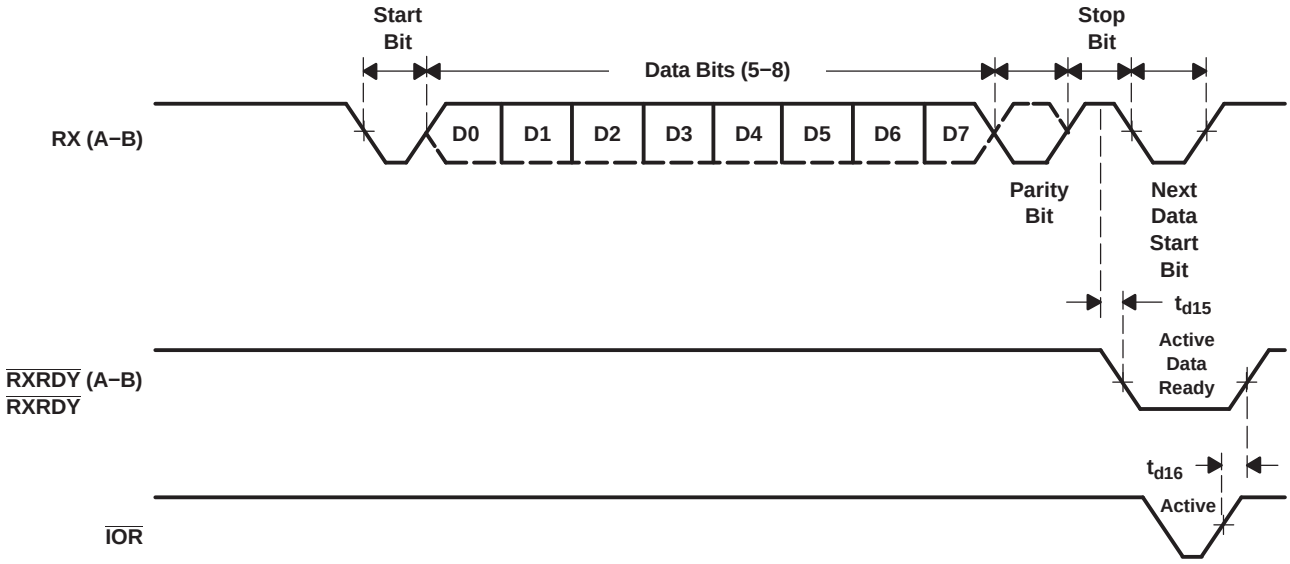

Figure 16. Receive Ready Timing in Non-FIFO Mode

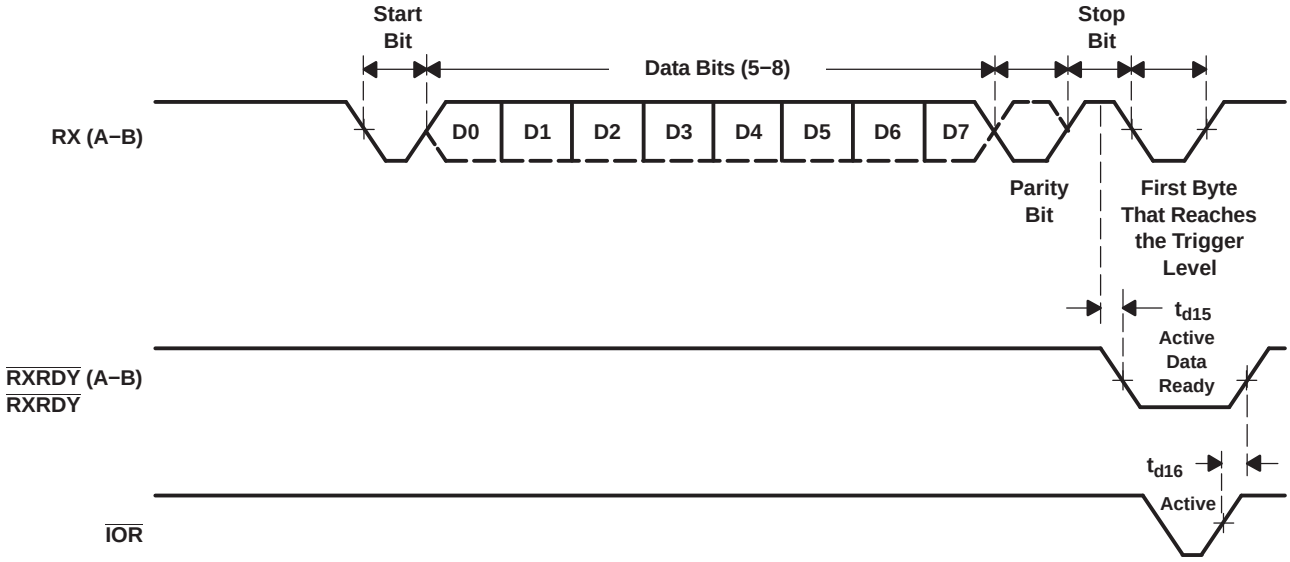

Figure 17. Receive Timing in FIFO Mode

TYPICAL CHARACTERISTICS (continued)

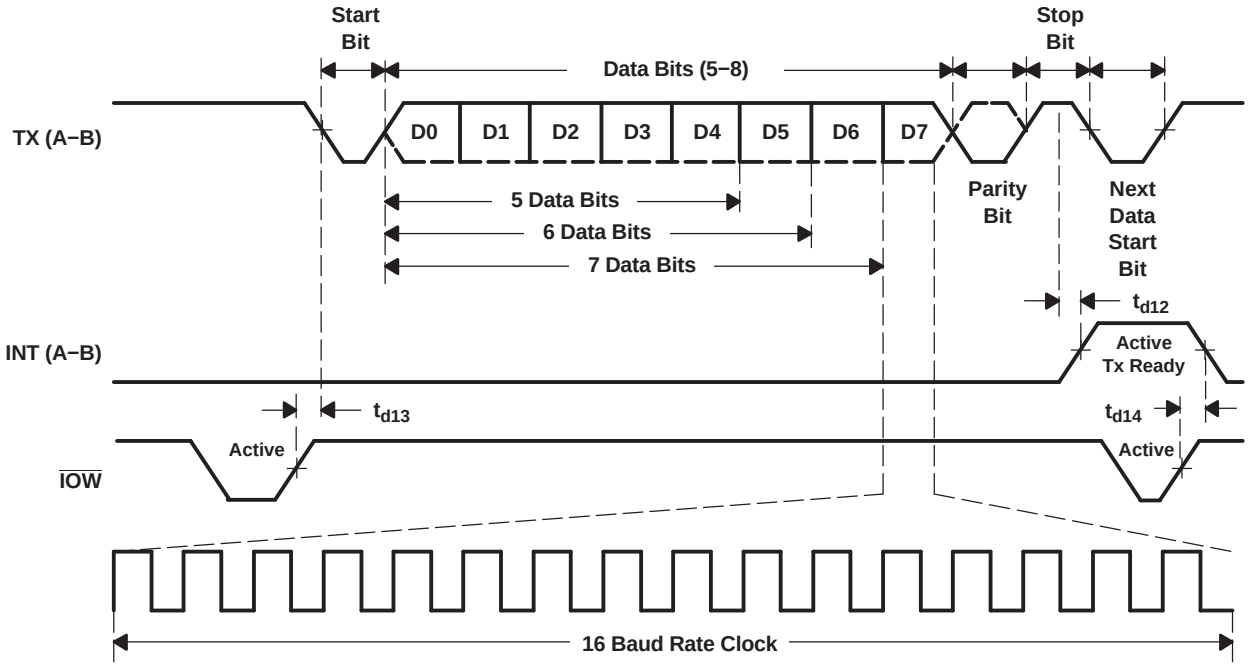

Figure 18. Transmit Timing

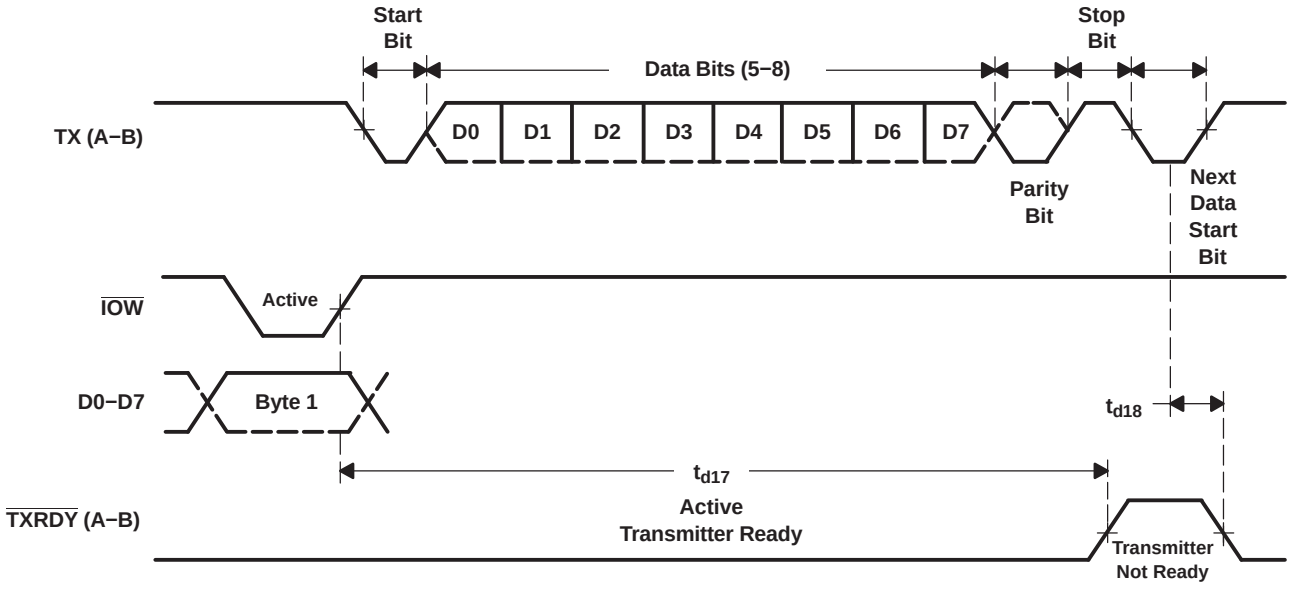

Figure 19. Transmit Ready Timing in Non-FIFO Mode

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TYPICAL CHARACTERISTICS (continued)

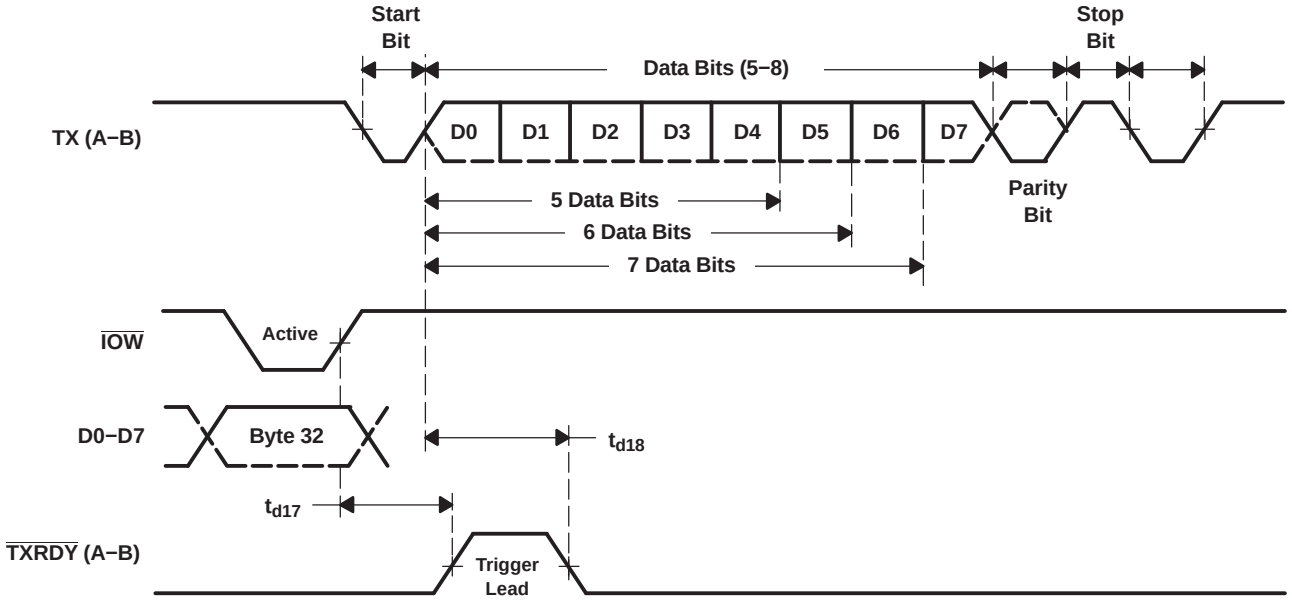

Figure 20. Transmit Ready Timing in FIFO Mode

Timing Error Condition

Texas Instruments has discovered a timing anomaly in the TL16C752B.

The problem only occurs under a special set of circumstances (non-FIFO mode) and can be worked around by using certain timing. Depending on actual system application, some customers may not see this problem. There are currently no plans to fix this problem, because it is felt that it is a minor issue. It is unlikely the device is used in non-FIFO mode, and if it is, the software workaround does not have a significant impact on throughput (< 1%).

Problem Description

When using the non-FIFO (single byte) mode of operation, it is possible that valid data could be reported as available by either the line status register (LSR) or the interrupt identification register (IIR), before the receiver holding register (RHR) can be read. In other words, the loading of valid data in RHR may be delayed when the part operates in non-FIFO mode. The data in the RHr is valid after a delay of one baud-clock period after the update of the LSR or IIR. The baud-clock runs at 16× the baud rate. The following table is a sample of baud rates and associated required delays. Depending on the operating environment, this time may well be transparent to the system, e.g., less than the context switch time of the interrupt service routine.

This problem does not exist when using FIFO mode (64 byte) mode of operation.

BAUDRATE (BIT PER SECOND)	REQUIRED DELAY (µs)
1200	52.1 ms
2400	26 ms
4800	13 ms
9600	6.5 ms
19200	3.3 ms
38400	1.6 ms
57600	1.1 ms
115200	0.5 ms
1000000	62.5 ns

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PRINCIPLES OF OPERATION

Register Map (1)

Each register is selected using address lines A[0], A[1], A[2], and in some cases, bits from other registers. The programming combinations for register selection are shown in **Table 7**. All registers shown in bold are accessed by a combination of address pins and register bits.

Table 7. Register Map – Read/Write Properties

A[2]	A[1]	A[0]	READ MODE	WRITE MODE
0	0	0	Receive holding register (RHR)	Transmit holding register (THR)
0	0	1	Interrupt enable register (IER)	Interrupt enable register
0	1	0	Interrupt identification register (IIR)	FIFO control register (FCR)
0	1	1	Line control register (LCR)	Line control register
1	0	0	Modem control register (MCR)	Modem control register
1	0	1	Line status register (LSR)	
1	1	0	Modem status register (MSR)	
1	1	1	Scratch register (SPR)	Scratch register (SPR)
0	**0**	**0**	**Divisor latch LSB (DLL)**	**Divisor latch LSB (DLL)**
0	**0**	**1**	**Divisor latch MSB (DLH)**	**Divisor latch MSB (DLH)**
0	**1**	**0**	**Enhanced feature register (EFR)**	**Enhanced feature register**
1	**0**	**0**	**Xon-1 word**	**Xon-1 word**
1	**0**	**1**	**Xon-2 word**	**Xon-2 word**
1	**1**	**0**	**Xoff-1 word**	**Xoff-1 word**
1	**1**	**1**	**Xoff-2 word**	**Xoff-2 word**
1	**1**	**0**	**Transmission control register (TCR)**	**Transmission control register**
1	**1**	**1**	**Trigger level register (TLR)**	**Trigger level register**
1	**1**	**1**	**FIFO ready register**	

(1) DLL and DLH are accessible only when LCR bit-7, is 1.
Enhanced feature register, Xon1, 2 and Xoff1, 2 are accessible only when LCR is set to 10111111 (8hBF).
Transmission control register and trigger level register are accessible only when EFR[4] = 1 and MCR[6] = 1, i.e. EFR[4] and MCR[6] are read/write enables.
FIFORdy register is accessible only when CSA and CSB = 0, MCR [2] = 1 and loopback is disabled (MCR[4]=0).
MCR[7] can only be modified when EFR[4] is set.

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Table 8 lists and describes the TL16C752B internal registers.

Table 8. TL16C752B Internal Registers(1) (2)

Addr	RGTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	READ/WRITE
000	RHR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read
000	THR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Write
001	IER	**0/$\overline{\text{CTS}}$ interrupt enable**	**0/$\overline{\text{RTS}}$ interrupt enable**	**0/Xoff sleep mode**	**0/X Sleep mode**	Modem status interrupt	Rx line status interrupt	THR empty interrupt	Rx data available interrupt	Read/Write
010	FCR	Rx trigger level	Rx trigger level	**0/TX trigger level**	**0/TX trigger level**	DMA mode select	Resets Tx FIFO	Resets Rx FIFO	Enables FIFOs	Write
010	IIR	FCR(0)	FCR(0)	0/CTS, RTS?	0/Xoff?	Interrupt priority Bit 2	Interrupt priority Bit 1	Interrupt priority Bit 0	Interrupt status	Read
011	LCR	DLAB and EFR enable	Break control Bit	Sets parity	Parity type select	Parity enable	Number of stop Bits	Word length	Word length	Read/Write
100	MCR	**1x or 1x/4 clock**	**TCR and TLR enable**	**0/Xon Any**	0/Enable loopback	IRQ enable OP	FIFO Rdy enable	RTS	DTR	Read/Write
101	LSR	0/Error in Rx FIFO	THR and TSR empty	THR empty	Break interrupt	Framing error	Parity error	Overrun error	Data in receiver	Read
110	MSR	CD	RI	DSR	CTS	ΔCD	ΔRI	ΔDSR	ΔCTS	Read
111	SPR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/Write
000	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/Write
001	DLH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Read/Write
010	EFR	Auto-$\overline{\text{CTS}}$	Auto-$\overline{\text{RTS}}$	Special character detect	**Enable enhanced functions**	S/W flow control Bit 3	S/W flow control Bit 2	S/W flow control Bit 1	S/W flow control Bit 0	Read/Write
100	Xon1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/Write
101	Xon2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/Write
110	Xoff1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/Write
111	Xoff2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/Write
110	TCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/Write
111	TLR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/Write
111	FIFO Rdy	0	0	RX FIFO B status	RX FIFO A status	0	0	TX FIFO B status	TX FIFO A status	Read

(1) The shaded bits can be modified only if register bit EFR[4] is enabled, i.e., if enhanced functions are enabled.
(2) See the notes under **Table 7** for more register access information.

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Receiver Holding Register (RHR) and The Receiver Shift Register (RSR)

The receiver section consists of the receiver holding register (RHR) and the receiver shift register (RSR). The RHR is actually a 64-byte FIFO. The RSR receives serial data from the RX terminal. The data is converted to parallel data and moved to the RHR. The receiver section is controlled by the line control register. If the FIFO is disabled, location zero of the FIFO is used to store the characters. (Note, in this case characters are overwritten if overflow occurs.) If overflow occurs, characters are lost. The RHR also stores the error status bits associated with each character.

Transmit Holding Register (THR) and TheTransmit Shift Register (TSR)

The transmitter section consists of the transmit holding register (THR) and the transmit shift register (TSR). The THR is actually a 64-byte FIFO. The THR receives data and shifts it into the TSR, where it is converted to serial data and moved out on the TX terminal. If the FIFO is disabled, the FIFO is still used to store the byte. Characters are lost if overflow occurs.

FIFO Control Register (FCR)

The FIFO control register is a write-only register, which is used for enabling the FIFOs, clearing the FIFOs, setting transmitter and receiver trigger levels, and selecting the type of DMA signalling. **Table 9** shows the FCR bit settings.

Table 9. FIFO Control Register (FCR) Bit Settings

BIT NO.	BIT SETTINGS
0	0 = Disable the transmit and receive FIFOs 1 = Enable the transmit and receive FIFOs
1	0 = No change 1 = Clears the receive FIFO and resets counter logic to zero. Returns to zero after clearing FIFO.
2	0 = No change 1 = Clears the receive FIFO and resets counter logic to zero. Returns to zero after clearing FIFO.
3	0 = DMA Mode 0 1 = DMA MOde 1
5:4	Sets the trigger level for the TX FIFO: 00–8 spaces 01–16 spaces 10–32 spaces 11–56 spaces
7:4	Sets the trigger level for the RX FIFO: 00–8 characters 01–16 characters 10–56 characters 11–60 characters

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Line Control Register (LCR)

The line control register controls the data communication format. The word length, number of stop bits, and parity type are selected by writing the appropriate bits to the LCR. **Table 10** shows the line control register bit settings.

Table 10. TL16C752B Internal Registers

BIT NO.	BIT SETTINGS
1:0	Specifies the word length to be transmitted or received. 00 – 5 bits 01 – 6 bits 10 – 7 bits 11 – 8 bits
2	Specifies the number of stop bits: 0 – 1 stop bits (word length = 5, 6, 7, 8) 1 – 1.5 stop bits (word length = 5) 1 – 2 stop bits (word length = 6, 7, 8)
3	0 = No parity 1 = A parity bit is generated during transmission and the receiver checks for received parity.
4	0 = Odd parity is generated (if LCR(3) = 1) 1 = Even parity is generated (if LCR(3) = 1)
5	Selects the forced parity format (if LCR(3) = 1) If LCR(5) = 1 and LCR(4) = 0 = the parity bit is forced to 1 in the transmitted and received data. If LCR(5) = 1 and LCR(4) = 1 = the parity bit is forced to 0 in the transmitted and received data.
6	Break control bit. 0 = Normal operating condition 1 = Forces the transmitter output to go low to alert the communication terminal.
7	0 = Normal operating condition 1 = Divisor latch enable

Line Status Register (LSR)

Table 11 shows the line status register bit settings.

Table 11. Line Status Register (LSR) Bit Settings

BIT NO.	BIT SETTINGS
0	0 = No data in the receive FIFO 1 = At least one character in the RX FIFO
1	0 = No overrun error 1 = Overrun error has occurred.
2	0 = No parity error in data being read from RX FIFO 1 = Parity error in data being read from RX FIFO
3	0 = No framing error in data being read from RX FIFO 1 = Framing error occurred in data being read from RX FIFO (i.e., received data did not have a valid stop bit)
4	0 = No break condition 1 = A break condition occurred and associated byte is 00. (i.e., RX was low for one character time frame).
5	0 = Transmit hold register is not empty 1 = Transmit hold register is empty. The processor can now load up to 64 bytes of data into the THR if the TX FIFO is enabled
6	0 = Transmitter hold and shift registers are not empty. 1 = Transmitter hold and shift registers are empty.
7	0 = Normal operation 1 = At least one parity error, framing error or break indication in the receiver FIFO. BIt 7 is cleared when no more errors are present in the FIFO.

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When the LSR is read, LSR[4:2] reflect the error bits [BI, FE, PE] of the character at the top of the RX FIFO (next character to be read). The LSR[4:2] registers do not physically exist, as the data read from the RX FIFO is output directly onto the output data-bus, DI[4:2], when the LSR is read. Therefore, errors in a character are identified by reading the LSR and then reading the RHR.

LSR[7] is set when there is an error anywhere in the RX FIFO and is cleared only when there are no more errors remaining in the FIFO.

NOTE

Reading the LSR does not cause an increment of the RX FIFO read pointer. The RX FIFO read pointer is incremented by reading the RHR.

NOTE

TI has found that the three error bits (parity, framing, break) may not be updated correctly in the first read of the LSR when the input clock (Xtal1) is running faster than 36 MHz. However, the second read should be correct. It is strongly recommended that when using this device with a clock faster than 36 MHz, that the LSR be read twice and only the second read be used for decision making. All other bits in the LSR should be correct on all reads.

Modem Control Register (MCR)

The MCR controls the interface with the modem, data set, or peripheral device that is emulating the modem. **Table 12** shows the modem control register bit settings.

Table 12. Modem Control Register (MCR) Bit Settings

BIT NO.	BIT SETTINGS
0	0 = Force $\overline{\text{DTR}}$ output to inactive (high) 1 = Force $\overline{\text{DTR}}$ output to active (low) In loopback controls MSR[5].
1	0 = Force $\overline{\text{RTS}}$ output to inactive (high) 1 = Force $\overline{\text{RTS}}$ output to active (low) In loopback controls MSR[4] If Auto-$\overline{\text{RTS}}$ is enabled the $\overline{\text{RTS}}$ output is controlled by hardware flow control
2	0 Disables the FIFO Rdy register 1 Enable the FIFO Rdy register In loopback controls MSR[6].
3	0 = Forces the INT(A - B) outputs to 3-state and $\overline{\text{OP}}$ output to high state 1 = Forces the INT(A - B) outputs to the active state and $\overline{\text{OP}}$ output to low state In loopback controls MSR[7].
4	0 = Normal operating mode 1 = Enable local loopback mode (internal) In this mode the MCR[3:0] signals are looped back into MSR[3:0] and the TX output is looped back to the RX input internally.
5	0 = Disable Xon any function 1 = Enable Xon any function
6	0 = No action 1 = Enable access to the TCR and TLR registers
7	0 = Divide by one clock input 1 = Divide by four clock input

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Modem Status Register (MSR)

The modem status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the processor. It also indicates when a control input from the modem changes state. **Table 13** shows the modem status register bit settings per channel.

Table 13. Modem Status Register (MSR) Bit Settings

BIT NO.	BIT SETTINGS
0	Indicates that the $\overline{CTS}$ input (or MCR[1] in loopback) has changed state. Cleared on a read.
1	Indicates that the $\overline{DSR}$ input (or MCR[0] in loopback) has changed state. Cleared on a read.
2	Indicates that the $\overline{RI}$ input (or MCR[2] in loopback) has changed state from low to high. Cleared on a read.
3	Indicates that the $\overline{CD}$ input (or MCR[3] in loopback) has changed state. Cleared on a read.
4	This bit is the complement of the $\overline{CTS}$ input during normal mode. During internal loopback mode, it is equivalent to MCR[1].
5	This bit is the complement of the $\overline{DSR}$ input during normal mode. During internal loopback mode, it is equivalent to MCR[0].
6	This bit is the complement of the $\overline{RI}$ input during normal mode. During internal loopback mode, it is equivalent to MCR[2].
7	This bit is the complement of the $\overline{CD}$ input during normal mode. During internal loopback mode, it is equivalent to MCR[3].

Interrupt Enable Register (IER)

The interrupt enable register (IER) enables each of the six types of interrupt, receiver error, RHR interrupt, THR interrupt, Xoff received, or $\overline{CTS}$/$\overline{RTS}$ change of state from low-to-high. The INT output signal is activated in response to interrupt generation. **Table 14** shows the IER bit settings.

Table 14. Interrupt Enable Register (IER) Bit Settings

BIT NO.	BIT SETTINGS
0	0 = Disable the RHR interrupt 1 = Enable the RHR interrupt
1	0 = Disable the THR interrupt 1 = Enable the THR interrupt
2	0 = Disable the receiver line status interrupt 1 = Enable the receiver line status interrupt
3	0 = Disable the modem status register interrupt 1 = Enable the modem status register interrupt
4	0 = Disable sleep mode 1 = Enable sleep mode
5	0 = Disable the Xoff interrupt 1 = Enable the Xoff interrupt
6	0 = Disable the $\overline{RTS}$ interrupt 1 = Enable the $\overline{RTS}$ interrupt
7	0 = Disable the $\overline{CTS}$ interrupt 1 = Enable the $\overline{CTS}$ interrupt

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Interrupt IdentificationRegister (IIR)

The interrupt identification register is a read-only 8-bit register, which provides the source of the interrupt in a prioritized manner. **Table 15** shows the IIR bit settings.

Table 15. Interrupt Identification Register (IIR) Bit Settings

BIT NO.	BIT SETTINGS
0	0 = A interrupt is pending 1 = No interrupt is pending
3:1	3-Bit encoded interrupt. See **Table 14**.
4	1 = Xoff/Special character has been detected.
5	$\overline{CTS}$/$\overline{RTS}$ low-to-high change of state.
7:6	Mirror the contents of FCR[0]

The interrupt priority list is shown in **Table 16.**

Table 16. Interrupt Priority List

PRIORITY LEVEL	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	BIT SETTINGS
1	0	0	0	1	1	0	Receiver line status error
2	0	0	1	1	0	0	Receiver timeout interrupt
2	0	0	0	1	0	0	RHR interrupt
3	0	0	0	0	1	0	THR interrupt
4	0	0	0	0	0	0	Modem interrupt
5	0	1	0	0	0	0	Received Xoff signal/special character
7	1	0	0	0	0	0	$\overline{CTS}$, $\overline{RTS}$ change of state from active (low) to inactive (high).

Enhanced Feature Register (EFR)

The enhanced feature register is an 8-bit register that enables or disables the enhanced features of the UART. **Table 17** shows the enhanced feature register bit settings.

Table 17. Enhanced Feature Register (EFR) Bit Settings

BIT NO.	BIT SETTINGS
3:0	Combinations of software flow control can be selected by programming bit 3-bit 0. See Table 1.
4	Enhanced functions enable bit 0 = Disables enhanced functions and writing to IER bits 4-7, FCR bits 4–5, MCR bits 5–7. 1 = Enables the enhanced function IER bits 4–7, FCR bit 4–5, and MCR bits 5–7 can be modified, i.e., this bit is therefore a write enable.
5	0 = Normal operation, 1 = Special character detect. Received data is compared with Xoff-2 data. If a match occurs the received data is transferred to FIFO and IIR bit 4 is set to 1 to indicate a special character has been detected.
6	$\overline{RTS}$ flow control enable bit 0 = Normal operation 1 = RTS flow control is enabled i.e., the $\overline{RTS}$ pin goes high when the receiver FIFO HALT trigger level TCR[3:0] is reached and goes low when the receiver FIFO RESTORE transmission trigger level TCR[7:4] is reached.
7	$\overline{CTS}$ flow control enable bit 0 = Normal operation 1 = $\overline{CTS}$ flow control is enabled i.e., transmission is halted when a high signal is detected on the $\overline{CTS}$ pin.

Divisor Latches (DLL, DLH)

The divisor lathes are two 8-bit registers which store the 16-bit divisor for generation of the baud clock in the baud rate generator. DLH stores the most significant part of the divisor. DLL stores the least significant part of the division.

Note that DLL and DLH can only be written to before sleep mode is enabled (i.e., before IER[4] is set).

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Transmission Control Register (TCR)

The transmission control register is an 8-bit register that is used to store the receive FIFO threshold levels to start/stop transmission during hardware/software flow control. **Table 18** shows the transmission control register bit settings.

Table 18. Transmission Control Register (TCR) Bit Settings

BIT NO.	BIT SETTINGS
3:0	RCV FIFO trigger level to halt transmission (0–60)
7:4	RCV FIFO trigger level to resume transmission (0–60)

TCR trigger levels are available from 0–60 bytes with a granularity of four.

NOTE

TCR can only be written to when EFR[4] = 1 and MCR[6] = 1. The programmer must program the TCR such that TCR[3:0] > TCR[7:4]. There is no built-in hardware check to make sure this condition is met. Also, the TCR must be programmed with this condition before Auto-$\overline{RTS}$ or software flow control is enabled to avoid spurious operation of the device.

Trigger Level Register (TLR)

The trigger level register is an 8-bit register that is pulsed to store the transmit and received FIFO trigger levels used for DMA and interrupt generation. Trigger levels from 4–60 can be programmed with a granularity of 4. **Table 19** shows the trigger level register bit settings.

Table 19. Trigger Level Register (TLR) Bit Settings

BIT NO.	BIT SETTINGS
3:0	Transmit FIFO trigger levels (4–60), number of spaces available
7:4	RCV FIFO trigger levels (4–60), number of characters available

NOTE

TLR can only be written to when EFR[4] = 1 and MCR[6] = 1. If TLR[3:0] or TLR[7:4] are 0, the selectable trigger levels via the FIFO control register (FCR) are used for the transmit and receive FIFO trigger levels. Trigger levels from 4–60 bytes are available with a granularity of four. The TLR should be programmed for N/4, where N is the desired trigger level.

When the trigger level setting in TLR is zero, the TL16C752B uses the trigger level setting defined in FCR. If TLR has a nonzero trigger level value, the trigger level defined in FCR is discarded. This applies to both the transmit FIFO and receive FIFO trigger level setting.

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FIFO Ready Register

The FIFO ready register provides real-time status of the transmit and receive FIFOs of both channels. **Table 20** shows the FIFO ready register bit settings. The trigger level mentioned below refers to the setting in either FCR (when TLR value is zero), or TLR (when it has a nonzero value).

Table 20. FIFO Ready Register

BIT NO.	BIT SETTINGS
0	0 = There are less than a TX trigger level number of spaces available in the TX FIFO of channel A. 1 = There are at least a TX trigger level number of spaces available in the TX FIFO of channel A.
1	0 = There are less than a TX trigger level number of spaces available in the TX FIFO of channel B. 1 = There are at least a TX trigger level number of spaces available in the TX FIFO of channel B.
3:2	Unused, always 0
4	0 = There are less than a RX trigger level number of characters in the RX FIFO of channel A. 1 = The RX FIFO of channel A has more than a RX trigger level number of characters available for reading or a timeout condition has occurred.
5	0 = There are less than a RX trigger level number of characters in the RX FIFO of channel B. 1 = The RX FIFO of channel B has more than a RX trigger level number of characters available for reading or a timeout condition has occurred.
7:6	Unused, always 0

The FIFORdy register is a read-only register that can be accessed when any of the two UARTs are selected $\overline{\text{CSA-B}}$ = 0, MCR[2] (FIFO Rdy Enable) is a logic 1 and loopback is disabled. The address is 111.

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TL16C752B Programmer's Guide

The base set of registers that is used during high speed data transfer have a straightforward access method. The extended function registers require special access bits to be decoded along with the address lines. The following guide helps with programming these registers. Note that the descriptions below are for individual register access. Some streamlining through interleaving can be obtained when programming all the registers.

Set baud rate to VALUE1, VALUE2	Read LCR (03), save in temp Set LCR (03) to 80 Set DLL (00) to VALUE1 Set DLM (01) to VALUE2 Set LCR (03) to temp
Set Xoff1, Xon1 to VALUE1, VALUE2	Read LCR (03), save in temp Set LCR (03) to BF Set Xoff1 (06) to VALUE1 Set Xon1 (04) to VALUE2 Set LCR (03) to temp
Set Xoff2, Xon2 to VALUE1, VALUE2	Read LCR (03), save in temp Set LCR (03) to BF Set Xoff2 (07) to VALUE1 Set Xon2 (05) to VALUE2 Set LCR (03) to temp
Set software flow control mode to VALUE	Read LCR (03), save in temp Set LCR (03) to BF Set EFR (02) to VALUE Set LCR (03) to temp
Set flow control threshold to VALUE	Read LCR (03), save in temp1 Set LCR (03) to BF Read EFR (02), save in temp2 Set EFR (02) to 10 + temp2 Set LCR (03) to 00 Read MCR (04), save in temp3 Set MCR (04) to 40 + temp3 Set TCR (06) to VALUE Set MCR (04) to temp3 Set LCR (03) to BF Set EFR (02) to temp2 Set LCR (03) to temp1
Set xmt and rcv FIFO thresholds to VALUE	Read LCR (03), save in temp1 Set LCR (03) to BF Read EFR (02), save in temp2 Set EFR (02) to 10 + temp2 Set LCR (03) to 00 Read MCR (04), save in temp3 Set MCR (04) to 40 + temp3 Set TLR (07) to VALUE Set MCR (04) to temp3 Set LCR (03) to BF Set EFR (02) to temp2 Set LCR (03) to temp1
Read FIFORdy register	Read MCR (04), save in temp1 Set temp2 = temp1 y EF; (x sign here means bit-AND) Set MCR (04) = 04 + temp2 Read FRR (07), save in temp2 Pass temp2 back to host Set MCR (04) to temp1
Set prescaler value to divide-by-one	Read LCR (03), save in temp1 Set LCR (03) to BF Read EFR (02), save in temp2 Set EFR (02) to 10 + temp2 Set LCR (03) to 00 Read MCR (04), save in temp3 Set MCR (04) to temp3 y 7F; (y sign here means bit-AND) Set LCR (03) to BF Set EFR (02) to temp2 Set LCR (03) to temp1

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Set prescaler value to divide-by-four	Read LCR (03), save in temp1 Set LCR (03) to BF Read EFR (02), save in temp2 Set EFR (02) to 10 + temp2 Set LCR (03) to 00 Read MCR (04), save in temp3 Set MCR (04) to temp3 + 80 Set LCR (03) to BF Set EFR (02) to temp2 Set LCR (03) to temp1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL16C752BLPTREP	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 110	16C752BLE	Samples
TL16C752BTPTREP	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	16C752BEP	Samples
V62/03626-01XE	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 110	16C752BEP	Samples
V62/03626-02XE	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 110	16C752BLE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TL16C752B-EP :

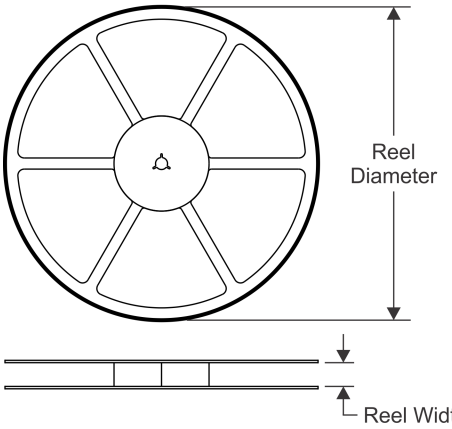
- Catalog: TL16C752B

NOTE: Qualified Version Definitions:

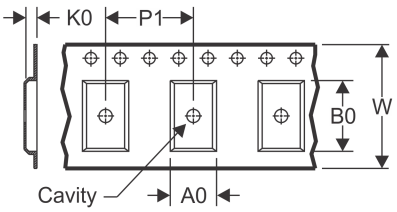
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

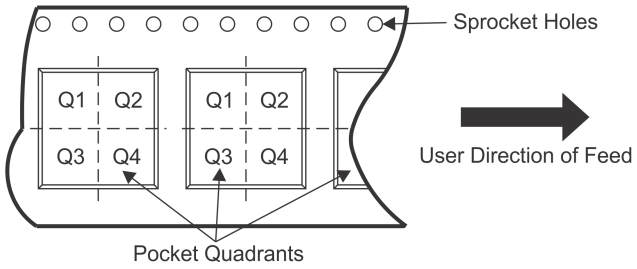


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

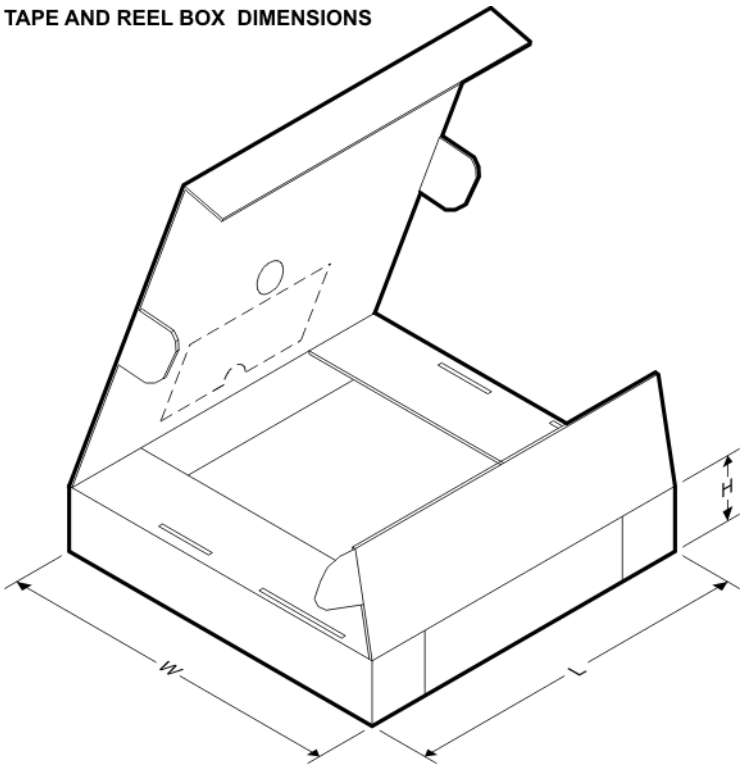
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL16C752BLPTREP	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q1
TL16C752BTPTREP	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

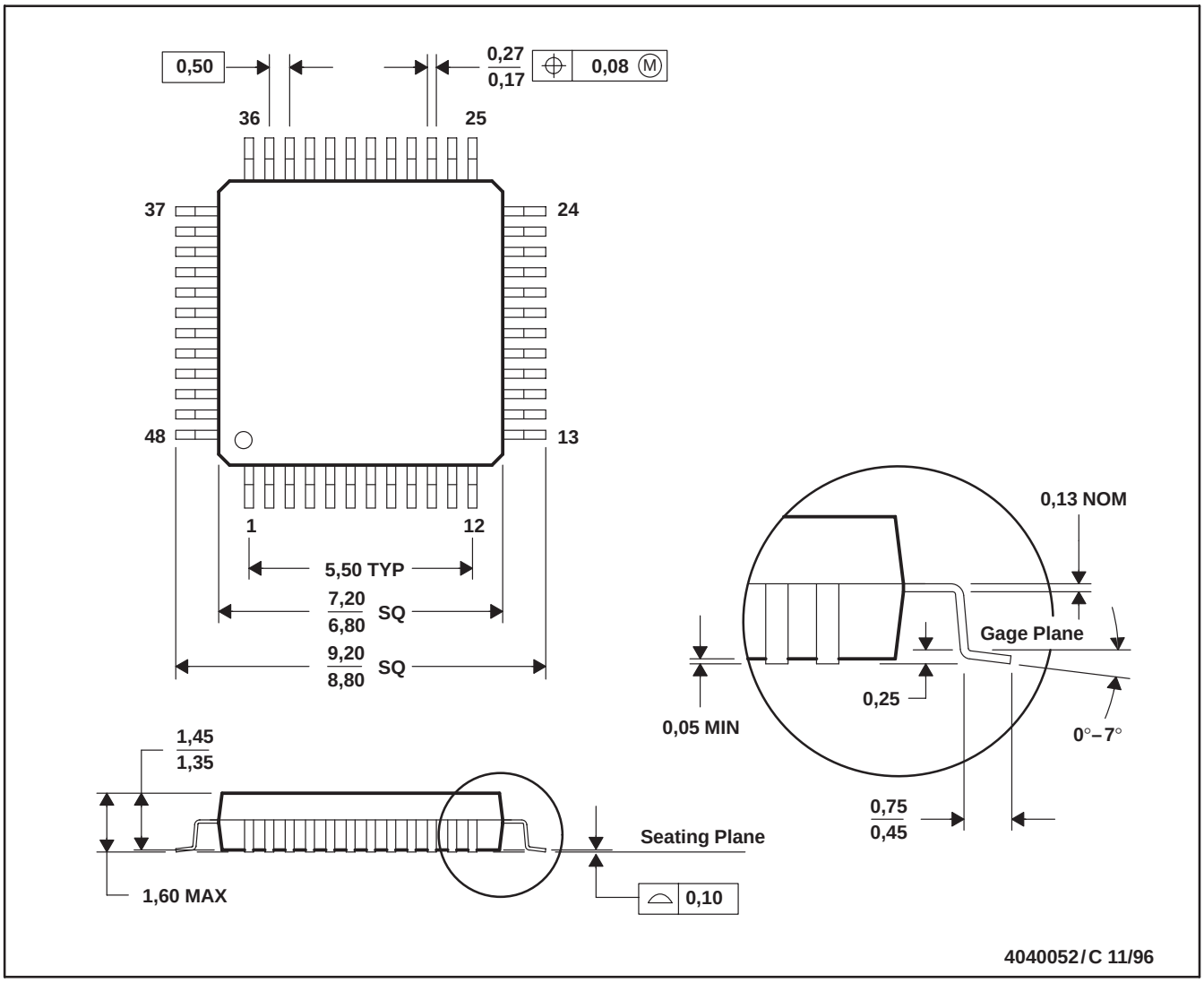


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL16C752BLPTREP	LQFP	PT	48	1000	350.0	350.0	43.0
TL16C752BTPTREP	LQFP	PT	48	1000	350.0	350.0	43.0

MTQF003A – OCTOBER 1994 – REVISED DECEMBER 1996

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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