THE DATASHEET OF

BQ24750RHDR

Host-Controlled Multi-Chemistry Battery Charger With Integrated System Power Selector and AC Overpower Protection

FEATURES

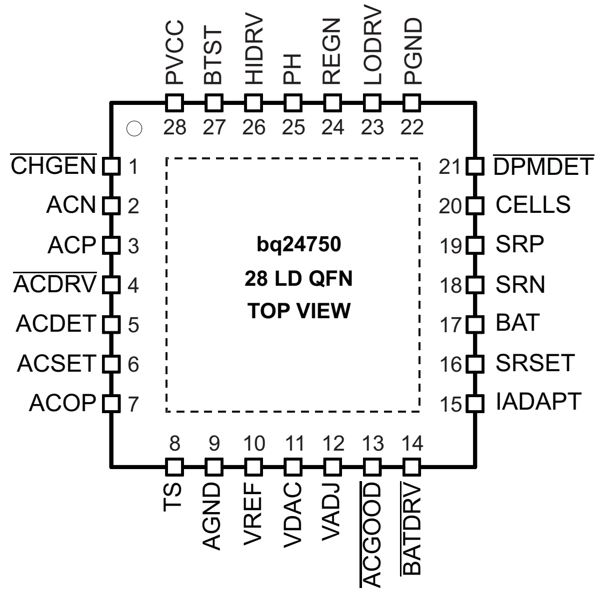
- NMOS-NMOS Synchronous Buck Converter with 300 kHz Frequency and >95% Efficiency
- 30-ns Minimum Driver Dead-time and 99.5% Maximum Effective Duty Cycle
- High-Accuracy Voltage and Current Regulation
  - ±0.5% Charge Voltage Accuracy
  - ±3% Charge Current Accuracy
  - ±3% Adapter Current Accuracy
  - ±2% Input Current Sense Amp Accuracy
- Integration
  - Automatic System Power Selection From AC/DC Adapter or Battery
  - Internal Loop Compensation
  - Internal Soft Start
- Safety
  - Input Overvoltage Protection (OVP)
  - Dynamic Power Management (DPM) with Status Indicator
  - Programmable Inrush Adapter Power (ACOP) and Overcurrent (ACOC) Limits
  - Reverse-Conduction Protection Input FET
  - Battery Thermistor Sense Input (TS) for Charge Qualification
- Supports Two, Three, or Four Li+ Cells
- 5–24 V AC/DC-Adapter Operating Range
- Analog Inputs with Ratiometric Programming via Resistors or DAC/GPIO Host Control
  - Charge Voltage (4–4.512 V/cell)
  - Charge Current (up to 10 A, with 10-mΩ Sense Resistor)
  - Adapter Current Limit (DPM)
- Status and Monitoring Outputs
  - AC/DC Adapter Present with Programmable Voltage Threshold
  - DPM Loop Active
  - Current Drawn from Input Source
- Supports Any Battery Chemistry: Li+, NiCd, NiMH, Lead Acid, etc.
- Charge Enable
- 10-µA Off-State Current
- 28-pin, 5x5-mm QFN package

APPLICATIONS

- Notebook and Ultra-Mobile Computers
- Portable Data-Capture Terminals
- Portable Printers
- Medical Diagnostics Equipment
- Battery Bay Chargers
- Battery Back-up Systems

DESCRIPTION

The bq24750 is a high-efficiency, synchronous battery charger with integrated compensation and system power selector logic, offering low component count for space-constrained multi-chemistry battery charging applications. Ratiometric charge current and voltage programming allows high regulation accuracies, and can be either hardwired with resistors or programmed by the system power-management microcontroller using a DAC or GPIOs.

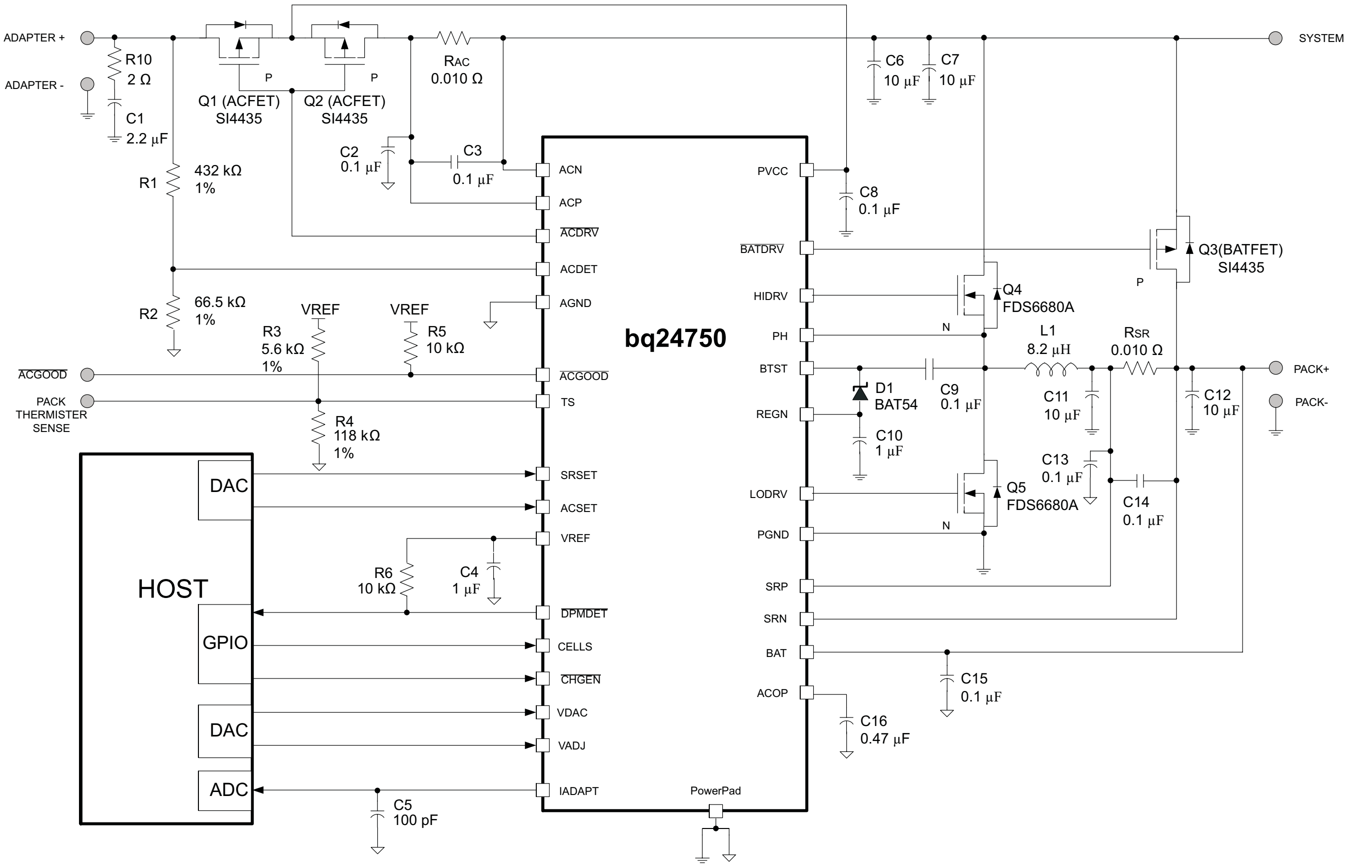


DESCRIPTION (CONTINUED)

The bq24750 charges two, three, or four series Li+ cells, supporting up to 10 A of charge current, and is available in a 28-pin, 5x5-mm QFN package.

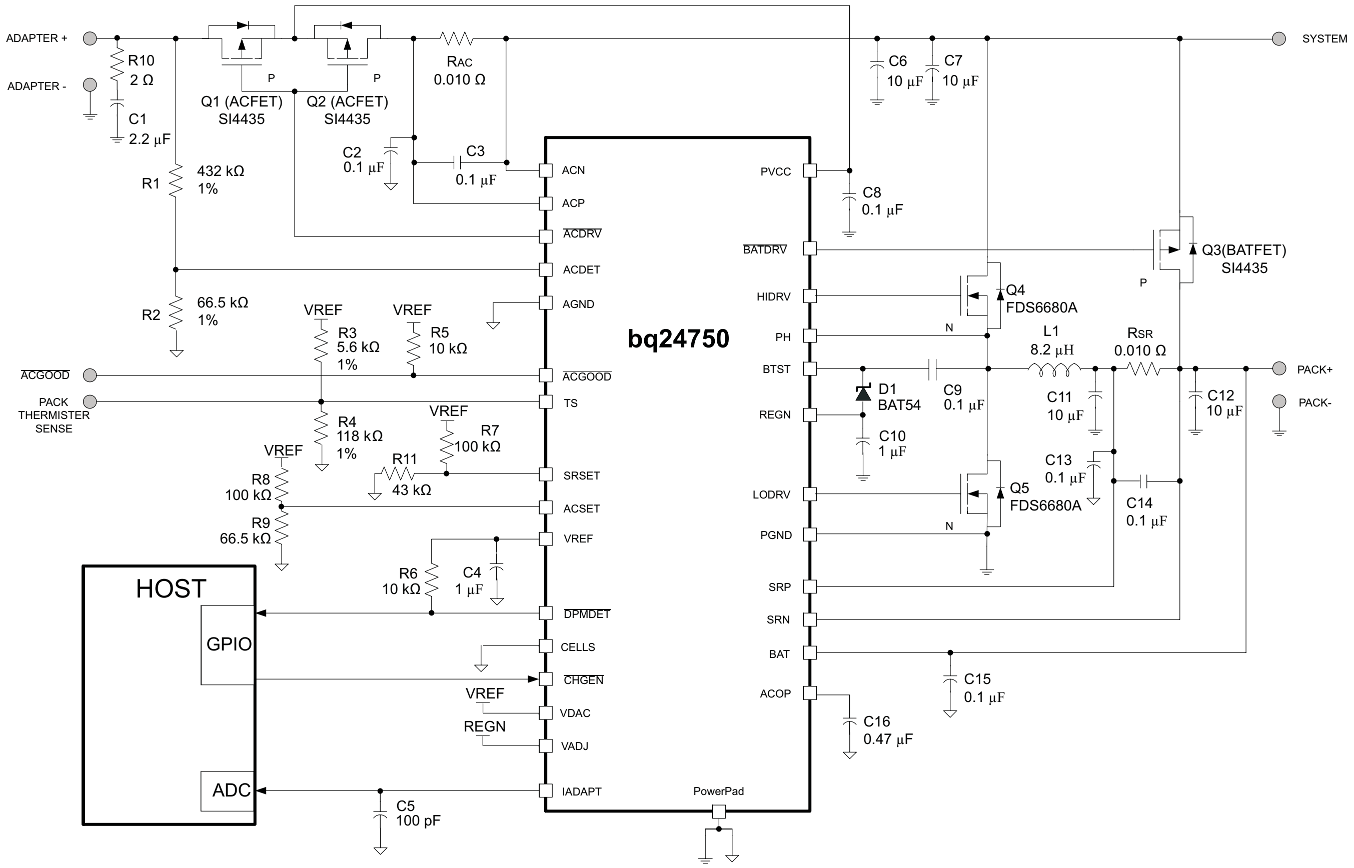
The bq24750 controls external switches to prevent battery discharge back to the input, connect the adapter to the system, and to connect the battery to the system using 6-V gate drives for better system efficiency. For maximum system safety, inrush-power limiting provides instantaneous response to high input voltage multiplied by current. This AC Over-Power protection (ACOP) feature limits the input-switch power to the programmed level on the ACOP pin, and latches off if the high-power condition persists to prevent overheating.

The bq24750 features Dynamic Power Management (DPM) and input power limiting. These features reduce battery charge current when the input power limit is reached to avoid overloading the AC adapter when supplying the load and the battery charger simultaneously. A highly-accurate current-sense amplifier enables precise measurement of input current from the AC adapter to monitor the overall system power.



A. V_{IN}= 20 V, V_{BAT} = 3-cell Li-Ion, I_{CHARGE} = 3 A, $I_{ADAPTER\_LIMIT}$ = 4 A, T_{BAT} = 0-45°C

Figure 1. Typical System Schematic, Voltage and Current Programmed by DAC



A. V_{IN}= 20 V, V_{BAT} = 3-cell Li-Ion, I_{CHARGE} = 3 A, $I_{ADAPTER\_LIMIT}$ = 4 A, T_{BAT} = 0-45°C

Figure 2. Typical System Schematic, Voltage and Current Programmed by Resistor

ORDERING INFORMATION

PART NUMBER	PACKAGE	ORDERING NUMBER (Tape and Reel)	QUANTITY
bq24750	28-PIN 5 x 5 mm QFN	bq24750RHDT	250
		bq24750RHDR	3000

THERMAL CHARACTERISTICS

PACKAGE	θ_{JA}	T_A = 70 °C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
QFN – RHD (1) (2)	39°C/W	2.36 W	0.028 W/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com

(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2x3 via matrix.

Table 1. TERMINAL FUNCTIONS – 28-PIN QFN

TERMINAL		DESCRIPTION
NAME	**NO.**	
$\overline{\text{CHGEN}}$	1	Charge enable active-low logic input. LO enables charge. HI disables charge.
ACN	2	Adapter current sense resistor, negative input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from ACN pin to AGND for common-mode filtering.
ACP	3	Adapter current sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from ACP pin to AGND for common-mode filtering.
$\overline{\text{ACDRV}}$	4	AC adapter to system-switch driver output. Connect directly to the gate of the ACFET P-channel power MOSFET and the reverse conduction blocking P-channel power MOSFET. Connect both FETs as common-source. Connect the ACFET drain to the system-load side. The PVCC should be connected to the common-source node to ensure that the driver logic is always active when needed. If needed, an optional capacitor from gate to source of the ACFET is used to slow down the ON and OFF times. The internal gate drive is asymmetrical, allowing a quick turn-off and slower turn-on in addition to the internal break-before-make logic with respect to the $\overline{\text{BATDRV}}$. The output goes into linear regulation mode when the input sensed current exceeds the ACOC threshold. $\overline{\text{ACDRV}}$ is latched off after ACOP voltage exceeds 2 V, to protect the charging system from an ACFET-overpower condition.
ACDET	5	Adapter detected voltage set input. Program the adapter detect threshold by connecting a resistor divider from adapter input to ACDET pin to AGND pin. Adapter voltage is detected if ACDET-pin voltage is greater than 2.4 V. The I_{ADAPT} current sense amplifier is active when the ACDET pin voltage is greater than 0.6 V. Input overvoltage, ACOV, disables charge and $\overline{\text{ACDRV}}$ when ACDET > 3.1 V. ACOV does not latch
ACSET	6	Adapter current set input. The voltage ratio of ACSET voltage versus VDAC voltage programs the input current regulation set-point during Dynamic Power Management (DPM). Program by connecting a resistor divider from VDAC to ACSET to AGND; or by connecting the output of an external DAC to the ACSET pin and connect the DAC supply to the VDAC pin.
ACOP	7	Input power limit set input. Program the input over-power time constant by placing a ceramic capacitor from ACOP to AGND. The capacitor sets the time that the input current limit, ACOC, can be sustained before exceeding the power-MOSFET power limit. When the ACOP voltage exceeds 2 V, then the $\overline{\text{ACDRV}}$ latches off to protect the charge system from an over-power condition, ACOP. Reset latch by toggling ACDET or PVCC_UVLO.
TS	8	Temperature qualification voltage input for battery pack negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to AGND.
AGND	9	Analog ground. Ground connection for low-current sensitive analog and digital signals. On PCB layout, connect to the analog ground plane, and only connect to PGND through the PowerPad underneath the IC.
VREF	10	3.3-V regulated voltage output. Place a 1-µF ceramic capacitor from VREF to AGND pin close to the IC. This voltage could be used for ratiometric programming of voltage and current regulation.
VDAC	11	Charge voltage set reference input. Connect the VREF or external DAC voltage source to the VDAC pin. Battery voltage, charge current, and input current are programmed as a ratio of the VDAC pin voltage versus the VADJ, SRSET, and ACSET pin voltages, respectively. Place resistor dividers from VDAC to VADJ, SRSET, and ACSET pins to AGND for programming. A DAC could be used by connecting the DAC supply to VDAC and connecting the output to VADJ, SRSET, or ACSET.
VADJ	12	Charge voltage set input. The voltage ratio of VADJ voltage versus VDAC voltage programs the battery voltage regulation set-point. Program by connecting a resistor divider from VDAC to VADJ, to AGND; or, by connecting the output of an external DAC to VADJ, and connect the DAC supply to VDAC. VADJ connected to REGN programs the default of 4.2 V per cell.
$\overline{\text{ACGOOD}}$	13	Valid adapter active-low detect logic open-drain output. Pulled low when Input voltage is above programmed ACDET. Connect a 10-kΩ pullup resistor from $\overline{\text{ACGOOD}}$ to VREF, or to a different pullup-supply rail.
$\overline{\text{BATDRV}}$	14	Battery to system switch driver output. Gate drive for the battery to system load BAT PMOS power FET to isolate the system from the battery to prevent current flow from the system to the battery, while allowing a low impedance path from battery to system and while discharging the battery pack to the system load. Connect this pin directly to the gate of the input BAT P-channel power MOSFET. Connect the source of the FET to the system load voltage node. Connect the drain of the FET to the battery pack positive node. An optional capacitor is placed from the gate to the source to slow-down the switching times. The internal gate drive is asymmetrical to allow a quick turn-off and slower turn-on, in addition to the internal break-before-make logic with respect to the $\overline{\text{ACDRV}}$.
IADAPT	15	Adapter current sense amplifier output. IADAPT voltage is 20 times the differential voltage across ACP-ACN. Place a 100-pF or less ceramic decoupling capacitor from IADAPT to AGND.
SRSET	16	Charge current set input. The voltage ratio of SRSET voltage versus VDAC voltage programs the charge current regulation set-point. Program by connecting a resistor divider from VDAC to SRSET to AGND; or by connecting the output of an external DAC to SRSET pin and connect the DAC supply to VDAC pin.
BAT	17	Battery voltage remote sense. Directly connect a kelvin sense trace from the battery pack positive terminal to the BAT pin to accurately sense the battery pack voltage. Place a 0.1-µF capacitor from BAT to AGND close to the IC to filter high-frequency noise.

Table 1. TERMINAL FUNCTIONS – 28-PIN QFN (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
SRN	18	Charge current sense resistor, negative input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-μF ceramic capacitor is placed from SRN pin to AGND for common-mode filtering.
SRP	19	Charge current sense resistor, positive input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-μF ceramic capacitor is placed from SRP pin to AGND for common-mode filtering.
CELLS	20	2, 3 or 4 cells selection logic input. Logic low programs 3 cell. Logic high programs 4 cell. Floating programs 2 cell.
$\overline{\text{DPMDET}}$	21	Dynamic power management (DPM) input current loop active, open-drain output status. Logic low indicates input current is being limited by reducing the charge current. Connect 10-kΩ pullup resistor from $\overline{\text{DPMDET}}$ to VREF or a different pullup-supply rail. Time delay is 10 ms.
PGND	22	Power ground. Ground connection for high-current power converter node. On PCB layout, connect directly to source of low-side power MOSFET, to ground connection of in put and output capacitors of the charger. Only connect to AGND through the PowerPad underneath the IC.
LODRV	23	PWM low side driver output. Connect to the gate of the low-side power MOSFET with a short trace.
REGN	24	PWM low side driver positive 6-V supply output. Connect a 1-μF ceramic capacitor from REGN to PGND, close to the IC. Use for high-side driver bootstrap voltage by connecting a small-signal Schottky diode from REGN to BTST.
PH	25	PWM high side driver negative supply. Connect to the phase switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor). Connect the 0.1-μF bootstrap capacitor from from PH to BTST.
HIDRV	26	PWM high side driver output. Connect to the gate of the high-side power MOSFET with a short trace.
BTST	27	PWM high side driver positive supply. Connect a 0.1-μF bootstrap ceramic capacitor from BTST to PH. Connect a small bootstrap Schottky diode from REGN to BTST.
PVCC	28	IC power positive supply. Connect to the common-source (diode-OR) point: source of high-side P-channel MOSFET and source of reverse-blocking power P-channel MOSFET. Place a 1-μF ceramic capacitor from PVCC to PGND pin close to the IC.
PowerPad		Exposed pad beneath the IC. AGND and PGND star-connected only at the PowerPad plane. Always solder PowerPad to the board, and have vias on the PowerPad plane connecting to AGND and PGND planes. It also serves as a thermal pad to dissipate the heat.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE	UNIT
Voltage range	PVCC, ACP, ACN, SRP, SRN, BAT, $\overline{\text{BATDRV}}$, $\overline{\text{ACDRV}}$	–0.3 to 30	V
	PH	–1 to 30	
	REGN, LODRV, VADJ, ACSET, SRSET, TS, ACDET, ACOP, $\overline{\text{CHGEN}}$, CELLS, $\overline{\text{ACGOOD}}$	–0.3 to 7	
	VDAC	–0.3 to 5.5	
	VREF, IADAPT	–0.3 to 3.6	
	BTST, HIDRV with respect to AGND and PGND	–0.3 to 36	
Maximum difference voltage	ACP–ACN, SRP–SRN, AGND–PGND	–0.5 to 0.5	V
Junction temperature range		–40 to 155	°C
Storage temperature range		–55 to 155	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage range	PH	–1		24	V
	PVCC, ACP, ACN, SRP, SRN, BAT, $\overline{\text{BATDRV}}$, $\overline{\text{ACDRV}}$	0		24	
	REGN, LODRV	0		6.5	
	VDAC, IADAPT	0		3.6	
	VREF		3.3		
	ACSET, SRSET, TS, ACDET, ACOP, $\overline{\text{CHGEN}}$, CELLS, $\overline{\text{ACGOOD}}$, $\overline{\text{DPMDET}}$	0		5.5	
	VADJ	0		6.5	
	BTST, HIDRV with respect to AGND and PGND	0		30	
	AGND, PGND	–0.3		0.3	
Maximum difference voltage: ACP–ACN, SRP–SRN		–0.3		0.3	V
Junction temperature range		–40		125	°C
Storage temperature range		–55		150	

ELECTRICAL CHARACTERISTICS

7 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{PVCC_OP}	PVCC Input voltage operating range		5		24	V
CHARGE VOLTAGE REGULATION						
$V_{BAT\_REG\_RNG}$	BAT voltage regulation range	4-4.512 V per cell, times 2,3,4 cells	8		18.048	V
V_{VDAC_OP}	VDAC reference voltage range		2.6		3.6	V
V_{ADJ_OP}	VADJ voltage range		0		REGN	V
	Charge voltage regulation accuracy	8 V, 8.4 V, 9.024 V	–0.5%		0.5%	
		12 V, 12.6 V, 13.536 V	–0.5%		0.5%	
		16 V, 16.8 V, 18.048 V	–0.5%		0.5%	
	Charge voltage regulation set to default to 4.2 V per cell	VADJ connected to REGN, 8.4 V, 12.6 V, 16.8 V	–0.5%		0.5%	
CHARGE CURRENT REGULATION						
V_{IREG_CHG}	Charge current regulation differential voltage range	$V_{IREG\_CHG} = V_{SRP} - V_{SRN}$	0		100	mV
V_{SRSET_OP}	SRSET voltage range		0		VDAC	V
	Charge current regulation accuracy	V_{IREG_CHG} = 40–100 mV	–3%		3%	
		V_{IREG_CHG} = 20 mV	–5%		5%	
		V_{IREG_CHG} = 5 mV	–25%		25%	
		V_{IREG_CHG} = 1.5 mV (V_{BAT}>4V)	–33%		33%	
INPUT CURRENT REGULATION						
V_{IREG_DPM}	Adapter current regulation differential voltage range	$V_{IREG\_DPM} = V_{ACP} - V_{ACN}$	0		100	mV
V_{ACSET_OP}	ACSET voltage range		0		VDAC	V
	Input current regulation accuracy	V_{IREG_DPM} = 40–100 mV	–3%		3%	
		V_{IREG_DPM} = 20 mV	–5%		5%	
		V_{IREG_DPM} = 5 mV	–25%		25%	
		V_{IREG_DPM} = 1.5 mV	–33%		33%	

ELECTRICAL CHARACTERISTICS (continued)

7 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	V_{ACDET} > 0.6 V, 0-30 mA	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	V_{VREF} = 0 V, V_{ACDET} > 0.6 V	35		75	mA
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{ACDET} > 0.6 V, 0-75 mA, PVCC > 10 V	5.6	5.9	6.2	V
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0 V, V_{ACDET} > 0.6 V	90		135	mA
ADAPTER CURRENT SENSE AMPLIFIER						
V_{ACP/N_OP}	Input common mode range	Voltage on ACP/ACN	0		24	V
V_{IADAPT}	IADAPT output voltage range		0		2	
I_{IADAPT}	IADAPT output current		0		1	mA
A_{IADAPT}	Current sense amplifier voltage gain	$A_{IADAPT} = V_{IADAPT} / V_{IREG\_DPM}$		20		V/V
	Adapter current sense accuracy	V_{IREG_DPM} = 40–100 mV	–2%		2%	
		V_{IREG_DPM} = 20 mV	–3%		3%	
		V_{IREG_DPM} = 5 mV	–25%		25%	
		V_{IREG_DPM} = 1.5 mV	–33%		33%	
I_{IADAPT_LIM}	Output current limit	V_{IADAPT} = 0 V	1%			mA
C_{IADAPT_MAX}	Maximum output load capacitance	For stability with 0 mA to 1 mA load			100	pF
ACDET COMPARATOR						
V_{ACDET_CHG}	ACDET adapter-detect rising threshold	Min voltage to enable charging, V_{ACDET} rising	2.376	2.40	2.424	V
$V_{ACDET\_CHG\_HYS}$	ACDET falling hysteresis	V_{ACDET} falling		40		mV
	ACDET rising deglitch	VACDET rising	518	700	908	ms
	ACDET falling deglitch	VACDET falling	7	9	11	ms
V_{ACDET_BIAS}	ACDET enable-bias rising threshold	Min voltage to enable all bias, V_{ACDET} rising	0.56	0.62	0.68	V
$V_{ACDET\_BIAS\_HYS}$	Adapter present falling hysteresis	V_{ACDET} falling		20		mV
	ACDET rising deglitch	V_{ACDET} rising		10		µs
	ACDET falling deglitch	V_{ACDET} falling		10		µs
PVCC / BAT COMPARATOR (REVERSE DISCHARGING PROTECTION)						
$V_{PVCC\text{-}BAT\_OP}$	Differential Voltage from PVCC to BAT		–20		24	V
$V_{PVCC\text{-}BAT\_FALL}$	PVCC to BAT falling threshold	$V_{PVCC} - V_{BAT}$ to turn off ACFET	140	185	240	mV
$V_{PVCC\text{-}BAT\_\_HYS}$	PVCC to BAT hysteresis			50		mV
	PVCC to BAT Rising Deglitch	$V_{PVCC} - V_{BAT} > V_{PVCC\text{-}BAT\_RISE}$	7	9	11	ms
	PVCC to BAT Falling Deglitch	$V_{PVCC} - V_{BAT} < V_{PVCC\text{-}BAT\_FALL}$		6		µs
INPUT UNDERVOLTAGE LOCK-OUT COMPARATOR (UVLO)						
UVLO	AC Undervoltage rising threshold	Measured on PVCC	3.5	4	4.5	V
$UVLO_{HYS}$	AC Undervoltage hysteresis, falling			260		mV
ACN / BAT COMPARATOR						
$V_{ACN\text{-}BAT\_FALL}$	ACN to BAT falling threshold	$V_{ACN} - V_{BAT}$ to turn on $\overline{BATDRV}$	175	285	340	mV
$V_{ACN\text{-}BAT\_HYS}$	ACN to BAT hysteresis			50		mV
	ACN to BAT rising deglitch	$V_{ACN} - V_{BAT} > V_{ACN\text{-}BAT\_RISE}$		20		µs
	ACN to BAT falling deglitch	$V_{ACN} - V_{BAT} < V_{ACN\text{-}BAT\_FALL}$		6		µs
BAT OVERVOLTAGE COMPARATOR						
V_{OV_RISE}	Overvoltage rising threshold	As percentage of V_{BAT_REG}		104%		
V_{OV_FALL}	Overvoltage falling threshold	As percentage of V_{BAT_REG}		102%		

ELECTRICAL CHARACTERISTICS (continued)

7 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE OVERCURRENT COMPARATOR						
V_{OC}	Charge overcurrent falling threshold	As percentage of I_{REG_CHG}		145 %		
	Minimum Current Limit (SRP-SRN)			50		mV
CHARGE UNDERCURRENT COMPARATOR (SYNCHRONOUS TO NON-SYNCHRONOUS TRANSITION)						
$V_{ISYNSET\_FALL}$	Charge undercurrent falling threshold	Changing from synchronous to non-sysnchronous	9.75	13	16.25	mV
$V_{ISYNSET\_HYS}$	Charge undercurrent rising hysteresis			8		mV
	Charge undercurrent, falling-current deglitch	$V_{IREG\_DPM} < V_{ISYNSET}$		20		µs
	Charge undercurrent, rising-current deglitch			640		
INPUT OVERPOWER COMPARATOR (ACOP)						
V_{ACOC}	ACOC Gain for initial ACOC current limit limit (Percentage of programmed VIREG_DPM)	Begins 700 ms after ACDET Input current limited to this threshold for fault protection		150		% V_{IREG_DPM}
$V_{ACOC\_CEILING}$	Maximum ACOC input current limit (V_{ACP}–V_{ACN})max	Internally limited ceiling $V_{ACOC\_MAX} = (V_{ACP}–V_{ACN})max$		100		mV
	ACOP Latch Blankout Time with ACOC active (begins 700 ms after ACDET)	Begins 700 ms after ACDET (does not allow ACOP latch-off, and no ACOP source current)		2		ms
V_{ACOP}	ACOP pin latch-off threshold voltage (See ACOP in *Terminal Functions table*)		1.95	2	2.05	V
K_{ACOP}	Gain for ACOP Source Current when in ACOC	Current source on when in ACOC limit. Function of voltage across power FET $I_{ACOP\_SOURCE} = K_{ACOP} \times (V_{PVCC} - V_{ACP})$		18		µA / V
I_{ACOP_SINK}	ACOP Sink Current when not in ACOC ACOP Latch is reset by going below ACDET or UVLO	Current sink on when not in ACOC		5		µA
INPUT OVERVOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	AC Overvoltage rising threshold on ACDET (See ACDET in *Terminal Functions*)	Measured on ACDET	3.007	3.1	3.193	V
V_{ACOV_HYS}	AC Overvoltage rising deglitch			1.3		ms
	AC Overvoltage falling deglitch			1.3		
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature Increasing		155		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis, falling			20		°C
THERMISTER COMPARATOR (TS)						
V_{LTF}	Cold temperature rising threshold	As percentage to V_{VREF}	72.5%	73.8 %	74.2%	
V_{LTF_HYS}	Rising hysteresis	As percentage to V_{VREF}	0.5%	1%	1.5%	
V_{TCO}	Cut-off temperature rising threshold	As percentage to V_{VREF}	28.7%	29.3 %	29.9%	
V_{HTF}	Hot temperature rising threshold	As percentage to V_{VREF}	33.7%	34.4 %	35.1%	
	Deglitch time for temperature out of range detection	$V_{TS} > V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$		10		ms
	Deglitch time for temperature in valid range detection	$V_{TS} > V_{LTF} – V_{LTF\_HYS}$ or $V_{TS} > V_{TCO}$, or $V_{TS} > V_{HTF}$		10		

ELECTRICAL CHARACTERISTICS (continued)

7 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY SWITCH ($\overline{\text{BATDRV}}$) DRIVER						
$R_{DS(off)\_BAT}$	BATFET Turn-off resistance	V_{ACN} > 5 V			160	Ω
$R_{DS(on)\_BAT}$	BATFET Turn-on resistance	V_{ACN} > 5 V			3	kΩ
$V_{\overline{BATDRV}\_REG}$	BATFET drive voltage	$V_{\overline{BATDRV}\_REG} = V_{ACN} - V_{\overline{BATDRV}}$ when V_{ACN} > 5 V and BATFET is on		6.5		V
	BATFET Power-up delay	Delay to turn off BATFET after adapter is detected (after ACDET > 2.4)	518	700	908	ms
AC SWITCH ($\overline{\text{ACDRV}}$) DRIVER						
$R_{DS(off)\_AC}$	ACFET turn-off resistance	V_{PVCC} > 5 V			80	Ω
$R_{DS(on)\_AC}$	ACFET turn-on resistance	V_{PVCC} > 5 V			2.5	kΩ
$V_{\overline{ACDRV}\_REG}$	ACFET drive voltage	$V_{\overline{ACDRV}\_REG} = V_{PVCC} - V_{\overline{ACDRV}}$ when V_{PVCC} > 5 V and ACFET is on		6.5		V
	ACFET Power-up Delay	Delay to turn on ACFET after adapter is detected (after ACDET > 2.4)	518	700	908	ms
AC / BAT MOSFET DRIVERS TIMING						
	Driver dead time	Dead time when switching between $\overline{\text{ACDRV}}$ and $\overline{\text{BATDRV}}$		10		µs
PWM HIGH SIDE DRIVER (HIDRV)						
$R_{DS\_HI\_ON}$	High side driver (HSD) turn-on resistance	$V_{BTST} - V_{PH}$ = 5.5 V, tested at 100 mA		3	6	Ω
$R_{DS\_HI\_OFF}$	High side driver turn-off resistance	$V_{BTST} - V_{PH}$ = 5.5 V, tested at 100 mA		0.7	1.4	Ω
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold voltage	$V_{BTST} - V_{PH}$ when low side refresh pulse is requested	4			V
PWM LOW SIDE DRIVER (LODRV)						
$R_{DS\_LO\_ON}$	Low side driver (LSD) turn-on resistance	REGN = 6 V, tested at 100 mA		3	6	Ω
$R_{DS\_LO\_OFF}$	Low side driver turn-off resistance	REGN = 6 V, tested at 100 mA		0.6	1.2	Ω
PWM DRIVERS TIMING						
	Driver Dead Time — Dead time when switching between LODRV and HIDRV. No load at LODRV and HIDRV		30			ns
PWM OSCILLATOR						
F_{SW}	PWM switching frequency		240		360	kHz
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of PVCC		6.6		%PVCC
QUIESCENT CURRENT						
I_{OFF_STATE}	Total off-state quiescent current into pins: SRP, SRN, BAT, BTST, PH, PVCC, ACP, ACN	V_{BAT} = 16.8 V, V_{ACDET} < 0.6 V, V_{PVCC} > 5 V, T_J = 0 to 85°C		7	10	µA
I_{AC}	Adapter quiescent current	V_{PVCC} = 20 V, charge disabled		2.8	4	mA
I_{BATQ_CD}	Total quiescent current into pins: SRP, SRN, BAT, BTST, PH	Adapter present, VACDET>2.4V, charge disabled		100	200	µA
INTERNAL SOFT START (8 steps to regulation current)						
	Soft start steps			8		step
	Soft start step time			1.7		ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-enable delay after power-up	Delay from when adapter is detected to when the charger is allowed to turn on	518	700	908	ms

ELECTRICAL CHARACTERISTICS (continued)

7 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT PIN CHARACTERISTICS ($\overline{\text{CHGEN}}$)						
V_{IN_LO}	Input low threshold voltage				0.8	V
V_{IN_HI}	Input high threshold voltage		2.1			
I_{BIAS}	Input bias current	$V_{\overline{CHGEN}}$ = 0 to V_{REGN}			1	µA
LOGIC INPUT PIN CHARACTERISTICS (CELLS)						
V_{IN_LO}	Input low threshold voltage, 3 cells	CELLS voltage falling edge			0.5	V
V_{IN_MID}	Input mid threshold voltage, 2 cells	CELLS voltage rising for MIN, CELLS voltage falling for MAX	0.8		1.8	
V_{IN_HI}	Input high threshold voltage, 4 cells	CELLS voltage rising	2.5			
I_{BIAS_FLOAT}	Input bias float current for 2-cell selection	$V_{\overline{CHGEN}}$ = 0 to V_{REGN}	–1		1	µA
OPEN-DRAIN LOGIC OUTPUT PIN CHARACTERISTICS ($\overline{\text{ACGOOD}}$)						
V_{OUT_LO}	Output low saturation voltage	Sink Current = 4 mA			0.5	V
	Delay, $\overline{\text{ACGOOD}}$ falling		518	700	908	ms
	Delay, $\overline{\text{ACGOOD}}$ rising			10		µs
OPEN-DRAIN LOGIC OUTPUT PIN CHARACTERISTICS ($\overline{\text{DPMDET}}$)						
V_{OUT_LO}	Output low saturation voltage	Sink Current = 5 mA			0.5	V
	Delay, $\overline{\text{DPMDET}}$ rising/falling			10		ms

TYPICAL CHARACTERISTICS

Table of Graphs[1]

Y-Axis	X-Axis	Figure
VREF Load and Line Regulation	vs Load Current	Figure 3
REGN Load and Line Regulation	vs Load Current	Figure 4
BAT Voltage	vs VADJ/VDAC Ratio	Figure 5
Charge Current	vs SRSET/VDAC Ratio	Figure 6
Input Current	vs ACSET/VDAC Ratio	Figure 7
BAT Voltage Regulation Accuracy	vs Charge Current	Figure 8
BAT Voltage Regulation Accuracy		Figure 9
Charge Current Regulation Accuracy		Figure 10
Input Current Regulation (DPM) Accuracy		Figure 11
V_{IADAPT} Input Current Sense Amplifier Accuracy		Figure 12
Input Regulation Current (DPM), and Charge Current	vs System Current	Figure 13
Transient System Load (DPM) Response		Figure 14
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Efficiency	vs Battery Charge Current	Figure 16
Battery Removal (from Constant Current Mode)		Figure 17
$\overline{\text{ACDRV}}$ and $\overline{\text{BATDRV}}$ Startup		Figure 18
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System Selector on Adapter Insertion with 390-µF SYS-to-PGND System Capacitor		Figure 20
System Selector on Adapter Removal with 390-µF SYS-to-PGND System Capacitor		Figure 21
System Selector on Adapter Insertion		Figure 22
Selector Gate Drive Voltages, 700 ms delay after ACDET		Figure 23
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Nonsynchronous to Synchronous Transition		Figure 26
Synchronous to Nonsynchronous Transition		Figure 27
Near 100% Duty Cycle Bootstrap Recharge Pulse		Figure 28
Battery Shorted Charger Response, Over Current Protection (OCP) and Charge Current Regulation		Figure 29
Continuous Conduction Mode (CCM) Switching Waveforms		Figure 30
Discontinuous Conduction Mode (DCM) Switching Waveforms		Figure 31

(1) Test results based on Figure 2 application schematic. V_{IN} = 20 V, V_{BAT} = 3-cell Li+, I_{CHG} = 3 A, $I_{ADAPTER\_LIMIT}$ = 4 A, T_A = 25°C, unless otherwise specified.

VREF LOAD AND LINE REGULATION vs Load Current

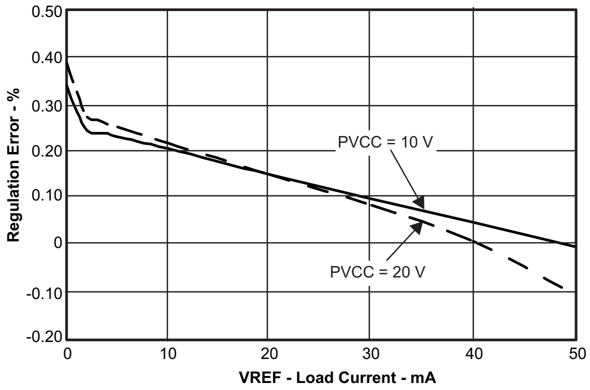


Figure 3.

REGN LOAD AND LINE REGULATION vs LOAD CURRENT

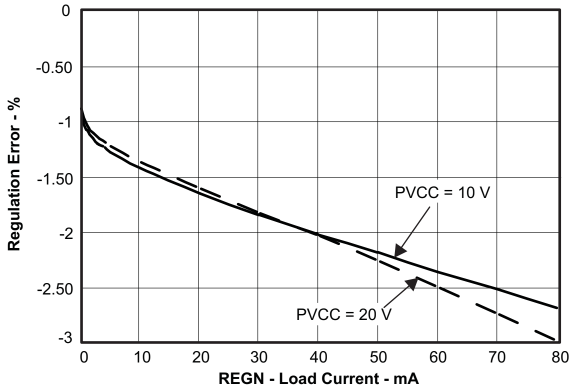


Figure 4.

BAT VOLTAGE vs VADJ/VDAC RATIO

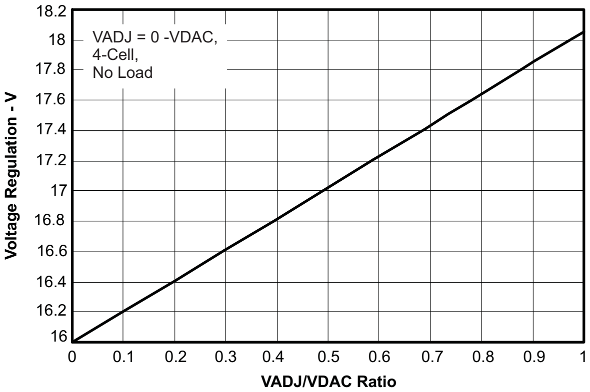


Figure 5.

CHARGE CURRENT vs SRSET/VDAC RATIO

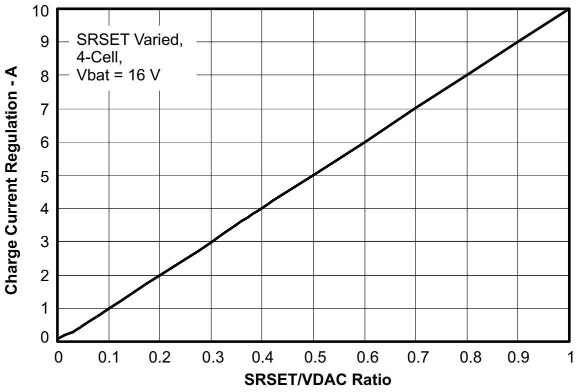


Figure 6.

INPUT CURRENT vs ACSET/VDAC RATIO

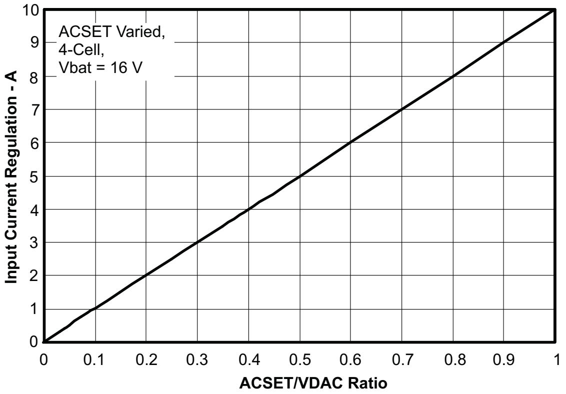


Figure 7.

BAT VOLTAGE REGULATION ACCURACY vs CHARGE CURRENT

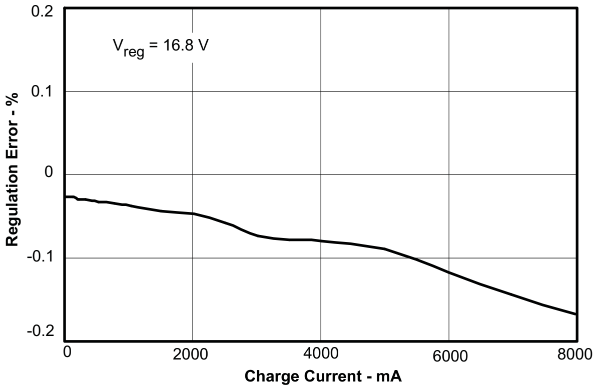


Figure 8.

BAT VOLTAGE REGULATION ACCURACY

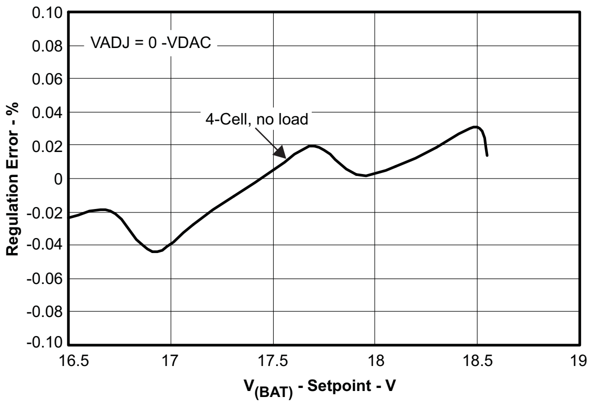


Figure 9.

CHARGE CURRENT REGULATION ACCURACY

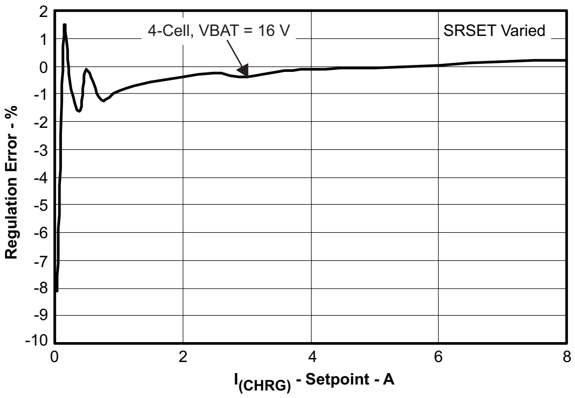


Figure 10.

INPUT CURRENT REGULATION (DPM) ACCURACY

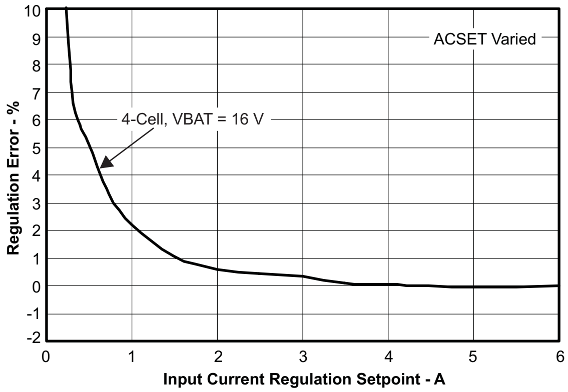


Figure 11.

V_{IADAPT} INPUT CURRENT SENSE AMPLIFIER ACCURACY

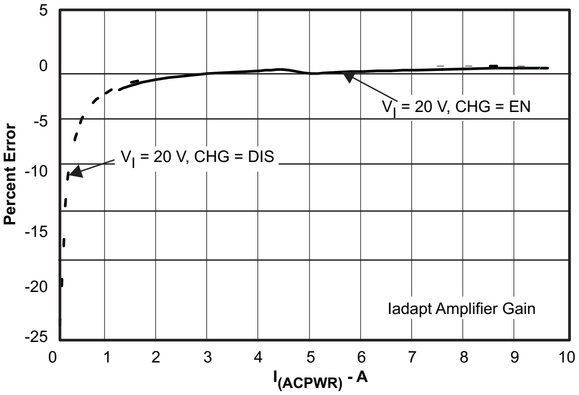


Figure 12.

INPUT REGULATION CURRENT (DPM), AND CHARGE CURRENT
VS
SYSTEM CURRENT

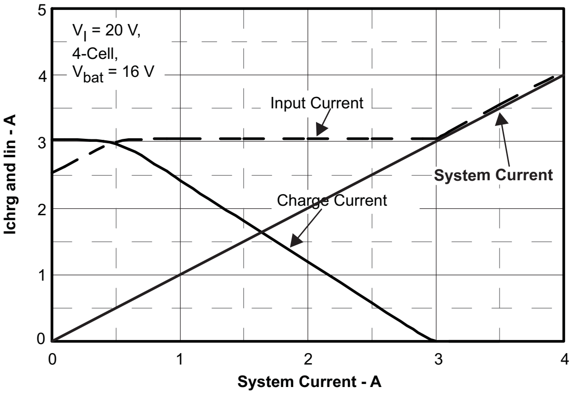


Figure 13.

TRANSIENT SYSTEM LOAD (DPM) RESPONSE

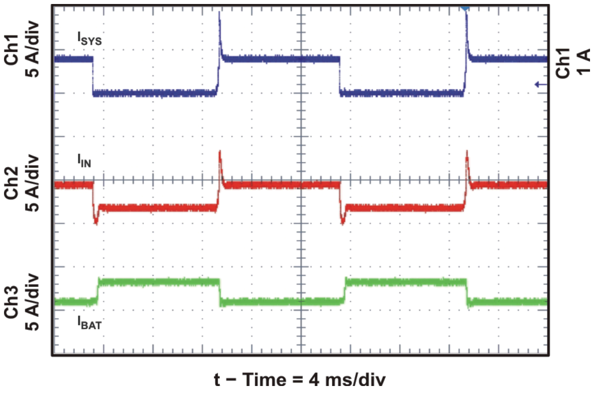
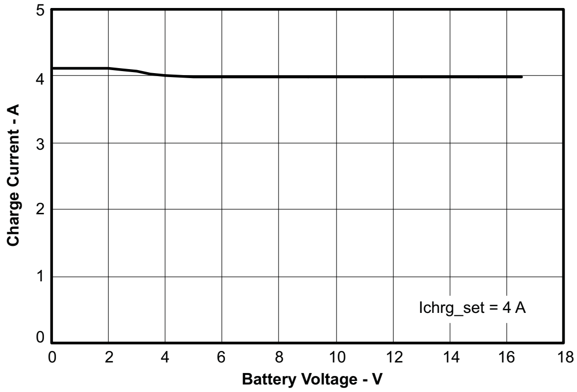
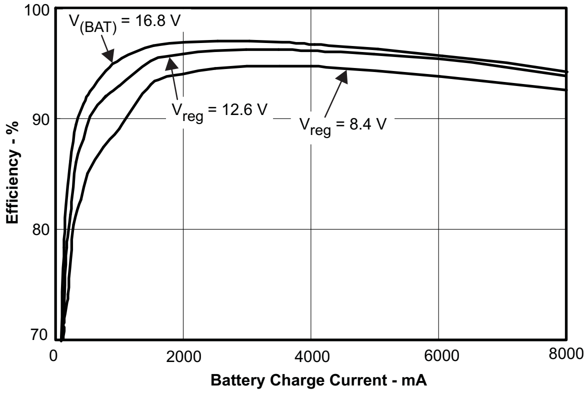


Figure 14.



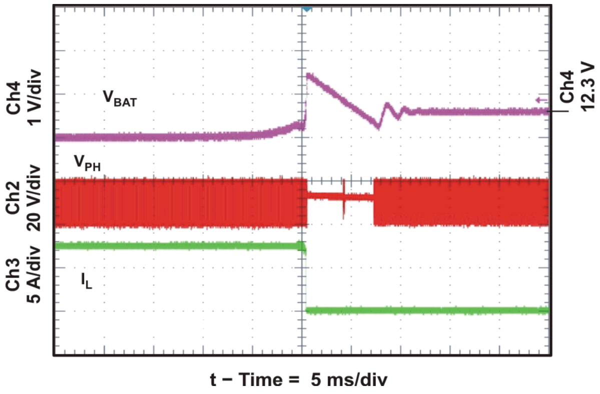
CHARGE CURRENT REGULATION
vs
BAT VOLTAGE

Figure 15.



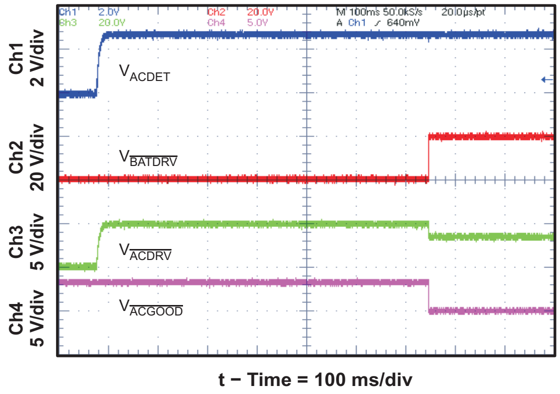
EFFICIENCY
vs
BATTERY CHARGE CURRENT

Figure 16.



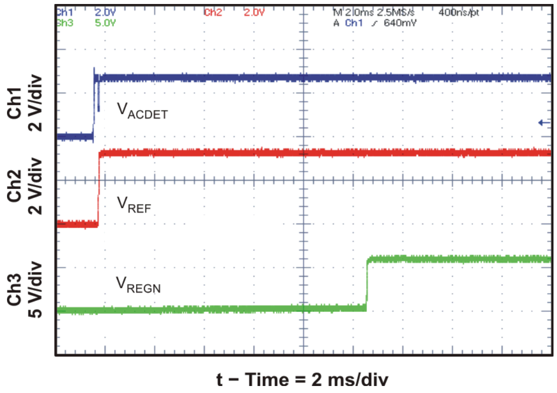
BATTERY REMOVAL

Figure 17.



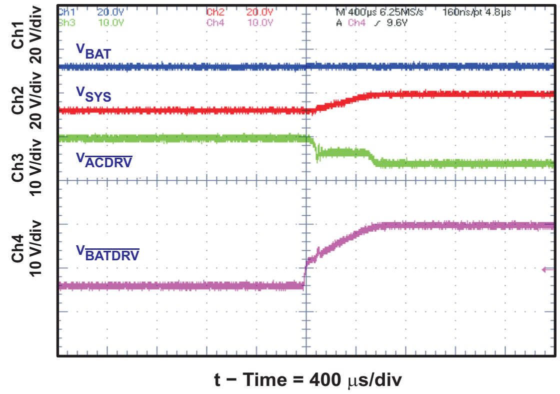
$\overline{\text{ACDRV}}$ AND $\overline{\text{BATDRV}}$ STARTUP

Figure 18.



REF AND REGN STARTUP

Figure 19.



SYSTEM SELECTOR ON ADAPTER INSERTION WITH
390 µF SYS-TO-PGND SYSTEM CAPACITOR

Figure 20.

SYSTEM SELECTOR ON ADAPTER REMOVAL WITH 390 µF SYS-TO-PGND SYSTEM CAPACITOR

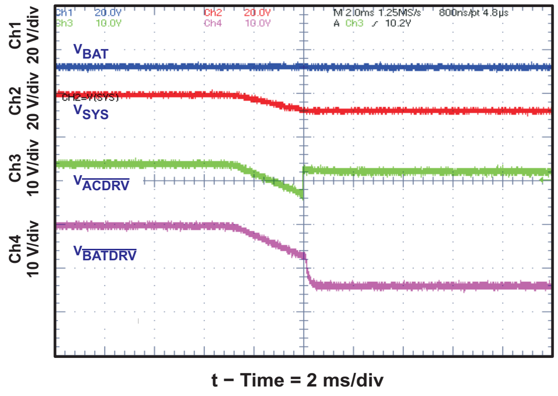


Figure 21.

SYSTEM SELECTOR ON ADAPTER INSERTION

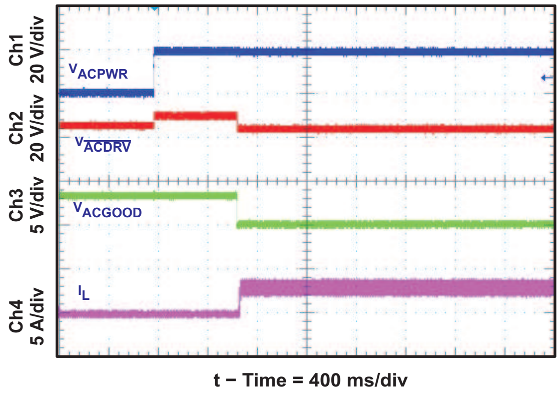


Figure 22.

SELECTOR GATE DRIVE VOLTAGES, 700 MS DELAY AFTER ACDET

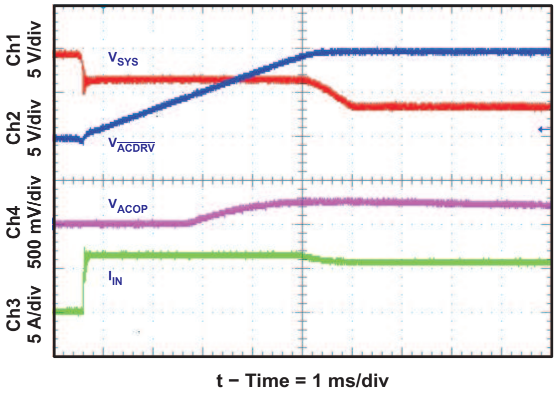


Figure 23.

CHARGER ON ADAPTER REMOVAL

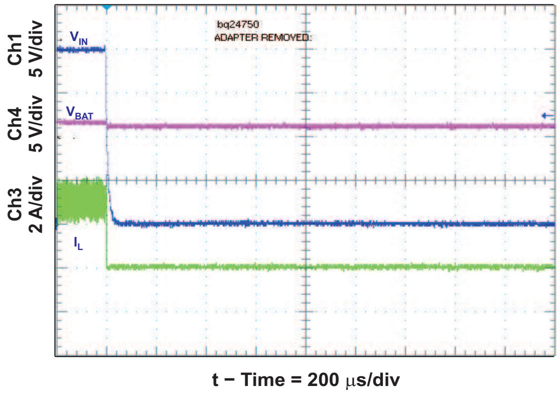


Figure 24.

CHARGE ENABLE / DISABLE AND CURRENT SOFT-START

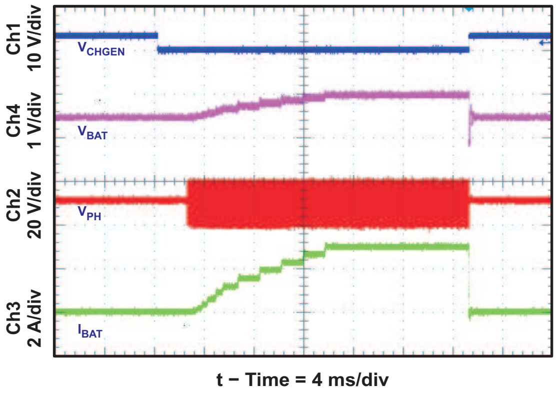


Figure 25.

NONSYNCHRONOUS TO SYNCHRONOUS TRANSITION

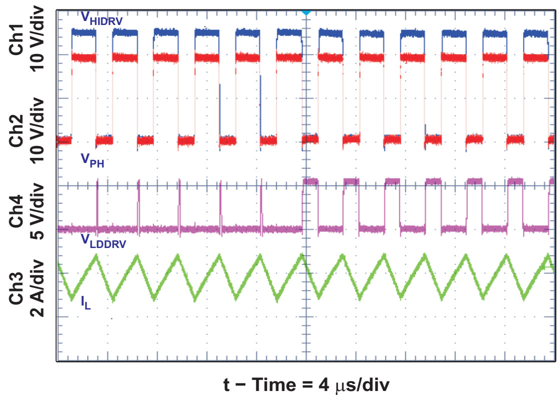


Figure 26.

SYNCHRONOUS TO NONSYNCHRONOUS TRANSITION

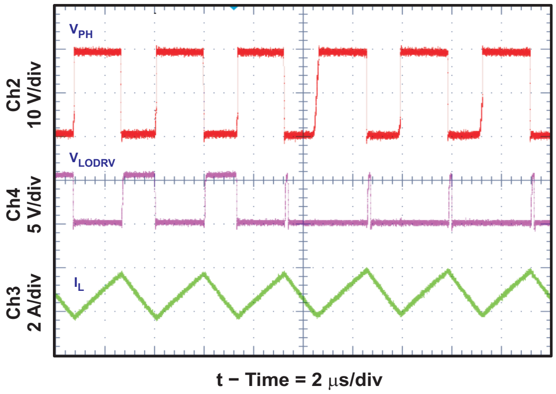


Figure 27.

NEAR 100% DUTY CYCLE BOOTSTRAP RECHARGE PULSE

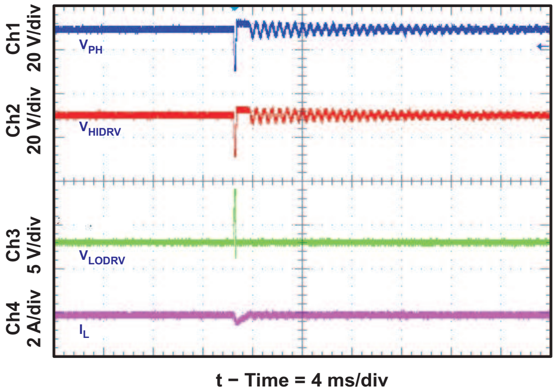


Figure 28.

BATTERY SHORTED CHARGER RESPONSE, OVERCURRENT PROTECTION (OCP) AND CHARGE CURRENT REGULATION

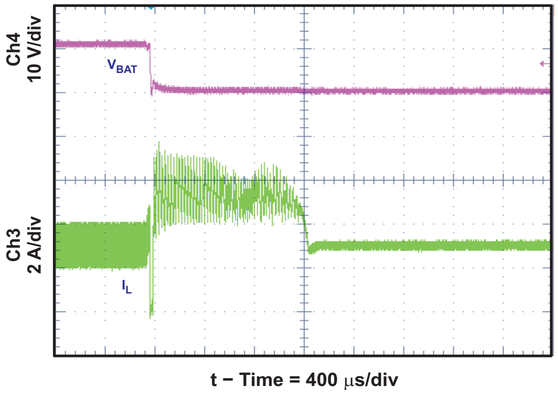


Figure 29.

CONTINUOUS CONDUCTION MODE (CCM) SWITCHING WAVEFORMS

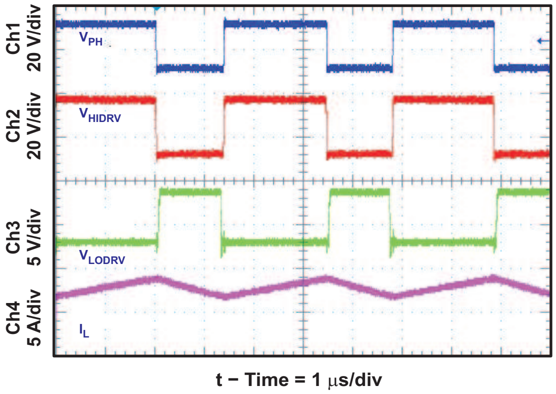


Figure 30.

DISCONTINUOUS CONDUCTION MODE (DCM) SWITCHING WAVEFORMS

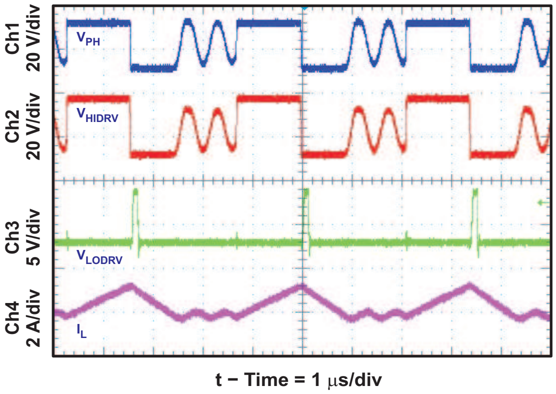
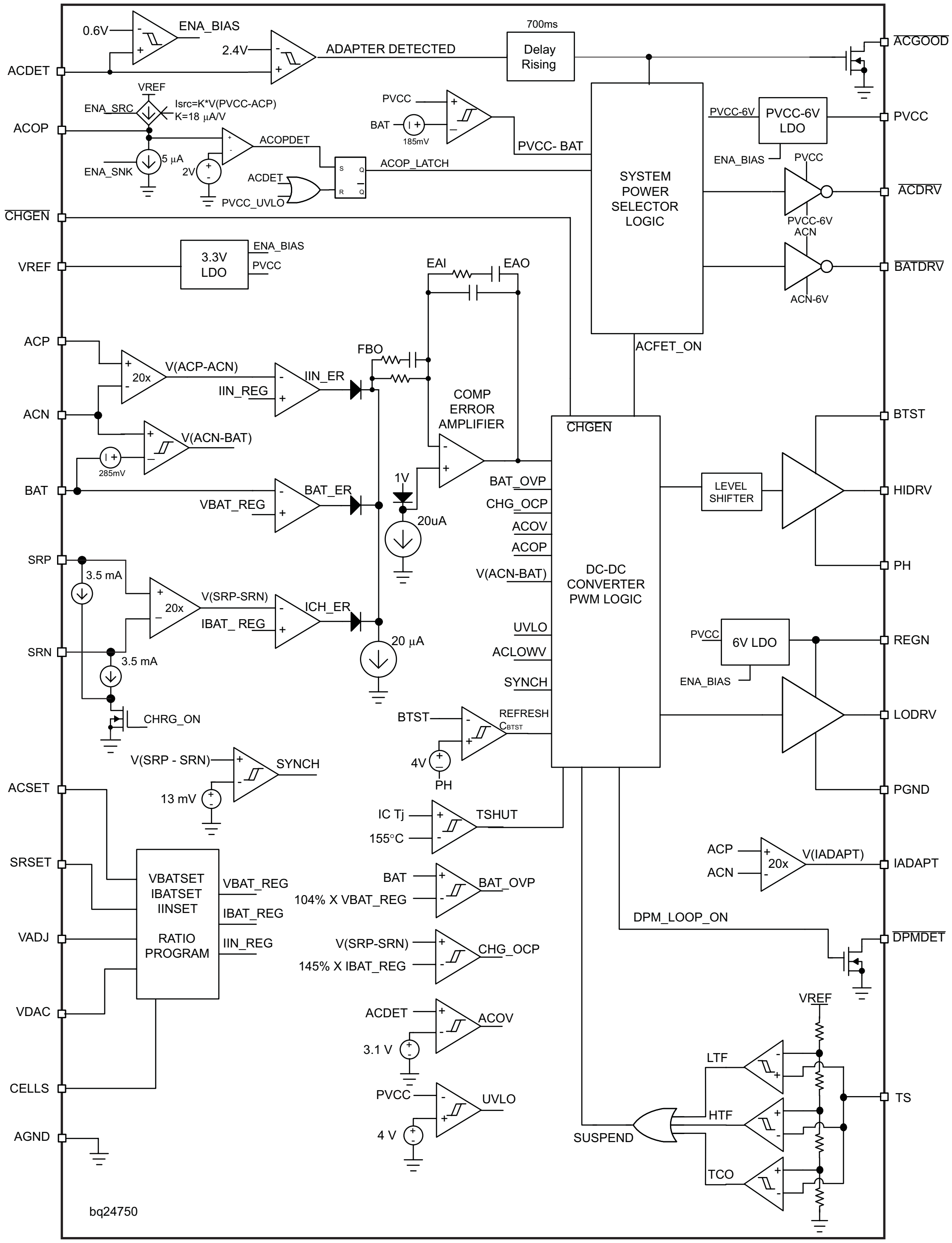


Figure 31.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Battery Voltage Regulation

The bq24750 uses a high-accuracy voltage regulator for the charging voltage. The internal default battery-voltage setting is V_{BATT} = 4.2 V × cell count. The regulation voltage is ratiometric with respect to VDAC. The ratio of VADJ and VDAC provides an extra 12.5% adjustment range on the V_{BATT} regulation voltage. By limiting the adjustment range to 12.5% of the regulation voltage, the external resistor mismatch error is reduced from ±1% to ±0.1%. Therefore, an overall voltage accuracy as good as 0.5% is maintained, even while using 1%-mismatched resistors. Ratiometric conversion also allows compatibility with D/As or microcontrollers (µC). The battery voltage is programmed through VADJ and VDAC using Equation 1.

$$V_{BATT} = \text{cell count} \times \left[4\text{ V} + \left(0.512 \times \frac{V_{VADJ}}{V_{VDAC}} \right) \right] \quad (1)$$

REGN – V_t = REGN – 0.5 V

The input voltage range of VDAC is between 2.6 V and 3.6 V. VADJ is set between 0 and VDAC. V_{BATT} defaults to 4.2 V × cell count when VADJ is connected to REGN.

CELLS pin is the logic input for selecting cell count. Connect CELLS to charge 2,3, or 4 Li+ cells. When charging other cell chemistries, use CELLS to select an output voltage range for the charger.

CELLS	CELL COUNT
Float	2
AGND	3
VREF	4

The per-cell charge-termination voltage is a function of the battery chemistry. Consult the battery manufacturer to determine this voltage.

The BAT pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, or directly on the output capacitor. A 0.1-µF ceramic capacitor from BAT to AGND is recommended to be as close to the BAT pin as possible to decouple high frequency noise.

Battery Current Regulation

The SRSET input sets the maximum charge current. Battery current is sensed by resistor R_{SR} connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 100 mV. Thus, for a 0.010-Ω sense resistor, the maximum charging current is 10 A. SRSET is ratiometric with respect to VDAC using Equation 2:

$$I_{CHARGE} = \frac{V_{SRSET}}{V_{VDAC}} \times \frac{0.10}{R_{SR}} \quad (2)$$

The input voltage range of SRSET is between 0 and V_{DAC}, up to 3.6 V.

The SRP and SRN pins are used to sense across R_{SR}, with a default value of 10 mΩ. However, resistors of other values can also be used. A larger sense-resistor value yields a larger sense voltage, and a higher regulation accuracy. However, this is at the expense of a higher conduction loss.

Input Adapter Current Regulation

The total input current from an AC adapter or other DC sources is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without Dynamic Power Management (DPM), the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the input current regulator reduces the charging current when the input current exceeds the input current limit set by ACSET. The current capacity of the AC adapter can be lowered, reducing system cost.

Similar to setting battery regulation current, adapter current is sensed by resistor R_{AC} connected between ACP and ACN. Its maximum value is set ACSET, which is ratiometric with respect to VDAC, using Equation 3.

$$I_{ADAPTER} = \frac{V_{ACSET}}{V_{VDAC}} \times \frac{0.10}{R_{AC}} \tag{3}$$

The input voltage range of ACSET is between 0 and V_{DAC}, up to 3.6 V.

The ACP and ACN pins are used to sense R_{AC} with a default value of 10 mΩ. However, resistors of other values can also be used. A larger sense-resistor value yields a larger sense voltage, and a higher regulation accuracy. However, this is at the expense of a higher conduction loss.

Adapter Detect and Power Up

An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. The adapter-detect threshold should typically be programmed to a value greater than the maximum battery voltage, and lower than the minimum allowed adapter voltage. The ACDET divider should be placed before the ACFET in order to sense the true adapter input voltage whether the ACFET is on or off. Before the adapter is detected, BATFET stays on and ACFET turns off.

If PVCC is below 4 V, the device is disabled.

If ACDET is below 0.6 V but PVCC is above 4 V, part of the bias is enabled, including a crude bandgap reference, ACFET drive and BATFET drive. IADAPT is disabled and pulled down to GND. The total quiescent current is less than 10 µA.

When ACDET rises above 0.6 V and PVCC is above 4 V, all the bias circuits are enabled and the REGN output goes to 6 V and VREF goes to 3.3 V. IADAPT becomes valid to proportionally reflect the adapter current.

When ACDET keeps rising and passes 2.4 V, a valid AC adapter is present. 700 ms later, the following occurs:

- $\overline{\text{ACGOOD}}$ goes low through external pull-up resistor to the host digital voltage rail;
- ACFET can turn on and BATFET turns off consequently; (refer to *System Power Selector*)
- Charging begins if all the conditions are satisfied. (refer to *Enable and Disable Charging*)

Enable and Disable Charging

The following conditions must be valid before charge is enabled:

- $\overline{\text{CHGEN}}$ is LOW
- PVCC > UVLO
- Adapter is detected
- Adapter voltage is higher than BAT + 185 mV
- Adapter is not over voltage (ACOV)
- 700 ms delay is complete after the adapter is detected plus 10 ms ACOC time
- Thermal Shut (TSHUT) is not valid
- TS is within the temperature qualification window
- VDAC > 2.4 V

System Power Selector

The bq24750 automatically switches between connecting the adapter or battery power to the system load. By default, the battery is connected to the system during power up or when a valid adapter is not present. When the adapter is detected, the battery is first disconnected from the system, then the adapter is connected. An automatic break-before-make algorithm prevents shoot-through currents when the selector transistors switch.

The $\overline{\text{ACDRV}}$ signal drives a pair of back-to-back p-channel power MOSFETs (with sources connected together and to PVCC) connected between the adapter and ACP. The FET connected to the adapter prevents reverse discharge from the battery to the adapter when it is turned off. The p-channel FET with the drain connected to the adapter input provides reverse battery discharge protection when off; and also minimizes system power dissipation, with its low R_{dson}, compared to a Schottky diode. The other p-channel FET connected to ACP separates the battery from the adapter, and provides both ACOC current limit and ACOP power limit to the system. The $\overline{\text{BATDRV}}$ signal controls a p-channel power MOSFET placed between BAT and the system.

When the adapter is not detected, the $\overline{\text{ACDRV}}$ output is pulled to PVCC to turn off the ACFET, disconnecting the adapter from system. $\overline{\text{BATDRV}}$ stays at ACN – 6 V to connect the battery to system.

At 700 ms after adapter is detected, the system begins to switch from the battery to the adapter. The PVCC voltage must be 185 mV above BAT to enable the switching. The break-before-make logic turns off both ACFET and BATFET for 10μs before ACFET turns on. This isolates the battery from shoot-through current or any large discharging current. The $\overline{\mathrm{BATDRV}}$ output is pulled up to ACN and the $\overline{\mathrm{ACDRV}}$ pin is set to PVCC – 6 V by an internal regulator to turn on the p-channel ACFET, connecting the adapter to the system.

When the adapter is removed, the system waits till ACN drops back to within 285 mV above BAT to switch from the adapter back to the battery. The break-before-make logic ensures a 10-μs dead time. The $\overline{\mathrm{ACDRV}}$ output is pulled up to PVCC and the $\overline{\mathrm{BATDRV}}$ pin is set to ACN – 6 V by an internal regulator to turn on the p-channel BATFET, connecting the battery to the system.

Asymmetrical gate drive for the $\overline{\mathrm{ACDRV}}$ and $\overline{\mathrm{BATDRV}}$ drivers provides fast turn-off and slow turn-on of the ACFET and BATFET to help the break-before-make logic and to allow a soft-start at turn-on of either FET. The soft-start time can be further increased, by putting a capacitor from gate to source of the p-channel power MOSFETs.

Automatic Internal Soft-Start Charger Current

The charger automatically soft-starts the charger regulation current every time the charger is enabled to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charger regulation current into 8 evenly divided steps up to the programmed charge current. Each step lasts approximately 1.7 ms, for a typical rise time of 13.6 ms. No external components are needed for this function.

Converter Operation

The synchronous-buck PWM converter uses a fixed-frequency (300 kHz) voltage mode with a feed-forward control scheme. A Type-III compensation network allows the use of ceramic capacitors at the output of the converter. The compensation input stage is internally connected between the feedback output (FBO) and the error-amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter is selected for a nominal resonant frequency of 8 kHz–12.5 kHz.

The resonant frequency, f_o, is given by: $f_O = \frac{1}{2\pi\sqrt{L_O C_O}}$ where (from Figure 1 schematic)

- $C_O = C11 + C12$
- $L_O = L1$

An internal sawtooth ramp is compared to the internal EAO error-control signal to vary the duty cycle of the converter. The ramp height is one-fifteenth of the input adapter voltage, making it always directly proportional to the input adapter voltage. This cancels out any loop-gain variation due to a change in input voltage, and simplifies the loop compensation. The ramp is offset by 200 mV in order to allow a 0% duty cycle when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the sawtooth ramp signal in order to operate with a 100% duty-cycle PWM request. Internal gate-drive logic allows a 99.98% duty-cycle while ensuring that the N-channel upper device always has enough voltage to stay fully on. If the BTST-to-PH voltage falls below 4 V for more than 3 cycles, the high-side N-channel power MOSFET is turned off and the low-side N-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BTST-PH) voltage is detected falling low again due to leakage current discharging the BTST capacitor below 4 V, and the reset pulse is reissued.

The 300-kHz fixed-frequency oscillator tightly controls the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature. This simplifies output-filter design, and keeps it out of the audible noise region. The charge-current sense resistor R_{SR} should be designed with at least half or more of the total output capacitance placed before the sense resistor, contacting both sense resistor and the output inductor; and the other half, or remaining capacitance placed after the sense resistor. The output capacitance should be divided and placed on both sides of the charge-current sense resistor. A ratio of 50:50 percent gives the best performance; but the node in which the output inductor and sense resistor connect should have a minimum of 50% of the total capacitance. This capacitance provides sufficient filtering to remove the switching noise and give better current-sense accuracy. The Type-III compensation provides phase boost near the cross-over frequency, giving sufficient phase margin.

Synchronous and Non-Synchronous Operation

The charger operates in non-synchronous mode when the sensed charge current is below the ISYNSET value. Otherwise, the charger operates in synchronous mode.

During synchronous mode, the low-side N-channel power MOSFET is on when the high-side N-channel power MOSFET is off. The internal gate-drive logic uses break-before-make switching to prevent shoot-through currents. During the 30-ns dead time where both FETs are off, the back-diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn-on keeps the power dissipation low, and allows safe charging at high currents. During synchronous mode, the inductor current always flows, and the device operates in Continuous Conduction Mode (CCM), creating a fixed two-pole system.

During non-synchronous operation, after the high-side N-channel power MOSFET turns off, and after the break-before-make dead-time, the low-side N-channel power MOSFET will turn-on for around 80ns, then the low-side power MOSFET will turn-off and stay off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The low-side MOSFET 80-ns on-time is required to ensure that the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle. This is important for battery chargers, where unlike regular dc-dc converters, there is a battery load that maintains a voltage and can both source and sink current. The 80-ns low-side pulse pulls the PH node (connection between high and low-side MOSFET) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After the 80 ns, the low-side MOSFET is kept off to prevent negative inductor current from occurring. The inductor current is blocked by the turned-off low-side MOSFET, and the inductor current becomes discontinuous. This mode is called Discontinuous Conduction Mode (DCM).

During the DCM mode, the loop response automatically changes and has a single-pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means that at very low currents, the loop response is slower, because there is less sinking current available to discharge the output voltage. At very low currents during non-synchronous operation, there may be a small amount of negative inductor current during the 80-ns recharge pulse. The charge should be low enough to be absorbed by the input capacitance.

Whenever BTST – PH < 4 V, the 80-ns recharge pulse occurs on LODRV, the high-side MOSFET does not turn on, and the low-side MOSFET does not turn on (only 80-ns recharge pulse).

In the bq24750, $V_{ISYNSET}=I_{SYN}\times R_{SR}$ is internally set to 13mV as the charge-current threshold at which the charger changes from non-synchronous to synchronous operation. The low-side driver turns on for only 80 ns to charge the boost capacitor. This is important to prevent negative inductor current, which may cause a boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors. This boost effect can lead to excessive voltage on the PVCC node and potential system damage. The inductor ripple current is given by:Equation 4

$$\frac{I_{RIPPLE\_MAX}}{2} \le I_{SYN} \le I_{RIPPLE\_MAX}$$

and

$$I_{RIPPLE} = \frac{(V_{IN} - V_{BAT}) \times \frac{V_{BAT}}{V_{IN}} \times \frac{1}{f_s}}{L} = \frac{V_{IN} \times (1 - D) \times D \times \frac{1}{f_s}}{L} \tag{4}$$

where:

V_{IN} = adapter voltage
V_{BAT} = BAT voltage
f_S = switching frequency
L = output inductor
D = duty-cycle

I_{RIPPLE_MAX} Happens when the duty-cycle(D) is mostly near to 0.5 at given V_{IN}, f_s, and L.

The ISYNSET comparator, or charge undercurrent comparator, compares the voltage between SRP-SRN and internal threshold. The threshold is set to 13 mV on the falling edge, with an 8-mV hysteresis on the rising edge with a 10% variation.

High Accuracy IADAPT Using Current Sense Amplifier (CSA)

An industry-standard, high-accuracy current-sense amplifier (CSA) allows a host processor or discrete logic to monitor the input current through the analog voltage output of the IADAPT pin. The CSA amplifies the input sensed voltage of ACP – ACN by 20× through the IADAPT pin. The IADAPT output is a voltage source 20× the input differential voltage. When PVCC is above 5V and ACDET is above 0.6V, IADAPT no longer stays at ground, but becomes active. If the designer needs to lower the voltage, a resistor divider from IOUT to AGND can be used, while still achieving accuracy over temperature as the resistors can be matched for their thermal coefficients.

A 200-pF capacitor connected on the output is recommended for decoupling high-frequency noise. An additional RC filter is optional, after the maximum 200-pF capacitor, if additional filtering is desired. Note that adding filtering also adds additional response delay.

Input Overvoltage Protection (ACOV)

ACOV provides protection to prevent system damage due to high input voltage. The controller enters ACOV when ACDET > 3.1 V. Charge is disabled, the adapter is disconnected from the system by turning off $\overline{\text{ACDRV}}$, and the battery is connected to the system by turning on $\overline{\text{BATDRV}}$. ACOV is not latched—normal operation resumes when the ACDET voltage returns below 3.1 V. ACOV threshold is 130% of the adapter-detect threshold.

Input Undervoltage Lockout (UVLO)

The system must have 5 V minimum of PVCC voltage for proper operation. This PVCC voltage can come from either the input adapter or the battery, using a diode-OR input. When the PVCC voltage is below 5 V, the bias circuits REGN, VREF, and the gate drive bias to ACFET and BATFET stay inactive, even with ACDET above 0.6 V.

NOTE:

> The bq24750 will not allow $\overline{\text{ACDRV}}$ to turn on in the unique condition that ACP<3V and PVCC>UVLO. In this condition, the break-before-make protection latch gets stuck in a state that it thinks the $\overline{\text{BATDRV}}$ is ON, and does not allow the $\overline{\text{ACDRV}}$ to turn on.

Battery Overvoltage Protection

The converter stops switching when BAT voltage goes above 104% of the regulation voltage. The converter will not allow the high-side FET to turn on until the BAT voltage goes below 102% of the regulation voltage. This allows one-cycle response to an overvoltage condition, such as when the load is removed or the battery is disconnected.

Charge Overcurrent Protection

The charger has a secondary overcurrent protection feature. It monitors the charge current, and prevents the current from exceeding 145% of regulated charge current. The high-side gate drive turns off when the overcurrent is detected, and automatically resumes when the current falls below the overcurrent threshold.

Thermal Shutdown Protection

The QFN package has low thermal impedance, providing good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As an added level of protection, the charger converter turns off and self-protects when the junction temperature exceeds the TSHUT threshold of 155°C. The charger stays off until the junction temperature falls below 135°C.

Status Register ($\overline{\text{ACGOOD}}$, $\overline{\text{DPMDET}}$ Pins)

Two status outputs are available, and both require external pullup resistors to pull the pins to the system digital rail for a high level.

$\overline{\text{ACGOOD}}$ goes low when ACDET is above 2.4 V and the 700-ms delay time is over. It indicates that the adapter voltage is high enough.

The $\overline{\text{DPMDET}}$ open-drain output goes low (after a 10-ms delay) when the DPM loop is active to reduce the battery charge current.

Temperature Qualification

The controller continuously monitors the battery temperature by measuring the voltage between the TS pin and AGND. In a typical application, a negative-temperature-coefficient thermistor (NTC) and an external voltage divider develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. If the battery temperature is outside of this range, the controller suspends charging and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. During the charge cycle, the battery temperature must be within the V_{LTF} to V_{TCO} thresholds. If the battery temperature is outside this range, the controller suspends charging and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. The controller suspends charging by turning off the PWM charge FETs. The V_{TSDET} voltage threshold is used to detect whether a battery is connected. Figure 32 summarizes the operation.

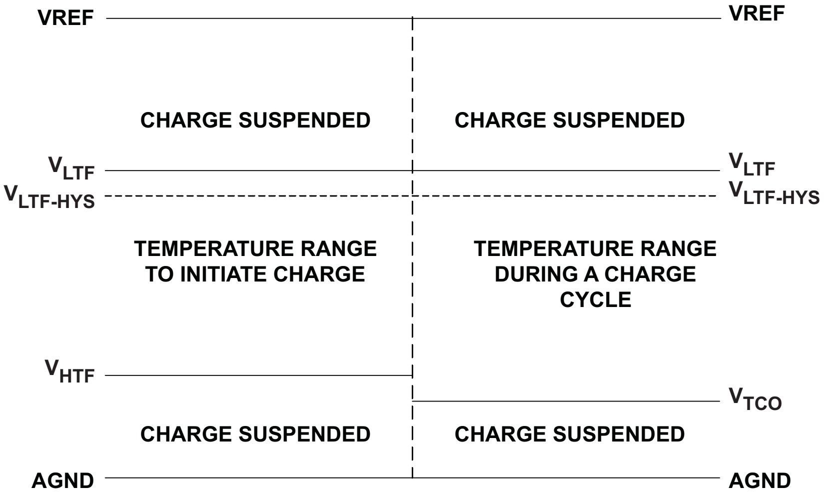


Figure 32. TS, Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor on the battery pack, as shown in Figure 33, the value RT1 and RT2 can be determined by using the following equations:

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

and

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{HTF}} \right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{HTF}} - 1 \right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1 \right)} \quad (5)$$

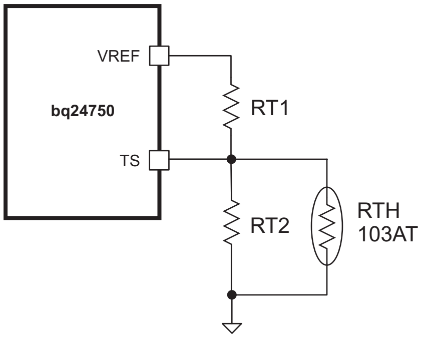


Figure 33. TS Resistor Network

Input Overpower Protection (ACOP)

The ACOC/ACOP circuit provides a reliable layer of safety protection that can complement other safety measues. ACOC/ACOP helps to protect from input current surge due to various conditions including:

- Adapter insertion and system selector connecting adapter to system where system capacitors need to charge
- Learn mode exit when adapter is reconnected to the system; system load over-current surge
- System shorted to ground
- Battery shorted to ground
- Phase shorted to ground
- High-side FET shorted from drain to source (SYSTEM shorted to PH)
- BATFET shorted from drain to source (SYSTEM shorted to BAT)

Several examples of the circuit protecting from these fault conditions are shown below.

For designs using the selector functions, an input overcurrent (ACOC) and input over-power protection function (ACOP) is provided. The threshold is set by an external capacitor from the ACOP pin to AGND. After the adapter is detected (ACDET pin > 2.4V), there is a 700-ms delay before $\overline{\text{ACGOOD}}$ is asserted low, and Q3 (BATFET) is turned-off. Then Q1/Q2 (ACFET) are turned on by the $\overline{\text{ACDRV}}$ pin. When Q1/Q2 (ACFET) are turned on, the ACFET allows operation in linear-regulation mode to limit the maximum input current, ACOC, to a safe level. The ACOC current limit is 1.5 times the programmed DPM input current limit set by the ratio of SRSET/VDAC. The maximum allowable current limit is 100 mV across ACP – ACN (10 A for a 10-mΩ sense resistor).

The first 2 ms after the $\overline{\text{ACDRV}}$ signal begins to turn on, ACOC may limit the current; but the controller is not allowed to latch off in order to allow a reasonable time for the sytem voltage to rise.

After 2 ms, ACOP is enabled. ACOP allows the ACFET to latch off before the ACFET can be damaged by excessive thermal dissipation. The controller only latches if the ACOP pin voltage exceeds 2 V with respect to AGND. In ACOP, a current source begins to charge the ACOP capacitor when the input current is being limited by ACOC. This current source is proportional to the voltage across the source-drain of the ACFET ($V_{PVCC-ACP}$) by an 18-µA/V ratio. This dependency allows faster capacitor charging if the voltage is larger (more power dissipation). It allows the time to be programmed by the ACOP capacitor selected. If the controller is not limiting current, a fixed 5-µA sink current into the ACOP pin to discharge the ACOP capacitor. This charge and discharge effect depends on whether there is a current-limit condition, and has a memory effect that averages the power over time, protecting the system from potentially hazardous repetitive faults. Whenever the ACOP threshold is exceeded, the charge is disabled and the adapter is disconnected from the system to protect the ACFET and the whole system. If the ACFET is latched off, the BATFET is turned on to connect the battery to the system.

The capacitor provides a predictable time to limit the power dissipation of the ACFET. Since the input current is constant at the ACOC current limit, the designer can calculate the power dissipation on the ACFET.

The ACOC current Limit threshold is equal to $\text{Power} = I_d \cdot V_{sd} = I_{ACOC\_LIM} \cdot V(PVCC - ACP)$.

The time it takes to charge to 2V can be calculated from

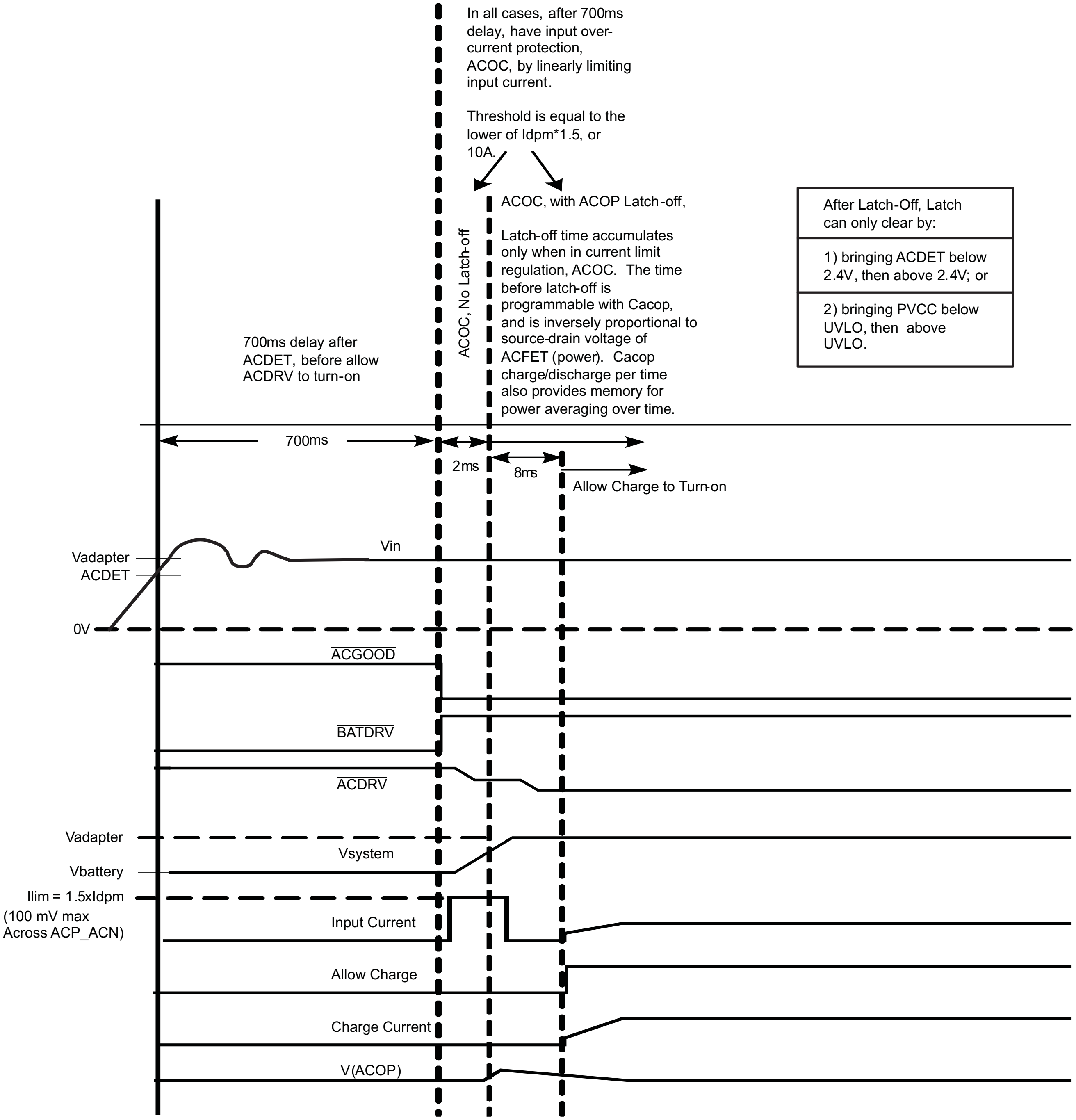
$$\Delta t = \frac{C_{ACOP} \cdot \Delta V_{ACOP}}{i_{ACOP}} = \frac{C_{ACOP} \cdot 2V}{18_{\mu A/V} \cdot V(PVCC - ACP)} \quad (6)$$

An ACOP fault latch off can only be cleared by bringing the ACDET pin voltage below 2.4 V, then above 2.4 V (i.e. remove adapter and reinsert), or by reducing the PVCC voltage below the UVLO threshold and raising it.

Conditions for ACOP Latch Off:

702ms after ACDET (adapter detected), and

a. ACOP voltage > 2V. The ACOP pin charges the ceramic capacitor when in an ACOC current-limit condition. The ACOP pin discharges the capacitor when not in ACOC current-limit.
b. ACOP protects from a single-pulse ACOC condition depending on duration and source-drain voltage of ACFET. Larger voltage across ACFET creates more power dissipation so latch-off protection occurs faster, by increasing the current source out of ACOP pin.
c. Memory effect (capacitor charging and discharging) allows protection from repititive ACOC conditions, depending on duration and frequency. (Figure 35)
d. In short conditions when the system is shorted to ground (ACN < 2.4 V)



A. ACFET overpower protection; initial current limit allows safe soft-start without system voltage droop.

Figure 34. ACOC Protection During Adapter Insertion

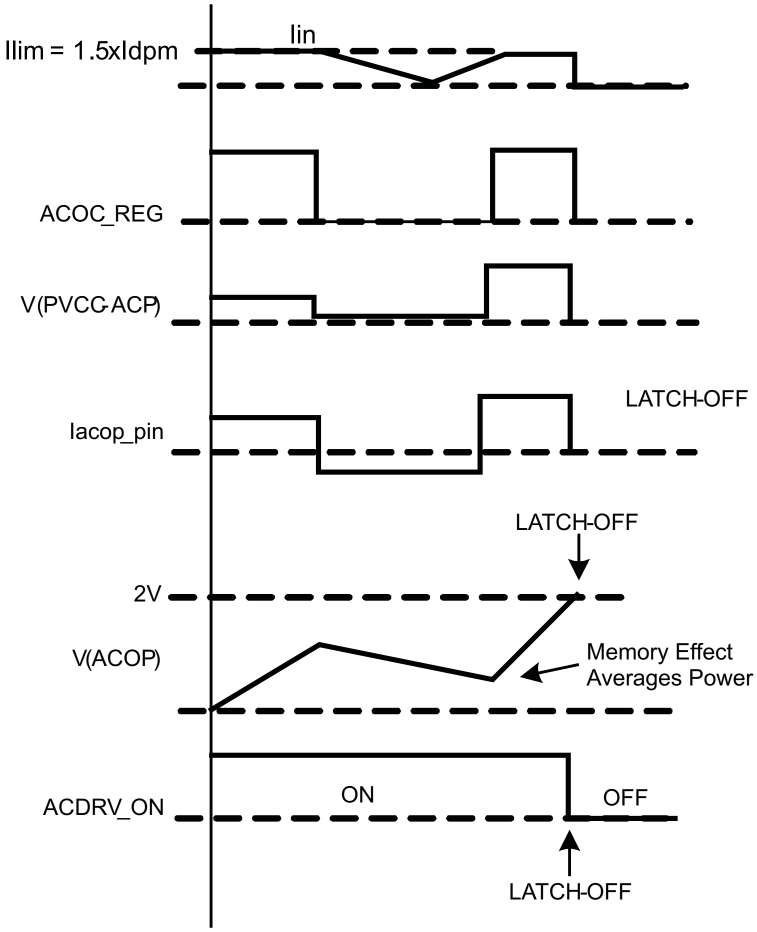


Figure 35. ACOC Protection and ACOP Latch Off with Memory Effect Example

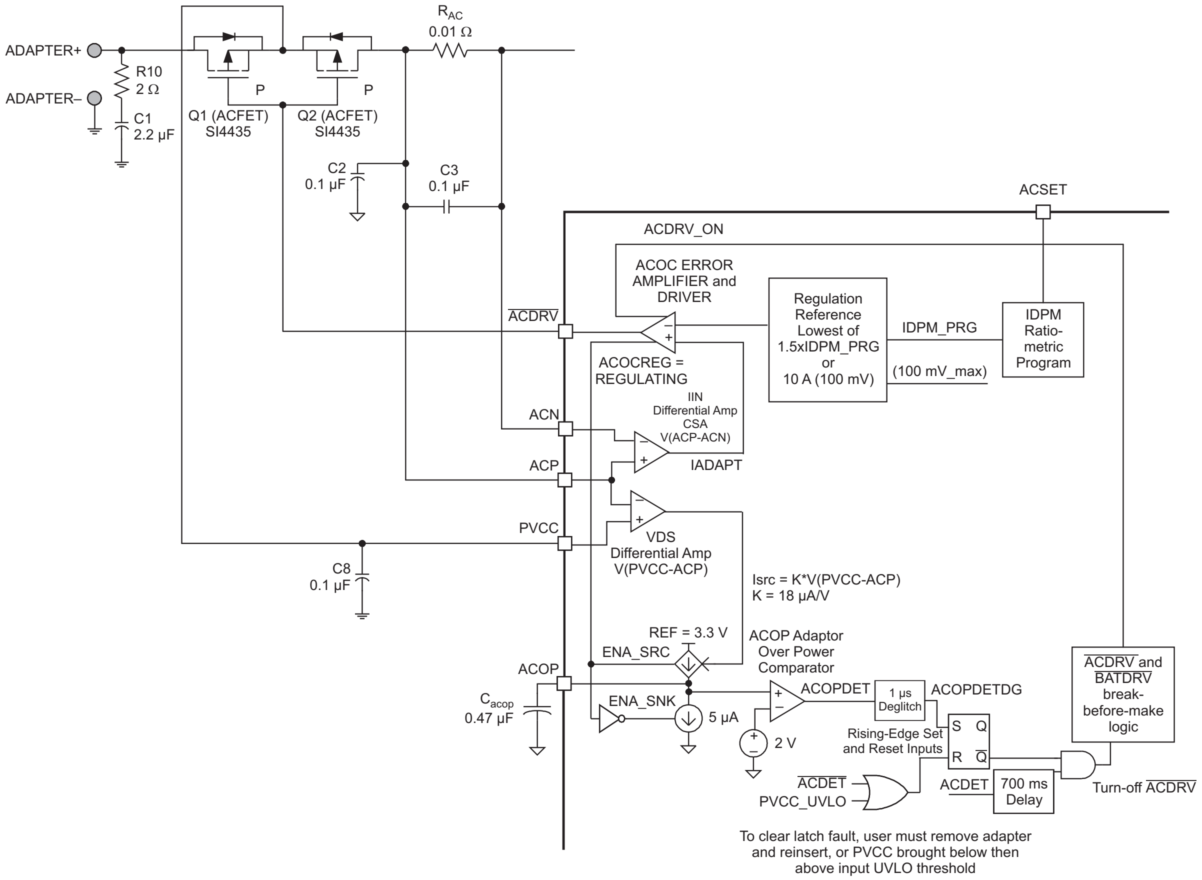


Figure 36. ACOC / ACOP Circuit Functional Block Diagram

Table 2. Component List for Typical System Circuit of Figure 1

PART DESIGNATOR	QTY	DESCRIPTION
Q1, Q2, Q3	3	P-channel MOSFET, –30 V, –6 A, SO-8, Vishay-Siliconix, Si4435
Q4, Q5	2	N-channel MOSFET, 30 V, 12.5 A, SO-8, Fairchild, FDS6680A
D1	1	Diode, Dual Schottky, 30 V, 200 mA, SOT23, Fairchild, BAT54C
R_{AC}, R_{SR}	2	Sense Resistor, 10 mΩ, 1%, 1 W, 2010, Vishay-Dale, WSL2010R0100F
L1	1	Inductor, 8.2 µH, 8.5 A, 24.8 mΩ, Vishay-Dale, IHLP5050CE-01
C1	1	Capacitor, Ceramic, 2.2 µF, 25 V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E225M
C6, C7, C11, C12	4	Capacitor, Ceramic, 10 µF, 35 V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E106M
C4, C10	2	Capacitor, Ceramic, 1 µF, 25 V, 10%, X7R, 2012, TDK, C2012X7R1E105K
C2, C3, C8, C9, C13, C14, C15	7	Capacitor, Ceramic, 0.1 µF, 50 V, 10%, X7R, 0805, Kemet, C0805C104K5RACTU
C5	1	Capacitor, Ceramic, 100 pF, 25 V, 10%, X7R, 0805, Kemet
C16	1	Capacitor, Ceramic, 0.47 µF, 25 V, 10%, X7R, 0805, Kemet
R5, R6	2	Resistor, Chip, 10 kΩ, 1/16 W, 5%, 0402
R1	1	Resistor, Chip, 432 kΩ, 1/16 W, 1%, 0402
R2	1	Resistor, Chip, 66.5 kΩ, 1/16 W, 1%, 0402
R3	1	Resistor, Chip, 5.6 kΩ, 1/16 W, 1%, 0402
R4	1	Resistor, Chip, 118 kΩ, 1/16 W, 1%, 0402
R10	1	Resistor, Chip, 2 Ω, 1 W, 5%, 2010

APPLICATION INFORMATION

Input Capacitance Calculation

During the adapter hot plug-in, the $\overline{\text{ACDRV}}$ has not been enabled. The AC switch is off and the simplified equivalent circuit of the input is shown in Figure 37.

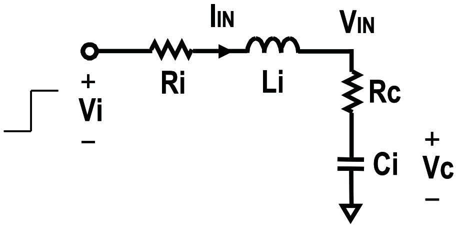


Figure 37. Simplified Equivalent Circuit During Adapter Insertion

The voltage on the input capacitor(s) is given by:

$$V_{IN}(t) = I_{IN}(t) \times R_C + V_{Ci(t)} = V_i e^{\frac{R_i}{2L_i}t}\left[\frac{R_i - R_C}{\omega L_i}\sin\omega t + \cos\omega t\right] \tag{7}$$

in which,

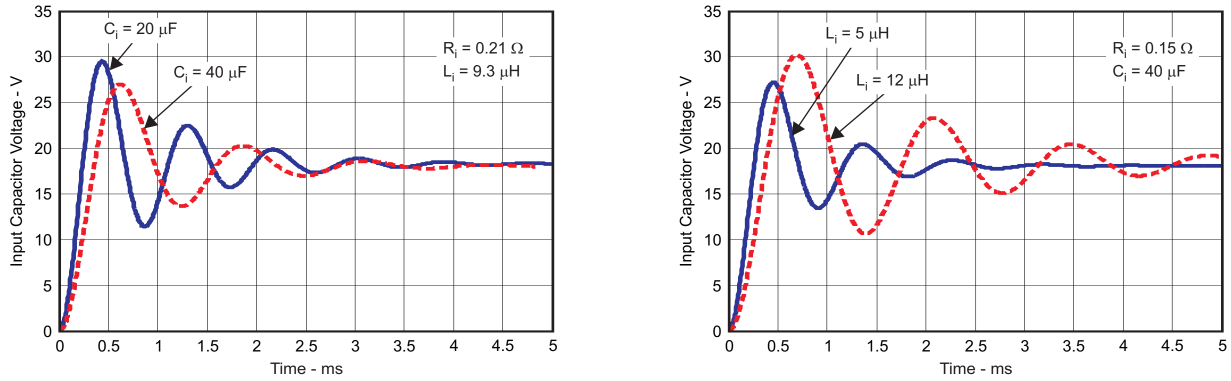
$$R_t = R_i + R_C \quad \omega = \sqrt{\frac{1}{L_iC_i} - \left(\frac{R_t}{2L_i}\right)^2} \quad I_{IN}(t) = \frac{V_i}{\omega L_i} e^{\frac{R_i}{2L_i}t} \sin\omega t \tag{8}$$

$$V_{Ci}(t) = V_i - V_i e^{\frac{R_t}{2L_i}t}\left(\frac{R_t}{2\omega L_i}\sin\omega t + \cos\omega t\right) \tag{9}$$

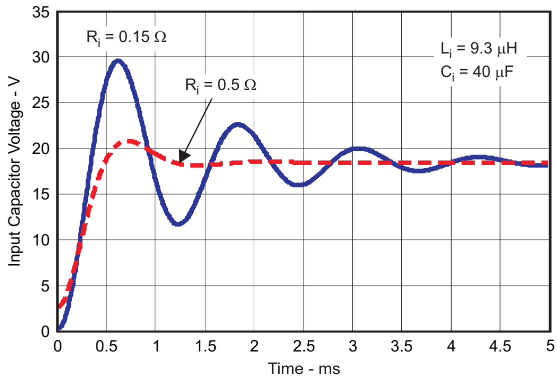
The damping conditions is:

$$R_i + R_C > 2\sqrt{\frac{L}{C}} \tag{10}$$

Figure 38 (a) demonstrates a higher Ci helps dampen the voltage spike. Figure 38 (b) demonstrates the effect of the input stray inductance Li upon the input voltage spike. Figure 38 (c) shows how increased resistance helps to suppress the input voltage spike.



(a) V_c with various C_i values **(b) V_c with various L_i values**

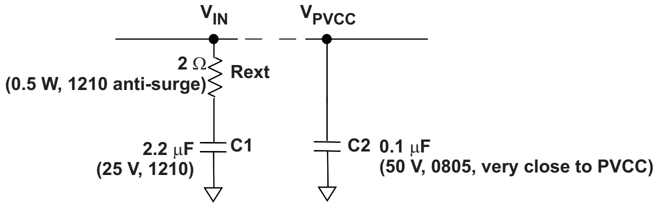


(c) V_c with various R_i values

Figure 38. Parametric Study Of The Input Voltage

As shown in Figure 38, minimizing the input stray inductance, increasing the input capacitance, and adding resistance (including using higher ESR capacitors) helps suppress the input voltage spike. However, a user often cannot control input stray inductance and increasing capacitance can increase costs. Therefore, the most efficient and cost-effective approach is to add an external resistor.

Figure 39 depicts the recommended input filter design. The measured input voltage and current waveforms are shown in Figure 40. The input voltage spike has been well damped by adding a 2Ω resistor, while keeping the capacitance low.



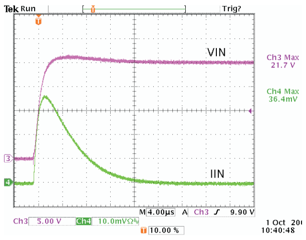


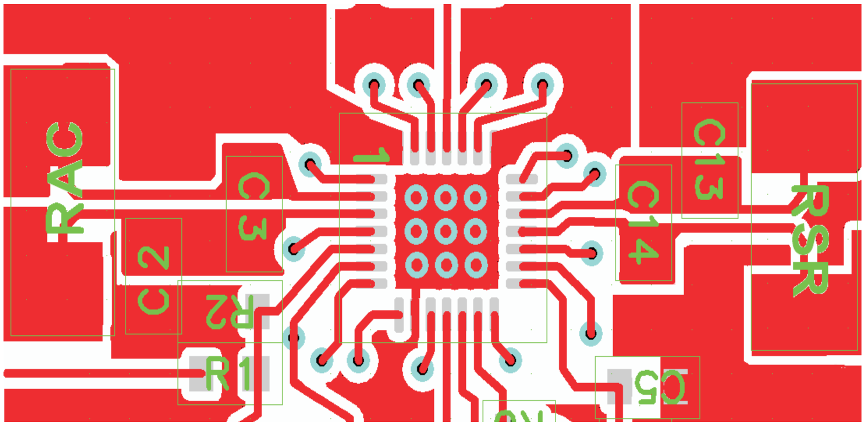
Figure 39. Recommended Input Filter Design **Figure 40. Adapter DC Side Hot Plug-in Test Waveforms**

PCB Layout Design Guideline

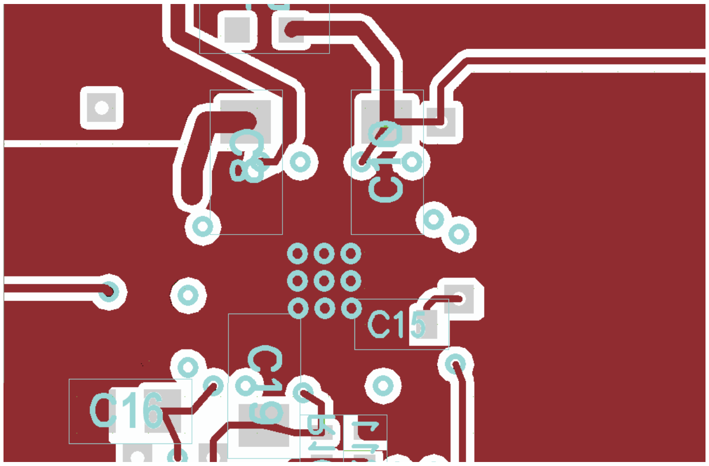
1. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
2. The control stage and the power stage should be routed separately. At each layer, the signal ground and the power ground are connected only at the power pad.
3. The AC current-sense resistor must be connected to ACP (pin 3) and ACN (pin 2) with a Kelvin contact. The area of this loop must be minimized. An additional 0.1μF decoupling capacitor for ACN is required to further reduce noise. The decoupling capacitors for these pins should be placed as close to the IC as possible.
4. The charge-current sense resistor must be connected to SRP (pin 19), SRN (pin 18) with a Kelvin contact. The area of this loop must be minimized. An additional 0.1μF decoupling capacitor for SRN is required to further reduce noise. The decoupling capacitors for these pins should be placed as close to the IC as possible.
5. Decoupling capacitors for PVCC (pin 28), VREF (pin 10), REGN (pin 24) should be placed underneath the IC (on the bottom layer) with the interconnections to the IC as short as possible.
6. Decoupling capacitors for BAT (pin 17), IADAPT (pin 15) must be placed close to the corresponding IC pins with the interconnections to the IC as short as possible.
7. Decoupling capacitor CX for the charger input must be placed very close to the Q4 drain and Q5 source.

Figure 41 shows the recommended component placement with trace and via locations.

For the QFN information, please refer to the following links: SCBA017 and SLUA271



(a) Top Layer



(b) Bottom Layer

Figure 41. Layout Example

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24750RHDR	NRND	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ 24750	
BQ24750RHDT	NRND	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ 24750	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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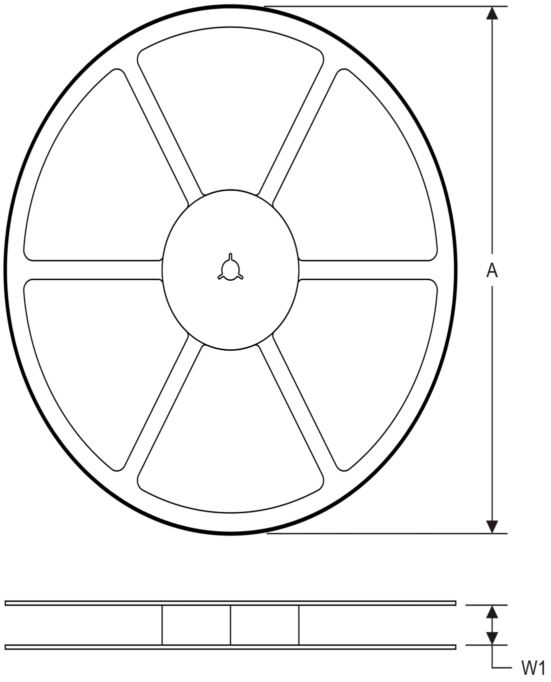
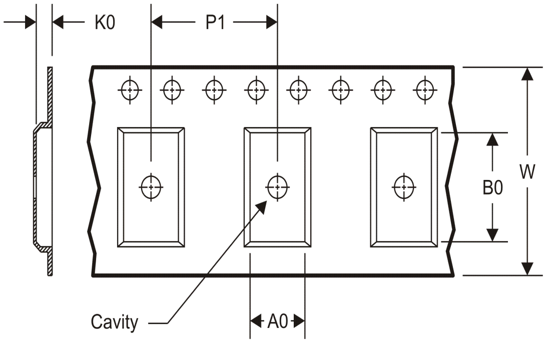
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



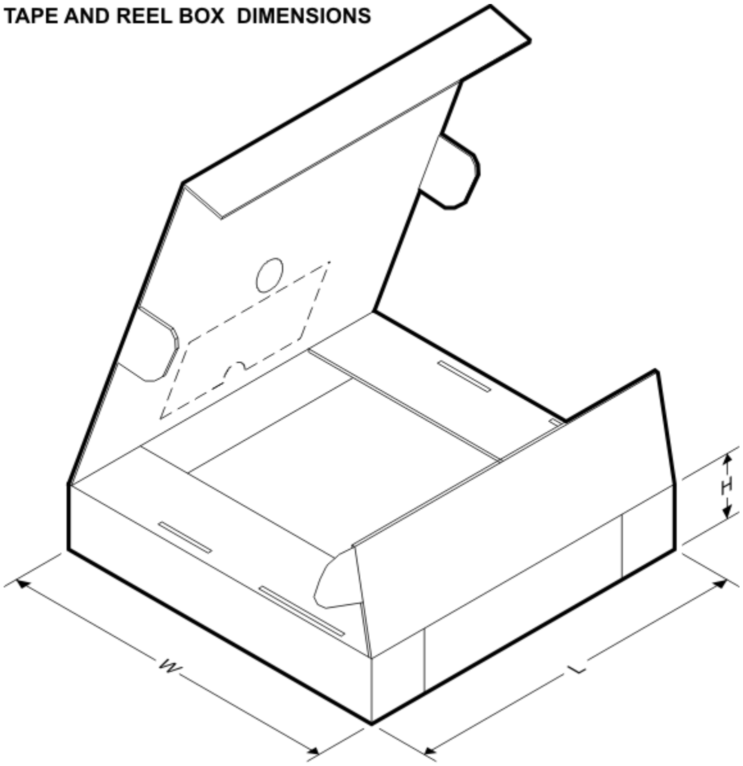
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24750RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24750RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24750RHDR	VQFN	RHD	28	3000	367.0	367.0	35.0
BQ24750RHDT	VQFN	RHD	28	250	210.0	185.0	35.0

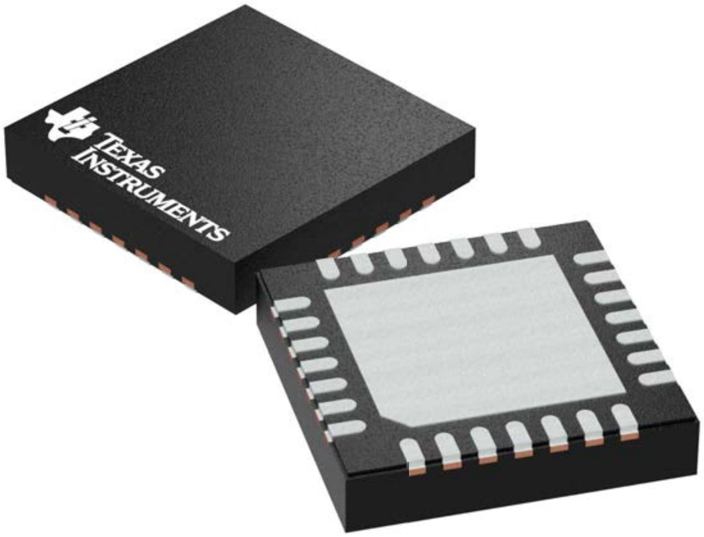
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

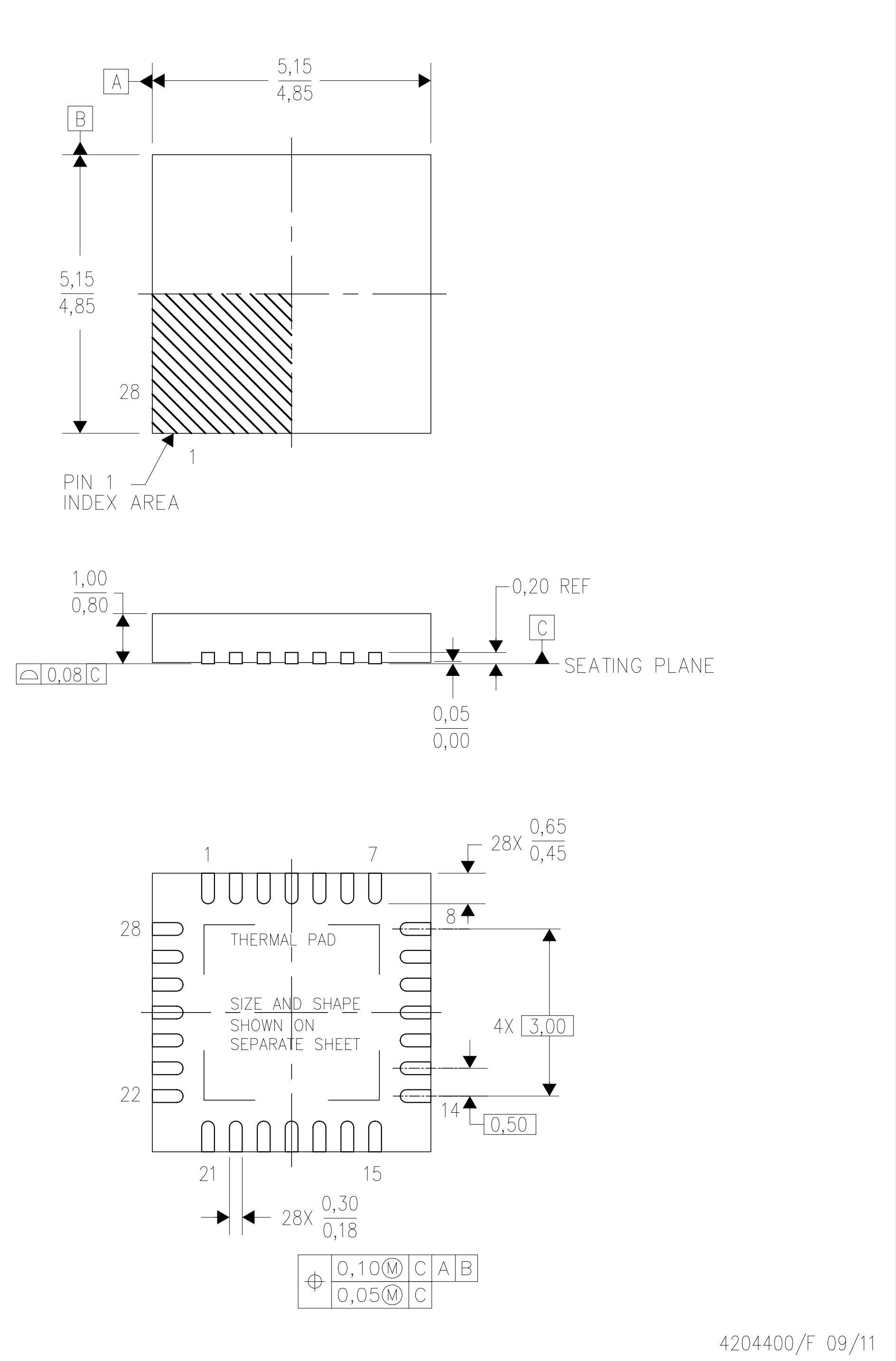
5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RHD (S-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

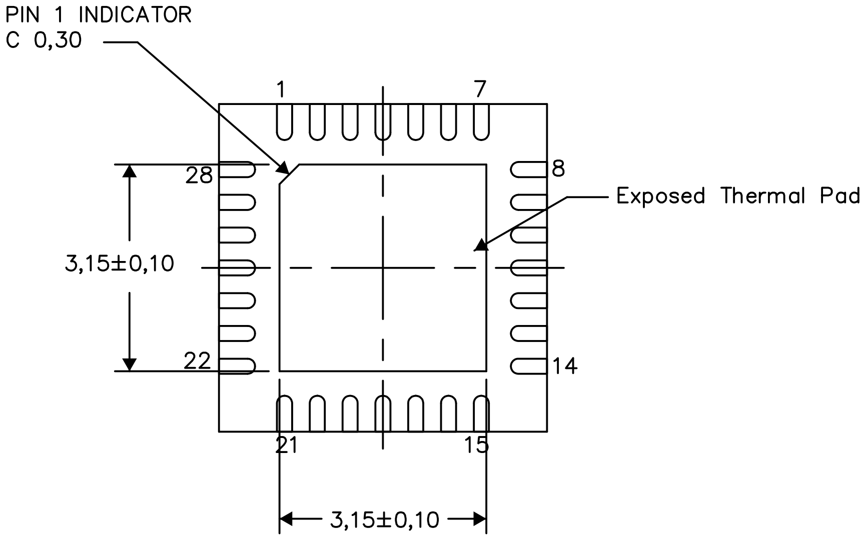
RHD (S-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



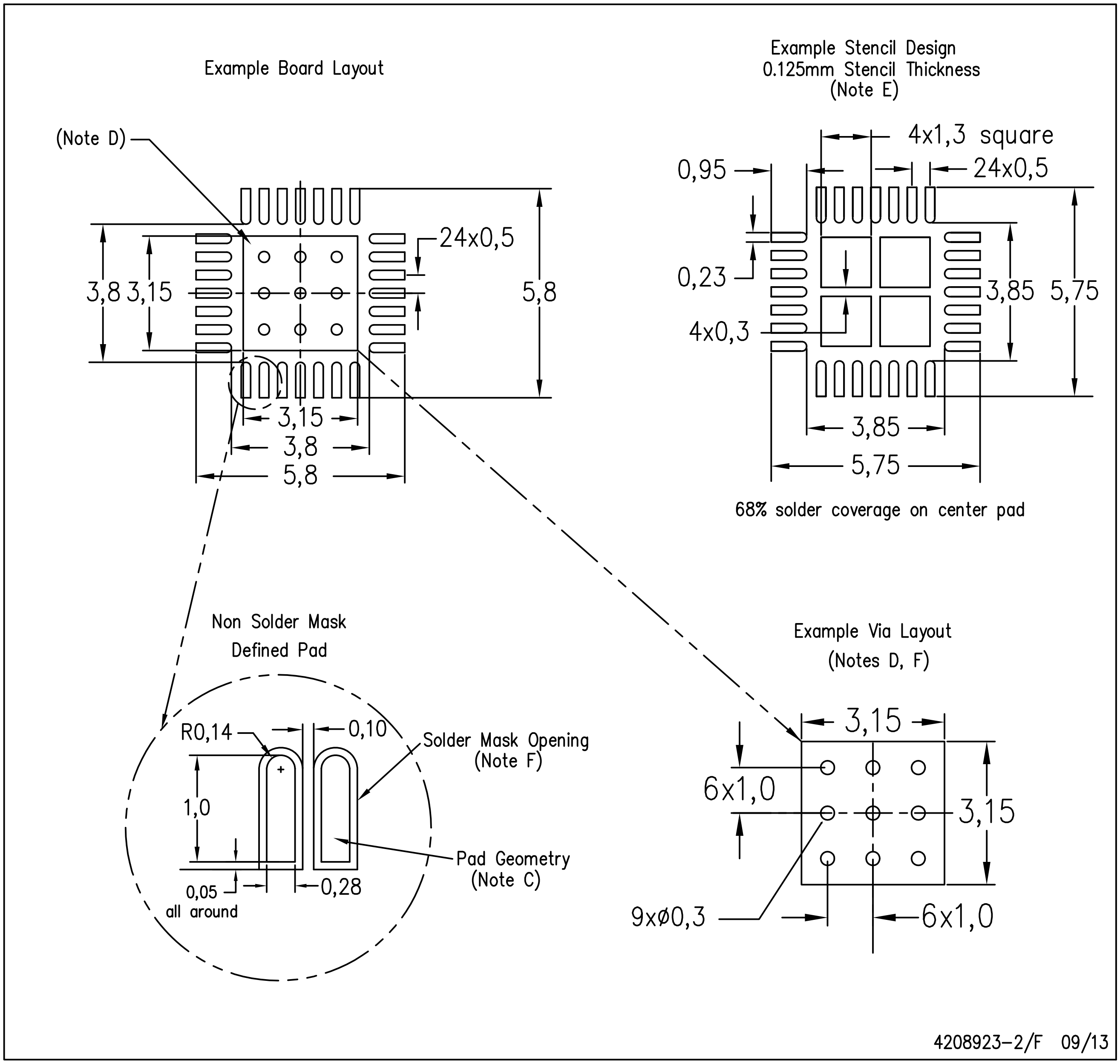
Bottom View

Exposed Thermal Pad Dimensions

4206358-2/L 05/15

NOTE: All linear dimensions are in millimeters

RHD (S-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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