THE DATASHEET OF

DAC121S101QCMK/NOPB

DAC121S101/-Q1 12-Bit Micro Power, RRO Digital-to-Analog Converter

1 Features

- DAC121S101-Q1 is AEC-Q100 Grade 1 Qualified and is Manufactured on an Automotive Grade Flow.
- Ensured Monotonicity
- Low Power Operation
- Rail-to-Rail Voltage Output
- Power-on Reset to Zero Volts Output
- Wide Temperature Range of −40°C to +125°C
- Wide Power Supply Range of 2.7 V to 5.5 V
- Small Packages
- Power Down Feature
- Key Specifications
  - 12-Bit Resolution
  - DNL -0.15, +0.25 LSB (Typical)
  - 8-µs Output Settling Time (Typical)
  - 4-mV Zero Code Error (Typical)
  - Full-Scale Error at −0.06 %FS (Typical)
  - 0.64-mW (3.6-V) / 1.43-mW (5.5-V) Normal Mode Power Consumption (Typical)
  - 0.14-µW (3.6-V) / 0.39-µW (5.5-V) Power-Down Mode (Typical)

2 Applications

- Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources
- Programmable Attenuators
- Automotive

3 Description

The DAC121S101 device is a full-featured, general-purpose, 12-bit voltage-output digital-to-analog converter (DAC) that can operate from a single 2.7-V to 5.5-V supply and consumes just 177 µA of current at 3.6 V. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 30 MHz over the specified supply voltage range and is compatible with standard SPI™, QSPI, MICROWIRE and DSP interfaces. Competitive devices are limited to 20-MHz clock rates at supply voltages in the 2.7 V to 3.6 V range.

The supply voltage for the DAC121S101 serves as its voltage reference, providing the widest possible output dynamic range. A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a microWatt.

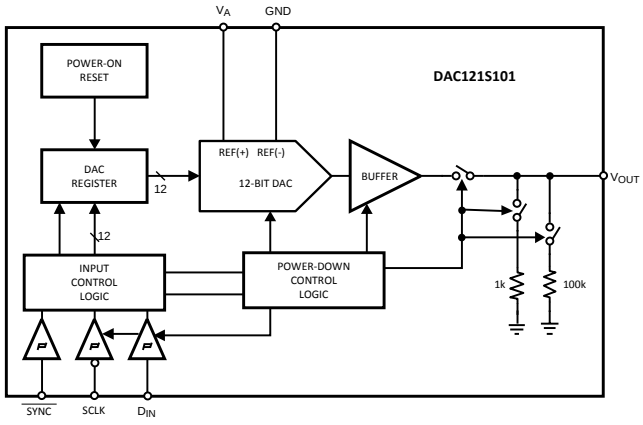
The low power consumption and small packages of the DAC121S101 make it an excellent choice for use in battery operated equipment.

Device Information(1)

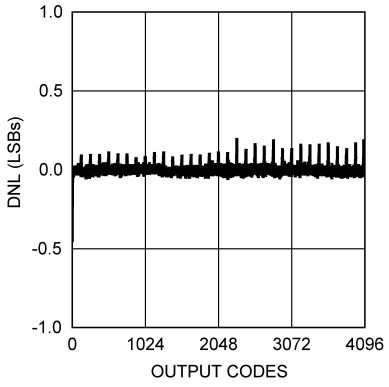
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC121S101	SOT (6)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
DAC121S101-Q1	SOT (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



DNL vs. Output Code



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (March 2013) to Revision J — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision H (February 2010) to Revision I — **Page**

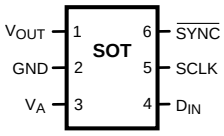
- Changed layout of National Data Sheet to TI format ... 25

5 Description continued

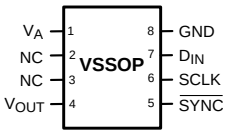
The DAC121S101 is a direct replacement for the AD5320 and the DAC7512 and is one of a family of pin compatible DACs, including the 8-bit DAC081S101 and the 10-bit DAC101S101. The DAC121S101 operates over the extended industrial temperature range of −40°C to +105°C while the DAC121S101-Q1 operates over the Grade 1 automotive temperature range of −40°C to +125°C. The DAC121S101 is available in a 6-lead SOT and an 8-lead VSSOP and the DAC121S101-Q1 is available in the 6-lead SOT only.

6 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



DAC121S101 (Only) DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT NO.	VSSOP NO.		
D_{IN}	4	7	Input	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
GND	2	8	—	Ground reference for all on-chip circuitry.
NC	—	2	—	No Connect. There is no internal connection to these pins.
		3		
SCLK	5	6	Input	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
$\overline{SYNC}$	6	5	Input	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{SYNC}$ is brought high before the 16th clock, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
V_A	3	1	—	Power supply and Reference input. Should be decoupled to GND.
V_{OUT}	1	4	Output	DAC Analog Output Voltage.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
Supply Voltage, V_A		6.5	V
Voltage on any Input Pin	−0.3	(V_A + 0.3)	V
Input Current at Any Pin (3)		10	mA
Package Input Current (3)		20	mA
Power Consumption at T_A = 25°C		See (4)	
Soldering Temperature, Infrared, 10 Seconds (5)		235	°C
Storage Temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified
(3) When the input voltage at any pin exceeds the power supplies (that is, less than GND, or greater than V_A), the current at that pin must be limited to 10 mA. The 20-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(4) The absolute maximum junction temperature (T_{JMAX}) for this device is 150°C. The maximum allowable power dissipation is dictated by T_{JMAX}, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions must always be avoided.
(5) See the section entitled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for methods of soldering surface mount devices.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Machine Model	±250	

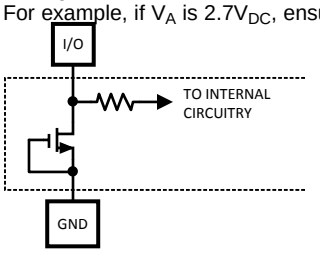
(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
Operating Temperature Range	DAC121S101	−40	T_A	105	°C
	DAC121S101-Q1	−40	T_A	125	°C
Supply Voltage, V_A		2.7		5.5	V
Any Input Voltage(3)		−0.1		(V_A + 0.1)	V
Output Load		0		1500	pF
SCLK Frequency				30	MHz

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified
(3) The analog inputs are protected as shown below. Input voltage magnitudes up to V_A + 300 mV or to 300 mV below GND will not damage this device. However, errors in the conversion result can occur if any input goes above V_A or below GND by more than 100 mV. For example, if V_A is 2.7V_{DC}, ensure that −100mV ≤ input voltages ≤2.8V_{DC} to ensure accurate conversions.



7.4 Thermal Information

THERMAL METRIC(1)		DAC121S101, DAC121S101-Q1		UNIT
		DGK (VSSOP)	DDC (SOT)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	240	250	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(1)	MAX(1)	UNIT
STATIC PERFORMANCE							
	Resolution	$T_{MIN} \le T_A \le T_{MAX}$		12			Bits
	Monotonicity	$T_{MIN} \le T_A \le T_{MAX}$		12			Bits
INL	Integral Non-Linearity	Over Decimal codes 48 to 4047	T_A = 25°C			±2.6	LSB
			$T_{MIN} \le T_A \le T_{MAX}$			±8	
DNL	Differential Non-Linearity	V_A = 2.7 V to 5.5 V	T_A = 25°C	−0.15		+0.25	LSB
			$T_{MIN} \le T_A \le T_{MAX}$	−0.7		+1	LSB
		V_A = 4.5 V to 5.5 V (2)	T_A = 25°C			±0.11	LSB
			$T_{MIN} \le T_A \le T_{MAX}$			±0.5	
ZE	Zero Code Error	I_{OUT} = 0	T_A = 25°C			+4	mV
			$T_{MIN} \le T_A \le T_{MAX}$			+15	
FSE	Full-Scale Error	I_{OUT} = 0	T_A = 25°C			−0.06	%FSR
			$T_{MIN} \le T_A \le T_{MAX}$			−1	
GE	Gain Error	All ones Loaded to DAC register	T_A = 25°C		−0.1		%FSR
			$T_{MIN} \le T_A \le T_{MAX}$		±1		
ZCED	Zero Code Error Drift				−20		µV/°C

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).
(2) This parameter is specified by design and/or characterization and is not tested in production.

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS			MIN(1)	TYP(1)	MAX(1)	UNIT
TC GE	Gain Error Tempco	V_A = 3 V				−0.7		ppm/°C
		V_A = 5 V				−1		ppm/°C
OUTPUT CHARACTERISTICS								
	Output Voltage Range(2)	$T_{MIN} \le T_A \le T_{MAX}$			0		V_A	V
ZCO	Zero Code Output	V_A = 3 V, I_{OUT} = 10 µA					1.8	mV
		V_A = 3 V, I_{OUT} = 100 µA					5	mV
		V_A = 5 V, I_{OUT} = 10 µA					3.7	mV
		V_A = 5 V, I_{OUT} = 100 µA					5.4	mV
FSO	Full Scale Output	V_A = 3 V, I_{OUT} = 10 µA					2.997	V
		V_A = 3 V, I_{OUT} = 100 µA					2.99	V
		V_A = 5 V, I_{OUT} = 10 µA					4.995	V
		V_A = 5 V, I_{OUT} = 100 µA					4.992	V
	Maximum Load Capacitance	R_L = ∞					1500	pF
		R_L = 2 kΩ					1500	pF
	DC Output Impedance						1.3	Ohm
I_{OS}	Output Short Circuit Current	V_A = 5 V, V_{OUT} = 0 V, Input code = FFFh					−63	mA
		V_A = 3 V, V_{OUT} = 0 V, Input code = FFFh					−50	mA
		V_A = 5 V, V_{OUT} = 5 V, Input code = 000h					74	mA
		V_A = 3 V, V_{OUT} = 3 V, Input code = 000h					53	mA
LOGIC INPUT								
I_{IN}	Input Current (2)	$T_{MIN} \le T_A \le T_{MAX}$					±1	µA
V_{IL}	Input Low Voltage (2)	V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$					0.8	V
		V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$					0.5	V
V_{IH}	Input High Voltage (2)	V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$			2.4			V
		V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$			2.1			V
C_{IN}	Input Capacitance (2)	$T_{MIN} \le T_A \le T_{MAX}$					3	pF
POWER REQUIREMENTS								
I_A	Supply Current (output unloaded)	Normal Mode f_{SCLK} = 30 MHz	V_A = 5.5 V	T_A = 25°C			260	µA
				$T_{MIN} \le T_A \le T_{MAX}$			312	
			V_A = 3.6 V	T_A = 25°C			177	µA
				$T_{MIN} \le T_A \le T_{MAX}$			217	
		Normal Mode f_{SCLK} = 20 MHz	V_A = 5.5 V	T_A = 25°C			224	µA
				$T_{MIN} \le T_A \le T_{MAX}$			279	
			V_A = 3.6 V	T_A = 25°C			158	µA
				$T_{MIN} \le T_A \le T_{MAX}$			197	
		Normal Mode f_{SCLK} = 0	V_A = 5.5 V				153	µA
			V_A = 3.6 V				118	µA
		All PD Modes, f_{SCLK} = 30 MHz	V_A = 5 V				84	µA
			V_A = 3 V				42	µA
		All PD Modes, f_{SCLK} = 20 MHz	V_A = 5 V				56	µA
			V_A = 3 V				28	µA
		All PD Modes, f_{SCLK} = 0 (2)	V_A = 5.5 V	T_A = 25°C			0.07	µA
				$T_{MIN} \le T_A \le T_{MAX}$			1	
			V_A = 3.6 V	T_A = 25°C			0.04	µA
				$T_{MIN} \le T_A \le T_{MAX}$			1	

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS			MIN(1)	TYP(1)	MAX(1)	UNIT
P_C	Power Consumption (output unloaded)	Normal Mode f_{SCLK} = 30 MHz	V_A = 5.5 V	T_A = 25°C			1.43	mW
				$T_{MIN} \le T_A \le T_{MAX}$			1.72	
			V_A = 3.6 V	T_A = 25°C			0.64	mW
				$T_{MIN} \le T_A \le T_{MAX}$			0.78	
		Normal Mode f_{SCLK} = 20 MHz	V_A = 5.5 V	T_A = 25°C			1.23	mW
				$T_{MIN} \le T_A \le T_{MAX}$			1.53	
			V_A = 3.6 V	T_A = 25°C			0.57	mW
				$T_{MIN} \le T_A \le T_{MAX}$			0.71	
		Normal Mode f_{SCLK} = 0	V_A = 5.5 V				0.84	µW
			V_A = 3.6 V				0.42	µW
		All PD Modes, f_{SCLK} = 30 MHz	V_A = 5 V				0.42	µW
			V_A = 3 V				0.13	µW
		All PD Modes, f_{SCLK} = 20 MHz	V_A = 5 V				0.28	µW
			V_A = 3 V				0.08	µW
		All PD Modes, f_{SCLK} = 0 (2)	V_A = 5.5 V	T_A = 25°C			0.39	µW
				$T_{MIN} \le T_A \le T_{MAX}$			5.5	
			V_A = 3.6 V	T_A = 25°C			0.14	µW
				$T_{MIN} \le T_A \le T_{MAX}$			3.6	
I_{OUT} / I_A	Power Efficiency	I_{LOAD} = 2 mA	V_A = 5 V			91%		
			V_A = 3 V			94%		

7.6 AC and Timing Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK Frequency	$T_{MIN} \le T_A \le T_{MAX}$					30	MHz
t_s	Output Voltage Settling Time (1)	400h to C00h code change, R_L = 2 kΩ	$C_L \le$ 200 pF	T_A = 25°C			8	µs
				$T_{MIN} \le T_A \le T_{MAX}$			10	
			C_L = 500 pF			12		µs
		00Fh to FF0h code change, R_L = 2 kΩ	$C_L \le$ 200 pF			8		µs
			C_L = 500 pF			12		µs
SR	Output Slew Rate					1		V/µs
	Glitch Impulse	Code change from 800h to 7FFh				12		nV-s
	Digital Feedthrough					0.5		nV-s
t_{WU}	Wake-Up Time	V_A = 5 V				6		µs
		V_A = 3 V				39		µs
$1/f_{SCLK}$	SCLK Cycle Time	$T_{MIN} \le T_A \le T_{MAX}$			33			ns
t_H	SCLK High time	T_A = 25°C			5			ns
		$T_{MIN} \le T_A \le T_{MAX}$			13			
t_L	SCLK Low Time	T_A = 25°C			5			ns
		$T_{MIN} \le T_A \le T_{MAX}$			13			
t_{SUCL}	Set-up Time $\overline{SYNC}$ to SCLK Rising Edge	T_A = 25°C			−15			ns
		$T_{MIN} \le T_A \le T_{MAX}$			0			
t_{SUD}	Data Set-up Time	T_A = 25°C			2.5			ns
		$T_{MIN} \le T_A \le T_{MAX}$			5			

(1) This parameter is specified by design and/or characterization and is not tested in production.

AC and Timing Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DHD}	Data Hold Time	T_A = 25°C		2.5			ns
		$T_{MIN} \le T_A \le T_{MAX}$		4.5			
t_{CS}	$\overline{SCLK}$ fall to rise of $\overline{SYNC}$	V_A = 5 V	T_A = 25°C	0			ns
			$T_{MIN} \le T_A \le T_{MAX}$	3			
		V_A = 3 V	T_A = 25°C	–2			ns
			$T_{MIN} \le T_A \le T_{MAX}$	1			
t_{SYNC}	$\overline{SYNC}$ High Time	2.7 ≤ V_A ≤ 3.6	T_A = 25°C	9			ns
			$T_{MIN} \le T_A \le T_{MAX}$	20			
		3.6 ≤ V_A ≤ 5.5	T_A = 25°C	5			ns
			$T_{MIN} \le T_A \le T_{MAX}$	10			

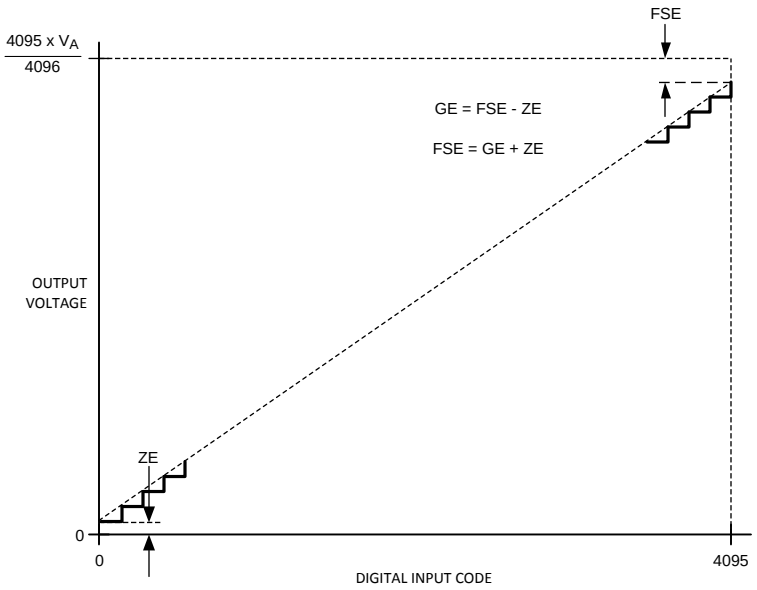


Figure 1. Input / Output Transfer Characteristic

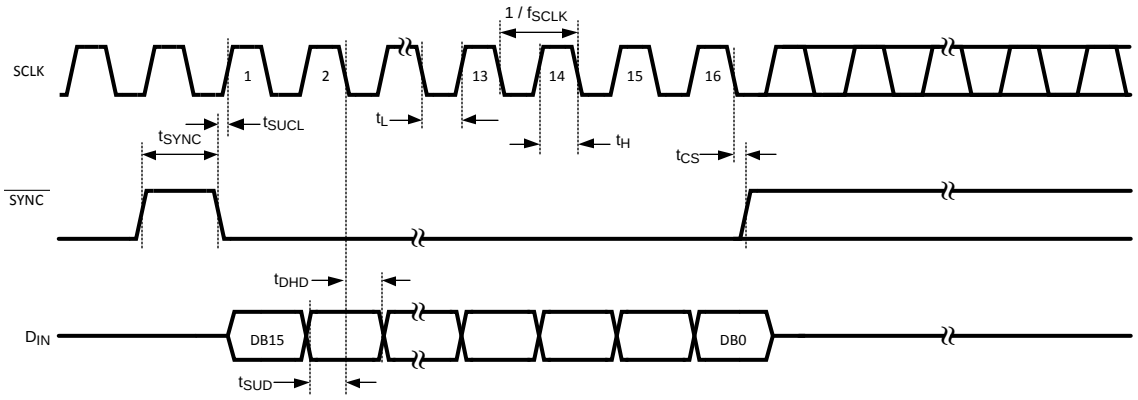


Figure 2. DAC121S101 Timing

7.7 Typical Characteristics

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 48 to 4047, unless otherwise stated

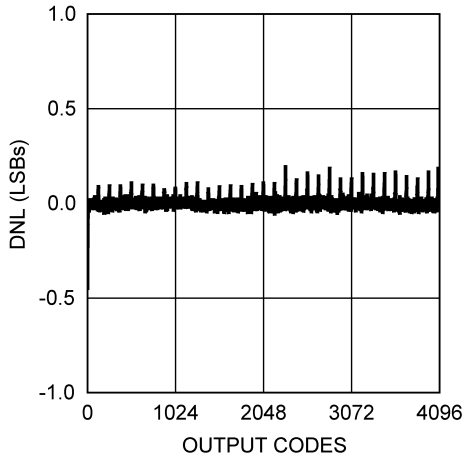


Figure 3. DNL at V_A = 3 V

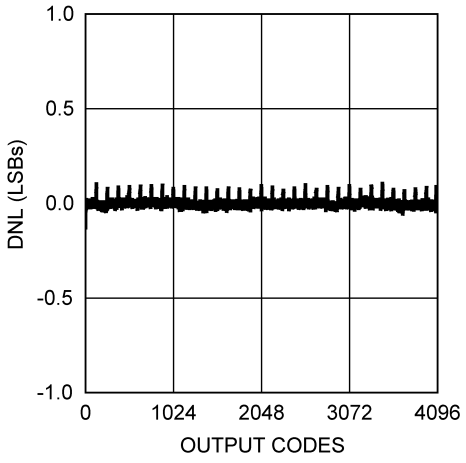


Figure 4. DNL at V_A = 5 V

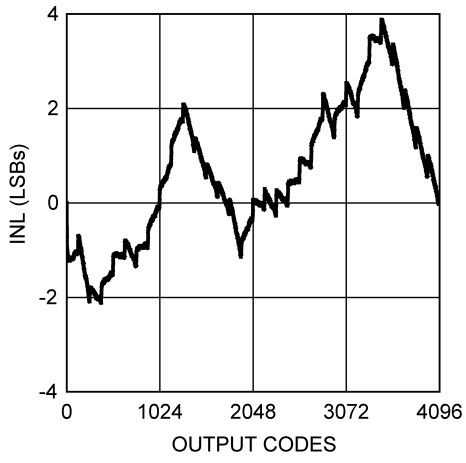


Figure 5. INL at V_A = 3 V

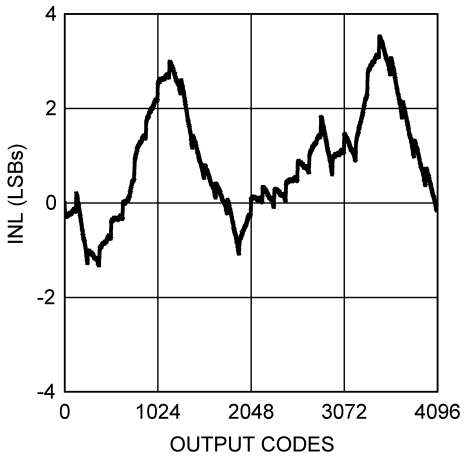


Figure 6. INL at V_A = 5 V

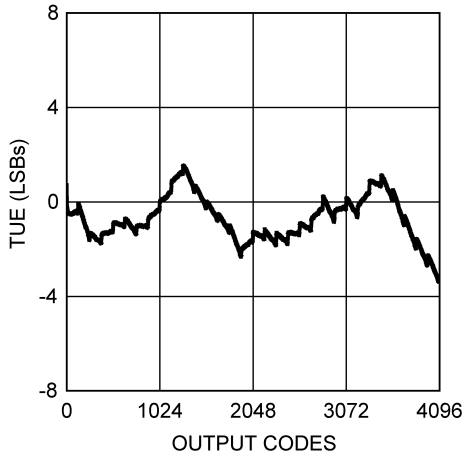


Figure 7. TUE at V_A = 3 V

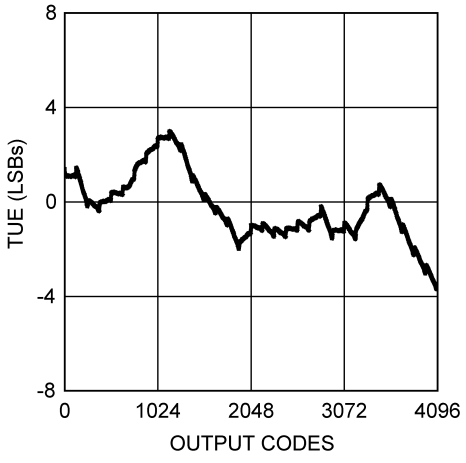


Figure 8. TUE at V_A = 5 V

Typical Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 48 to 4047, unless otherwise stated

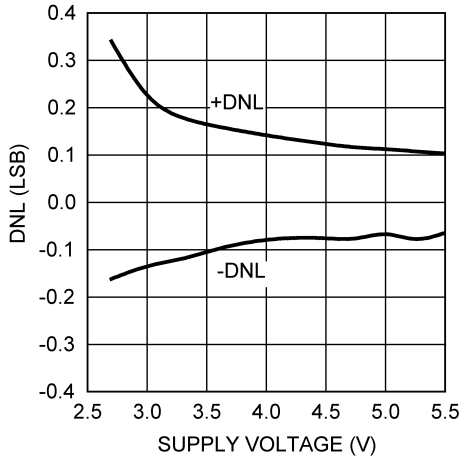


Figure 9. DNL vs. V_A

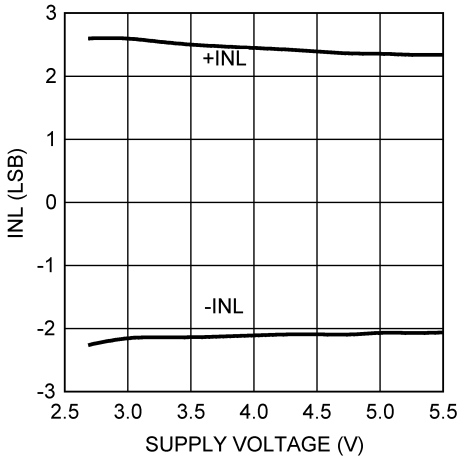


Figure 10. INL vs. V_A

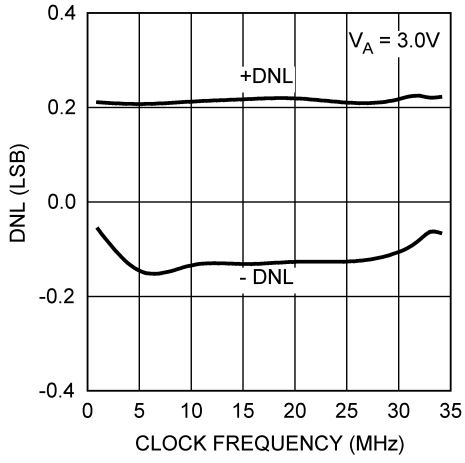


Figure 11. 3-V DNL vs. f_{SCLK}

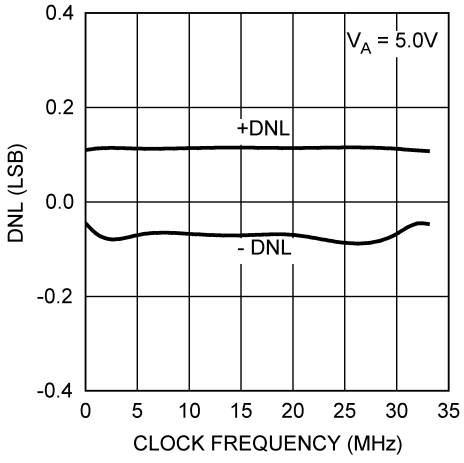


Figure 12. 5-V DNL vs. f_{SCLK}

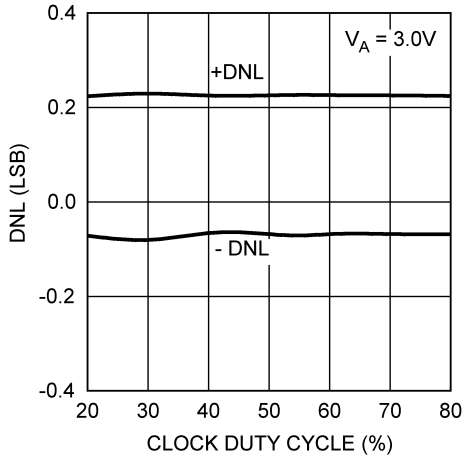


Figure 13. 3-V DNL vs. Clock Duty Cycle

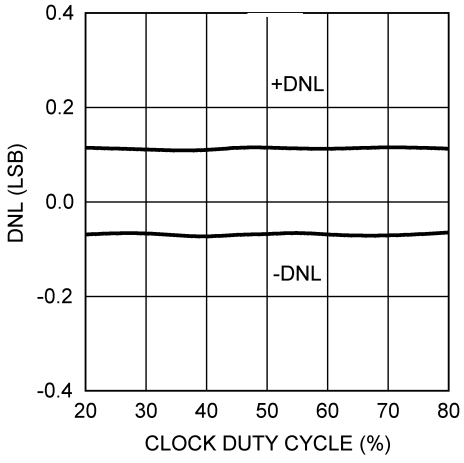


Figure 14. 5-V DNL vs. Clock Duty Cycle

Typical Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 48 to 4047, unless otherwise stated

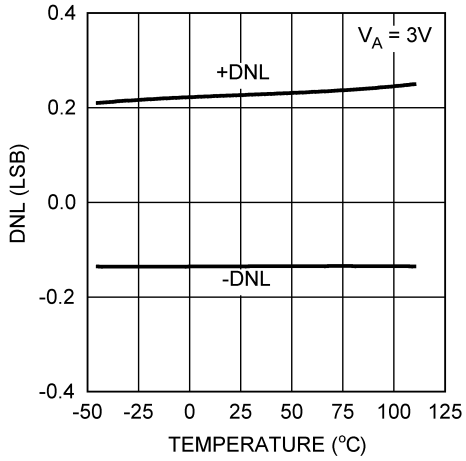


Figure 15. 3-V DNL vs. Temperature

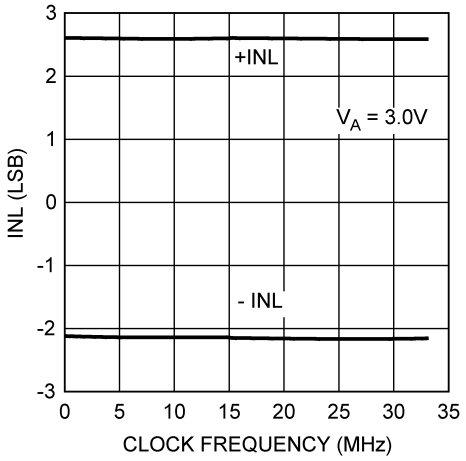


Figure 16. 3-V INL vs. f_{SCLK}

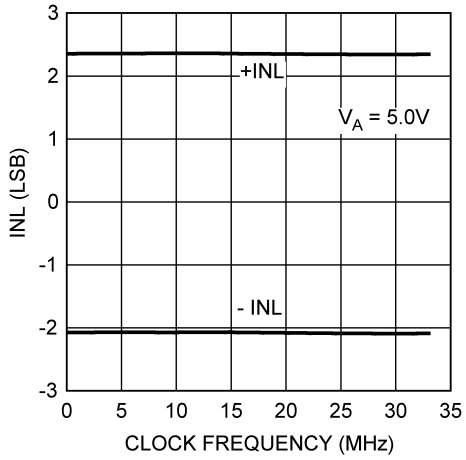


Figure 17. 5-V INL vs. f_{SCLK}

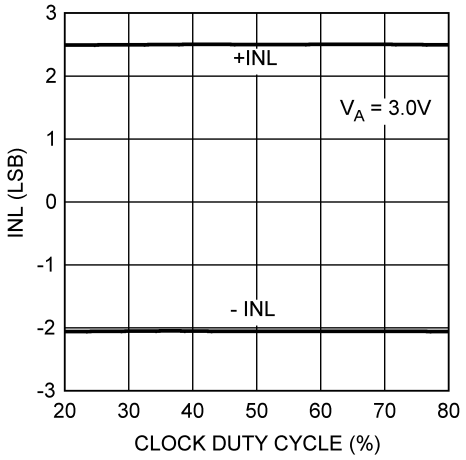


Figure 18. 3-V INL vs. Clock Duty Cycle

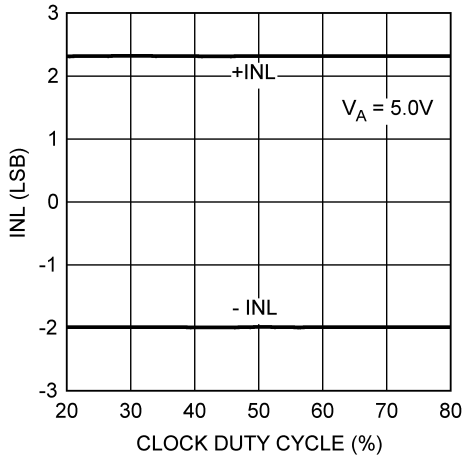


Figure 19. 5-V INL vs. Clock Duty Cycle

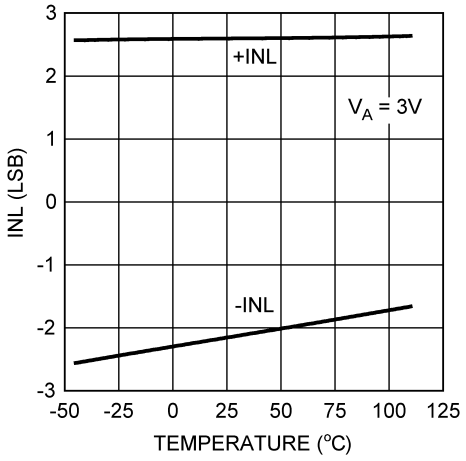


Figure 20. 3-V INL vs. Temperature

Typical Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 48 to 4047, unless otherwise stated

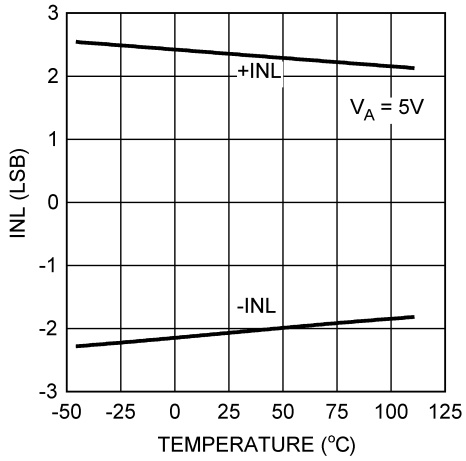


Figure 21. 5-V INL vs. Temperature

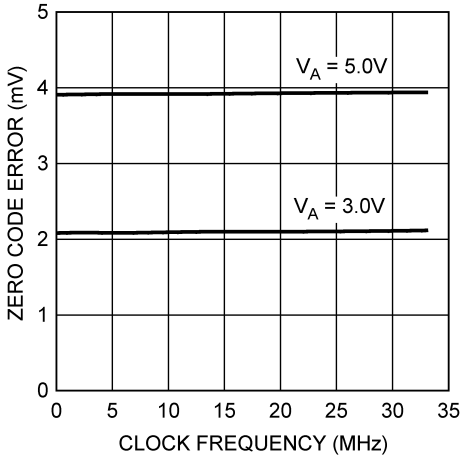


Figure 22. Zero Code Error vs. f_{SCLK}

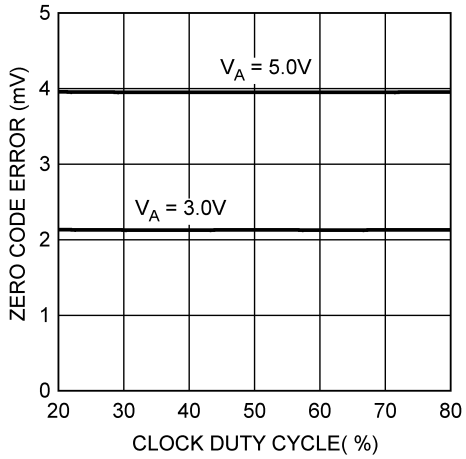


Figure 23. Zero Code Error vs. Clock Duty Cycle

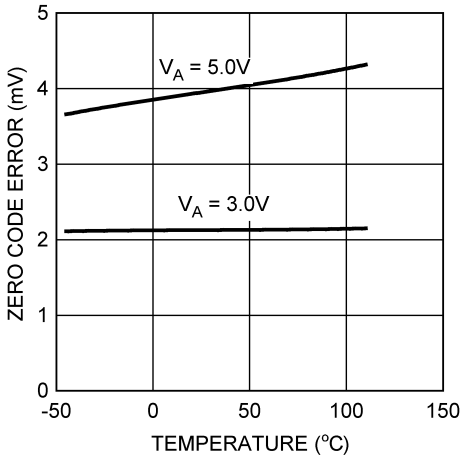


Figure 24. Zero Code Error vs. Temperature

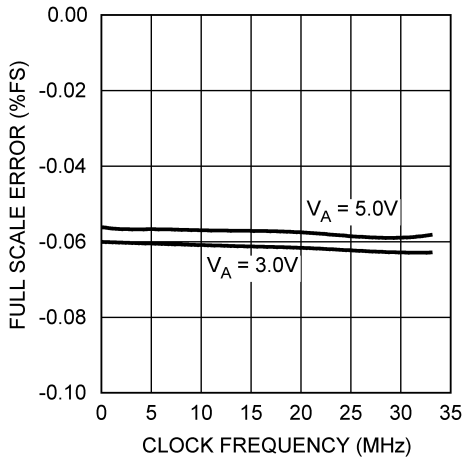


Figure 25. Full-Scale Error vs. f_{SCLK}

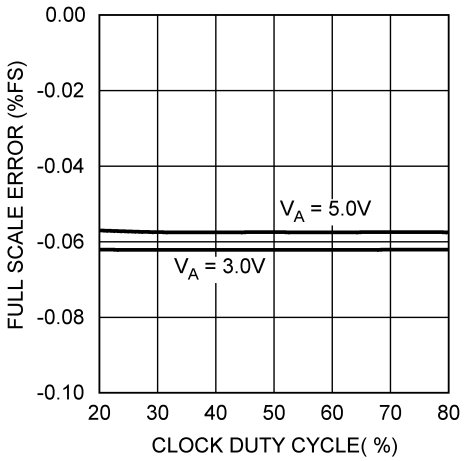


Figure 26. Full-Scale Error vs. Clock Duty Cycle

Typical Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 48 to 4047, unless otherwise stated

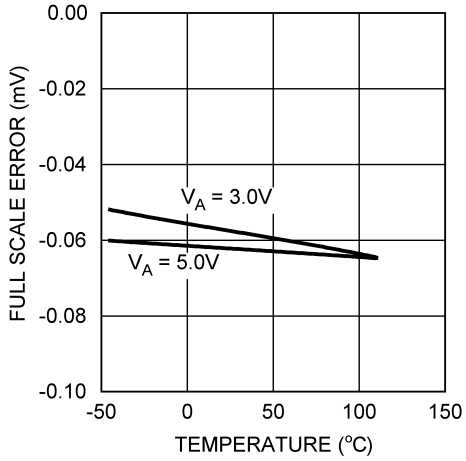


Figure 27. Full-Scale Error vs. Temperature

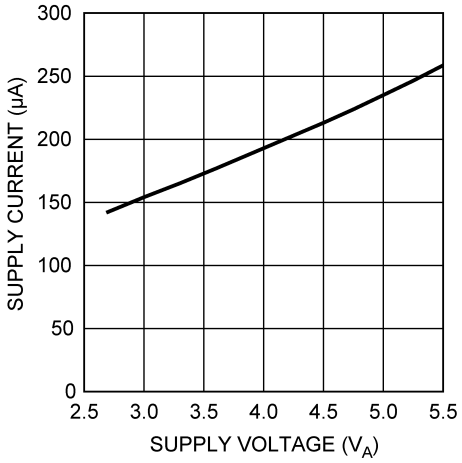


Figure 28. Supply Current vs. V_A

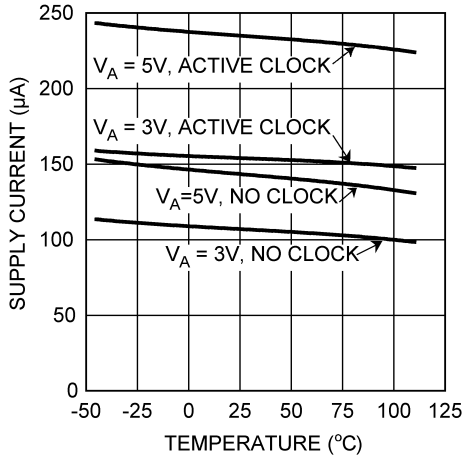


Figure 29. Supply Current vs. Temperature

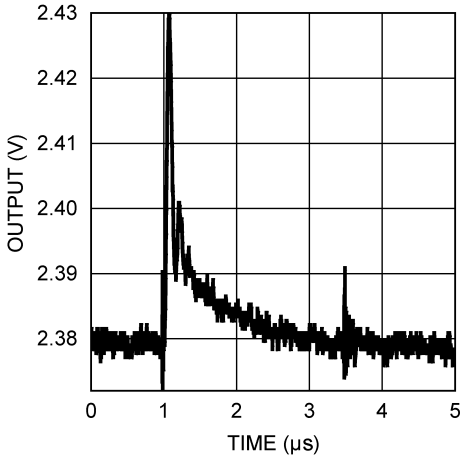


Figure 30. 5-V Glitch Response

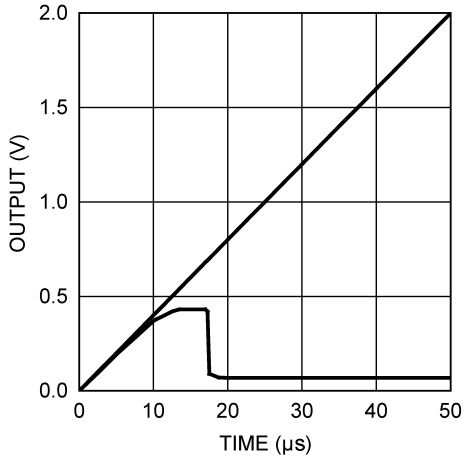


Figure 31. Power-On Reset

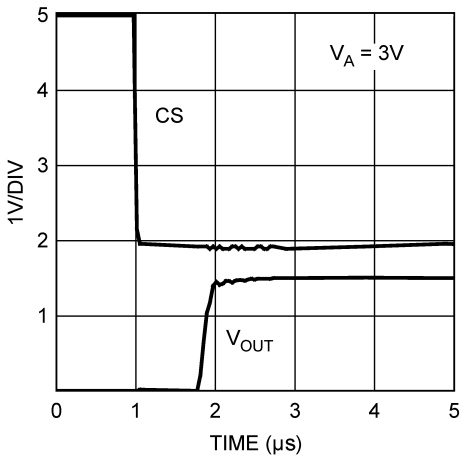


Figure 32. 3-V Wake-Up Time

Typical Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 48 to 4047, unless otherwise stated

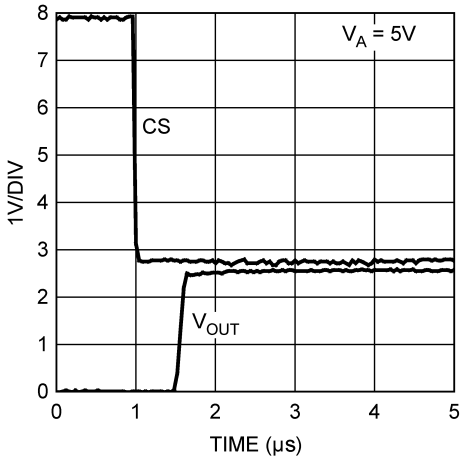


Figure 33. 5-V Wake-Up Time

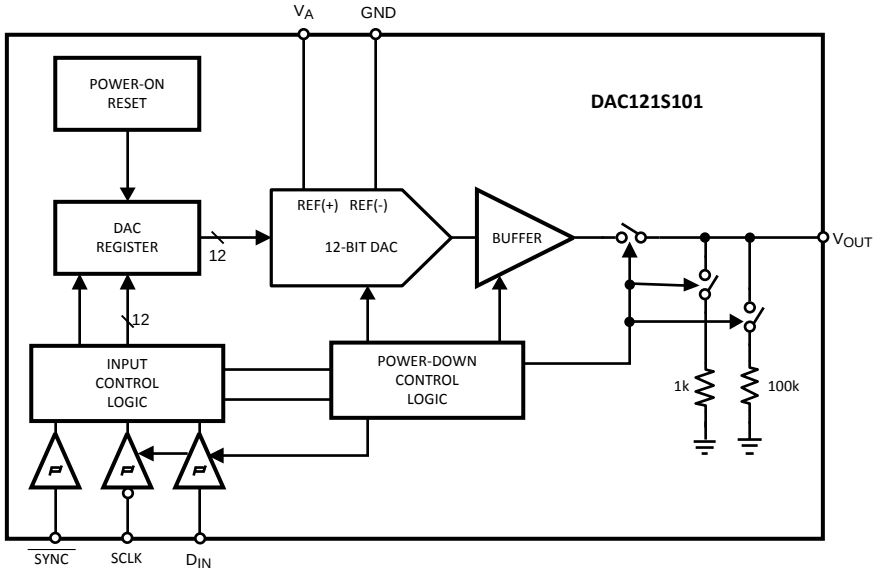
8 Detailed Description

8.1 Overview

The DAC121S101 device is a full-featured, general purpose 12-bit voltage-output digital-to-analog converter (DAC) with 10-µs settling time. Control of the output of the DAC is achieved over a 3-wire SPI interface. Once the DAC output has been set, additional communication with the DAC is not required unless the output condition needs to be changed. Likewise, the DAC121S101 power on state is 0 V. The DAC output will remain at 0 V until a valid write sequence is made.

A unique benefit of the DAC121S101 is the logic levels of the SPI™ input pins. The logic levels of SCLK, DIN, and SYNCB are independent of VA. As a result, the DAC121S101 can operate at a supply voltage (V_A) that is higher than the microcontroller that is controlling the DAC. This feature is advantageous in applications where the analog circuitry is being run at 5 V in order to maximize signal-to-noise ratio and digital logic is running at 3 V in order to conserve power.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Section

The DAC121S101 is fabricated on a CMOS process with an architecture that consists of switches and a resistor string that are followed by an output buffer. The power supply serves as the reference voltage. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT} = V_A \times (D / 4096) \quad (1)$$

where

- *D* is the decimal equivalent of the binary code that is loaded into the DAC register and can take on any value between 0 and 4095.

8.3.2 Resistor String

The resistor string is shown in Figure 34. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. This configuration ensures that the DAC is monotonic.

Feature Description (continued)

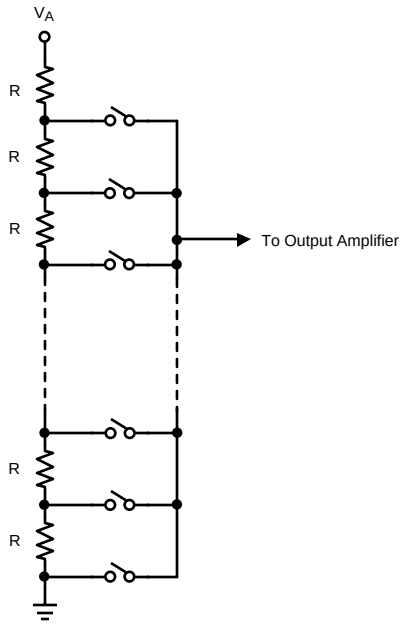


Figure 34. DAC Resistor String

8.3.3 Output Amplifier

The output buffer amplifier is a rail-to-rail type, providing an output voltage range of 0 V to V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0 V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. The output capabilities of the amplifier are described in the *Electrical Characteristics*.

8.4 Device Functional Modes

8.4.1 Power-On Reset

The power-on reset circuit controls the output voltage during power-up. Upon application of power the DAC register is filled with zeros and the output voltage is 0 V and remains there until a valid write sequence is made to the DAC.

8.4.2 Power-Down Modes

The DAC121S101 has four modes of operation. These modes are set with two bits (DB13 and DB12) in the control register.

Table 1. Modes of Operation

DB13	DB12	OPERATING MODE
0	0	Normal Operation
0	1	Power-Down with 1kΩ to GND
1	0	Power-Down with 100kΩ to GND
1	1	Power-Down with Hi-Z

When both DB13 and DB12 are 0, the device operates normally. For the other three possible combinations of these bits the supply current drops to its power-down level and the output is pulled down with either a 1-kΩ or a 100-KΩ resistor, or is in a high-impedance state, as described in Table 1.

The bias generator, output amplifier, the resistor string and other linear circuitry are all shut down in any of the power-down modes. However, the contents of the DAC register are unaffected when in power-down, so when coming out of power down the output voltage returns to the same voltage it was before entering power down. Minimum power consumption is achieved in the power-down mode with SCLK disabled and $\overline{SYNC}$ and D_{IN} idled low. The time to exit power-down (Wake-Up Time) is typically t_{WU} µsec as stated in the A.C. and Timing Characteristics Table.

8.5 Programming

8.5.1 Serial Interface

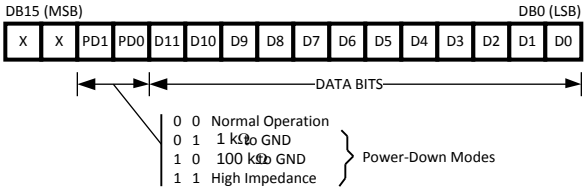
The three-wire interface is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See the Timing Diagram for information on a write sequence.

A write sequence begins by bringing the $\overline{SYNC}$ line low. Once $\overline{SYNC}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the mode of operation and/or a change in the DAC register contents) is executed. At this point the $\overline{SYNC}$ line may be kept low or brought high. In either case, it must be brought high for the minimum specified time before the next write sequence as a falling edge of $\overline{SYNC}$ can initiate the next write cycle.

Since the $\overline{SYNC}$ and D_{IN} buffers draw more current when they are high, they must be idled low between write sequences to minimize power consumption.

8.5.2 Input Shift Register

The input shift register, , has sixteen bits. The first two bits are don't cares and are followed by two bits that determine the mode of operation (normal mode or one of three power-down modes). The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK. See Figure 2.



Input Register Contents

Normally, the $\overline{SYNC}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{SYNC}$ is brought high before the 16th falling edge, the shift register is reset and the write sequence is invalid. The DAC register is not updated and there is no change in the mode of operation or in the output voltage.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 DSP and Microprocessor Interfacing

The simplicity of the DAC121S101 implies ease of use. However, it is important to recognize that any data converter that uses its supply voltage as its reference voltage will have essentially zero PSRR (power supply rejection ratio). Therefore, it is necessary to provide a noise-free supply voltage to the device.

Interfacing the DAC121S101 to microprocessors and DSPs is quite simple. The following guidelines are offered to hasten the design process.

9.1.1.1 ADSP-2101/ADSP2103 Interfacing

Figure 35 shows a serial interface between the DAC121S101 and the ADSP-2101/ADSP2103. The DSP must be set to operate in the SPORT Transmit Alternate Framing Mode. It is programmed through the SPORT control register and must be configured for Internal Clock Operation, Active Low Framing and 16-bit Word Length. Transmission is started by writing a word to the Tx register after the SPORT mode has been enabled.

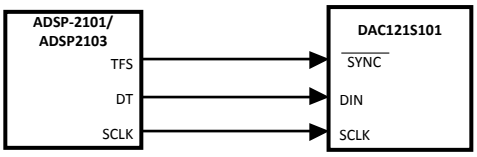


Figure 35. ADSP-2101/2103 Interface

9.1.1.1.1 80C51/80L51 Interface

A serial interface between the DAC121S101 and the 80C51/80L51 microcontroller is shown in Figure 36. The SYNC signal comes from a bit-programmable pin on the microcontroller. The example shown here uses port line P3.3. This line is taken low when data is to transmitted to the DAC121S101. Because the 80C51/80L51 transmits 8-bit bytes, only eight falling clock edges occur in the transmit cycle. To load data into the DAC, the P3.3 line must be left low after the first eight bits are transmitted. A second write cycle is initiated to transmit the second byte of data, after which port line P3.3 is brought high. The 80C51/80L51 transmit routine must recognize that the 80C51/80L51 transmits data with the LSB first while the DAC121S101 requires data with the MSB first.

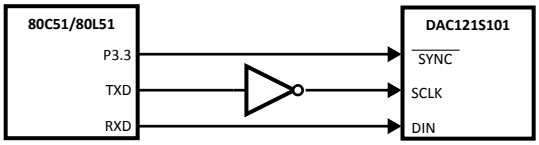


Figure 36. 80C51/80L51 Interface

9.1.1.1.2 68HC11 Interface

A serial interface between the DAC121S101 and the 68HC11 microcontroller is shown in Figure 37. The SYNC line of the DAC121S101 is driven from a port line (PC7 in the figure), similar to the 80C51/80L51.

Application Information (continued)

The 68HC11 must be configured with its CPOL bit as a zero and its CPHA bit as a one. This configuration causes data on the MOSI output to be valid on the falling edge of SCLK. PC7 is taken low to transmit data to the DAC. The 68HC11 transmits data in 8-bit bytes with eight falling clock edges. Data is transmitted with the MSB first. PC7 must remain low after the first eight bits are transferred. A second write cycle is initiated to transmit the second byte of data to the DAC, after which PC7 must be raised to end the write sequence.

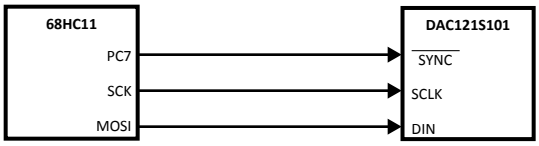


Figure 37. 68HC11 Interface

9.1.1.1.3 Microwire Interface

Figure 38 shows an interface between a Microwire compatible device and the DAC121S101. Data is clocked out on the rising edges of the SCLK signal.

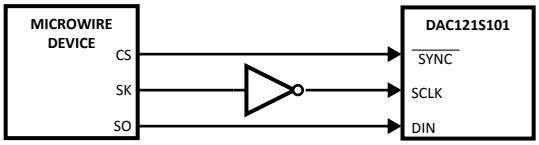


Figure 38. Microwire Interface

9.1.2 Bipolar Operation

The DAC121S101 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in Figure 39. This circuit will provide an output voltage range of ±5 V. A rail-to-rail amplifier must be used if the amplifier supplies are limited to ±5 V.

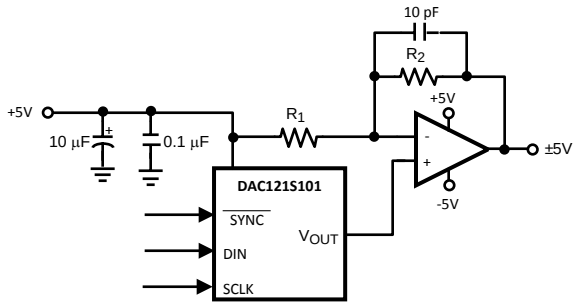


Figure 39. Bipolar Operation

The output voltage of this circuit for any code is found to be

$$V_O = (V_A \times (D / 4096) \times ((R1 + R2) / R1) - V_A \times R2 / R \quad (2)$$

where

- D is the input code in decimal form.

With VA = 5 V and R1 = R2,

$$V_O = (10 \times D / 4096) - 5\ V \quad (3)$$

A list of rail-to-rail amplifiers suitable for this application are indicated in Table 2.

Application Information (continued)

Table 2. Some Rail-to-Rail Amplifiers

AMP	PKGS	Typ V_{OS}	Typ I_{SUPPLY}
LMC7111	PDIP SOT-23	0.9 mV	25 µA
LM7301	SOIC SOT-23	0.03 mV	620 µA
LM8261	SOT-23	0.7 mV	1 mA

9.2 Typical Application

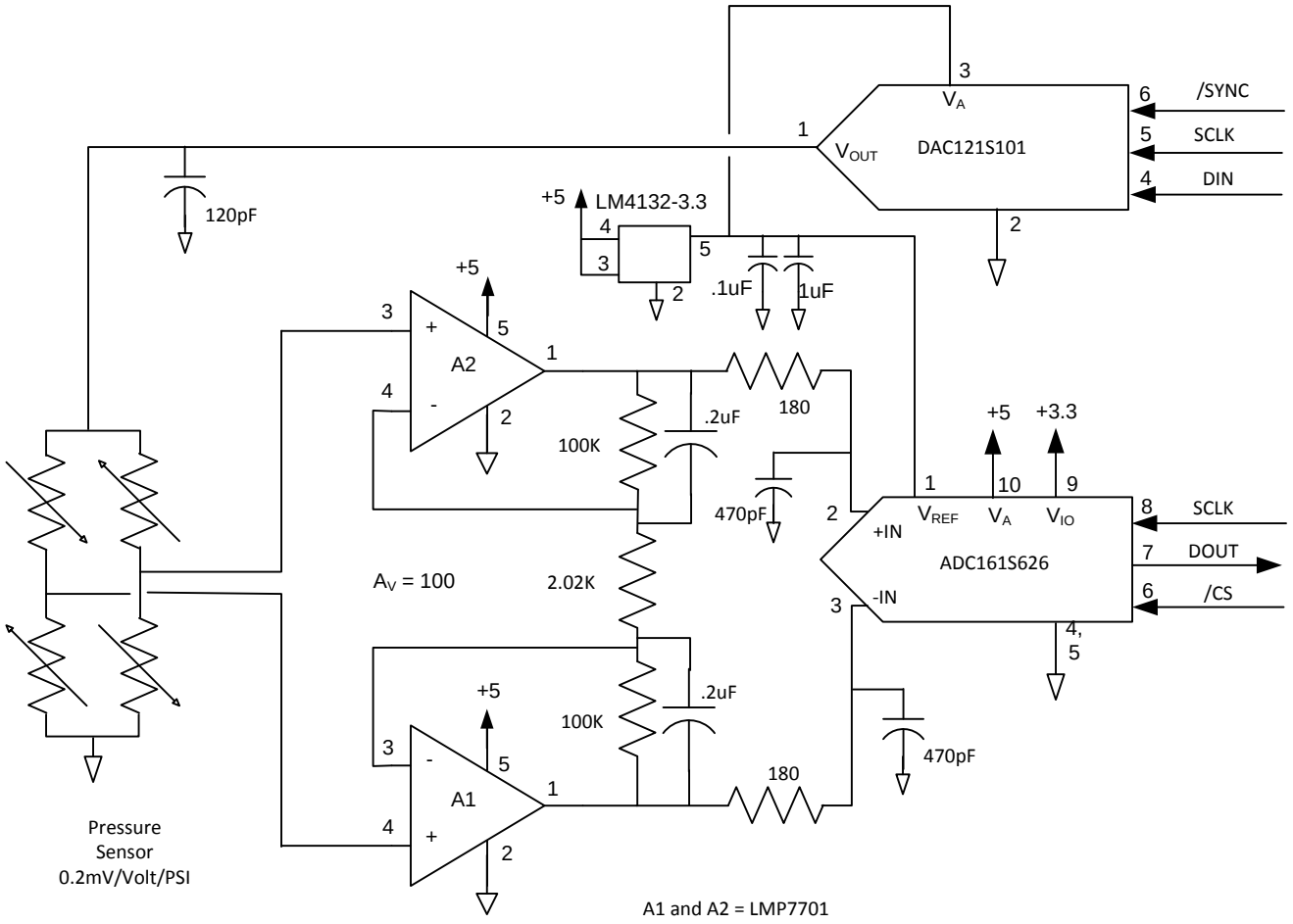


Figure 40. Pressure Sensor Gain Adjust

9.2.1 Design Requirements

A positive supply only data acquisition system capable of digitizing a pressure sensor output. In addition to digitizing the pressure sensor output, the system designer can use the DAC121S101 to correct for gain errors in the pressure sensor output by adjusting the bias voltage to the bridge pressure sensor.

Typical Application (continued)

9.2.2 Detailed Design Procedure

As shown in Equation 4, the output of the pressure sensor is relative to the imbalance of the resistive bridge times the output of the DAC121S101, thus providing the desired gain correction.

$$\text{Pressure Sensor Output} = (\text{DAC\_Output} \times [(R2 / (R1 + R2) - (R4 / (R3 + R4)] \quad (4)$$

Likewise for the ADC161S626, Equation 5 shows that the ADC output is function of the Pressure Sensor Output times relative to the ratio of the ADC input divided by the DAC121S101 output voltage.

$$\text{ADC161S626 Output} = (\text{Pressure Sensor Output} \times 100 / (2 \times \text{VREF})) \times 2^{16} \quad (5)$$

9.2.3 Application Curve

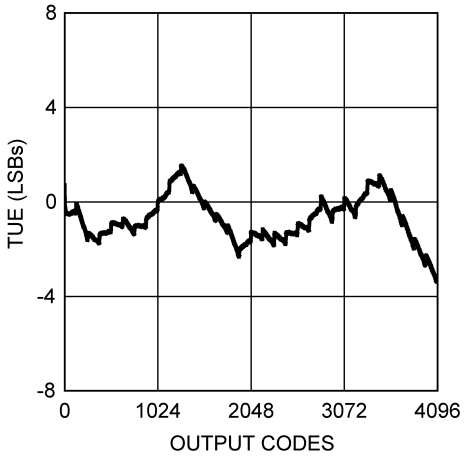


Figure 41. Total Unadjusted Error vs. Output Code

10 Power Supply Recommendations

NOTE

Information in the following power supply recommendations section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Using References as Power Supplies

Recall the need for a quiet supply source for devices that use their power supply voltage as a reference voltage.

Because the DAC121S101 consumes very little power, a reference source may be used as the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low noise regulators can also be used for the power supply of the DAC121S101. Listed below are a few power supply options for the DAC121S101.

10.1.1 LM4130

The LM4130 reference, with its 0.05% accuracy over temperature, is a good choice as a power source for the DAC121S101. Its primary disadvantage is the lack of 3-V and 5-V versions. However, the 4.096-V version is useful if a 0 to 4.095-V output range is desirable or acceptable. Bypassing the LM4130 VIN pin with a 0.1-µF capacitor and the VOUT pin with a 2.2-µF capacitor will improve stability and reduce output noise. The LM4130 comes in a space-saving 5-pin SOT23.

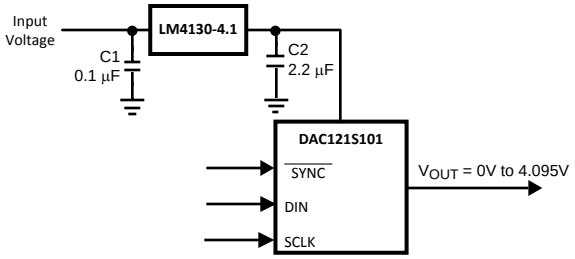


Figure 42. The LM4130 as a Power Supply

10.1.2 LM4050

Available with accuracy of 0.44%, the LM4050 shunt reference is also a good choice as a power regulator for the DAC121S101. It does not come in a 3-V version, but 4.096-V and 5-V versions are available. It comes in a space-saving 3-pin SOT23.

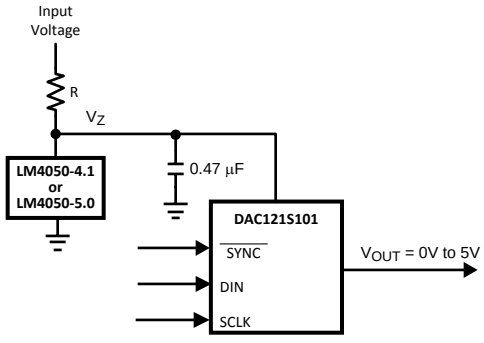


Figure 43. The LM4050 as a Power Supply

Using References as Power Supplies (continued)

The minimum resistor value in the circuit of Figure 43 must be chosen such that the maximum current through the LM4050 does not exceed its 15-mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, the resistor value at its minimum due to tolerance, and the DAC121S101 draws zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC121S101 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC121S101 draws its maximum current. These conditions can be summarized as

$$R(min) = (V_{IN}(max) - V_Z(min) / (I_A(min) + I_Z(max)) \quad (6)$$

and

$$R(max) = (V_{IN}(min) - V_Z(max) / (I_A(max) + I_Z(min)) \quad (7)$$

where

- $V_Z(min)$ and $V_Z(max)$ are the nominal LM4050 output voltages ± the LM4050 output tolerance over temperature,
- $I_Z(max)$ is the maximum allowable current through the LM4050,
- $I_Z(min)$ is the minimum current required by the LM4050 for proper regulation,
- $I_A(max)$ is the maximum DAC121S101 supply current,
- and $I_A(min)$ is the minimum DAC121S101 supply current.

10.1.3 LP3985

The LP3985 is a low noise, ultra-low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC121S101. It comes in 3-V, 3.3-V and 5-V versions, among others, and sports a low 30-µV noise specification at low frequencies. Because low-frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT-23 and 5-bump DSBGA packages.

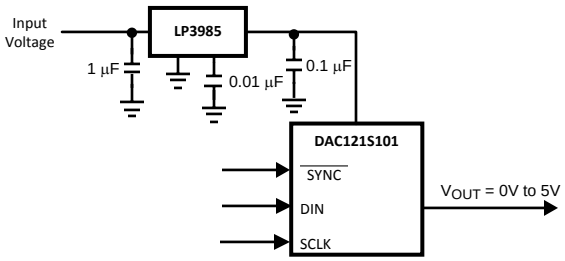


Figure 44. Using the LP3985 Regulator

An input capacitance of 1 µF without any ESR requirement is required at the LP3985 input, while a 1-µF ceramic capacitor with an ESR requirement of 5 mΩ to 500 mΩ is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

Using References as Power Supplies (continued)

10.1.4 LP2980

The LP2980 is an ultra-low dropout regulator with a 0.5% or 1.0% accuracy over temperature, depending upon grade. It is available in 3-V, 3.3-V and 5-V versions, among others.

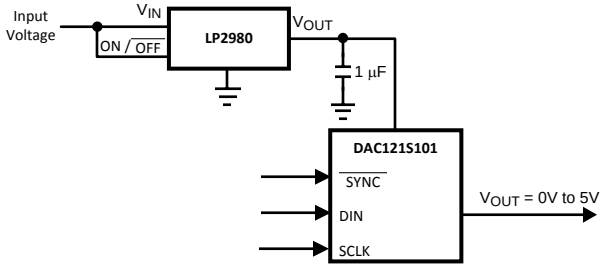


Figure 45. Using the LP2980 Regulator

Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1-µF over temperature, but values of 2.2 µF or more will provide even better performance. The ESR of this capacitor must be within the range specified in the LP2980 data sheet. Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Aluminum electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

11 Layout

11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The power applied to VA must be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. As with the GND connection, VA must be connected to a power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point.

The DAC121S101 power supply must be bypassed with a 10-µF and a 0.1-µF capacitor as close as possible to the device with the 0.1 µF right at the device supply pin. The 10-µF capacitor must be a tantalum type and the 0.1-µF capacitor must be a low ESL, low ESR type. The power supply for the DAC121S101 must only be used for analog circuits.

For best accuracy and minimum noise, the printed-circuit-board containing the DAC121S101 must have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes must be located in the same board layer. There must be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will use a *fencing* technique to prevent the mixing of analog and digital ground current. Separate ground planes must only be used when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC121S101. Take special care to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines must have controlled impedances.

11.2 Layout Example

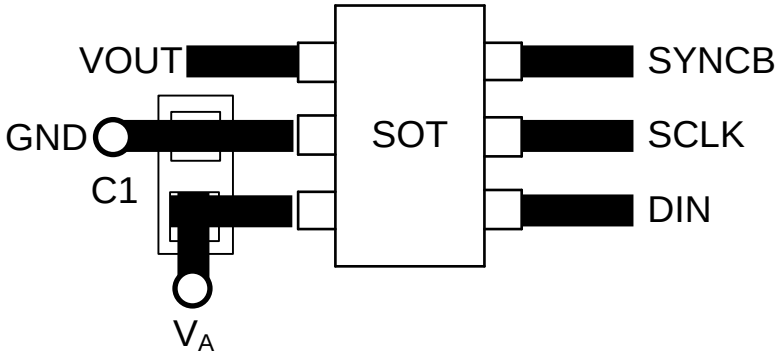


Figure 46. Typical Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

12.1.1.1 Specification Definitions

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB, which is V_{REF} / 4096 = V_A / 4096.

DIGITAL FEEDTHROUGH is a measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC outputs are not updated. It is measured with a full-scale code change on the data bus.

FULL-SCALE ERROR is the difference between the actual output voltage with a full scale code (FFFh) loaded into the DAC and the value of V_A x 4095 / 4096.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as GE = FSE - ZE, where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

GLITCH IMPULSE is the energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the *Electrical Characteristics*.

LEAST SIGNIFICANT BIT (LSB) is the bit that has the smallest value or weight of all bits in a word. This value is

$$LSB = V_{REF} / 2^n \quad (8)$$

where V_{REF} is the supply voltage for this product, and "n" is the DAC resolution in bits, which is 12 for the DAC121S101.

MAXIMUM LOAD CAPACITANCE is the maximum capacitance that can be driven by the DAC with output stability maintained.

MONOTONICITY is the condition of being monotonic, where the DAC has an output that never decreases when the input code increases.

MOST SIGNIFICANT BIT (MSB) is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of V_A.

POWER EFFICIENCY is the ratio of the output current to the total supply current. The output current comes from the power supply. The difference between the supply and output currents is the power consumed by the device without a load.

SETTLING TIME is the time for the output to settle to within 1/2 LSB of the final value after the input code is updated.

WAKE-UP TIME is the time for the output to settle to within 1/2 LSB of the final value after the device is commanded to the active mode from any of the power down modes.

ZERO CODE ERROR is the output error, or voltage, present at the DAC output after a code of 000h has been entered.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *LM4130 Precision Micropower Low Dropout Voltage Reference*, SNVS048
- *LM4050 Precision Micropower Shunt Voltage Reference*, SNOS455
- *LP3985 Micropower, 150mA Low-Noise Ultra Low-Dropout CMOS Voltage Regulator*, SNVS087
- *LP2980 Micropower 50-mA Ultralow-Dropout Voltage Regulator*, SLVS715
- *LMC7111 Tiny CMOS Operational Amplifier with Rail-to-Rail Input and Output*, SNOS753
- *LM7301 Low Power, 4 MHz GBW, Rail-to-Rail Input-Output Operational Amplifier in TinyP*, SNOS879
- *LM8261 Single RRIO, High Output Current & Unlimited Cap Load Op Amp in SOT23-5*, SNOS469

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola, Inc..
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC121S101CIMK	NRND	SOT-23-THIN	DDC	6	1000	TBD	Call TI	Call TI	-40 to 105	X61C	
DAC121S101CIMK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	X61C	Samples
DAC121S101CIMKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	X61C	Samples
DAC121S101CIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	X60C	Samples
DAC121S101QCMK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	X61Q	Samples
DAC121S101QCMKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	X61Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF DAC121S101, DAC121S101-Q1 :

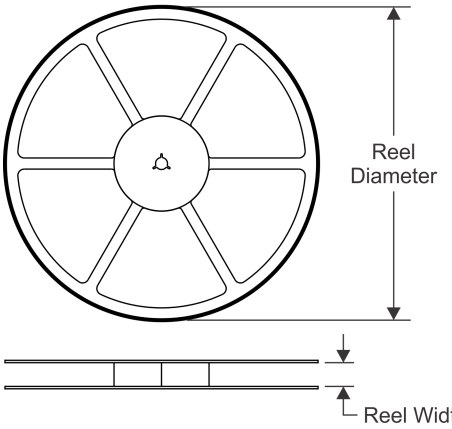
- Automotive: DAC121S101-Q1
- Military: DAC121S101

NOTE: Qualified Version Definitions:

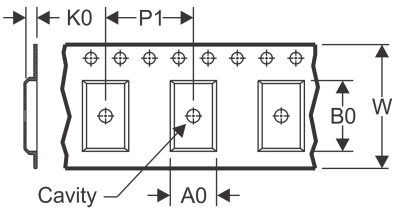
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

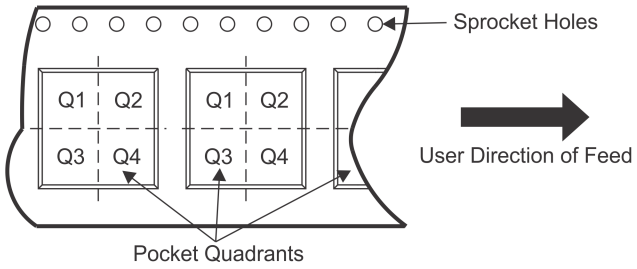


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

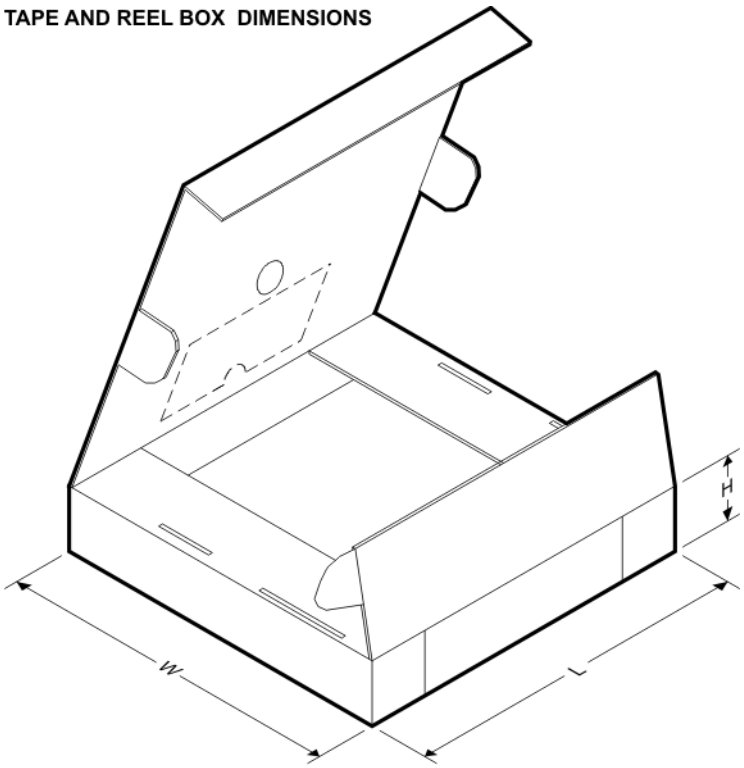
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC121S101CIMK	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC121S101CIMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC121S101CIMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC121S101CIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC121S101QCMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC121S101QCMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

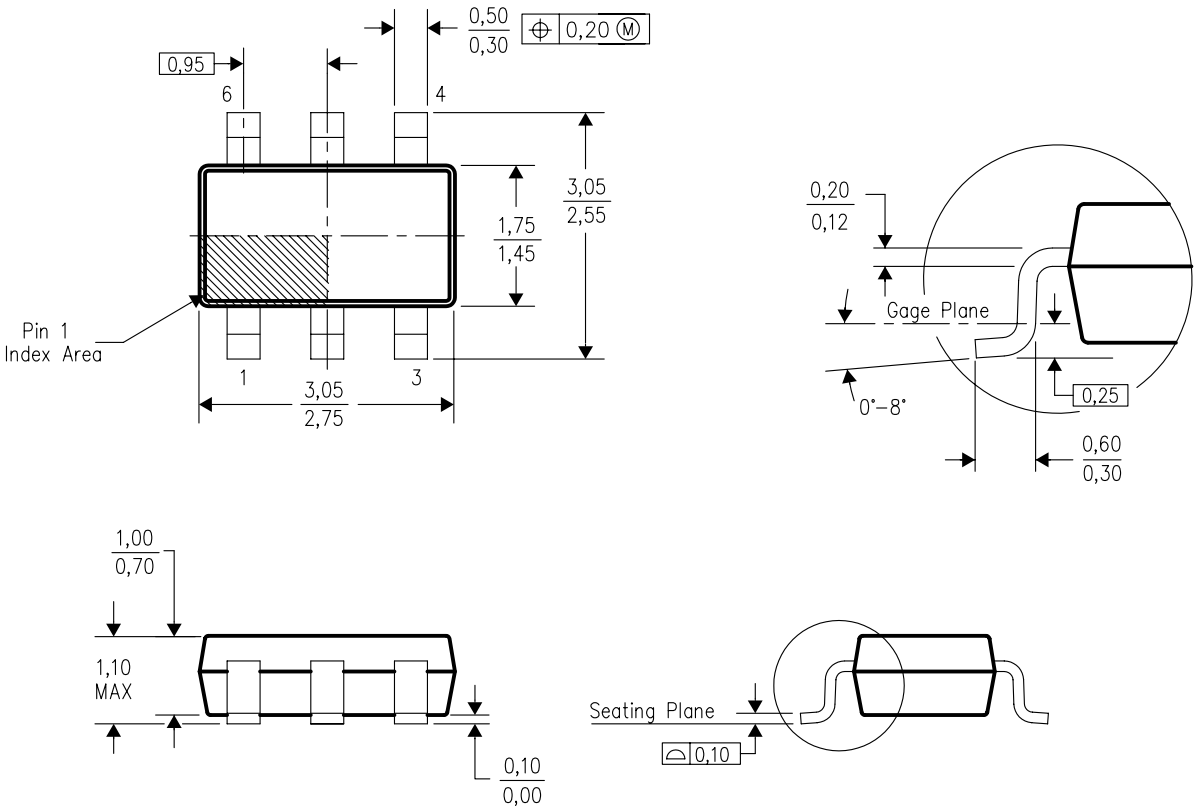
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC121S101CIMK	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
DAC121S101CIMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
DAC121S101CIMKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
DAC121S101CIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
DAC121S101QCMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
DAC121S101QCMKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

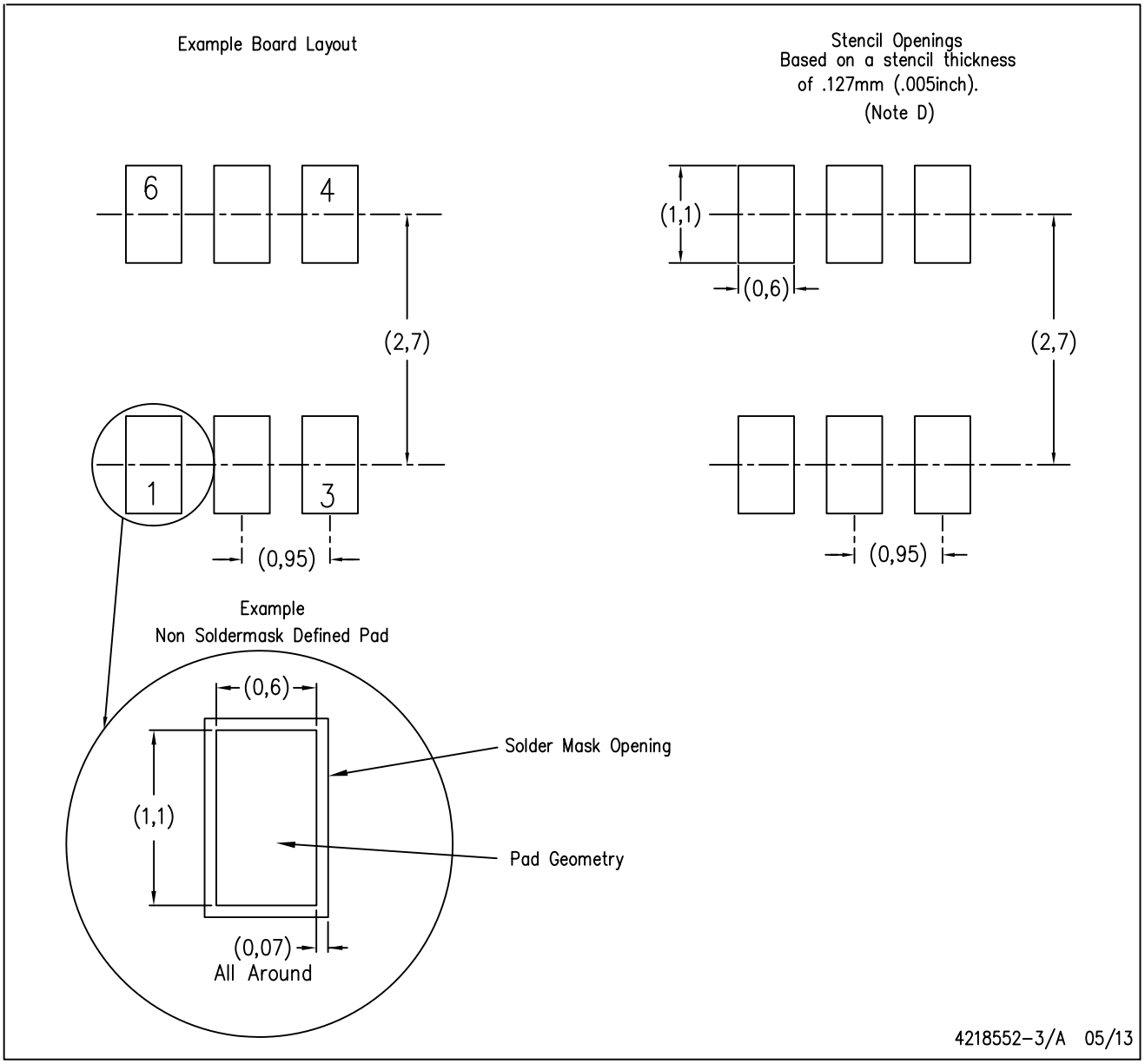
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

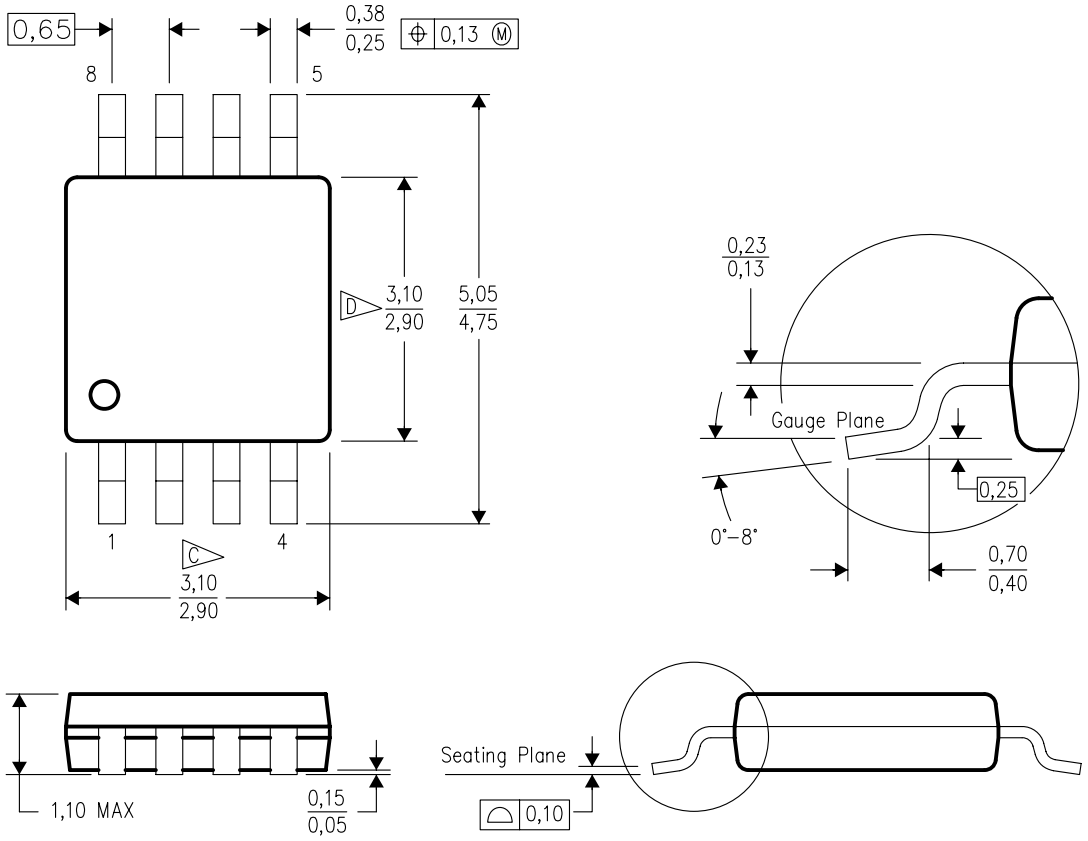
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

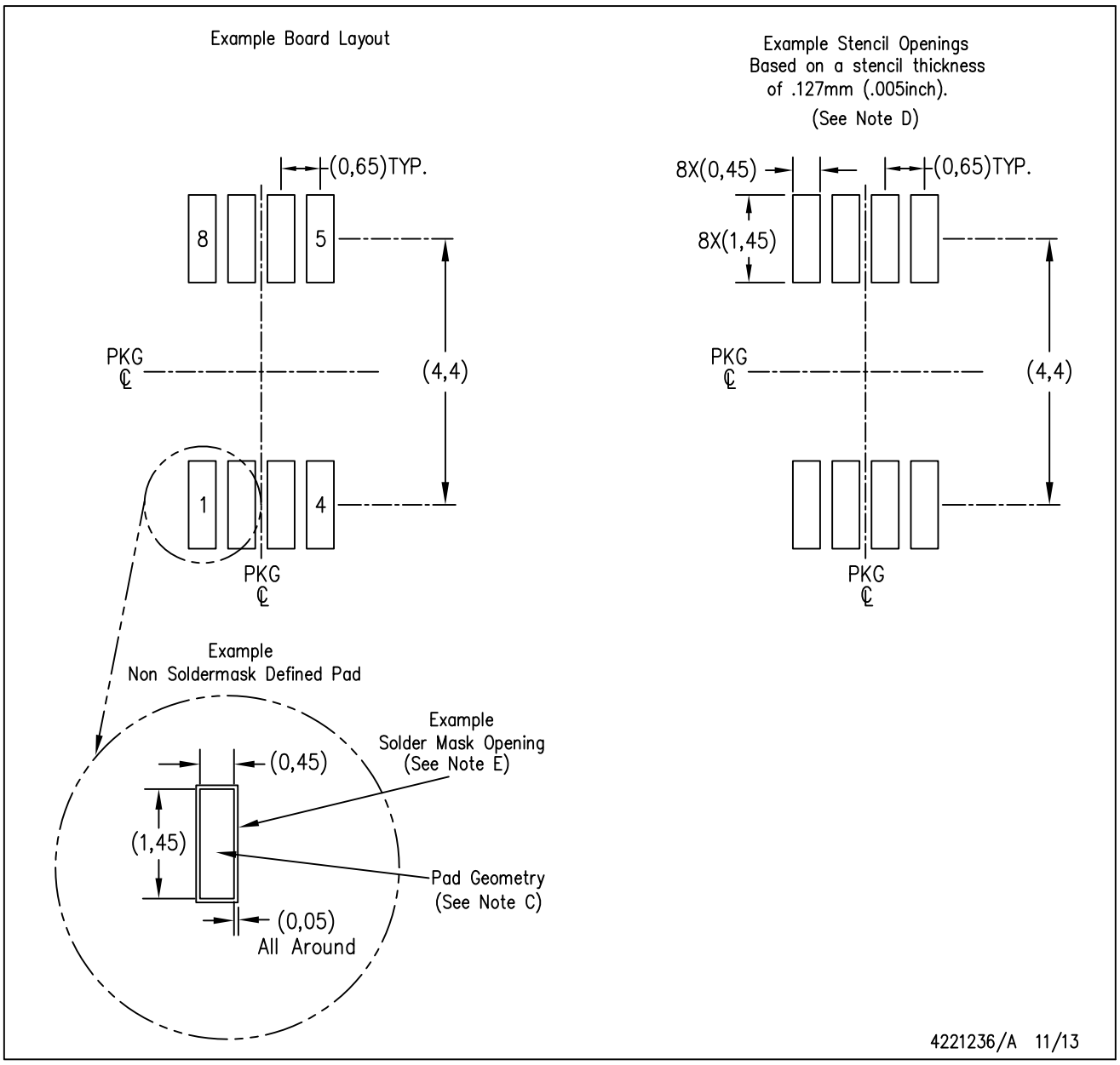
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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