THE DATASHEET OF

HIP2104FRAANZ-T7A

HIP2103, HIP2104

60V, 1A/2A Peak, Half-Bridge Driver with 4V UVLO

The HIP2103 and HIP2104 are half-bridge drivers designed for applications using DC motors, 3-phase brushless DC motors, or other similar loads.

The two inputs (HI and LI) independently control the high-side driver (HO) and the low-side driver (LO). HI and LI can be configured to enable/disable the device, which lowers the number of connections to a microcontroller and the cost.

The low I_{DD} bias current in the Sleep Mode prevents battery drain when the device is not in use, which eliminates the need for an external switch to disconnect the driver from the battery.

Integrated pull-down resistors on all of the inputs (LI, HI, VDen, and VCen) reduce the need for external resistors. An active low resistance pull-down on the LO output ensures that the low-side bridge FET remains off during the Sleep Mode or when V_{DD} is below the Undervoltage Lockout (UVLO) threshold.

The HIP2104 has a 12V linear regulator and a 3.3V linear regulator with separate enable pins. The 12V regulator provides internal bias for V_{DD} and the 3.3V regulator provides bias for an external microcontroller (and/or other low voltage ICs), which eliminates the need for discrete LDOs or DC/DC converters.

Related Literature

For a full list of related documents, visit our website:

- HIP2103, HIP2104 device pages

Features

- 60V maximum bootstrap supply voltage
- 3.3V and 12V LDOs with dedicated enable pins (HIP2104)
- 5µA sleep mode quiescent current
- V_{DD} undervoltage lockout
- 3.3V or 5V CMOS compatible inputs with hysteresis
- Integrated bootstrap FET (replaces traditional boot strap diode)
- HIP2103 is available in a 3x3mm, 8 Ld TDFN package
- HIP2104 is available in a 4x4mm, 12 Ld DFN package
- Pb-Free (RoHS Compliant)

Applications

- Half-bridge, full bridge, and BLDC motor drives (see Figures 3, 4, 5)
- UPS and inverters
- Class-D amplifiers
- Any switch mode power circuit requiring a half-bridge driver

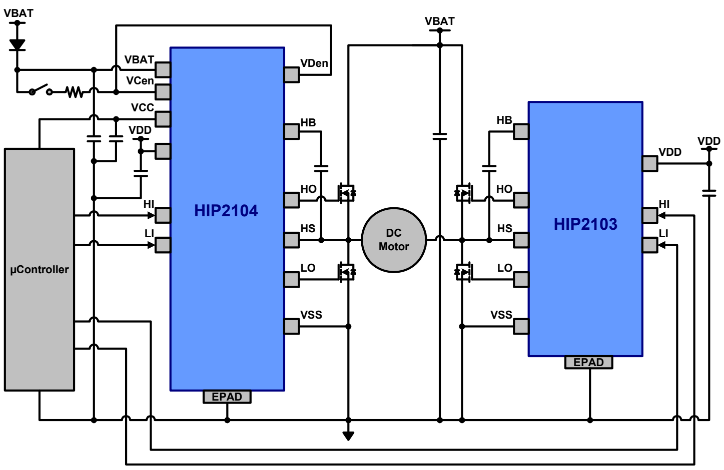


Figure 1. Typical Full Bridge Application

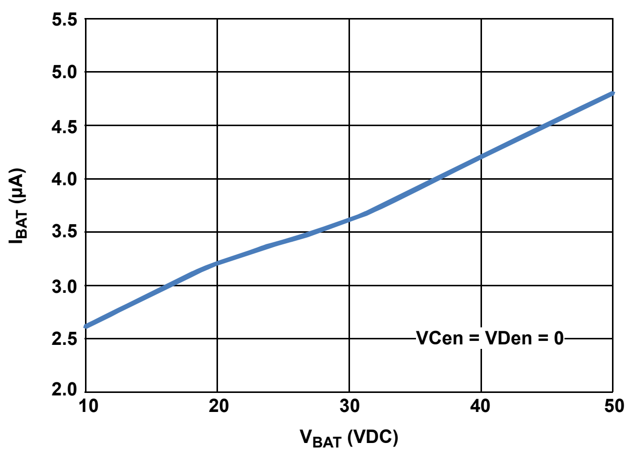


Figure 2. HIP2104 Shutdown Current vs V_{BAT}

Contents

1. Overview

1.1 Typical Applications

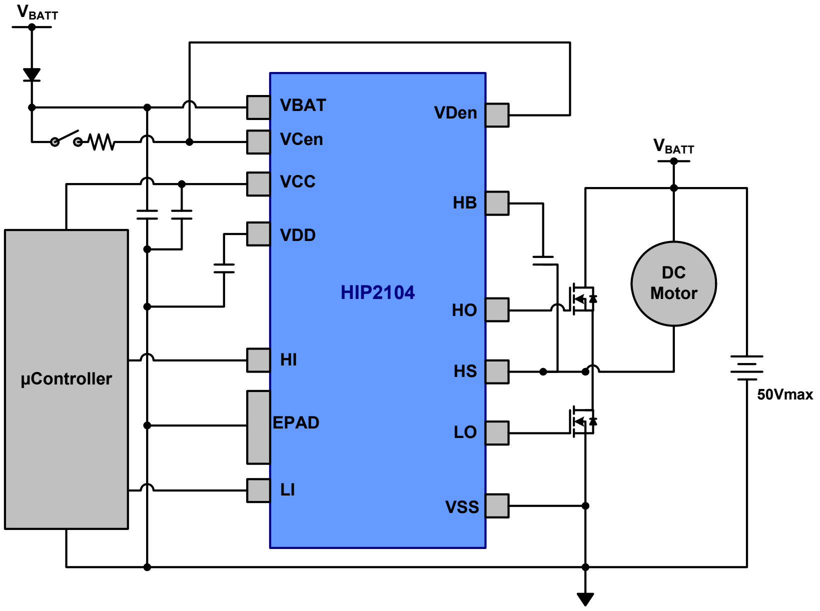


Figure 3. Half-Bridge Motor Drive Topology

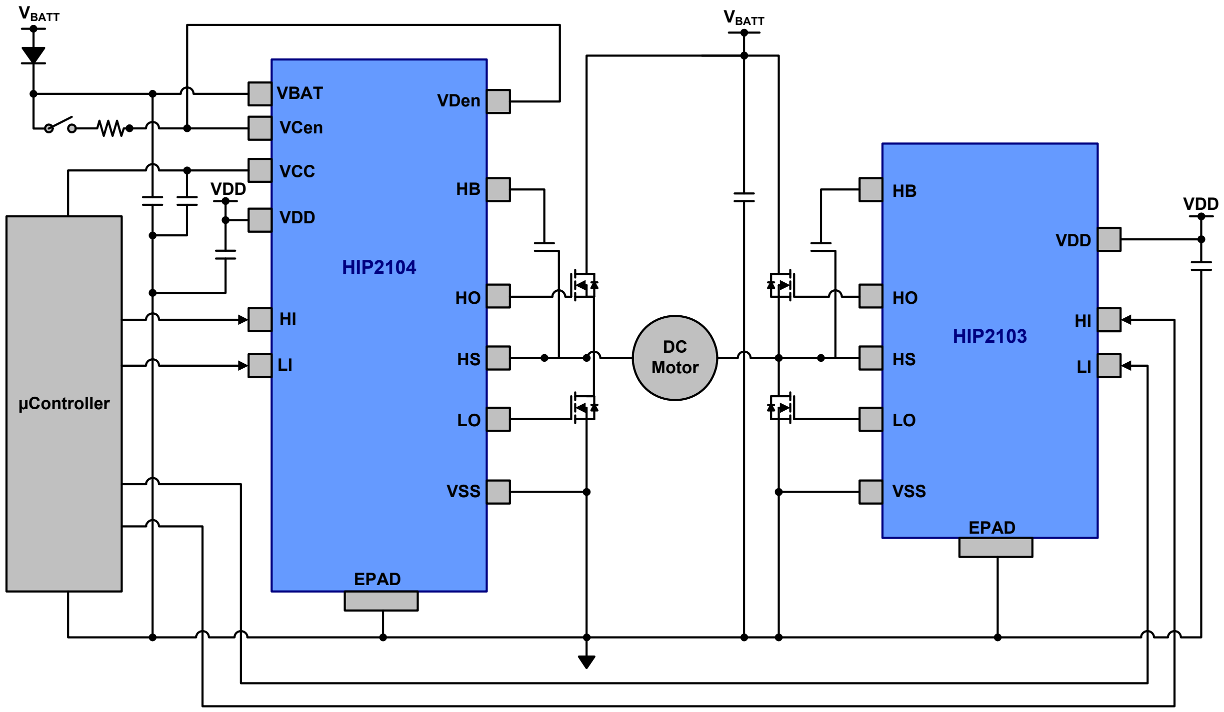


Figure 4. Full Bridge Motor Driver Topology

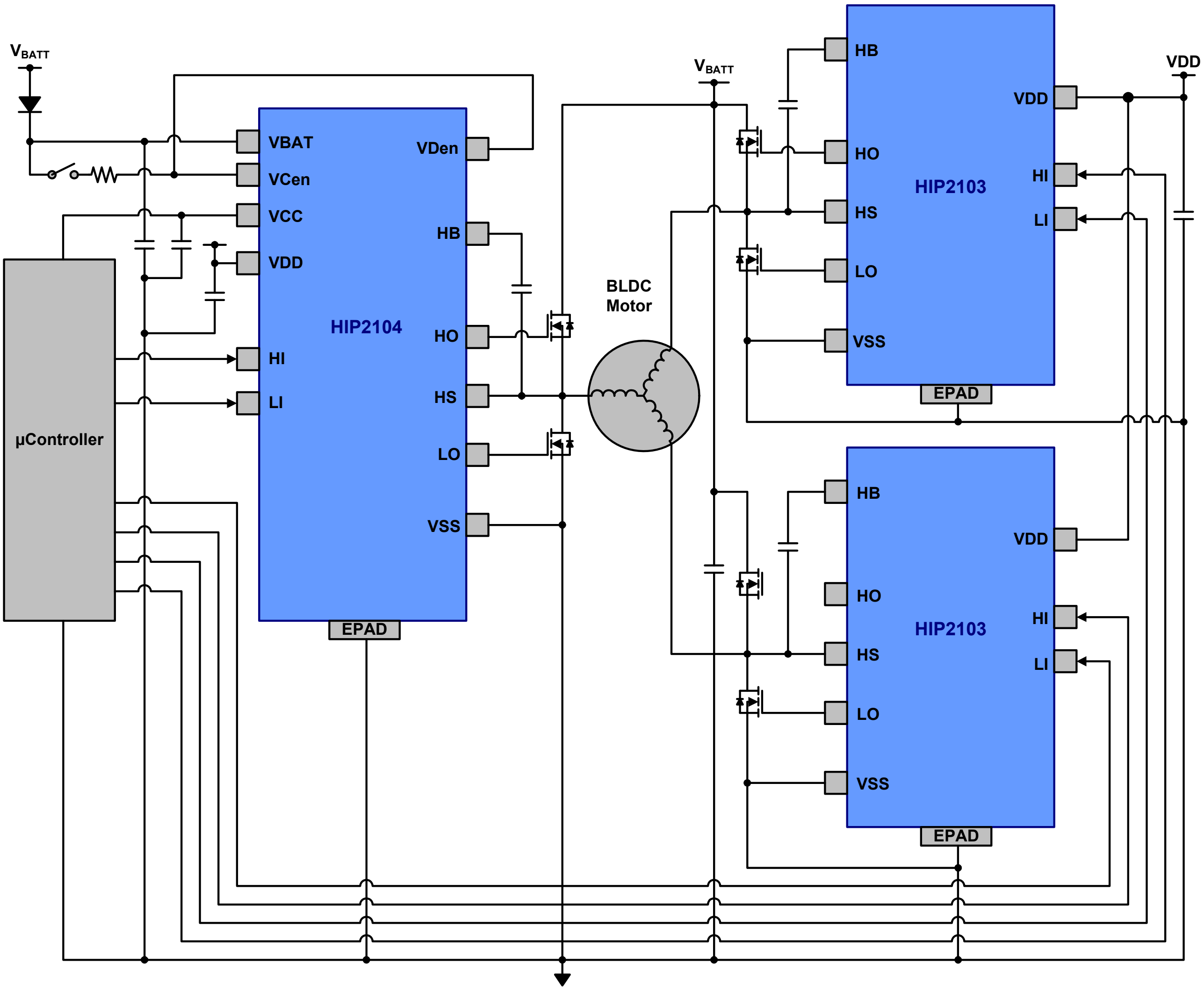
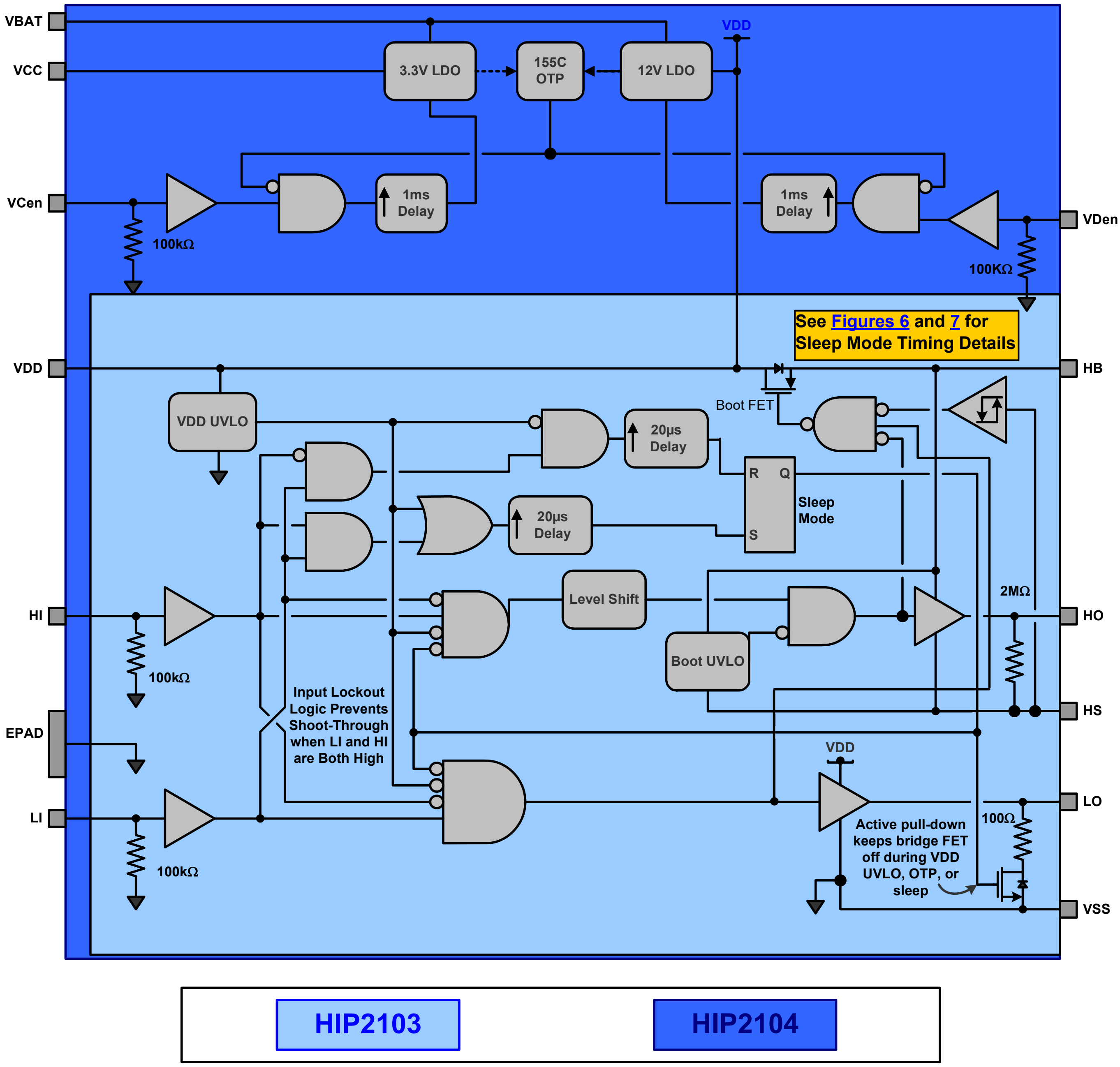


Figure 5. BLDC (3-Phase) Motor Drive Topology

1.2 Block Diagram



1.3 Ordering Information

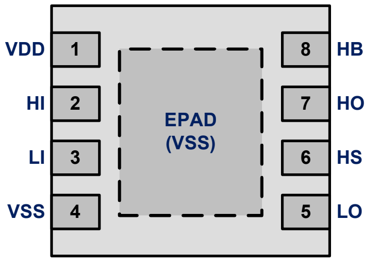
Part Number (Notes 2, 3, 4)	Part Marking	UVLO (V)	VCC Regulator (V)	VDD Regulator (V)	Tape and Reel (Units) (Notes 1)	Package (RoHS Compliant)	Pkg. Dwg. #
HIP2103FRTAAZ	DZBF	4.0	N/A	N/A	-	8 Ld 3x3 TDFN	L8.3x3A
HIP2103FRTAAZ-T	DZBF	4.0	N/A	N/A	6k	8 Ld 3x3 TDFN	L8.3x3A
HIP2103FRTAAZ-T7A	DZBF	4.0	N/A	N/A	250	8 Ld 3x3 TDFN	L8.3x3A
HIP2104FRAANZ	2104AN	4.0	3.3	12	-	12 Ld 4x4 DFN	L12.4x4A
HIP2104FRAANZ-T	2104AN	4.0	3.3	12	6k	12 Ld 4x4 DFN	L12.4x4A

Part Number (Notes 2, 3, 4)	Part Marking	UVLO (V)	VCC Regulator (V)	VDD Regulator (V)	Tape and Reel (Units) (Notes 1)	Package (RoHS Compliant)	Pkg. Dwg. #
HIP2104FRAANZ-T7A	2104AN	4.0	3.3	12	250	12 Ld 4x4 DFN	L12.4x4A
HIP2103-4DEMO1Z	HIP2103, HIP2104 3-phase, Full, or Half Bridge Motor Drive Demonstration Board						
HIP2103-4DEMO2Z	Demonstration Board 3-Phase Module with HIP2103, HIP2104 Drivers						
HIP2104DBEVAL1Z	HIP2104 Evaluation Board (Daughter Board)						
HIP2103DBEVAL1Z	HIP2103 Evaluation Board (Daughter Board)						
HIP2103_4MBEVAL1Z	HIP2103, HIP2104 Evaluation Board (Mother Board)						

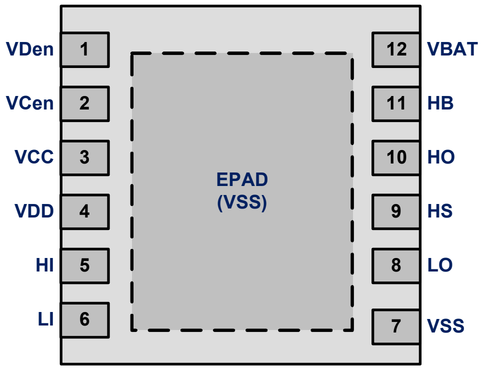
Notes:
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the HIP2103 and HIP2104 device pages. For more information about MSL, see TB363.
4. All part numbers are rated -40°C to +125°C for the recommended operating junction temperature range.

1.4 Pin Configurations

HIP2103
(8 Ld 3x3 TDFN)
Top View



HIP2104
(12 Ld 4x4 DFN)
Top View



1.5 Pin Descriptions

HIP2103 8 Ld TDFN	HIP2104 12 Ld DFN	Symbol	Description
-	1	VDen	HIP2104 only. Enable input for the VDD linear regulator, 3.3V or 5V logic compatible, VBAT tolerant. VDD output is turned on after 1ms debouncing period.
-	2	VCen	HIP2104 only. Enable input for the VCC linear regulator, 3.3V or 5V logic compatible, VBAT tolerant. VCC output is turned on after 1ms debouncing period.
-	3	VCC	HIP2104 only. 3.3V/75mA output voltage of linear regulator. Enabled by VCen.
1	4	VDD	HIP2103: Driver supply voltage, 4.5V to 14V. HIP2104: 12V/75mA output voltage of linear regulator and driver supply voltage. Enabled by VDen.
2	5	HI	High side input, 3.3V or 5V logic compatible. Internal 100kΩ pull-down resistor on the HI pin pulls HI to logic 0 when floating.
3	6	LI	Low side input, 3.3V or 5V logic compatible. Internal 100kΩ pull-down resistor on the LI pin pulls LI to logic 0 when floating.
4	7	VSS	Signal ground.
5	8	LO	Low-side driver output. Connect to the lower NFET gate.
6	9	HS	High-side NFET source connection. Connect the bootstrap capacitor from HB to this pin.
7	10	HO	High-side driver output. Connect to the upper NFET gate.
8	11	HB	High-side Boot capacitor. Connect bootstrap capacitor from HS to this pin.
-	12	VBAT	(HIP2104 only) positive battery (bridge voltage) connection.
EP	EP	EPAD	Exposed pad. Connect EPAD to VSS. Renesas recommends connecting the EPAD to a low thermal impedance on the PCB for optimum thermal performance.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter (Note 5)	Minimum	Maximum	Unit
Supply Voltage V_{DD} (HIP2103 only)	-0.3	16	V
Bridge Supply Voltage V_{BAT} (HIP2104 Only)	-0.3	60	V
High side Bias Voltage (V_{HB} - V_{HS}) (Note 10)	-0.3	16	V
Logic Inputs VCen, VDen (HIP2104 Only)	- 0.3	V_{BAT} + 0.3	V
Logic Inputs LI, HI	- 0.3	V_{DD} + 0.3	V
Output Voltage LO	- 0.3	V_{DD} + 0.3	V
Output Voltage HO	V_{HS} - 0.3	V_{HB} + 0.3	V
Voltage on HS (Note 10)	-10	60	V
Voltage on HB	V_{HS} - 0.3	66	V
Average Current in Boot Diode (Note 6)		100	mA
Maximum Boot Capacitor Value		10	µF
Average Output Current in HO and LO (Note 6)		200	mA
ESD Rating	**Value**		**Unit**
Human Body Model Class 2 (Tested per JESD22-A114E)	2		kV
Charged Device Model Class IV	1		kV
Latch-Up (Tested per JESD-78B; Class 2, Level A) all pins	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Notes:
5. All voltages are referenced to VSS unless otherwise specified.
6. When driving a power MOSFET or similar capacitive load, the average output current is the average of the rectified output current. The peak output currents of this driver are self limiting by trans conductance or $r_{DS(ON)}$ and do not require any external components to minimize the peaks. If the output is driving a non-capacitive load, such as an LED, the maximum output current must be limited by external means to less than the specified recommended rectified average output current.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld DFN Package (Notes 7, 8)	46	7
12 Ld TDFN Package (Notes 7, 8)	44	7

Notes:
7. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
8. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
9. The maximum value of V_{HS} must be limited so that V_{HB} does not exceed 60V.
10. If the duration of the negative voltage is significant with respect to the time constant to charge the boot capacitor (across HB and HS) the voltage on the boot capacitor can charge as high as V_{DD} - (-V_{HS}) = (V_{DD} +V_{HS}) potentially violating the Voltage Rating for (V_{HB} - V_{HS}).
11. When V_{BAT} < ~13V, the output of VDD sags. The 5V minimum specified for V_{BAT} is the minimum level for which the UVLO does not activate.

Parameter	Minimum	Maximum	Unit
Max Power Dissipation at +25°C in Free Air			
8 Ld DFN Package		2.3	W
12 Ld TDFN Package		2.2	W

Parameter	Minimum	Maximum	Unit
Max Power Dissipation at +25°C on Copper Plane			
8 Ld DFN Package		14.3	W
12 Ld TDFN Package		14.3	W
Storage Temperature Range	-65	+150	°C
Maximum Operating Junction Temperature Range	-40	+150	
Nominal Over-Temperature Shutdown		+155	°C
Over Temperature Shut-down Range	+145	+165	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operating Conditions

Parameter (Note 5)	Minimum	Maximum	Unit
Junction Temperature	-40	+125	°C
Supply Voltage, V_{BAT} (HIP2104 only) (Note 11)	5.0	50	V
Supply Voltage, V_{DD}	4.5	14	V
High Side Bias Voltage (V_{HB} - V_{HS}) (Note 10)	-0.3	14	V
Voltage on HS, Transient, V_{HS} (Notes 9, 10)	-10	50	V
Voltage on HB	V_{HS} - 0.3V	60	V
Voltage on HS, Continuous		40	V
Logic Inputs VCen, VDen (HIP2104 only)	0	V_{BAT}	V
Output Voltage (LO)	GND	V_{DD}	V
Output Voltage (HO)	V_{HS}	V_{HB}	V
Average Output Current in HO and LO (Note 6)	0	150	mA

2.4 DC Electrical Specifications

V_{DD} = V_{HB} = 12V (for HIP2103), V_{SS} = V_{HS} = 0V, V_{BAT} = 18V (for HIP2104), LI = HI = 0V. No load on HO and LO unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C**.

Parameters	Symbol	Test Conditions	T_J = +25°C			T_J = -40°C to +125°C		Unit
			Min	Typ	Max	Min (Note 12)	Max (Note 12)	
Linear Bias Supplies (HIP2104 Only)								
V_{DD} Output Voltage Over Rated Line, Load, and Temperature	V_{DD12}	Nominal V_{DD} = 12V	-2.5	+2.1	+4.8	**-5**	**+5**	%
V_{DD} Output Current Limit (Brick Wall)	I_{DD12}		83	151	237	**80**	**245**	mA
V_{DD} Drop Output Voltage (Figure 10)	VDdout	Load = 75mA				**0.06**	**0.7**	V
V_{CC} Output Voltage Over Rated Line, Load, and Temperature	$V_{CC3.3}$	Nominal V_{CC} = 3.3V	-3.9	+1.8	+4.3	**-5**	**+5**	%
V_{CC} Output Current Limit (Brick Wall)	I_{CC}		83	149	237	**80**	**245**	mA
V_{CC} Drop Output Voltage (Figure 11)	VCdout	Load = 75mA				**0.5**	**0.9**	V
Bias Currents								
V_{DD} Sleep Mode Current (HIP2103)	I_{DDS}	HI = LI = 1, after 10 to 30µs delay		9.4			**20**	µA
V_{BAT} Shutdown Current (HIP2104)	$I_{DDSbatt}$	VCen = VDen = 0, after 10 to 30µs delay, V_{BAT} = 50V		4.8			**15**	µA

V_{DD} = V_{HB} = 12V (for HIP2103), V_{SS} = V_{HS} = 0V, V_{BAT} = 18V (for HIP2104), LI = HI = 0V. No load on HO and LO unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C. (Continued)**

Parameters	Symbol	Test Conditions	T_J = +25°C			T_J = -40°C to +125°C		Unit
			Min	Typ	Max	Min (Note 12)	Max (Note 12)	
V_{BAT} (HIP2104) or VDD (HIP2103) Operating Current	I_{DDO20}	f = 20kHz, HI = $\overline{LI}$ = 50% square wave V_{DD} = 12V for HIP2103		832			**1040**	µA
	I_{DDO10}	f = 10kHz, HI = $\overline{LI}$ = 50% square wave V_{DD} = 12V for HIP2103		661			**825**	µA
HB to HS Quiescent Current	IHBQ	HI = 1, LO = 0, V_{HS} = 0V, V_{HB} = 12V		135			**160**	µA
HB to HS Operating Current	I_{HBS20K}	LI = 0, HI = 50% square wave 20kHz, V_{HS} = 0V, V_{HB} = 12V		206			**245**	µA
	I_{HBS10K}	LI = 0, HI = 50% square wave 10kHz, V_{HS} = 0V, V_{HB} = 12V		167			**193**	µA
HB to V_{SS} Operating Current	I_{HB20K}	LI = 0, HI = 50% square wave 20kHz, V_{HB} = 60V, V_{HS} = 50V		201			**240**	µA
	I_{HB10K}	LI = 0, HI = 50% square wave 10kHz, V_{HB} = 60V, V_{HS} = 50V		164			**190**	µA
HB to V_{SS} Quiescent Current	I_{HBQ}	LI = HI = 0V; V_{HB} = 60V, V_{HS} = 50V		120			**145**	µA
HS to V_{SS} Current, Sleep Mode	I_{HBS}	LI = HI = 1; HB open, V_{HS} = 50V		0.03			**+1**	µA
Input Pins								
Low Level Input Voltage Threshold	V_{IL}	V_{DD} = 12V		1.44		**1.18**	**1.63**	V
High Level Input Voltage Threshold	V_{IH}			2.06		**1.73**	**2.4**	V
Input Voltage Hysteresis	V_{Hys}			0.62		**0.48**	**0.85**	V
Low Level Input Voltage Threshold	V_{IL}	V_{DD} = 5V		1.13		**0.9**	**1.25**	V
High Level Input Voltage Threshold	V_{IH}			1.63		**1.38**	**1.84**	V
Input Voltage Hysteresis	V_{Hys}			0.50		**0.36**	**0.63**	V
Input Pull-Down	R_I			100		**80**	**130**	kΩ
Undervoltage Lockout (Note 13)								
V_{DD} Falling Threshold	V_{UVF}			4.2		**3.98**	**4.36**	V
V_{DD} Threshold Hysteresis	V_{UVH}			0.34		**0.267**	**0.37**	V
Boot FET								
On Resistance	R_{Don}	I_{VDD-HB} = 100mA, HI = 0, LI = 1		8.2		**2.42**	**15**	Ω
LO Gate Driver								
Sinking $r_{DS(ON)}$	RDS_{LOL}	I_{LO} = 100mA, LI = 0		2.68		**0.61**	**11**	Ω
Sourcing $r_{DS(ON)}$	RDS_{LOH}	I_{LO} = -75mA, HI = 1		6.47		**2.3**	**15**	Ω
Peak Pull-Up Current	I_{LOH12}	HI = 1 V_{DD} = 12V, C_{LOAD} = 1000pF		1				A
	I_{LOH5}	HI = 1 V_{DD} = 5V, C_{LOAD} = 1000pF (HIP2103 only)						A
Peak Pull-Down Current	I_{LOL12}	HI = 0 V_{DD} = 12V, C_{LOAD} = 1000pF		2				A
	I_{LOL5}	HI = 0 V_{DD} = 5V, C_{LOAD} = 1000pF (HIP2103 only)						A
HO Gate Driver								
Sinking $r_{DS(ON)}$	RDS_{HOL}	I_{HO} = 100mA, HI = 0		2.68		**0.61**	**11**	Ω
Sourcing $r_{DS(ON)}$	RDS_{HOH}	I_{HO} = -100mA, HI = 1		6.47		**2.3**	**15**	Ω

$V_{DD} = V_{HB}$ = 12V (for HIP2103), $V_{SS} = V_{HS}$ = 0V, V_{BAT} = 18V (for HIP2104), LI = HI = 0V. No load on HO and LO unless otherwise specified.
Boldface limits apply across the operating junction temperature range, -40°C to +125°C. (Continued)

Parameters	Symbol	Test Conditions	T_J = +25°C			T_J = -40°C to +125°C		Unit
			Min	Typ	Max	Min (Note 12)	Max (Note 12)	
Peak Pull-Up Current	I_{HOH12}	HI = 1 V_{DD} = 12V, C_{LOAD} = 1000pF		1				A
	I_{HOH5}	HI = 1 V_{DD} = 5V, C_{LOAD} = 1000pF (HIP2103 only)		1				A
Peak Pull-Down Current	I_{HOL12}	HI = 0 V_{DD} = 12V, C_{LOAD} = 1000pF		2				A
	I_{HOL5}	HI = 0 V_{DD} = 5V, C_{LOAD} = 1000pF (HIP2103 only)						A

Notes:

12. Parameters with Min and/or Max limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
13. The UV lockout does not disable the V_{DD} and V_{CC} outputs.

2.5 AC Electrical Specifications

V_{DD} = 12V, GND = 0V, No Load on OUTA or OUTB, Unless Otherwise Specified. V_{DD} load = 1µF and V_{CC} load = 1µF (HIP2104 only)
Boldface limits apply across the operating junction temperature range, -40°C to +125°C.

Parameters	Symbol	Test Conditions	T_J = +25°C			T_J = -40°C to +125°C		Unit
			Min	Typ	Max	Min	Max	
VDen and VCen Turn-On Delay (Figure 8) (HIP2104 only)	t_{VDen} t_{VCen}	VDen = VCen = 1, $V_{CC} = V_{DD}$ = 10%, V_{BAT} = 50V		1.69		**1.0**	**2.5**	ms
VDen and VCen Turn-on Delay (Figure 8) (HIP2104 only)	t_{VDen} t_{VCen}	VDen = VCen = 1, $V_{CC} = V_{DD}$ = 10%, V_{BAT} = 18V		1.68		**1.1**	**2.54**	ms
VDen and VCen Turn-on Delay Matching (Figure 8) (VDen - VCen) (HIP2104 only)	t_{VenM}	VDen = VCen = 1, V_{CC} = 10%, V_{DD} = 10% V_{BAT} = 50V		40		**-290**	**340**	ns
VDen and VCen Turn-on Delay Matching (Figure 8) (VDen - VCen) (HIP2104 only)	t_{VenM}	VDen = VCen = 1, V_{CC} = 10%, V_{DD} = 10% V_{BAT} = 18V		40		**-290**	**350**	ns
LO Turn-Off Propagation Delay (LI to LO falling) (Figure 9)	t_{FL12}	HI = 0, LI = 1 to 0 V_{DD} = 12V		27		**13**	**39**	ns
	t_{FL5}	HI = 0, LI = 1 to 0 V_{DD} = 5V (HIP2103 only)		30		**23**	**46**	ns
HO Turn-Off Propagation Delay (HI to HO falling) (Figure 9)	t_{FH12}	LI = 0, HI = 1 to 0 V_{DD} = 12V		23		**10**	**35**	ns
	t_{FH5}	LI = 0, HI = 1 to 0 Vv = 5V (HIP2103 only)		27		**19**	**38**	ns
LO Turn-On Propagation Delay (LI to LO rising) (Figure 9)	t_{RL12}	HI = 0, LI = 0 to 1 V_{DD} = 12V		21		**7**	**32**	ns
	t_{RL5}	HI = 0, LI = 0 to 1 V_{DD} = 5V (HIP2103 only)		25		**12**	**37**	ns
HO Turn-On Propagation Delay (HI to HO rising) (Figure 9)	t_{RH12}	LI = 0, HI = 0 to 1 V_{DD} = 12V		23		**9**	**35**	ns
	t_{RH5}	LI = 0, HI = 0 to 1 V_{DD} = 5V (HIP2103 only)		28		**15**	**40**	ns
Turn-On/Off Propagation Mismatch (HO rising to LO falling) (Figure 9)	t_{MONHL}	LI = 1 -> 0 HI = 0 -> 1		-2.5		**-8**	**+3**	ns
Turn-On/Off Propagation Mismatch (LO rising to HO falling) (Figure 9)	t_{MONLH}	HI = 1 -> 0 LI = 0 -> 1		-4.2		**-9.0**	**+5.4**	ns

V_{DD} = 12V, GND = 0V, No Load on OUTA or OUTB, Unless Otherwise Specified. V_{DD} load = 1µF and V_{CC} load = 1µF (HIP2104 only)
Boldface limits apply across the operating junction temperature range, -40°C to +125°C. (Continued)

Parameters	Symbol	Test Conditions	T_J = +25°C			T_J = -40°C to +125°C		Unit
			Min	Typ	Max	Min	Max	
LO Output Rise Time (10% to 90%)	t_{R12}	CL = 1nF V_{DD} = 12V		20.5		**7**	**35**	ns
	t_{R5}	CL = 1nF V_{DD} = 5V (HIP2103 only)		19.5		**6**	**32**	ns
HO Output Rise Time (10% to 90%)	t_{R12}	CL = 1nF V_{DD} = 12V		21		**8**	**35**	ns
	t_{R5}	CL = 1nF V_{DD} = 5V (HIP2103 only)		21		**8**	**34**	ns
LO Output Fall Time (90% to 10%)	t_{F12}	CL = 1nF V_{DD} = 12V		17		**3**	**30**	ns
	t_{F5}	CL = 1nF V_{DD} = 5V (HIP2103 only)		17		**3**	**30**	ns
HO Output Fall Time (90% to 10%)	t_{F12}	CL = 1nF V_{DD} = 12V		16		**2**	**30**	ns
	t_{F5}	CL = 1nF V_{DD} = 5V (HIP2103 only)		16		**1.5**	**29**	ns
Time Delay to Set Sleep Mode (Note 14, Figure 7)	t_{SlpS}	HI = LI = 0 -> 1		17		**9**	**27**	µs
Time Delay to Reset Sleep Mode (Note 14, Figure 7)	t_{SlpR}	HI = 0, LI = 0 -> 1		17		**9**	**27**	µs

Note:
14. When HI and LI are on simultaneously, HO and LO are never on simultaneously. This feature is intended to initiate sleep. This feature cannot be used to prevent shoot-through for normal alternating switching between LI and HI. Dead time must be provided when HI = 0 -> LI = 1, or LI = 0 -> HI = 1. See Timing Diagrams (Figure 7 on page 13).

2.6 Timing Diagrams

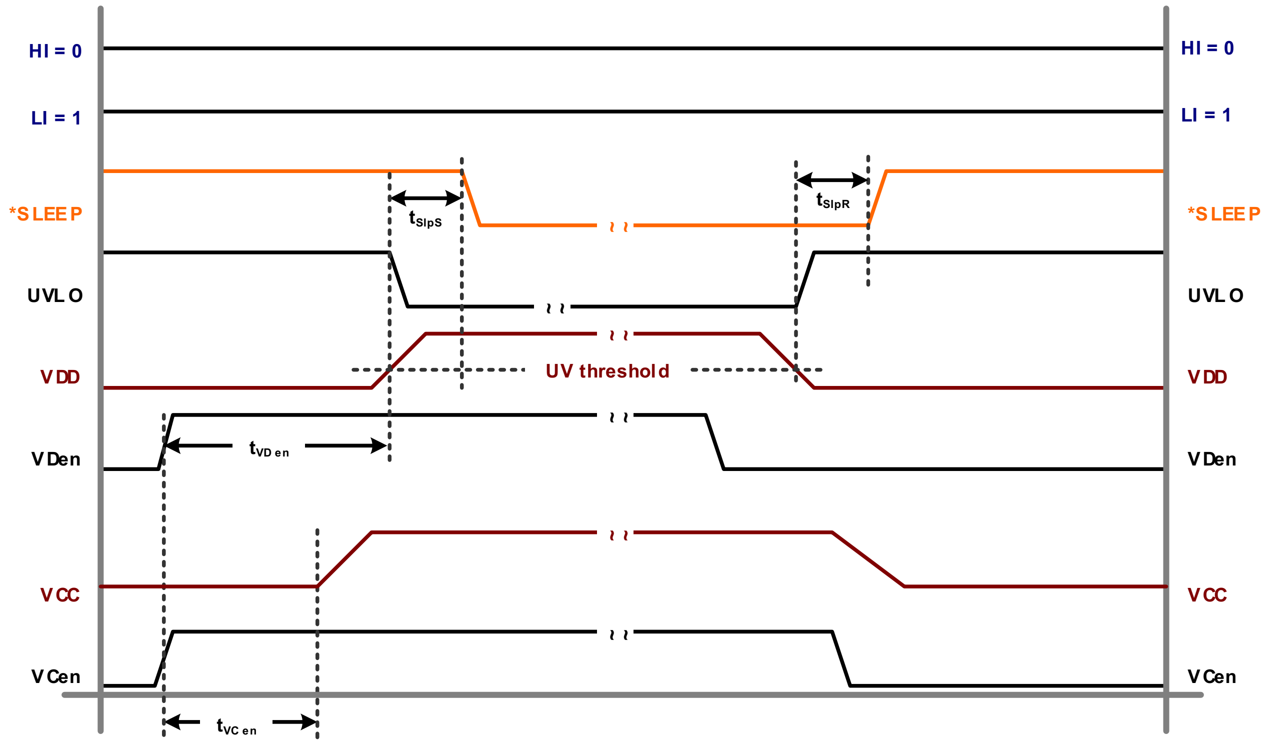


Figure 6. VDD Power-On/Off Timing for Sleep Mode

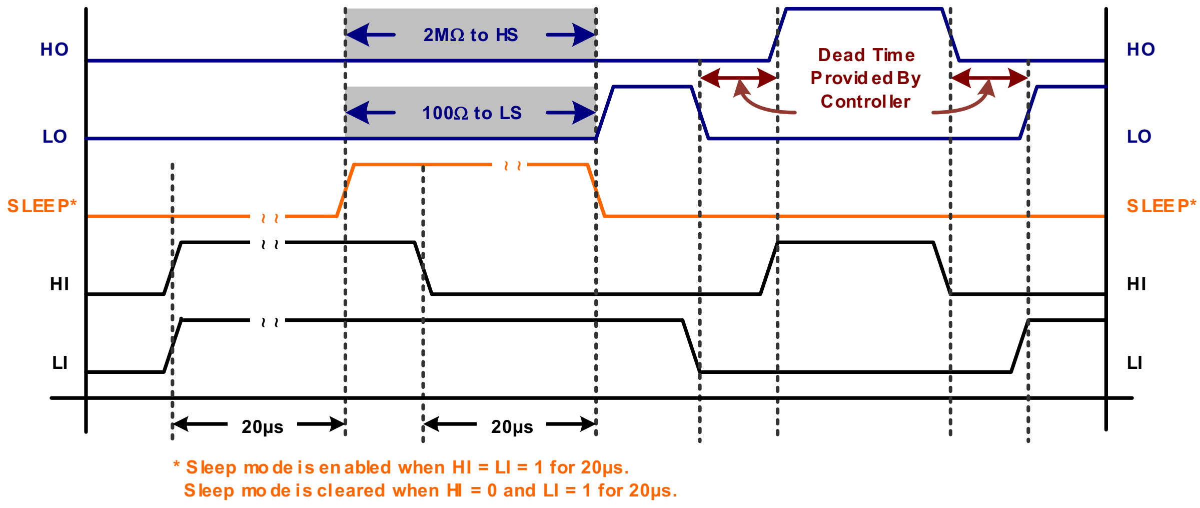


Figure 7. Sleep Mode Enabled or Cleared by HI and LI Inputs

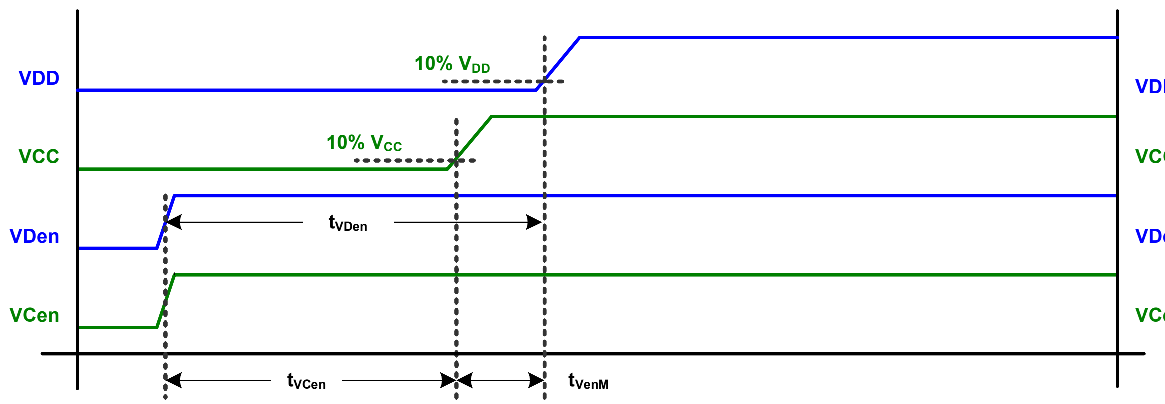


Figure 8. VCen and VDen Delay Matching

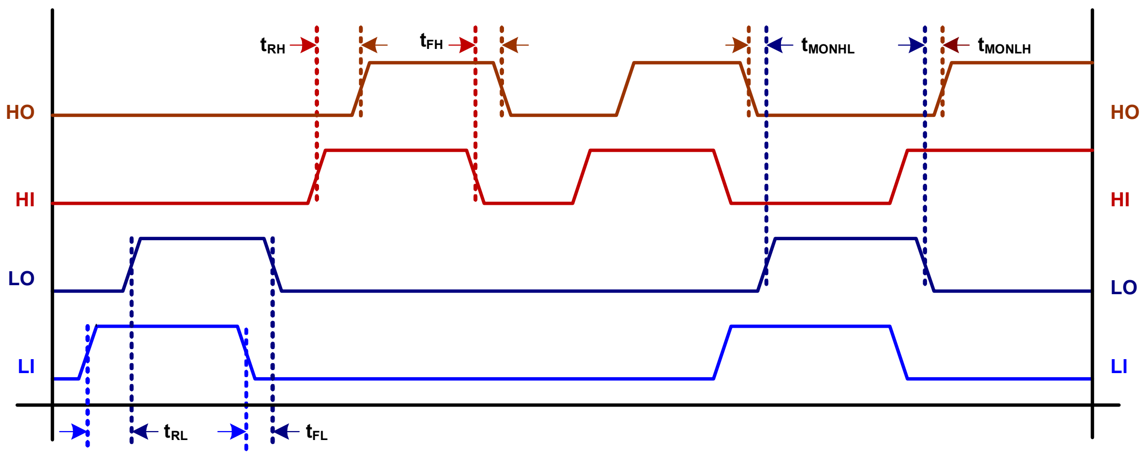


Figure 9. Propagation Delays

3. Typical Perfomance Curves

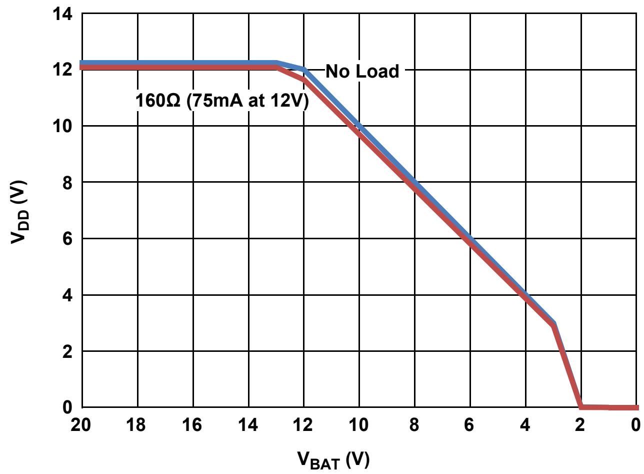


Figure 10. V_{DD} Dropout vs V_{BAT} (HIP2104 Only)

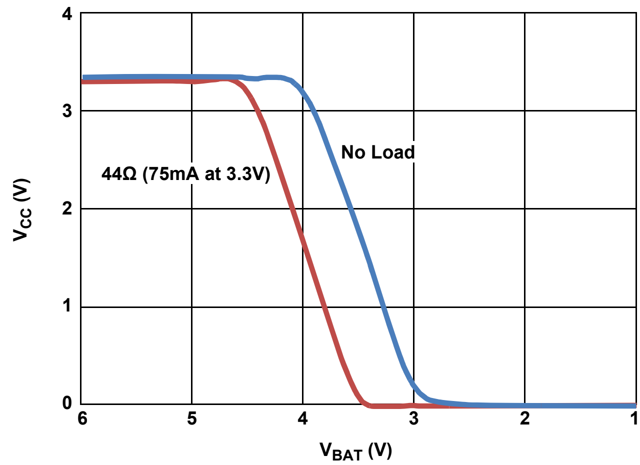


Figure 11. V_{CC} Dropout vs V_{BAT} (HIP2104 Only)

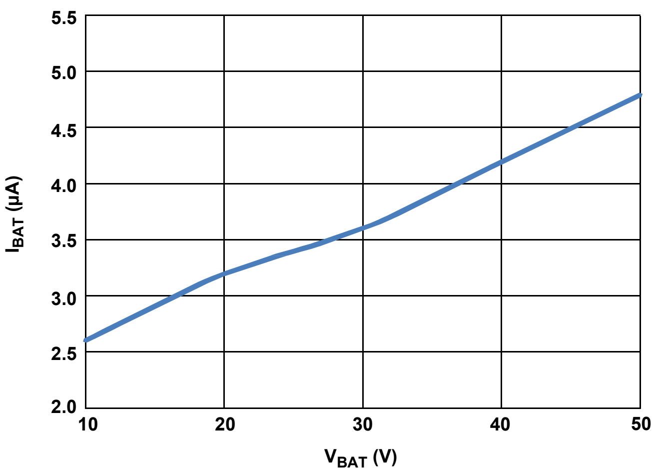


Figure 12. HIP2104 Shutdown Current (VCEN = VDEN = 0, HS = V_{BAT})

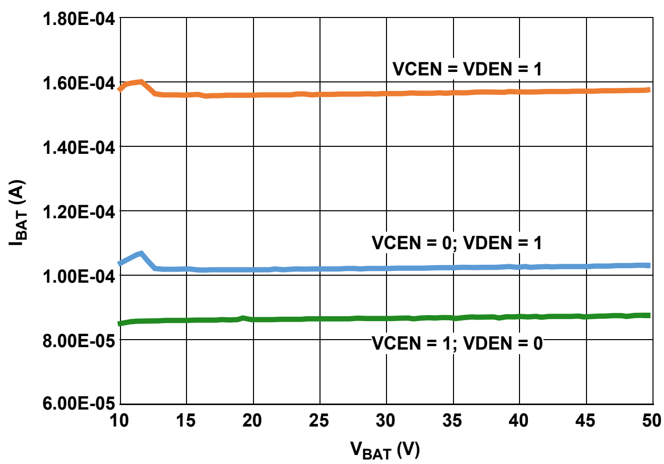


Figure 13. HIP2104 V_{BAT} Current vs V_{BAT} Voltage

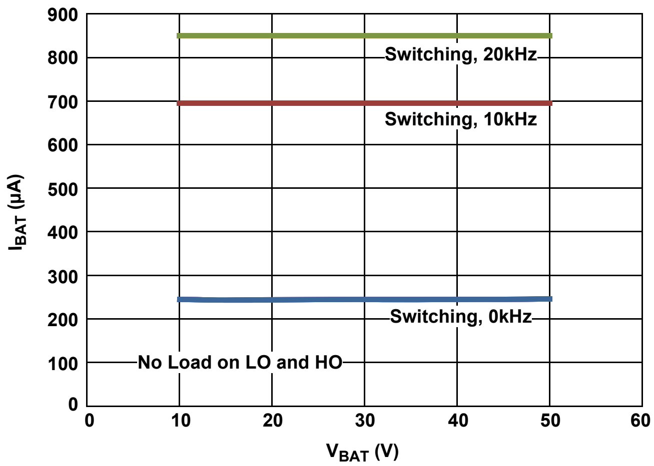


Figure 14. HIP2104 V_{BAT} Operating Current

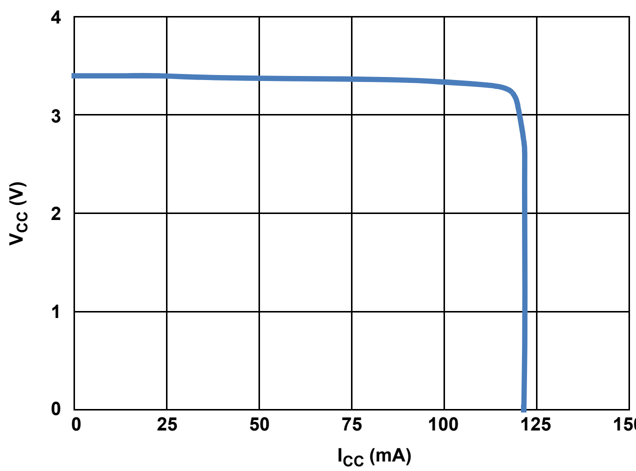


Figure 15. HIP2104 V_{CC} Current Limit

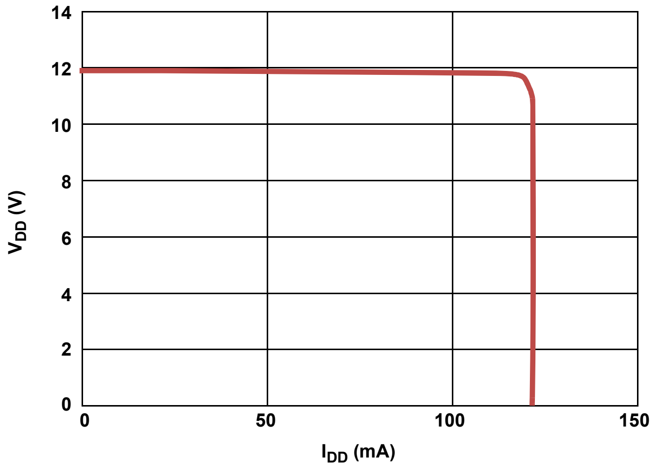


Figure 16. HIP2104 V_{DD} Current Limit

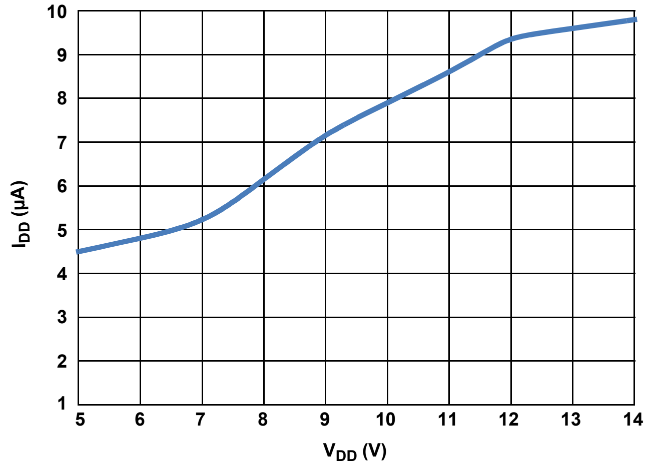


Figure 17. HIP2103 Sleep Current (HI = LI = 1)

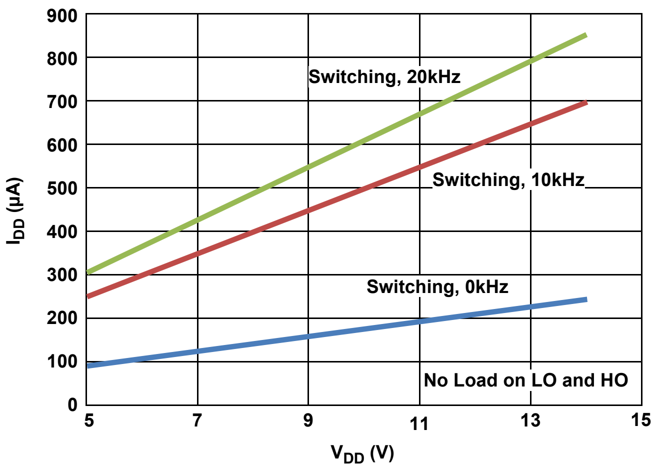


Figure 18. HIP2103 Operating Current

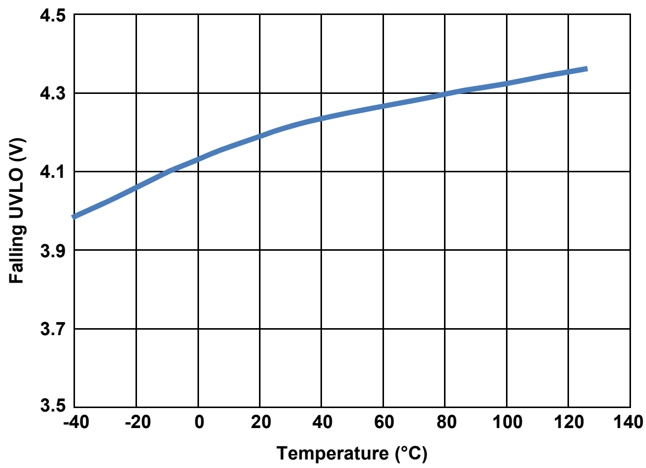


Figure 19. HIP2103 and HIP2104 Falling VDD Undervoltage Lockout Threshold

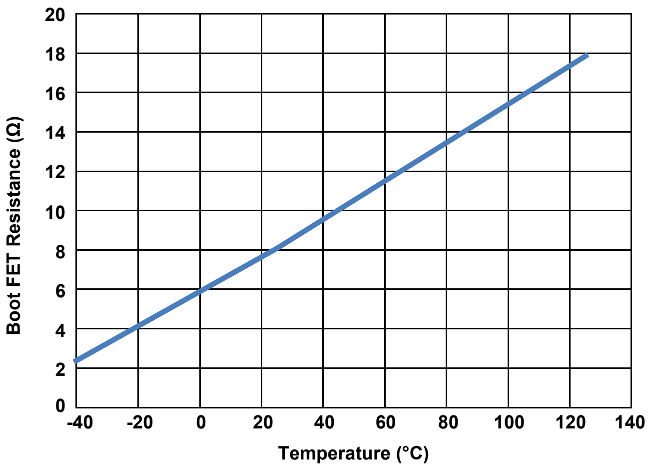


Figure 20. Boot FET Resistance

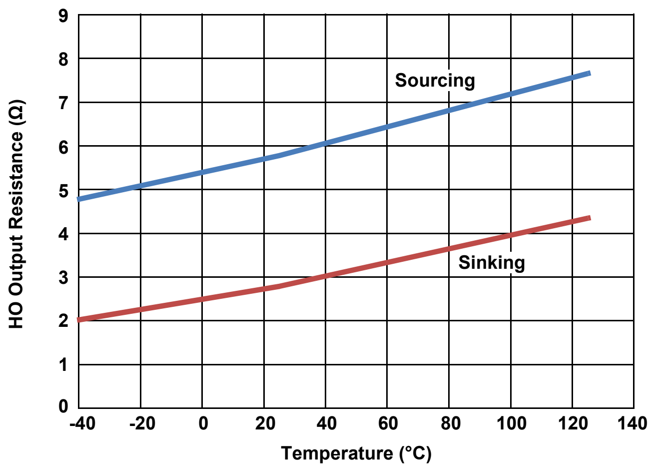


Figure 21. HO Output Resistance

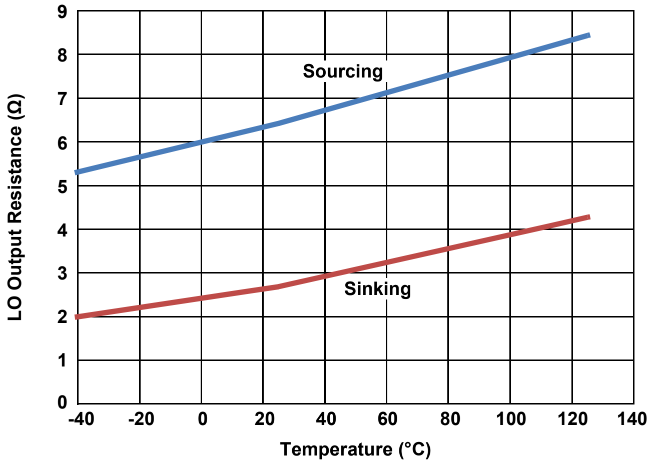


Figure 22. LO Output Resistance

4. Functional Description

The HIP2103 has independent control inputs, LI and HI, for each output, LO and HO. There is no logic inversion for these input/output pairs. To minimize the possibility of shoot-through failures of the bridge FETs caused by improper LI and HI signals from an external controller, internal logic in the driver prevents both outputs being high simultaneously. When either input is high, the high input must go low before a high on the other input propagates to its respective drive output. If both inputs are high simultaneously, both outputs are low. If one input is high, followed by the other input going high, the internal logic prevents any shoot through. Note that the internal logic does not prevent shoot-through if the dead time provided by the external controller is not sufficiently long as required by the turn-on and turn-off times of the bridge FETS.

If both inputs are high simultaneously for longer than 30µs, the driver initiates a Sleep Mode to reduce the bias current to minimize the battery drain. When in Sleep Mode, the HO output is in a high-impedance state (2MΩ between HO and HS) and the LO output is held low with an active 100Ω pull-down resistor. The 100Ω pull-down prevents inadvertent shoot-through resulting from transients on the bridge voltage while both drivers are in Sleep Mode.

The Undervoltage Lockout (UVLO) on V_{DD} drives HO and LO low when VDD is less than the UV threshold. Sleep Mode is initiated if UVLO is asserted for longer than 30µs.

The high-side driver bias is established by the boot capacitor connected between HB and HS. The charge on the boot capacitor is provided by the internal boot FET that is connected between VDD and HB. The current path to charge the boot capacitor is enabled (boot FET is on) when the drain voltage on the low-side bridge FET (VHO) is <1V and HO = 0. When the boot FET is on, the boot capacitor is charged to approximately V_{DD}.

The boot FET turns off when H0 = 1. The boot capacitor provides the charge necessary to turn on the FET and maintains the bias voltage on the high-side driver for the duration of the period while the FET is on. See "Selecting the Boot Capacitor Value" on page 18 for details on selecting the boot capacitor value.

The peak charge current is limited in amplitude by the inherent resistance of the boot FET and by the delta voltage between V_{DD} and the drain-source voltage of the low-side bridge FET (V_{HS}) less the boot capacitor voltage. Assuming that the low-side FET's on-time is sufficiently long to fully charge the boot capacitor, the boot voltage charges very close to V_{DD} (less the voltage across the drain-source of the low-side bridge FET).

When the HI input transitions high, the high-side bridge FET is driven on. Because the HS node is connected to the source of the high-side FET, the HS node rises almost to the level of the bridge voltage, V_{BAT} (less the conduction voltage across the bridge FET). Because the boot capacitor voltage is referenced to the source voltage of the high-side FET, the HB node is V_{DD} volts above the HS node. Simultaneously with HI = 1, the boot FET is turned off preventing the boot capacitor from discharging back to VDD. Because the high-side driver circuit is referenced to the HS node, the HO output is now approximately $V_{HB} + V_{BAT}$ above ground.

During the low-to-high transition of the phase node (HS), the boot capacitor sources the necessary gate charge to fully enhance the high-side bridge FET gate. After the gate of the bridge FET is fully charged, the boot capacitor no longer sources charge to the gate but continues to provide bias current to the high-side driver through out the period while the high-side bride FET is on.

To prevent the voltage on the boot capacitor from drooping excessively, the boot capacitor value must be sized appropriately. If the boot voltage droops to the UVLO threshold, the high-side FET is turned off to prevent damage due to insufficient gate voltage.

4.1 HIP2104 LDOs

The HIP2104 integrates two internal LDOs, VCC and VDD. The 3.3V on VCC provides bias for an external MCU or other controller. The 12V on VDD provides bias for the gate driver outputs and bootstrap circuit on the HIP2104 and additionally for biasing the VDD pin on one or more HIP2103 when used in a 3-phase Brushless DC (BLDC) or multi-phase DC/DC half-bridge topologies. The VCC LDO's maximum output current is 75mA at 3.3V. The VDD LDO's maximum output is also 75mA at 12V. **Note:** Dynamic operating current on the HIP2103/HIP2104 drivers is a function of operating frequency and capacitive loading, which determines the loading on the VDD LDO.

4.2 Input Signals

All input logic to the HIP2103 and HIP2104 is compatible with 3.3V or 5V logic levels. The HI and LI inputs are tolerant to voltages up to the V_{DD} supply. The VDen and VCen (the HIP2104 LDO's VDD and VCC enable signals) inputs are tolerant to voltages up to V_{BAT}.

A fail-safe mechanism is included to improve system reliability and to minimize the possibility of catastrophic bridge failures due to controller malfunction. Internal logic prevents both outputs from turning on simultaneously when HI and LI are both high simultaneously. Dead time is still required on the rising edge of the HI (or LI) input when the LI (or HI) input transitions low.

4.3 Sleep Mode

The HIP2103 and HIP2104 feature a Sleep Mode operation where the drivers enter a low power state when inactive. The HIP2103 and HIP2104's low Sleep Mode current (quiescent current consumed by VDD bias) is invoked by setting both the LI and HI inputs of each driver high simultaneously or if the VDD voltage enters into UVLO. See Figures 6 and 7 for details on entering and exiting Sleep Mode. Sleep Mode only disables the half-bridge driver outputs. The HIP2104 Sleep Mode does not control the operation of the VCC and VDD LDO. They are controlled only by the VCen and VDen inputs. Upon V_{DD} power up (and clearing UVLO status), the HIP2103 and HIP2104 remains in Sleep Mode until it is exited by setting LI = 1 for time period t_{SlpR}.

4.4 Selecting the Boot Capacitor Value

The boot capacitor value is chosen not only to supply the internal bias current of the high-side driver but more significantly, to provide the gate charge of the driven FET without causing the boot voltage to sag excessively. In practice, the boot capacitor should have a total charge that is about 20 times the gate charge of the driven power FET for approximately a 5% drop in voltage after charge has been transferred from the boot capacitor to the gate capacitance.

The following parameters are required to calculate the value of the boot capacitor for a specific amount of voltage droop when using the HIP2103 and HIP2104. In the following example, some values used are specific to the HIP2103 and HIP2104 and others are arbitrary. The values should be changed to comply with the actual application.

V_{DD} = 12V	This is the nominal value of VDD for the HIP2104
VHB = V_{DD} = VHO	High-side driver bias voltage referenced to VHS
Period = 100µs	This is the longest expected switching period
IHB = I_{HBS20K} + I_{HB20K} = 295µA	High-side driver bias current at 20kHz
RGS = 10kΩ	Gate-source resistor
Ripple = 5%	Desired ripple voltage on the boot capacitor
Igate_leak = 100nA	Gate leakage current (from vendor datasheet)
Qg40_12V = 45nC	From Figure 23 on page 19

The following equations calculate the total charge required for the Period:

Qc = Qg40_12V + Period x (IHB + VHO/RGS + Igate_leak)

Cboot = Qc/(Ripple * V_{DD})

Cboot = 0.324µF

If the gate-to-source resistor is removed (RGS is usually not needed or recommended):

Cboot = 0.124µF

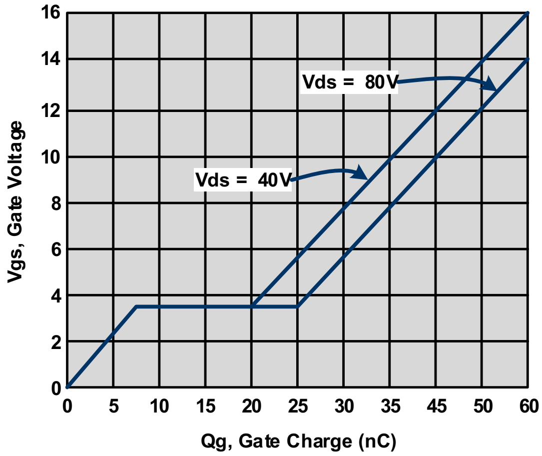


Figure 23. Typical MOSFET Gate Charge vs Gate Voltage

5. Application Examples

Figures 3, 4, and 5 are examples of how the HIP2103 and HIP2104 can be configured for various motor drive applications with the HIP2104 supplying the 12V bias for the other HIP2103s and the V_{CC} (3.3V) bias for the controller. VCen and VDen are used to turn on and off the internal linear regulators of the HIP2104. Because entire switching of the bias supplies is implemented with logic, a signal switch, instead of a power switch, can be used to turn on and off the driver and controller. A switch debouncing delay of 1ms is provided on VDen and VCen.

The external diode on V_{BATT} is used to hold up the voltage on the V_{BAT} input in the presence of severe ripple as usually seen on Li-ion batteries.

In the case of the HIP2104, when VDen is low, the driver sections enter Sleep Mode. When VCen is low, the bias to the controller is removed, resulting in the lowest possible idle current in both the controller and the driver minimizing the drain on the battery when the motor drive is off. Sleep Mode can also be initiated on the HIP2104 by driving HI and LI high simultaneously. In this case, the Sleep Mode current is substantially higher (~250µA) because the V_{DD} and V_{CC} outputs are still active.

For the HIP2103, Sleep Mode is initiated when HI and LI are both high simultaneously as previously described. If VDD is provided by an accompanying HIP2104, turning off the VDD output of the HIP2104 also results with virtually no sleep current in the HIP2103 because there is no bias. For example, in the BLDC configuration, the sleep mode current is ~5µA (in the HIP2104) and no current in both of the HIP2103s.

5.1 Transients on the HS Node

An important operating condition that is frequently overlooked is the transient on the HS pin that occurs when the bridge FETs turn on or off. The Absolute Maximum negative transient (see page 8) allowed on the HS pin is -10V without any time restrictions on the duration of the transient. In most well designed PCBs, all that is required is that the transient is less negative than -10V.

The negative transient on the HS pin is the result of the parasitic inductance of the low-side drain-source conductor path on the PCB. Even the parasitic inductance of the low-side FET body contributes to this transient. When the high-side bridge FET turns off (see Figure 24 on page 21), as a consequence of the inductive characteristics of a motor load, the current that was flowing in the high-side FET (blue) must rapidly commutate through the low-side FET (red). The amplitude of the negative transient impressed on the HS node is (L x di/dt), where L is the total parasitic inductance of the low-side FET drain-source path and di/dt is the rate at which the high-side FET is turned off. With the increasing current levels of new generation motor drives, appropriately clamping of this transient becomes more significant for the proper operation of bridge drivers. Fortunately, the HIP2103 and HIP2104 can withstand greater amplitudes of negative transients than what is available in many other bridge drivers. The maximum negative voltage on the HS pin is rated for -10V with no time during limit.

Another component of negative voltage is from the body diode of the low-side FET during the dead time. When current is flowing from source to drain, the conduction voltage is approximately 1V to 1.5V negative impressed on the HS pin (possibly greater during fault load conditions). Because the HIP2103 and HIP2104 are rated for -10V without any time constraints, this negative voltage component is of no consequence.

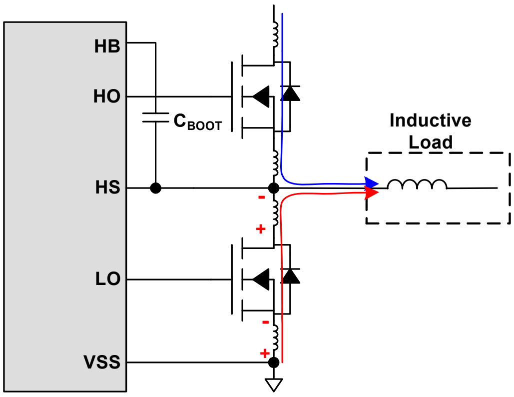


Figure 24. Parasitic Inductance on HS Node

In the unlikely event that the negative transient exceeds -10V, there are several ways of reducing the negative amplitude of this transient. If the bridge FETs are turned off more slowly to reduce di/dt, the amplitude is reduced but at the expense of more switching losses in the FETs. Careful PCB design also reduces the value of the parasitic inductance. However, in extreme cases, these two solutions by themselves may not be sufficient. Figure 25 shows a simple method for clamping the negative transient. Two series connected, fast 1A PN junction diodes are connected between HS and VSS as shown. It is important that these diodes are placed as close as possible to the HS and VSS pins to minimize the parasitic inductance of this current path between the two pins. Two diodes in series are required because they are in parallel with the body diode of the low-side FET. If only one diode is used for the clamp, it conducts some of the negative load current that is flowing in the body diode of the low-side FET.

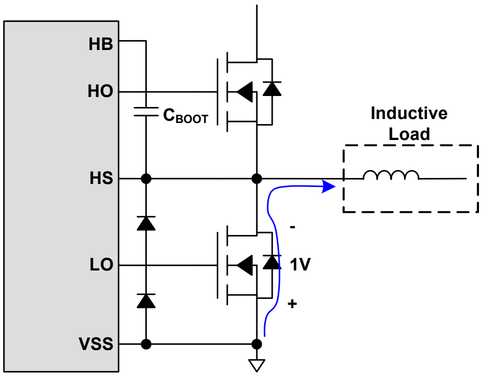


Figure 25. Two Clamping Diodes to Suppress Negative Transients

An alternative to the two series connected diodes is one diode and a resistor (Figure 26 on page 22). In this case, it is necessary to limit the current in the diode with a small value resistor, R_{HS}, connected between the phase node of the 1/2 bridge and the HS pin. Observe that R_{HS} is effectively in series with the HO output and serves as a peak current limiting gate resistor on HO.

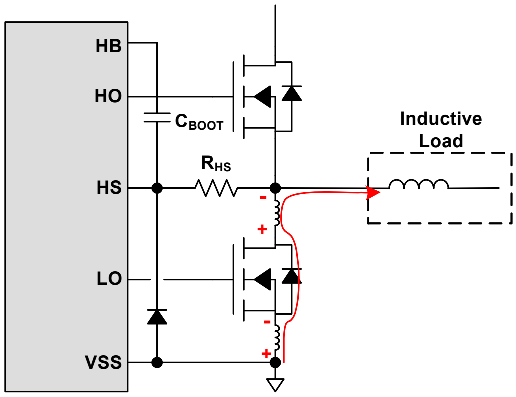


Figure 26. Resistor and Diode Negative Transient Clamp

The value of R_{HS} is determined by how much average current in the clamping diode is acceptable. Current in the low-side FET flows through the body diode during the dead time resulting with a negative voltage on HS that is typically about -1.5V. When the low-side FET is turned on, the current through the body diode is shunted away into the channel and the conduction voltage from source to drain is typically much less than the conduction voltage through the body diode. Consequently, significant current flows in the clamping diode only during the dead time. Because the dead time is much less than the low-side FET's on-time, the resulting average current in the clamping diode is very low. The value of R_{HS} is then chosen to limit the peak current in the clamping diode and usually just a few ohms is necessary.

The methods to clamp the negative transients with diodes can still result with high frequency oscillations on the HS node depending on the parasitics of the PCB design. An alternative to the clamping diode in Figure 26 is a small value capacitor instead of the diode. This capacitor and R_{HS} is very effective for minimizing the negative spike amplitude and oscillations.

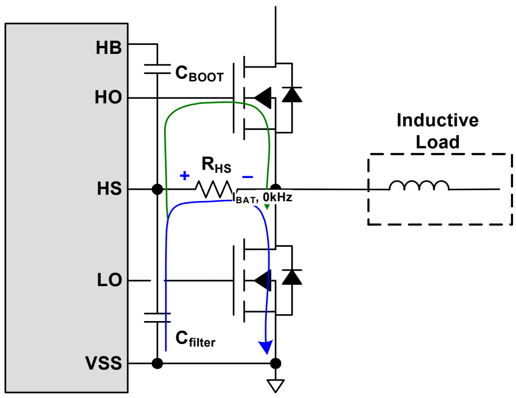


Figure 27. Resistor and Capacitor Negative Transient Filter

However, this solution also has its limitations. Depending on the value of the filter capacitor and the PWM switching frequency, R_{HS} can dissipate significant power because the voltage on the capacitor is switching between the bridge voltage and ground. Usually, the power dissipated by R_{HS} is small because the switching frequency for most motor drives is <20kHz and the value used for C_{filter} is typically about 1000pF.

Another issue is that the charge on C_{filter} is partially transferred to the gate of the high-side FET when the low-side FET turns on. When the phase node goes low, a voltage is impressed across R_{HS} as shown in Figure 27. Because HO is low, the voltage across R_{HS} is also across the gate of the high-side FET. If the filter capacitor is very large, the voltage on the gate approaches the bridge voltage turning on the high-side FET resulting with shoot-through. Fortunately, the voltage across R_{HS} is much less than the bridge voltage for two reasons. First, the voltage across R_{HS} is determined by the turn-on time of the low-side FET. As the low-side FET is turning on, the charge on the filter capacitor is depleting lessening the voltage across R_{HS}. Also, because the relatively large gate capacitance of the high-side FET is in parallel with $R_{HS,}$ the voltage impressed on the gate is further reduced. In a practical application using values of C_{filter} = 4700pF and R_{HS} = 1Ω, the voltage impressed on the bridge FET is less than 1V.

The emphasis of suppressing transients on the HS pin has been with negative transients. **Note:** A similar transient with a positive polarity occurs when the low-side FET turns off. This is usually not a problem unless the bridge voltage is close to the maximum rated operating voltage of 50V. **Note:** The maximum voltage ratings for the HS and HB nodes also must be observed when the positive transient occurs.

The maximum rating for (VHB - VHS) must also not be overlooked. When a negative transient, Vneg, is present on the HS pin, the voltage differential across HB and HS approaches VDD + Vneg. If the transient duration is short compared to the charging time constant of the boot diode and boot capacitor, the voltage across HB and HS is not significantly affected. However, another source of negative voltage on the HS pin increases the boot capacitor voltage. While current is flowing from the source to drain of the low-side FET during the dead time, the current flows through body diode of the FET. Depending on the size of the FET and the amplitude of the reverse current, the voltage across the diode can be as high as -1.5V and much higher during a load fault. Because this negative voltage has little impedance, the boot capacitor can charge to a voltage greater than VDD (for example VDD + 1.5V). It may be necessary to either clamp the voltage as described in Figures 25 through 27 and/or keep the dead time as short as possible.

6. General PCB Layout Guidelines

The AC performance of the HIP2103 and HIP2104 depends significantly on the design of the PCB. The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET.
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they are usually more effective than parallel traces.
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt induces currents and consequently, noise voltages in the low level signal lines.
- When practical, minimize impedances in low-level signal circuits. Magnetically induced noise on a 10kΩ resistor, is 10x larger than the noise on a 1kΩ resistor.
- Be aware of magnetic fields emanating from motors and inductors. Gaps in the magnetic cores of these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling.
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductance in the V_{BAT}, V_{DD}, and GND leads. To be effective, these capacitors must also have the shortest possible conduction paths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits, especially on LO and LO. If an external gate resistor is unacceptable, the layout must be improved to minimize lead inductance.
- Keep high dv/dt nodes away from low level circuits. Use guard banding to shunt away dv/dt injected currents from sensitive circuits.
- Avoid having a signal ground plane under a high amplitude dv/dt circuit. The parasitic capacitance of a ground plane, Cp, relative to the high amplitude dv/dt circuit results in injected (Cp x dv/dt) currents into the signal ground paths where C is the parasitic capacitance of the ground plane.
- Do power dissipation and voltage drop calculations of the power traces. Many PCB/CAD programs have built in tools for calculation of trace resistance. The internet is also a good source for resistance calculators for PCB trace resistance.
- Large power components (such as power FETs, electrolytic capacitors, and power resistors) have internal parasitic inductance that cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components, especially parasitic inductance.

7. General EPAD Heatsinking Considerations

The EPAD of the HIP2103 and HIP2104 is electrically connected to VSS through the IC substrate. The EPAD has two main functions:

- To provide a quiet signal ground
- To provide heat sinking for the IC

The EPAD must be connected to a ground plane and switching currents from the driven FETs should not pass through the ground plane under the IC.

Figure 28 is a PCB layout example of how to use vias to remove heat from the IC through the EPAD.

For maximum heatsinking, it is recommended that a ground plane, connected to the EPAD, is added to both sides of the PCB. A via array within the area of the EPAD conducts heat from the EPAD to the GND plane on the bottom layer. The number of vias and the size of the GND planes required for adequate heatsinking is determined by the power dissipated by the HIP2103 and HIP2104, the air flow, and the maximum temperature of the air around the IC.

Note that a separate plane is added under the high side drive circuits and is connected to HS. In a manner similar to the ground plane, the HS plane provides the lowest possible parasitic inductance for the HO/HS gate drive current loop.

See AN1899 “HIP2103 and HIP2104 3-phase, Full, or Half Bridge Motor Driver” for an example of PCB layout of a real application.

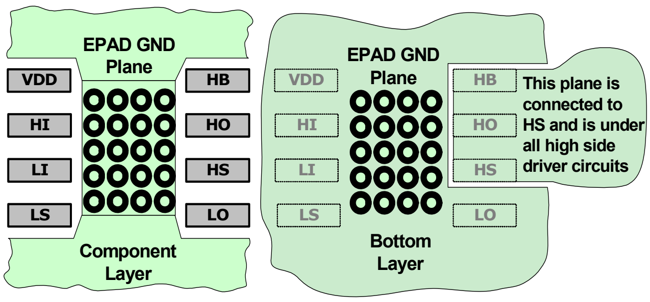


Figure 28. Typical PCB Pattern for Thermal Vias

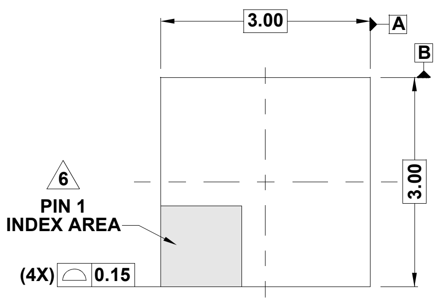
8. Revision History

Rev.	Date	Description
1.00	Jul.22.19	Applied new formatting throughout document. Updated Related Literature. Updated Features section. Updated Description on page 1. Added Label to Figure 2. Updated Block Diagram. Updated Pin Descriptions Updated Ordering information table by adding tape and reel information, adding boards, and updating notes. Updated Note 10. Added additional “Voltage on HS” and updated previous one in the Recommended Operating Conditions section. Removed VDD Rated Output Current and VCC Rated Output Current specifications from DC Electrical Specification table. Updated Sinking rDS(ON) specs (Typical from “6.1” to “2.68” and Minimum “4.4” to “0.61”). Updated Sourcing rDS(ON) specs (Typical from “11.9” to “6.47” and Minimum “9.7” to “2.3”). Updated Test condition for On Resistance specification. Updated Figure 6. Replaced Figure 13. Updated Labels on Figures 10 - 22. Added Input Signals, HIP2104 LDOs, and Sleep Mode sections. Removed About Intersil section. Updated POD L8.3x3A and L12.4x4A to the latest revisions changes are as follows: Tiebar Note updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). Updated Disclaimer
0.00	Nov.27.13	Initial release

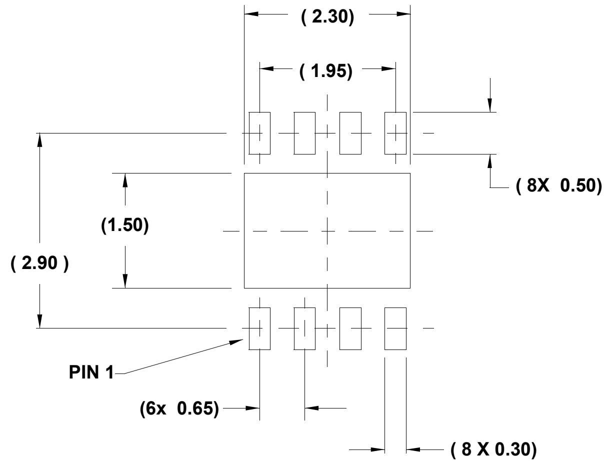
9. Package Outline Drawings

For the most recent package outline drawing, see L8.3x3A.

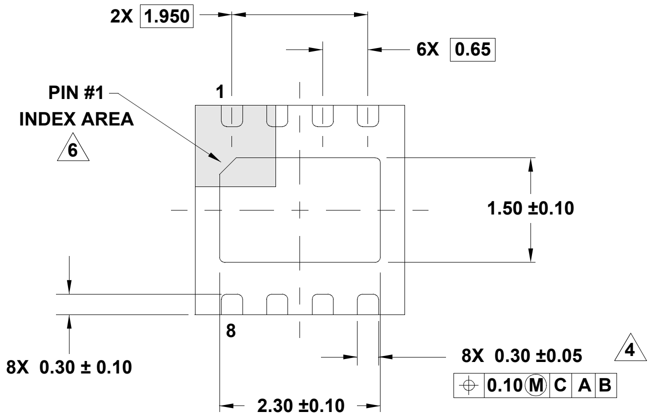
L8.3x3A
8 Lead Thin Dual Flat No-Lead Plastic Package (TDFN)
Rev 5, 5/15



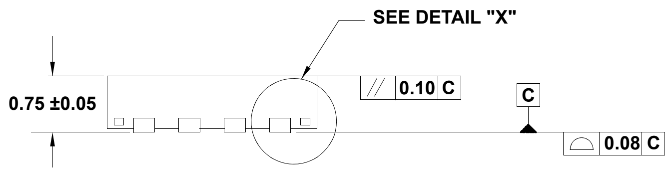
TOP VIEW



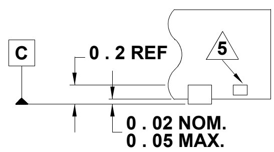
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



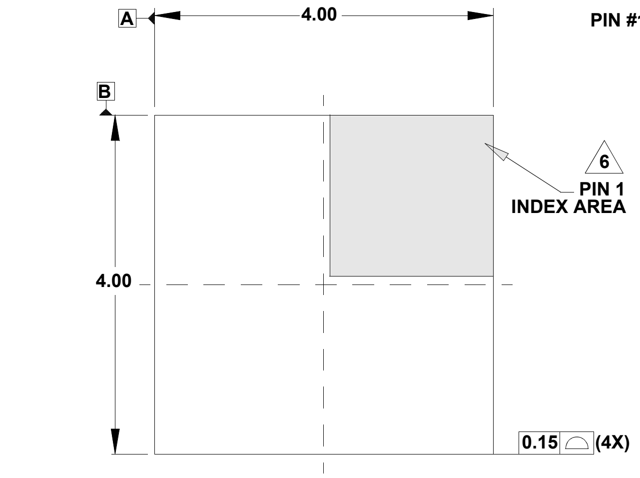
DETAIL "X"

NOTES:

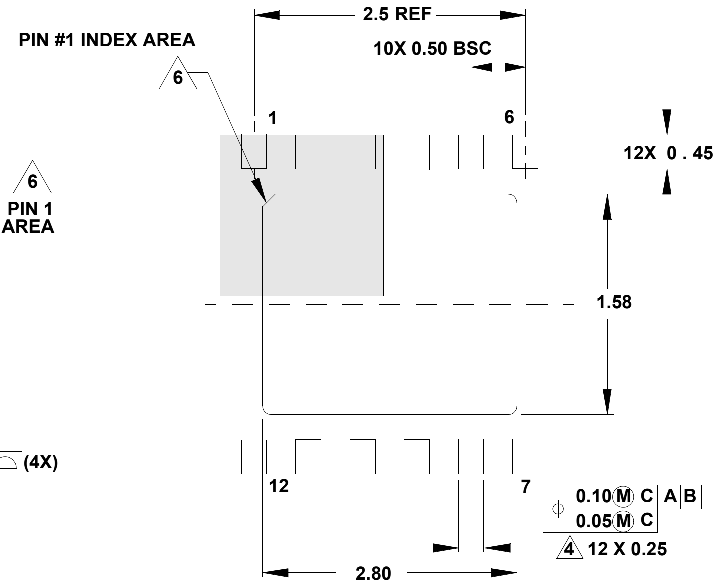
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

L12.4x4A
12 Lead Dual Flat No-Lead Plastic Package (DFN)
Rev 3, 3/15

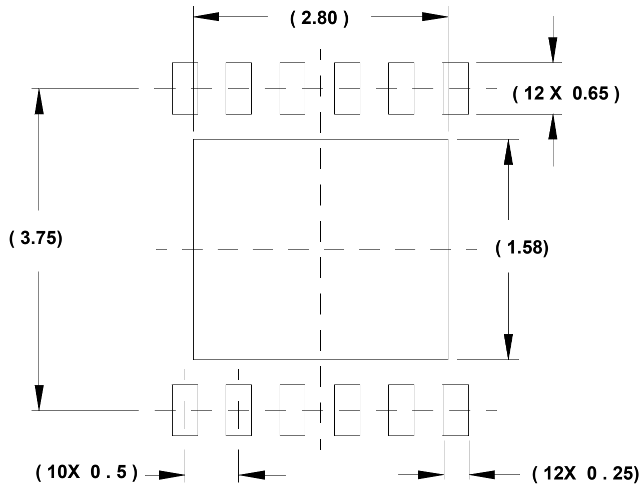
For the most recent package outline drawing, see L12.4x4A.



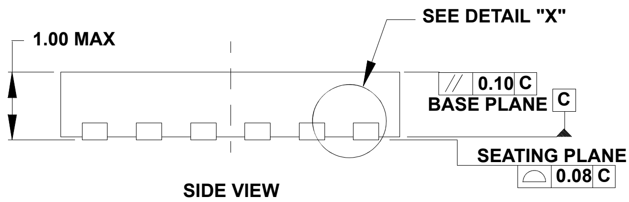
TOP VIEW



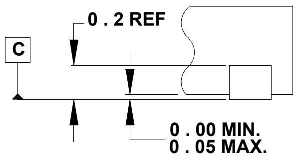
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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