

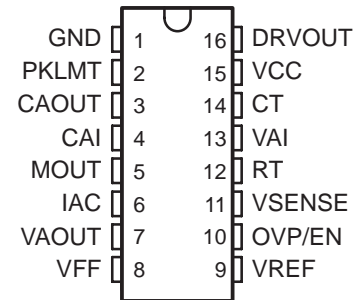


**THE DATASHEET OF
UCC3819N**



- Controls Boost Preregulator to Near-Unity Power Factor
- World Wide Line Operation
- Over-Voltage Protection
- Accurate Power Limiting
- Average Current Mode Control
- Improved Noise Immunity
- Improved Feed-Forward Line Regulation
- Leading Edge Modulation
- 150- μ A Typical Start-Up Current
- Low-Power BiCMOS Operation
- 10.8-V to 17-V Operation
- Programmable Output Voltage (Tracking Boost Topology)

D, DW, N, and PW PACKAGES
(TOP VIEW)



description

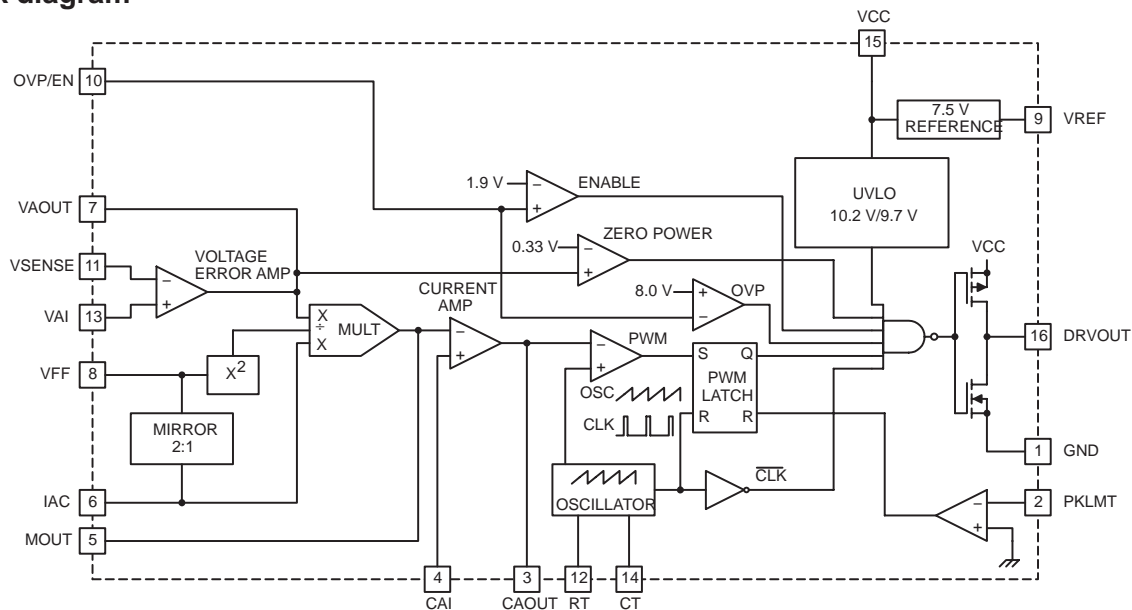
The UCC2819/UCC3819 provides all the functions necessary for active power factor corrected prerregulators. The controller achieves near unity power factor by shaping the ac-input line current waveform to correspond to that of the ac-input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

Designed in Texas Instrument's BiCMOS process, the UCC3819 offers new features such as lower start-up current, lower power dissipation, overvoltage protection, a shunt UVLO detect circuitry and a leading-edge modulation technique to reduce ripple current in the bulk capacitor.

The UCC3819 allows the output voltage to be programmed by bringing out the error amplifier noninverting input.

Available in the 16-pin D, DW, N, and PW packages.

block diagram



UDG-01009



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

UCC2819, UCC3819 PROGRAMMABLE OUTPUT POWER FACTOR PREREGULATOR

SLUS482B - APRIL 2001 – REVISED DECEMBER 2004

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, VCC	18 V
Gate drive current, continuous	0.2 A
Gate drive current	1.2 A
Input voltage, CAI, MOUT	8 V
Input voltage, PKLMT	5 V
Input voltage, VSENSE, OVP/EN, VAI	10 V
Input current, RT, IAC, PKLMT	10 mA
Maximum negative voltage, DRVOUT, PKLMT, MOUT	-0.5 V
Power dissipation	1 W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

AVAILABLE OPTIONS

T _J	PACKAGE DEVICES			
	D PACKAGE	DW PACKAGE	N PACKAGE	PW PACKAGE
0°C to 70°C	UCC3819D	UCC3819DW	UCC3819N	UCC3819PW
-40°C to 85°C	UCC2819D	UCC2819DW	UCC2819N	UCC2819PW

† The D, DW, and PW packages are available taped and reeled. Add TR suffix to device type (e.g. UCC3819DTR) to order quantities of 2500 devices per reel.

electrical characteristics, T_A = 0°C to 70°C for the UCC3819, -40°C to 85°C for the UCC2819, VCC = 12 V, R_T = 22 kΩ, C_T = 270 pF, (unless otherwise noted)

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply current, off	VCC = (VCC turnon threshold - 0.3 V)		150	300	μA
Supply current, on	VCC = 12 V, No load on DRVOUT	2	4	6	mA

UVLO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC turnon threshold		9.7	10.2	10.8	V
VCC turnoff threshold		9.4	9.7		V
UVLO hysteresis		0.3	0.5		V

voltage amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIO	VAOUT = 2.75 V, VCM = 3.75 V	-15		15	mV
VAI bias current	VAOUT = 2.75 V, VCM = 3.75 V		50	200	nA
VSENSE bias current	VSENSE = VREF, VAOUT = 2.5 V		50	200	nA
CMRR	VCM = 1 V to 7.5 V	50	70		dB
Open loop gain	VAOUT = 2 V to 5 V	50	90		dB
High-level output voltage	I _L = -150 μA	5.3	5.5	5.6	V
Low-level output voltage	I _L = 150 μA	0	50	150	mV

electrical characteristics, $T_A = 0^\circ\text{C}$ to 70°C for the UCC3819, -40°C to 85°C for the UCC2819, $V_{CC} = 12\text{ V}$, $R_T = 22\text{ k}\Omega$, $C_T = 270\text{ pF}$, (unless otherwise noted)

over voltage protection and enable

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over voltage reference		$V_{REF} + 0.48$	$V_{REF} + 0.50$	$V_{REF} + 0.52$	V
Hysteresis		300	500	600	mV
Enable threshold		1.7	1.9	2.1	V
Enable hysteresis		0.1	0.2	0.3	V

current amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input offset voltage	$V_{CM} = 0\text{ V}$, $V_{CAOUT} = 3\text{ V}$	-3.5	0	2.5	mV
Input bias current	$V_{CM} = 0\text{ V}$, $V_{CAOUT} = 3\text{ V}$		-50	-100	nA
Input offset current	$V_{CM} = 0\text{ V}$, $V_{CAOUT} = 3\text{ V}$		25	100	nA
Open loop gain	$V_{CM} = 0\text{ V}$, $V_{CAOUT} = 2\text{ V}$ to 5 V	90			dB
Common-mode rejection ratio	$V_{CM} = 0\text{ V}$ to 1.5 V , $V_{CAOUT} = 3\text{ V}$	60	80		dB
High-level output voltage	$I_L = -120\text{ }\mu\text{A}$	5.6	6.5	6.8	V
Low-level output voltage	$I_L = 1\text{ mA}$	0.1	0.2	0.5	V
Gain bandwidth product	See Note 1		2.5		MHz

voltage reference

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage, (UCC3819)	$T_A = 0^\circ\text{C}$ to 70°C	7.387	7.5	7.613	V
Input voltage, (UCC2819)	$T_A = -40^\circ\text{C}$ to 85°C	7.369	7.5	7.631	V
Load regulation	$I_{REF} = 1\text{ mA}$ to 2 mA	0		10	mV
Line regulation	$V_{CC} = 10.8\text{ V}$ to 15 V , See Note 2	0		10	mV
Short-circuit current	$V_{REF} = 0\text{ V}$	-20	-25	-50	mA

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Initial accuracy	$T_A = 25^\circ\text{C}$	85	100	115	kHz
Voltage stability	$V_{CC} = 10.8\text{ V}$ to 15 V	-1		1	%
Total variation	Line, temp, See Note 1	80		120	kHz
Ramp peak voltage		4.5	5	5.5	V
Ramp amplitude voltage (peak to peak)		3.5	4	4.5	V

- NOTES: 1. Ensured by design, Not production tested.
 2. Reference variation for $V_{CC} < 10.8\text{ V}$ is shown in Figure 2.

UCC2819, UCC3819 PROGRAMMABLE OUTPUT POWER FACTOR PREREGULATOR

SLUS482B - APRIL 2001 – REVISED DECEMBER 2004

electrical characteristics, $T_A = 0^\circ\text{C}$ to 70°C for the UCC3819, -40°C to 85°C for the UCC2819, $V_{CC} = 12\text{ V}$, $R_T = 22\text{ k}\Omega$, $C_T = 270\text{ pF}$, (unless otherwise noted)

peak current limit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PKLMT reference voltage		-15		15	mV
PKLMT propagation delay		150	350	500	ns

multiplier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{MOUT} , high line, low power output current, (0°C to 85°C)	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 1.25\text{ V}$	0	-6	-20	μA
I_{MOUT} , high line, low power output current, (-40°C to 85°C)	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 1.25\text{ V}$	0		-23	μA
I_{MOUT} , high line, high power output current	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 5\text{ V}$	-70	-90	-105	μA
I_{MOUT} , low line, low power output current	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.4\text{ V}$, $VA_{OUT} = 1.25\text{ V}$	-10	-19	-50	μA
I_{MOUT} , low line, high power output current	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.4\text{ V}$, $VA_{OUT} = 5\text{ V}$	-268	-300	-346	μA
I_{MOUT} , IAC limited	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.3\text{ V}$, $VA_{OUT} = 5\text{ V}$	-250	-300	-400	μA
Gain constant (K)	$I_{AC} = 300\text{ }\mu\text{A}$, $V_{FF} = 3\text{ V}$, $VA_{OUT} = 2.5\text{ V}$	0.5	1	1.5	1/V
I_{MOUT} , zero current	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.4\text{ V}$, $VA_{OUT} = 0.25\text{ V}$		0	-2	μA
	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 0.25\text{ V}$		0	-2	μA
I_{MOUT} , zero current, (0°C to 85°C)	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 0.5\text{ V}$		0	-3	μA
I_{MOUT} , zero current, (-40°C to 85°C)	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 0.5\text{ V}$		0	-3.5	μA
Power limit ($I_{MOUT} \times V_{FF}$)	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.4\text{ V}$, $VA_{OUT} = 5\text{ V}$	-375	-420	-485	μW

feed-forward

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VFF output current	$I_{AC} = 300\text{ }\mu\text{A}$	-140	-150	-160	μA

gate driver

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Pullup resistance	$I_O = -100\text{ mA}$ to -200 mA		5	12	Ω
Pulldown resistance	$I_O = 100\text{ mA}$		2	10	Ω
Output rise time	$C_L = 1\text{ nF}$, $R_L = 10\text{ }\Omega$, $V_{DRVOUT} = 0.7\text{ V}$ to 9 V		25	50	ns
Output fall time	$C_L = 1\text{ nF}$, $R_L = 10\text{ }\Omega$, $V_{DRVOUT} = 9\text{ V}$ to 0.7 V		10	50	ns
Maximum duty cycle		93	95	100	%
Minimum controlled duty cycle	At 100 kHz			2	%

zero power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Zero power comparator threshold	Measured on VA_{OUT}	0.20	0.33	0.50	V

pin descriptions

CAI: (current amplifier noninverting input) Place a resistor between this pin and the GND side of current-sense resistor. This input and the inverting input (MOUT) remain functional down to and below GND.

CAOUT: (current amplifier output) This is the output of a wide bandwidth operational amplifier that senses line current and commands the PFC pulse-width modulator (PWM) to force the correct duty cycle. Compensation components are placed between CAOUT and MOUT.

CT: (oscillator timing capacitor) A capacitor from CT to GND sets the PWM oscillator frequency according to:

$$f \approx \left(\frac{0.6}{RT \times CT} \right)$$

The lead from the oscillator timing capacitor to GND should be as short and direct as possible.

DRVOUT: (gate drive) The output drive for the boost switch is a totem-pole MOSFET gate driver on DRVOUT. Use a series gate resistor to prevent interaction between the gate impedance and the output driver that might cause the DRVOUT to overshoot excessively. See characteristic curve (Figure 13) to determine minimum required gate resistor value. Some overshoot of the DRVOUT output is always expected when driving a capacitive load.

GND: (ground) All voltages measured with respect to ground. VCC and REF should be bypassed directly to GND with a 0.1-μF or larger ceramic capacitor.

IAC: (current proportional to input voltage) This input to the analog multiplier is a current proportional to instantaneous line voltage. The multiplier is tailored for very low distortion from this current input (I_{IAC}) to multiplier output. The recommended maximum I_{IAC} is 500 μA.

MOUT: (multiplier output and current amplifier inverting input) The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high-impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier output current is limited to $(2 \times I_{IAC})$. The multiplier output current is given by the equation:

$$I_{MOUT} = \frac{I_{IAC} \times (V_{VAOUT} - 1)}{V_{VFF}^2 \times K}$$

where $K = \frac{1}{V}$ is the multiplier gain constant.

OVP/EN: (over-voltage/enable) A window comparator input that disables the output driver if the boost output voltage is a programmed level above the nominal or disables both the PFC output driver and resets SS if pulled below 1.9 V (typ).

PKLMT: (PFC peak current limit) The threshold for peak limit is 0 V. Use a resistor divider from the negative side of the current sense resistor to VREF to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0 V.

RT: (oscillator charging current) A resistor from RT to GND is used to program oscillator charging current. A resistor between 10 kΩ and 100 kΩ is recommended. Nominal voltage on this pin is 3 V.

UCC2819, UCC3819 PROGRAMMABLE OUTPUT POWER FACTOR PREREGULATOR

SLUS482B - APRIL 2001 – REVISED DECEMBER 2004

pin descriptions (continued)

VAI: (voltage amplifier non-inverting input) This input can be tied to the VREF or any other voltage reference (≤ 7.5 V) to set the boost regulator output voltage.

VAOUT: (voltage amplifier output) This is the output of the operational amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5 V to prevent overshoot.

VCC: (positive supply voltage) Connect to a stable source of at least 20 mA between 10 V and 17 V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices are inhibited unless V_{VCC} exceeds the upper under-voltage lockout voltage threshold and remains above the lower threshold.

VFF: (feed-forward voltage) The RMS voltage signal generated at this pin by mirroring 1/2 of the I_{AC} into a single pole external filter. At low line, the VFF roll should be 14 V.

VSENSE: (voltage amplifier inverting input) This is normally connected to a compensation network and to the boost converter output through a divider network.

VREF: (voltage reference output) VREF is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 20 mA to peripheral circuitry and is internally short-circuit current limited. VREF is disabled and remains at 0 V when V_{VCC} is below the UVLO threshold. Bypass VREF to GND with a 0.1- μ F or larger ceramic capacitor for best stability. Please refer to Figures 8 and 9 for VREF line and load regulation characteristics.

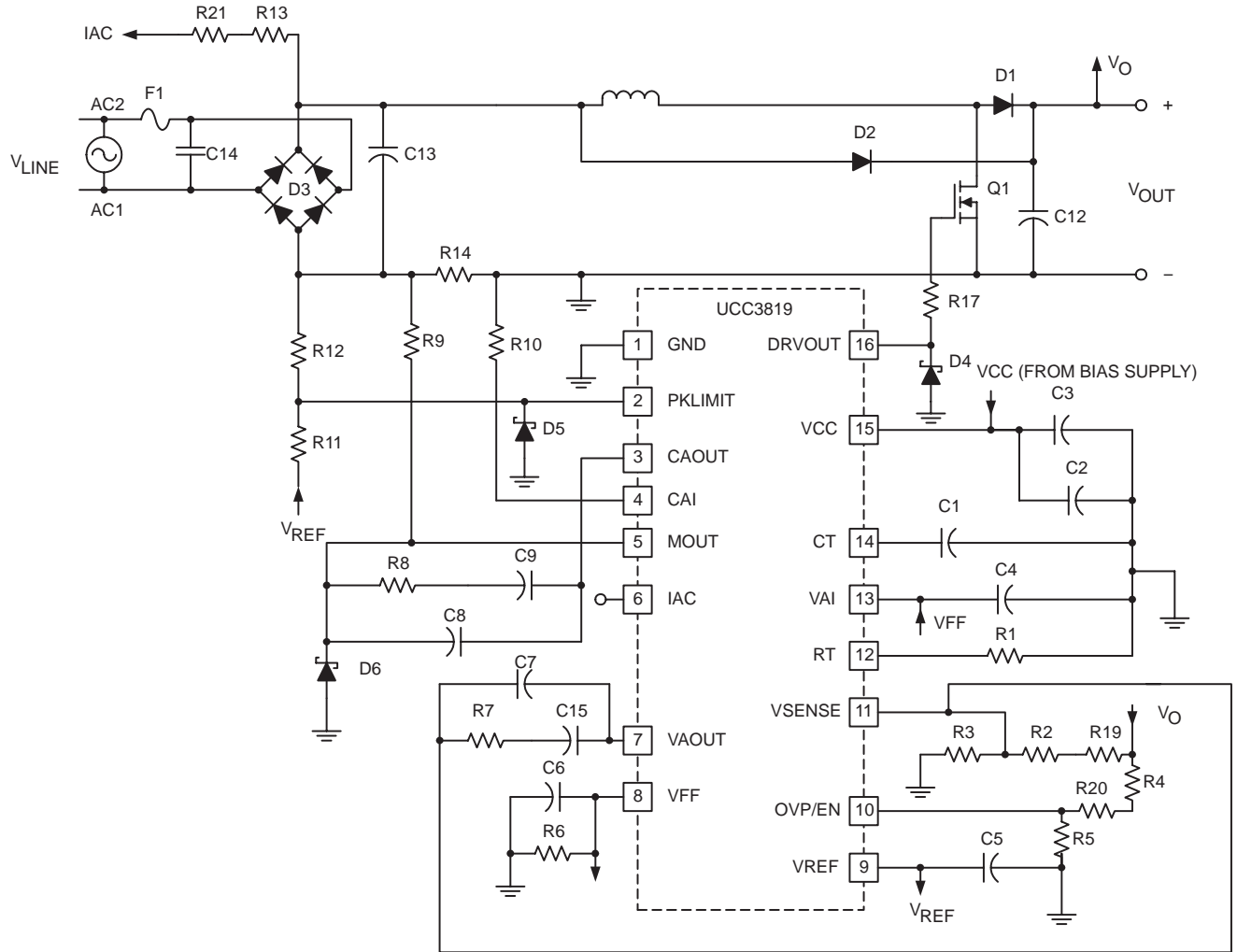
APPLICATION INFORMATION

The UCC3819 is based on the UCC3818 PFC preregulator. For a more detailed application information for this part, please refer to the UCC3818 datasheet product folder.

The main difference between the UCC3818 and the UCC3819 is that the non-inverting input of the voltage error amplifier is made available to the user through an external pin (VAI) in the UCC3819. The SS pin and function were eliminated to accommodate this change.

The benefit of VAI pin is that it can be used to dynamically change the PFC output voltage based on the line voltage (RMS) level or other conditions. Figure 1 shows one suggested implementation of the tracking boost PFC converter as this approach is sometimes referred to. The VAI pin is tied to the VFF pin and hence output voltage scales up with the line voltage. The benefit of this approach is that at lower line voltages the output voltage is lower and that leads to smaller boost inductor value, lower MOSFET conduction losses and reduced component stresses. In order for this feature to work, the downstream converter has to operate over a wider input range.

APPLICATION INFORMATION



UDG-01008

Figure 1. Suggested Implementation of UCC3819 in a Tracking Boost PFC Preregulator

APPLICATION INFORMATION

**REFERENCE VOLTAGE
 vs
 SUPPLY VOLTAGE**

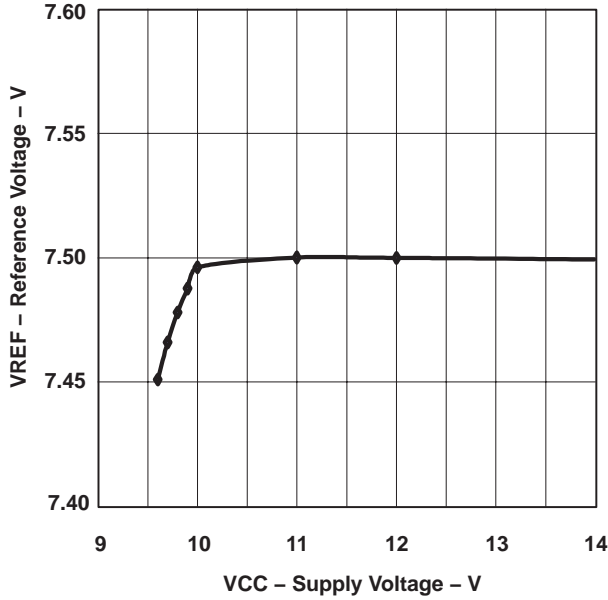


Figure 2

**REFERENCE VOLTAGE
 vs
 REFERENCE CURRENT**

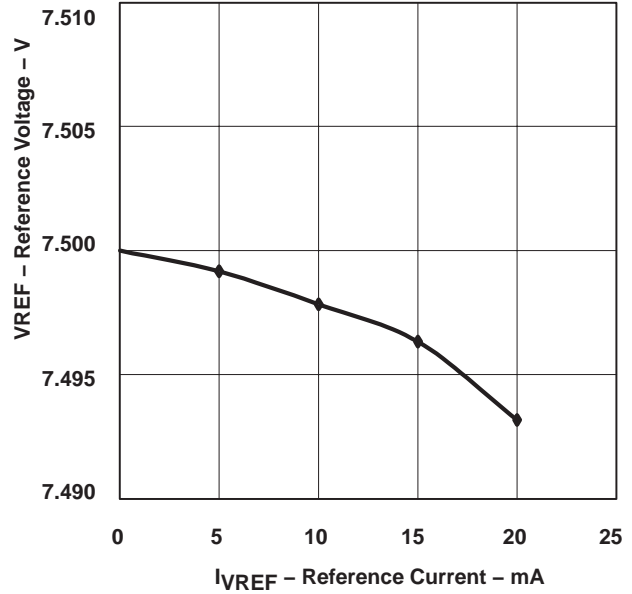


Figure 3

**MULTIPLIER OUTPUT CURRENT
 vs
 VOLTAGE ERROR AMPLIFIER OUTPUT**

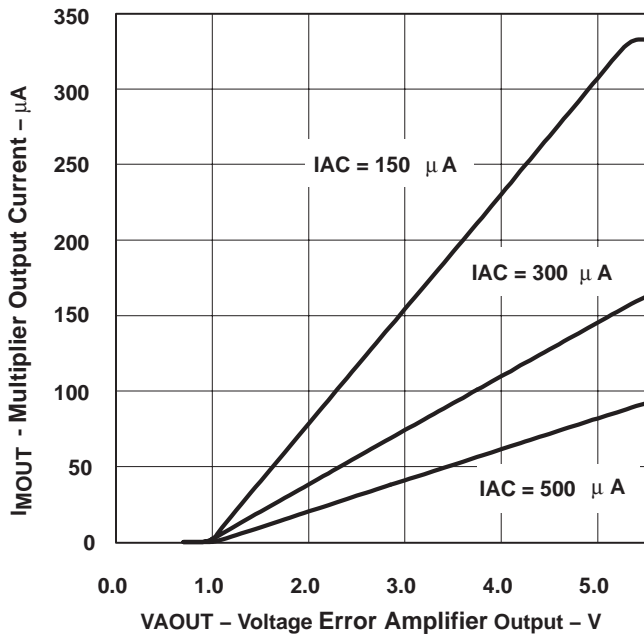


Figure 4

**MULTIPLIER GAIN
 vs
 VOLTAGE ERROR AMPLIFIER OUTPUT**

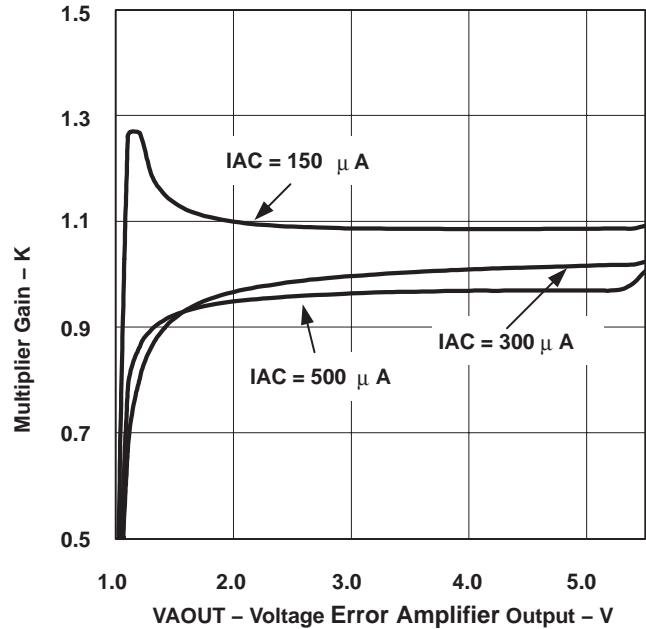


Figure 5

APPLICATION INFORMATION

MULTIPLIER CONSTANT POWER PERFORMANCE

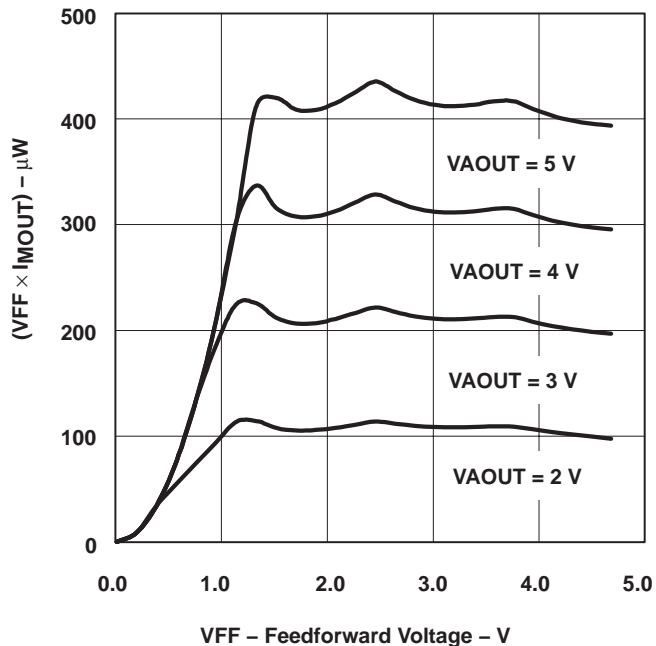


Figure 6

**RECOMMENDED MINIMUM GATE RESISTANCE
 VS
 SUPPLY VOLTAGE**

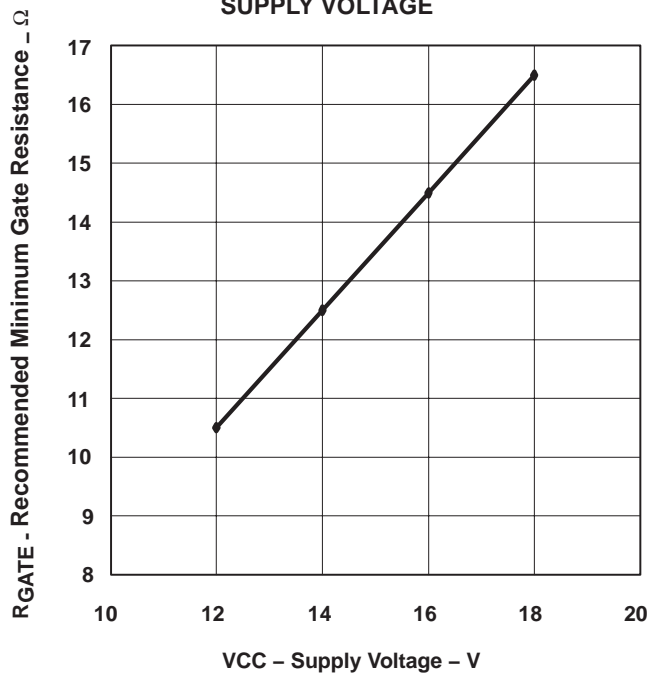


Figure 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2819D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2819D	Samples
UCC2819DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2819D	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

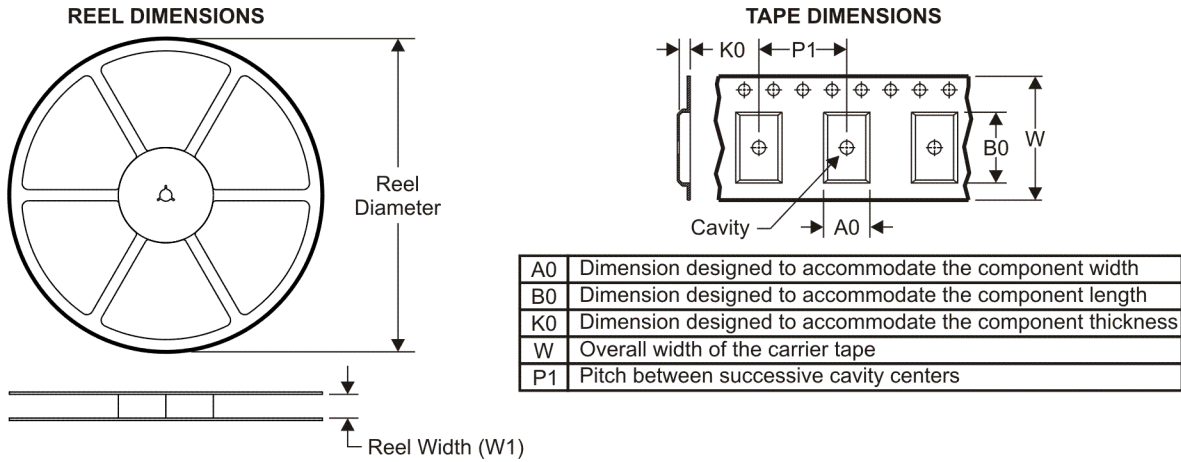
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2819DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2819DTR	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View UCC3819N](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management