THE DATASHEET OF

ML4821CP

ML4821

Power Factor Controller

Features

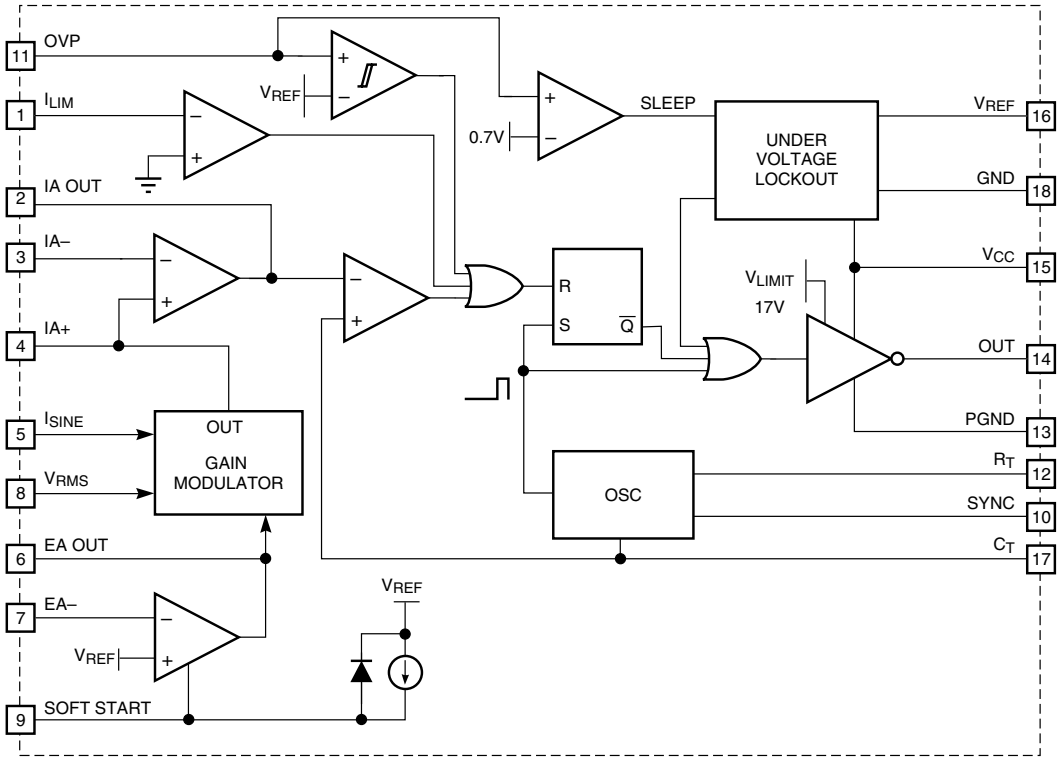
- Average current sensing for lowest possible harmonic distortion
- Average line compensation with brown-out control
- Precision buffered 5V reference
- 1A peak current totem-pole output drive
- Overvoltage comparator eliminates output "runaway" due to load removal
- Wide common mode range in current sense comparators for better noise immunity
- Large oscillator amplitude for better noise immunity
- Output driver internally limited to 17V
- "Sleep mode" shutdown input

General Description

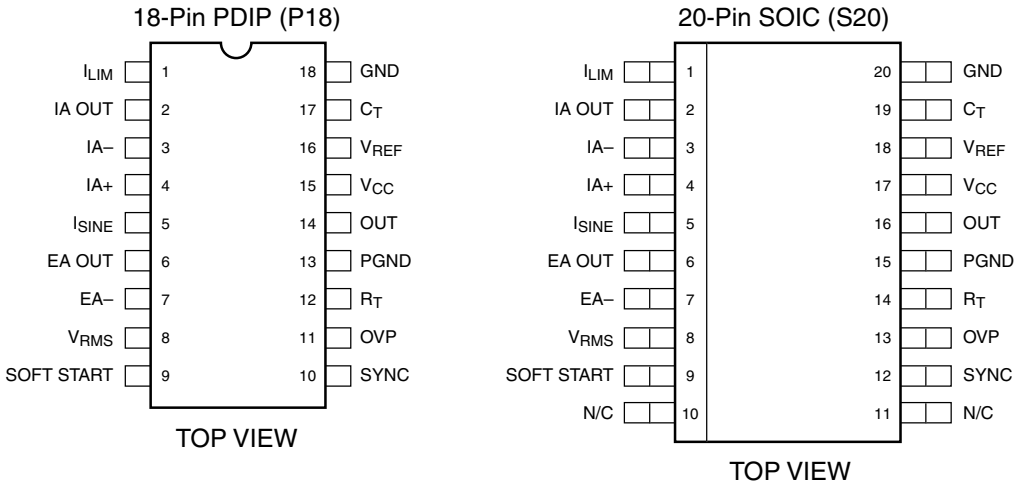
The ML4821 provides complete control for a "boost" type power factor correction system using the average current sensing method. Special care has been taken in the design of the ML4821 to increase system noise immunity. The circuit includes a precision reference, gain modulator, average current error amplifier, output error amplifier, over-voltage protection comparator, shutdown logic, as well as a high current output. In addition, start-up is simplified by an under-voltage lockout circuit.

In a typical application, the ML4821 controls the AC input current by adjusting the pulse width of the output MOSFET. This modulates the line current so that its shape conforms to the shape of the input voltage. The reference for the current regulator is a product of the sinusoidal line voltage times the output of the error amplifier which is regulating the output DC voltage. Average line voltage compensation is provided in the gain modulator to ensure constant loop gain over a wide input voltage range. This compensation includes a special "brown-out" control which reduces output power below 90V RMS input.

Block Diagram



Pin Connection



Pin Description

Pin Number		Name	Function
18-Pin DIP	20-Pin SOIC		
1	1	I_{LIM}	Peak cycle-by-cycle current limit input
2	2	IA OUT	Output and compensation node of the average current error amplifier
3	3	IA–	Inverting input of the average current error amplifier
4	4	IA+	Non-Inverting input of the average current error amplifier and output of the gain modulator
5	5	I_{SINE}	Gain modulator input
6	6	EA OUT	Output of output voltage error amplifier
7	7	INV	Inverting input to error amplifier
8	8	V_{RMS}	Input for average line voltage compensation
9	9	SOFT START	Normally connected to soft start capacitor
10	12	SYNC	Oscillator synchronization input
11	13	OVP	Inhibits output pulses when the voltage at this pin exceeds 5V. Also, when the voltage at this pin is less than 0.7V, the IC goes into low current shut-down mode.
12	14	R_T	Timing resistor for the oscillator
13	15	PWR GND	Return for the high current totem pole output
14	16	OUT	High current totem pole output
15	17	V_{CC}	Positive supply for the IC
16	18	V_{REF}	Buffered output for the 5V voltage reference
17	19	C_T	Timing capacitor for the oscillator.
18	20	GND	Analog signal ground

Absolute maximum ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min	Max	Units
Supply Current (I_{CC})		35	mA
OUT Current, Source or Sink		1.0	A
Output Energy (capacitive load per cycle)		5	µJ
I_{SINE} Input Current		1.2	mA
EA OUT Source Current		50	mA
Oscillator Charge Current		2	mA
Input Voltage	GND –0.3V	5.5	V
Junction Temperature		150	°C
Storage Temperature Range	–65	150	°C
Lead Temperature (Soldering 10 sec.)		260	°C
Thermal Resistance (θ_{JA}) Plastic DIP Plastic SOIC		 75 95	 °C/W °C/W

Operating Conditions

Temperature Range	Min	Max	Units
ML4821CX	0	70	°C

Electrical Characteristics

Unless otherwise specified, R_T = 6.2kΩ, C_T = 720pF, T_A = Operating Temperature Range, V_{CC} = 15V (Notes 1 & 2).

Parameter	Conditions	Min.	Typ.	Max.	Units
Oscillator					
Initial accuracy	T_A = 25°C	90	100	110	kHz
Voltage stability	12V < V_{CC} < 18V		1		%
Temperature stability			2		%
Total Variation	Line, Temperature	85		115	kHz
Ramp Valley to Peak		4.7	5.2	5.6	V
R_T Voltage		4.8	5.0	5.2	V
Discharge Current	C_T= 2V, R_T = Open	7.8	8.4	9.3	mA
SYNC Input Threshold		1.5	2.0	3.0	V
Reference					
Output Voltage	T_A = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line regulation	12V < V_{CC} < 24V		2	10	mV
Load regulation	1mA < I_O < 20mA		2	15	mV
Temperature stability			.4		%
Total Variation	line, load, temp	4.9		5.1	V
Output Noise Voltage	10Hz to 10kHz		50		µV
Long Term Stability	T_A = 125°C, 1000 hrs		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA

Electrical Characteristics (continued)

Unless otherwise specified, R_T = 6.2kΩ, C_T = 720pF, T_A = Operating Temperature Range, V_{CC} = 15V (Notes 1 & 2).

Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Error Amplifier					
Input Offset Voltage		0		–15	mV
Input Bias Current			–50	–800	nA
Open Loop Gain	2 < EA OUT < 6V	60	75		dB
PSRR	12V < V_{CC} < 24V	70	100		dB
Output Sink Current	EA OUT = 4V, INV = 5.5V	300	500		µA
Output Source Current	EA OUT = 4.0V, INV = 4.8V	–10	–30		mA
Output High Voltage	I_{PIN6} = –5mA, V_{PIN7} = 4.8V	7.0	7.5		V
Output Low Voltage	I_{PIN6} = 0, EA– = 5.5V		0	0.5	V
Unity Gain Bandwidth			1.0		MHz
Soft Start Charge Current	V_{PIN9} = 4V	–22	–38	–50	µA
Current Error Amplifier					
Input Offset Voltage		–5	0	5	mV
Input Bias Current			–0.15	–1	µA
Input Offset Current				400	nA
Open Loop Gain	2 < EA OUT < 7V	80	100		dB
PSRR	12V < V_{CC} < 24V	65	85		dB
Output Voltage Low	I_{OL} = 300µA		0	0.5	V
Output Voltage High	I_{OH} = –10mA	7.0	7.5		V
Input Common Mode Range		–0.3		2.5	V
Gain Modulator					
Gain	V_{INV} = 4.8V, V_{RMS} = 0V V_{INV} = 4.8V, V_{RMS} = 1.75V V_{INV} = 4.8V, V_{RMS} = 2.6V V_{INV} = 4.8V, V_{RMS} = 5.2V	0.75 3.1 1.25 0.22	1.2 3.88 1.75 0.38	1.3 4.5 2.15 0.50	
Output Current	V_{INV} = 5.2V, V_{RMS} = 5.2V		–2	–4	µA
Output Current Limit	V_{INV} = 4.8V, I_{SINE} = 500µA, V_{RMS} = 1.75V	360	395	420	µA
I_{LIM} Comparator					
Input Offset Voltage				+15	mV
Input Bias Current			–100	–200	µA
OVP Comparator					
Input Offset Voltage	Output Off	–25		5	mV
Hysteresis	Output On	85	105	130	mV
Input Bias Current			–0.3	–3	µA
Propagation Delay			150		ns
Shutdown Threshold		0.4	0.7	1.0	V
PWM Comparator					
Input Common Mode Range		0		8	V
Propagation Delay			150		ns

Electrical Characteristics (continued)

Unless otherwise specified, R_T = 6.2kΩ, C_T = 720pF, T_A = Operating Temperature Range, V_{CC} = 15V (Notes 1 & 2).

Parameter	Conditions	Min.	Typ.	Max.	Units
Output					
Output Voltage Low	I_{OUT} = 20mA I_{OUT} = 200mA		0.1 1.6	0.4 2.4	V V
Output Voltage High	I_{OUT} = –20mA I_{OUT} = –200mA	13 12	13.5 13.4		V V
Output Voltage Low in UVLO	I_{OUT} = –5mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		ns
Undervoltage Lockout					
Start-up Threshold		14.5		16.5	V
Shut-Down Threshold		8.5		11.0	V
V_{REF} Good Threshold			4.4		V
Supply					
Supply Current	Start-up, V_{CC} = 14V, T_A = 25°C Operating, T_A = 25°C		0.6 26	1.2 32	mA mA
Internal Shunt Zener Voltage	I_{CC} = 35mA	25	27	35	V

Notes:

1. Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.
2. V_{CC} is raised above the start-up threshold first to activate the IC, then returned to 15V
3. Gain Modulator gain is defined as: $\frac{I_{OUTIA+}}{I_{INEAOUT}}$

Functional Description

Oscillator

The ML4821 oscillator charges the external capacitor connected to C_T with a current equal to $2.5/R_T$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1.

The oscillator period can be described by the following relationship:

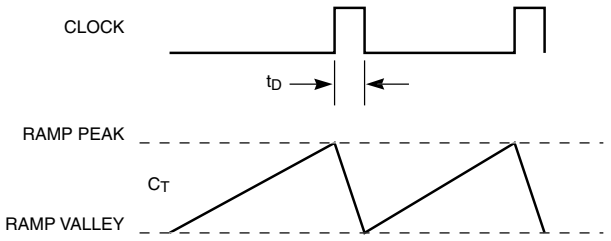
$$T_{OSC} = T_{RAMP} + T_{DISCHARGE}$$

where:

$$T_{RAMP} = C(\text{Ramp Valley to Peak}) \div (I_{RT}/2)$$

and:

$$T_{DISCHARGE} = C(\text{Ramp Valley to Pk}) \div (8.4mA - I_{RT}/2)$$



The ML4821 oscillator includes a SYNC input for synchronizing to an external frequency source. A positive pulse on this pin of 2V (typ) resets the oscillators comparator and initiates a discharge cycle for C_T. The R_T and C_T component values which set the ML4821 oscillator frequency should be selected to produce a lower frequency than the external frequency source.

VOLTAGE and Current ERROR Amplifiers

The ML4821 voltage error amplifier is a high open loop gain, wide bandwidth amplifier with a class A output. The soft start circuit controls the input to this amplifier for closed loop soft start operation.

The current error amplifier (IA) is similar to the voltage error amplifier but is designed for very low offsets to allow the selection of a low value resistor for R_{SENSE}.

Output Driver Stage

The ML4821 Output Driver is a 1A peak output high speed totem pole circuit designed to quickly drive capacitive loads, such as power MOSFET gates. The driver circuit's output voltage is internally limited to 17V.

Gain Modulator

The ML4821 gain modulator responds linearly to current injected into the I_{SINE} pin, and in an inverse-square fashion to voltage on the V_{RMS} pin. At very low voltages on the V_{RMS} pin, the gain modulator enforces a power limit, or "brown-out protection", upon the overall PFC circuit (Figures 6 and 7). The rectified line input sine wave is converted to a current for the I_{SINE} input via a dropping resistor. In this way, most ground noise produces an insignificant effect on the reference to the PWM comparator. This gives the ML4821 a high degree of immunity to the disturbances common in high-power switching circuits.

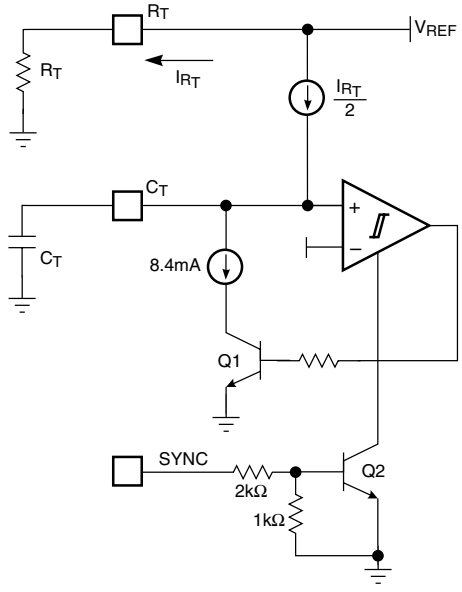


Figure 1. Oscillator Block Diagram

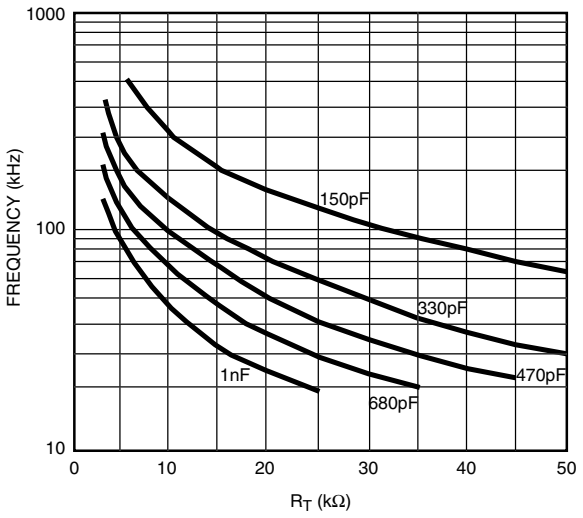


Figure 2. Oscillator Timing Resistance vs. Frequency

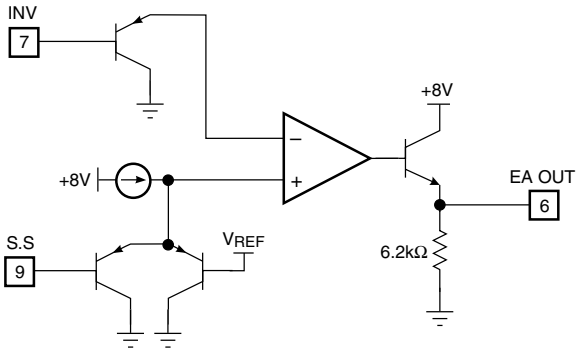


Figure 3. Error and Current Amplifier Configuration

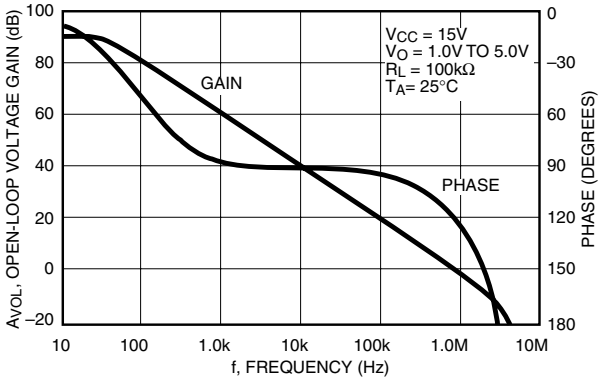


Figure 4. Error Amplifier Open-loop Gain and Phase vs. Frequency.

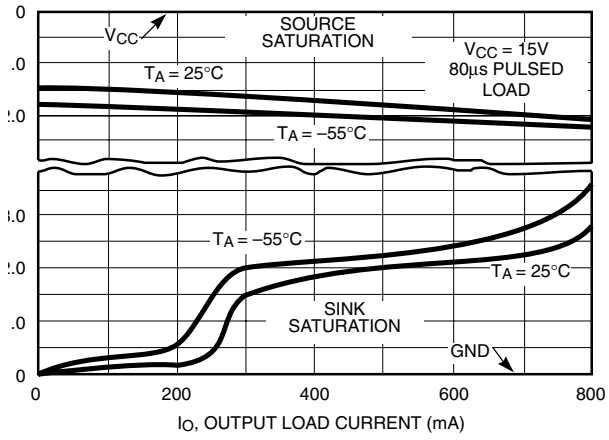


Figure 5. Output Saturation Voltage vs. Output Current.

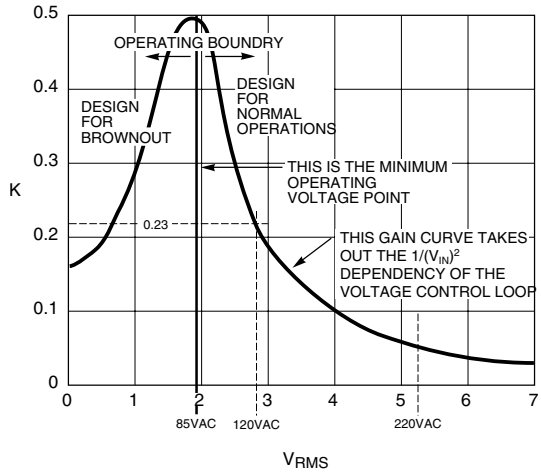


Figure 6. K-factor. Gain Modulator gain with respect to the voltage at V_{RMS}.

The output of the gain modulator is a current which appears on IA+ to form the reference for the current error amplifier and is given as:

$$I_{GM} = K \times I_{SINE} \times (V_{EA} - 0.8)$$

where:

I_{SINE} is the current in the dropping resistor, V_{EA} is the output of the error amplifier and K is a constant determined by the V_{RMS} input.

$$I_{GM(MAX)} = \frac{2.5}{R_T}$$

The output current of the gain modulator is limited to:

This sets the system current limit.The multiplier output current is converted into the reference voltage for the current (IA) amplifier through a resistor to ground on IA+.

Figure 6 shows the gain adjustor (K) with respect to the voltage at V_{RMS}. The curve has been separated in two parts. The right hand part is for operation under normal conditions in the voltage range from minimum line voltage to maximum line voltage (90VAC to 260VAC). 85VAC on the curve has been chosen to account for tolerances. Under normal operating conditions as input voltage decreases the gain increases compensating for the drop in the loop gain.

Under brownout conditions (below 85VAC) the gain decreases to limit the amount of current that is drawn from the line thus preventing an overload condition. This is a very useful feature since in many cases the load for a PFC is a constant power load. The input current has to go high to compensate for a drop in the input voltage.

Under Voltage Lockout, OVP and Current Limit

On power-up the ML4821 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 9V, the UVLO condition is imposed. During the UVLO condition, the V_{REF} pin is "off", making it usable as a "flag" for starting up a down-stream PWM converter.

OVP, Shutdown, and IC Bias

When the input to the OVP comparator exceeds V_{REF}, the output of the ML4821 is inhibited. The OVP input also functions as a "sleep" input, putting the IC into the low quiescent UVLO state when the OVP pin is pulled below 0.7V.

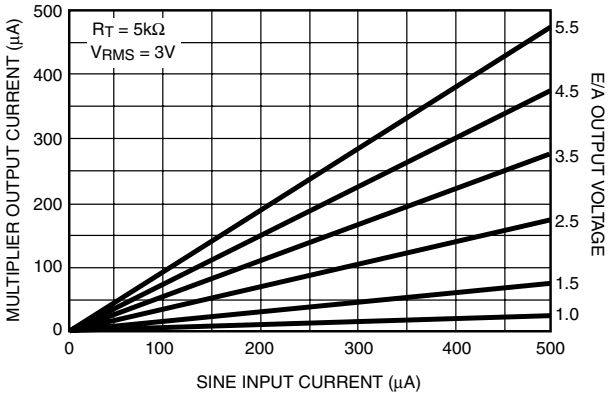


Figure 7. Gain Modulator Linearity.

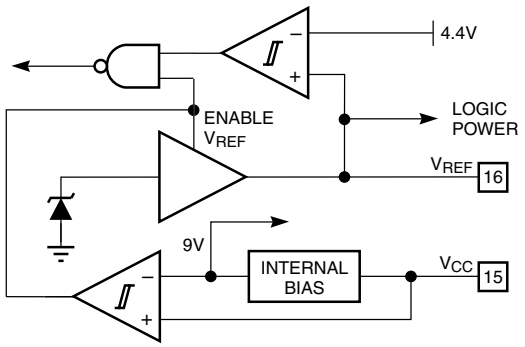


Figure 8. Under-Voltage Lockout Block Diagram.

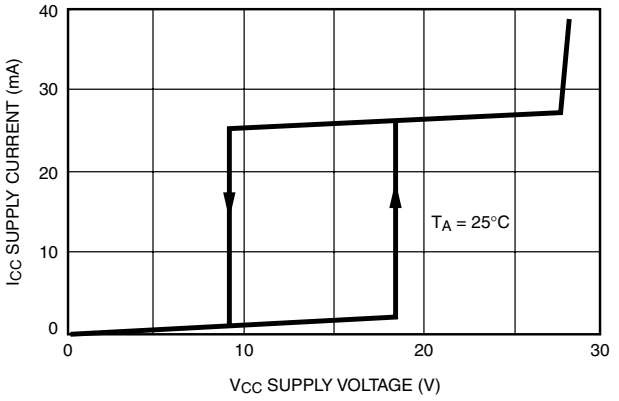


Figure 9. Total Supply Current vs. Supply Voltage.

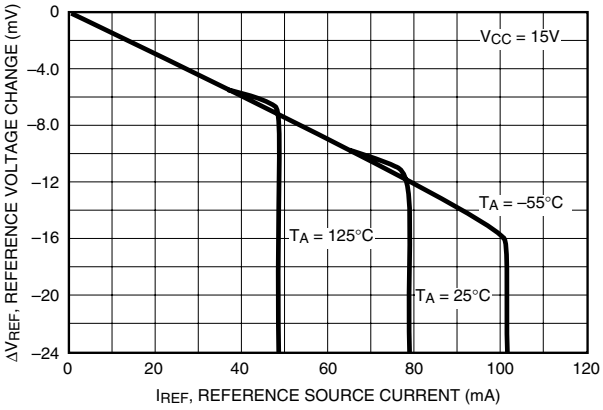


Figure 10. Reference Load Regulation.

Off-line Start-up and Bias Supply Generation

The circuit in Figure 11 supplies V_{CC} power to the ML4821. Start-up current is delivered via R10. The IC starts when V_{CC} reaches 15.5V. After that time running power is delivered through the tap on L1. The configuration shown delivers a voltage proportional to the PFC output bus voltage.

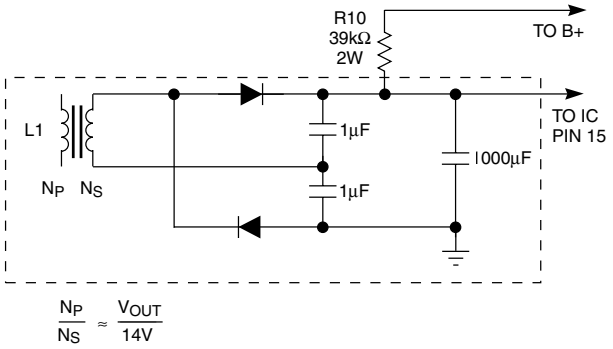


Figure 11. Bias and Start-up Circuit.

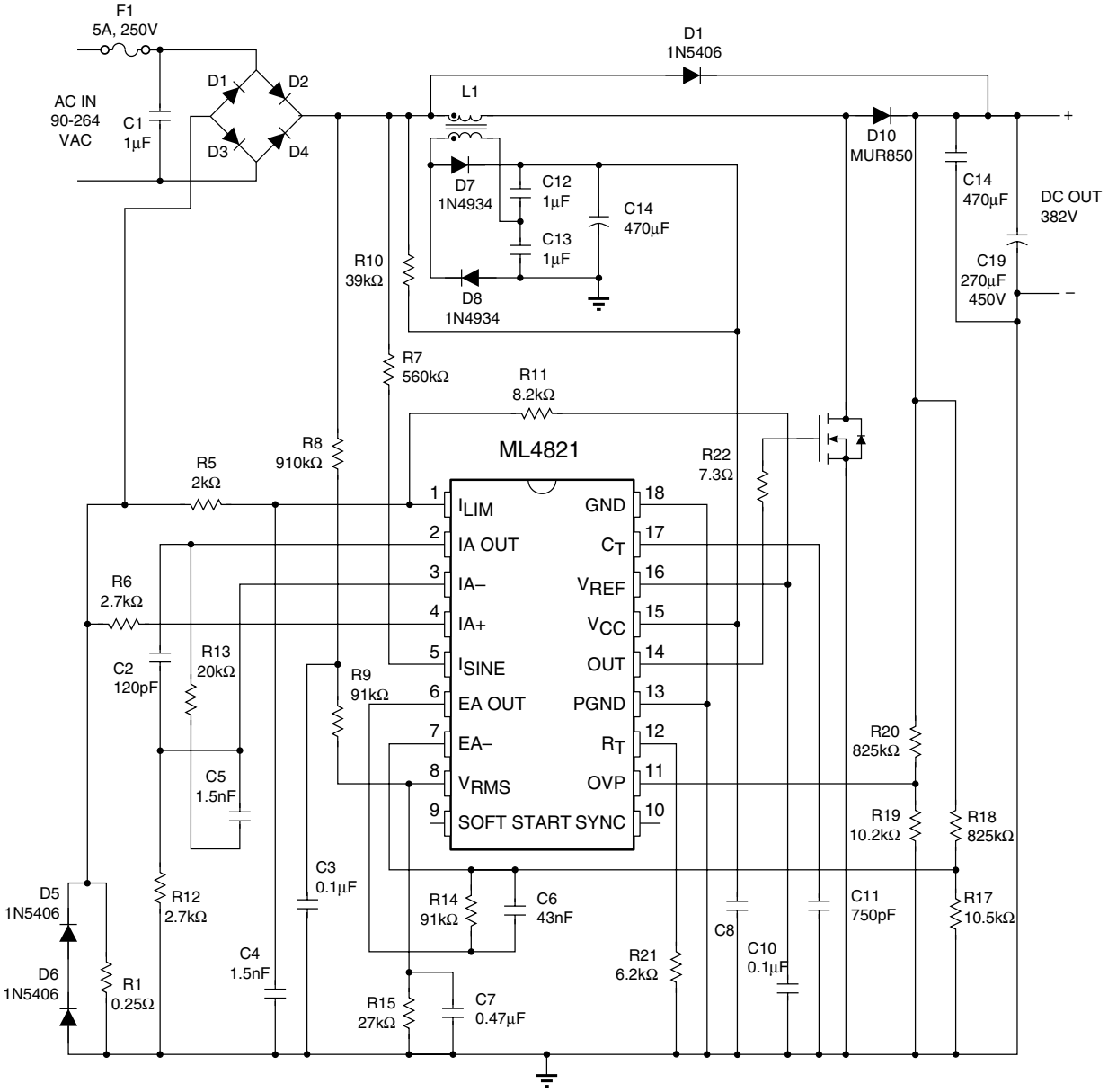
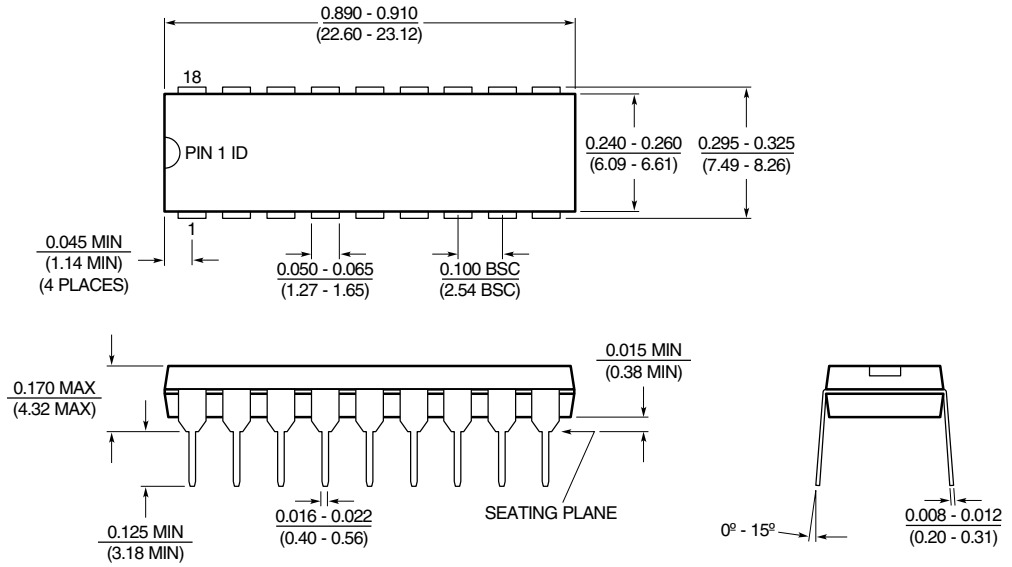


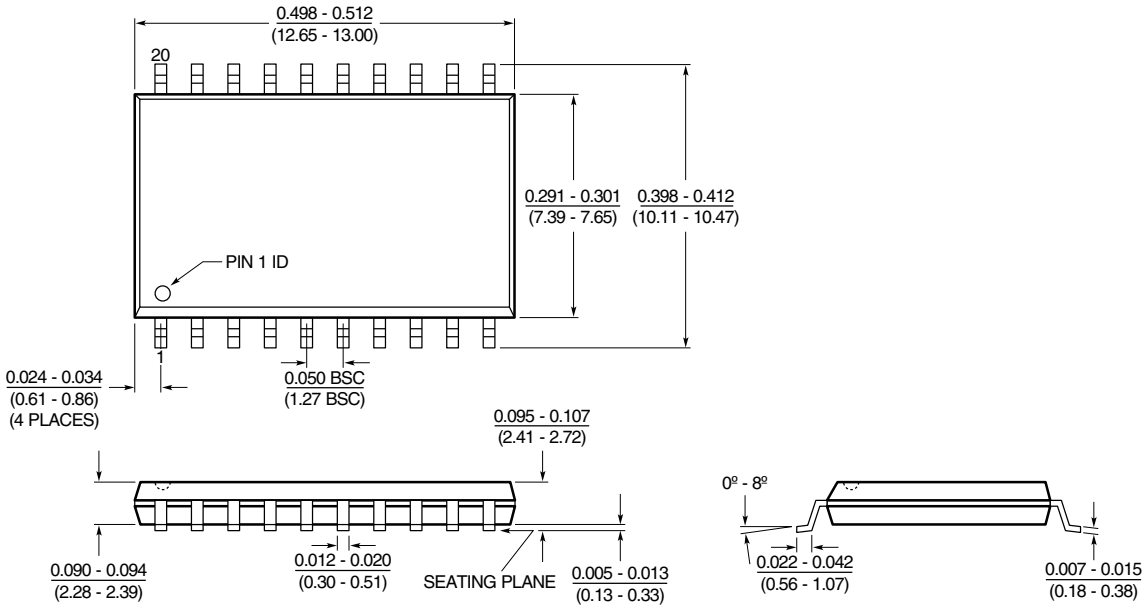
Figure 12. 200W Output PFC Circuit

Mechanical Dimensions inches (millimeters)

Package: P18
18-Pin PDIP



Package: S20
20-Pin SOIC



Ordering Information

Part Number	Temperature Range	Package
ML4821CP	0˚C to 70˚C	18-Pin PDIP (P18)
ML4821CS	0˚C to 70˚C	20-Pin SOIC (S20)

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