



**THE DATASHEET OF  
MAX5911ESA+T**





# -48V Simple Swapper Hot-Swap Switches

MAX5911/MAX5912

## General Description

The MAX5911/MAX5912 are fully integrated hot-swap switches for negative supply rails. These devices allow the safe insertion and removal of circuit cards into live backplanes or ports without causing problematic glitches on the negative power-supply rail. They also monitor various circuit parameters and disconnect the load if a fault condition occurs, alerting the host with a logic-level  $\overline{\text{FAULT}}$  output. The MAX5911/MAX5912 operate over a voltage range of -16V to -65V and are designed to permit hot plugging of an IP phone into a hub, but are not limited to that operation.

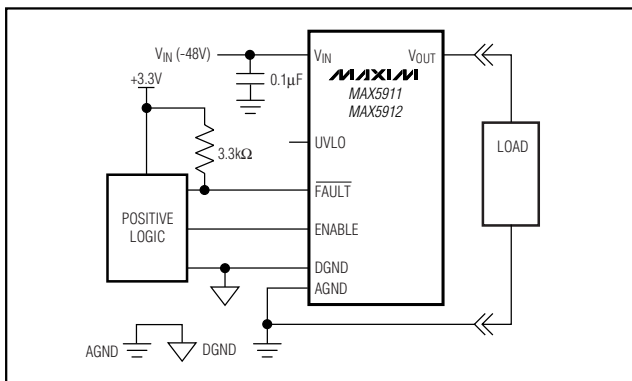
During startup, an internal power FET regulates the current between the backplane power source and the load to 280mA for MAX5911 and 415mA for MAX5912. After startup, the FET is fully enhanced to reduce its on-resistance. To ensure robust operation, the MAX5911/MAX5912 contain built-in safety features that prevent damage to the internal FET. They include an enable input, which responds to positive logic signals (+3.3V or +5V), allowing the host system to disconnect the load. ENABLE is also used to reset the device after a latching fault condition occurs.

The MAX5911/MAX5912 Simple Swapper™ hot-swap ICs monitor four parameters for these fault conditions: undervoltage lockout (UVLO), power-not-good, zero-current detection, and thermal shutdown. These devices are available in the extended temperature range, -40°C to +85°C. The MAX5911 and MAX5912 come in 8-pin and 16-pin SOIC packages, respectively.

## Applications

IP Phones	Internet Appliances
Network Routers	Power-Over-LAN
Network Switches	

## Typical Operating Circuit



## Features

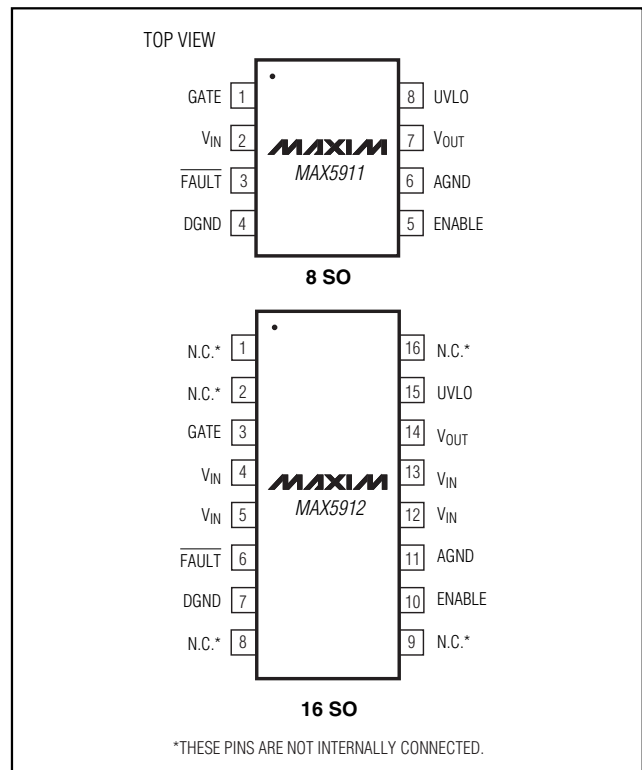
- ◆ Provides Safe Hot Swap for -16V to -65V Power Supplies
- ◆ 280mA Current Limit for MAX5911
- ◆ 415mA Current Limit for MAX5912
- ◆ Zero-Current Load Disconnect
- ◆ Integrated Power FET
- ◆ Status Output Reports Fault Condition
- ◆ Internal Switch-Protection Circuitry
- ◆ Built-In Thermal Shutdown
- ◆ DGND Can Vary Up to ±5V with Respect to AGND

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5911ESA	-40°C to +85°C	8 SO
MAX5912ESE	-40°C to +85°C	16 SO

Simple Swapper is a trademark of Maxim Integrated Products, Inc.

## Pin Configurations



# -48V Simple Swapper Hot-Swap Switches

## ABSOLUTE MAXIMUM RATINGS

Voltages are with respect to AGND, unless otherwise noted.

V <sub>IN</sub> .....	+0.3V to -70V
V <sub>OUT</sub> .....	+0.3V to (V <sub>IN</sub> - 0.3V)
ENABLE to DGND .....	-0.3V to +11V
ENABLE to V <sub>IN</sub> .....	-0.3V to +70V
FAULT to DGND .....	-0.3V to +11V
UVLO to V <sub>IN</sub> .....	-0.3V to +11V
DGND .....	-5V to +5V
DGND to V <sub>IN</sub> .....	-0.3V to +70V
FAULT Sink Current .....	10mA

Continuous Output Current .....	Internally Limited
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
8-Pin SO (derate 5.9mW/°C above +70°C) .....	470mW
16-Pin SO (derate 12.9mW/°C above +70°C) .....	1039mW
Operating Temperature Range .....	-40°C to +85°C
Junction Temperature .....	+150°C
Storage Temperature Range .....	-60°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL SPECIFICATIONS

(V<sub>IN</sub> = -48V, AGND = DGND = 0, UVLO = open circuit, V<sub>ENABLE</sub> = +3.3V, and T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Input Voltage Range	V <sub>IN</sub>		-65		-16	V	
Supply Current	I <sub>IN</sub>	Measured at AGND at the end of output voltage slew		1.5	2.5	mA	
Maximum V <sub>OUT</sub> Current	I <sub>OUT(MAX)</sub>	V <sub>OUT</sub> = V <sub>IN</sub> + 5V	MAX5911	-310	-280	-250	mA
			MAX5912	-457	-415	-373	
DMOS On-Resistance	R <sub>DS(ON)</sub>	MAX5911 I <sub>OUT</sub> = -225mA, MAX5912 I <sub>OUT</sub> = -350mA		2.5	4	Ω	
V <sub>OUT</sub> Leakage Current		Measured on V <sub>OUT</sub> when internal DMOS is shut off			10	μA	
ENABLE Low Voltage	V <sub>IL</sub>	Referenced to DGND			0.8	V	
ENABLE High Voltage	V <sub>IH</sub>	Referenced to DGND	2.0			V	
ENABLE High Input Current	I <sub>IH</sub>	V <sub>ENABLE</sub> = +3.3V		140	300	μA	
ENABLE Low Pulse Width (Note 1)	t <sub>EPW</sub>		200			ns	
FAULT Output Low Voltage	V <sub>OL</sub>	I <sub>FAULT</sub> = 3mA			0.4	V	
FAULT Output Leakage Current	I <sub>OH</sub>	V <sub>FAULT</sub> = +3.3V			10	μA	
Zero-Current Detection Threshold	I <sub>FTH</sub>	Decreasing load current	-12	-8	-4	mA	
Zero-Current Detection Threshold Hysteresis	I <sub>FHY</sub>			1.5		mA	
Zero-Current Detection Delay (Note 2)	I <sub>FDEL</sub>		280	350	520	ms	
Current-Limit Delay (Note 3)	t <sub>LIMIT</sub>	V <sub>OUT</sub> shorted to AGND		10	20	μs	
Power-Good Threshold	V <sub>PG</sub>	V <sub>IN</sub> - V <sub>OUT</sub>  ,  V <sub>IN</sub> - V <sub>OUT</sub>   decreasing	1.95	2.15	2.35	V	
Power-Good Hysteresis	PGHYS	% of V <sub>PG</sub>		5		%	

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MAX5911/MAX5912

## ELECTRICAL SPECIFICATIONS (continued)

( $V_{IN} = -48V$ ,  $AGND = DGND = 0$ ,  $UVLO = \text{open circuit}$ ,  $V_{ENABLE} = +3.3V$ , and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Not-Good Output Delay (Note 4)	$PG_{DEL}$	After $ V_{IN} - V_{OUT} $ increases above $(V_{PG} + PG_{HYS})$	8	14	20	ms
Thermal Shutdown Temperature (Note 5)	$T_J$			140		$^\circ\text{C}$
Default UVLO		UVLO open circuit, $ V_{IN} $ increasing	-30	-28	-26	V
UVLO Hysteresis		UVLO open circuit, percentage of UVLO threshold		12		%
UVLO Comparator Threshold		Referenced to $V_{IN}$ , UVLO open circuit, $ V_{IN} $ increasing		+1.258		V
UVLO Input Resistance	$R_{UVLO}$			95		$k\Omega$

**Note 1:** Minimum ENABLE low pulse width required to unlatch fault condition.

**Note 2:** The delay from  $I_{OUT}$  falling below the zero-current threshold until  $\overline{FAULT}$  is latched low and  $V_{OUT}$  is disabled.

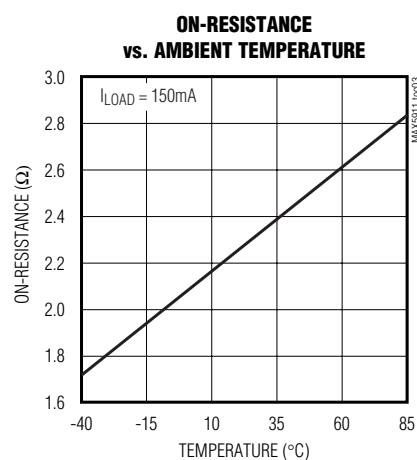
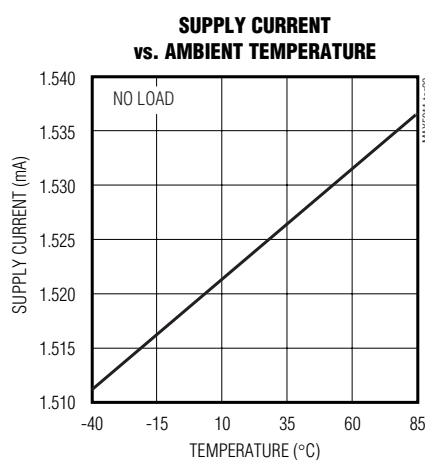
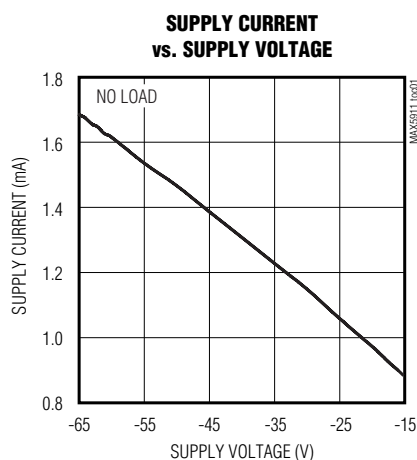
**Note 3:** The time from an output overcurrent or short-circuit condition until the output goes into current limit.

**Note 4:** The time from  $V_{OUT}$  falling until  $\overline{FAULT}$  is asserted low.  $\overline{FAULT}$  is not latched for Power-Not-Good condition.

**Note 5:** When the device goes into thermal shutdown, the output is disabled and  $\overline{FAULT}$  is latched low.

## Typical Operating Characteristics

( $V_{IN} = -48V$ ,  $AGND = DGND = 0$ ,  $UVLO = \text{open circuit}$ ,  $V_{ENABLE} = +3.3V$ ,  $R_{LOAD} = 1.8k\Omega$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

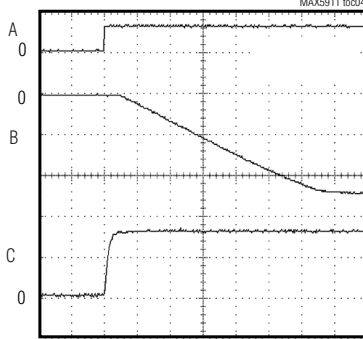


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## Typical Operating Characteristics (continued)

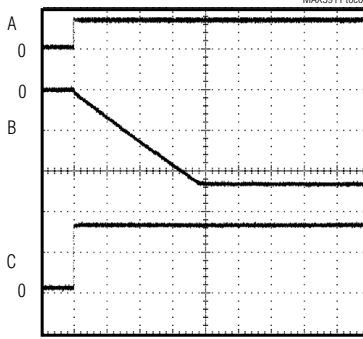
( $V_{IN} = -48V$ ,  $AGND = DGND = 0$ ,  $UVLO = \text{open circuit}$ ,  $V_{ENABLE} = +3.3V$ ,  $R_{LOAD} = 1.8k\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

**MAX5911 TURN-ON WAVEFORMS**  
( $R_L = 1.8k\Omega$ ,  $C_L = \text{NONE}$ )



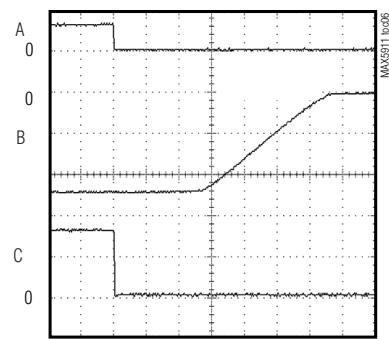
$t = 10\mu s/div$   
A: ENABLE, 5V/div      C: FAULT, 2V/div  
B: V<sub>OUT</sub>, 20V/div

**MAX5911 TURN-ON WAVEFORMS**  
( $R_L = 1.8k\Omega$ ,  $C_L = 47\mu F$ )



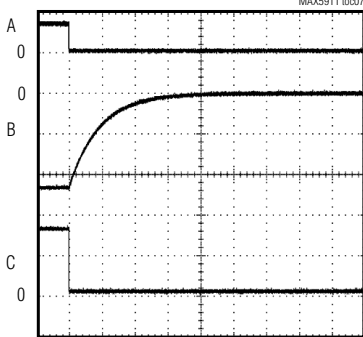
$t = 2ms/div$   
A: ENABLE, 5V/div      C: FAULT, 2V/div  
B: V<sub>OUT</sub>, 20V/div

**MAX5911 TURN-OFF WAVEFORMS**  
( $R_L = 1.8k\Omega$ ,  $C_L = \text{NONE}$ )



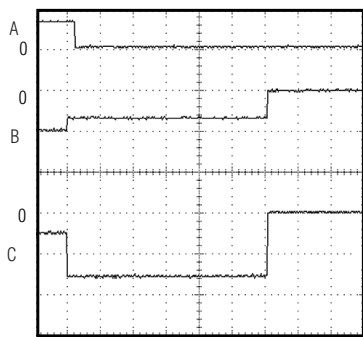
$t = 10\mu s/div$   
A: ENABLE, 5V/div      C: FAULT, 2V/div  
B: V<sub>OUT</sub>, 20V/div

**MAX5911 TURN-OFF WAVEFORMS**  
( $R_L = 1.8k\Omega$ ,  $C_L = 47\mu F$ )



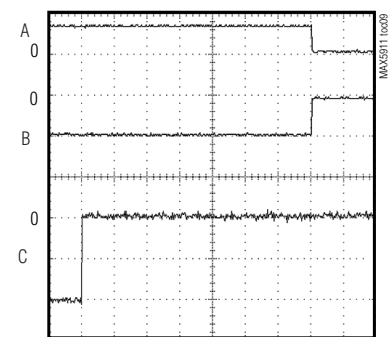
$t = 100ms/div$   
A: ENABLE, 5V/div      C: FAULT, 2V/div  
B: V<sub>OUT</sub>, 20V/div

**MAX5911 OVERCURRENT RESPONSE**



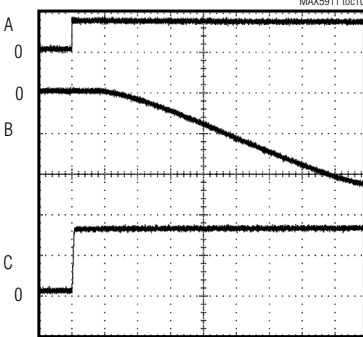
$t = 50ms/div$   
A: FAULT, 5V/div      C: I<sub>OUT</sub>, 200mA/div  
B: V<sub>OUT</sub>, 50V/div

**MAX5911 ZERO-CURRENT RESPONSE**



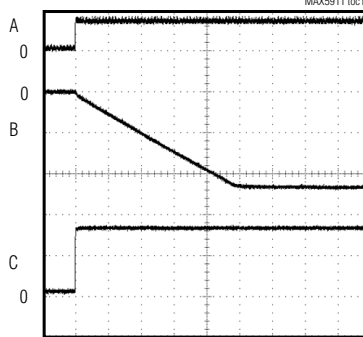
$t = 50ms/div$   
A: FAULT, 5V/div      C: I<sub>OUT</sub>, 50mA/div  
B: V<sub>OUT</sub>, 50V/div

**MAX5912 TURN-ON WAVEFORMS**  
( $R_L = 1.8k\Omega$ ,  $C_L = \text{NONE}$ )



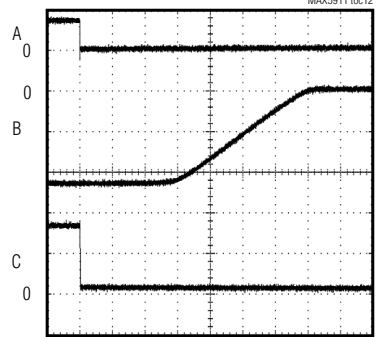
$t = 10\mu s/div$   
A: ENABLE, 5V/div      C: FAULT, 2V/div  
B: V<sub>OUT</sub>, 20V/div

**MAX5912 TURN-ON WAVEFORMS**  
( $R_L = 1.8k\Omega$ ,  $C_L = 47\mu F$ )



$t = 1ms/div$   
A: ENABLE, 5V/div      C: FAULT, 2V/div  
B: V<sub>OUT</sub>, 20V/div

**MAX5912 TURN-OFF WAVEFORMS**  
( $R_L = 1.8k\Omega$ ,  $C_L = \text{NONE}$ )



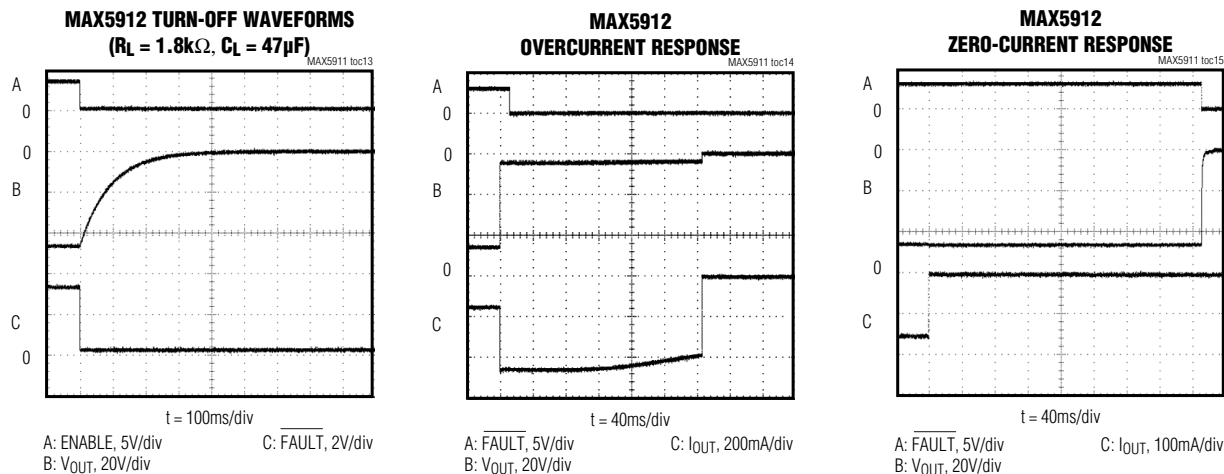
$t = 10\mu s/div$   
A: ENABLE, 5V/div      C: FAULT, 2V/div  
B: V<sub>OUT</sub>, 20V/div

# -48V Simple Swapper Hot-Swap Switches

MAX5911/MAX5912

## Typical Operating Characteristics (continued)

( $V_{IN} = -48V$ ,  $AGND = DGND = 0$ ,  $UVLO = \text{open circuit}$ ,  $V_{ENABLE} = +3.3V$ ,  $R_{LOAD} = 1.8k\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Description

PIN		NAME	FUNCTION
MAX5911	MAX5912		
1	3	GATE	Gate of the Internal Power MOSFET. Normally leave open circuit. To slow down the output voltage ramp, connect two capacitors, one to $V_{IN}$ and one to $V_{OUT}$ . See <i>GATE Connections</i> for details.
2	4, 5, 12, 13	$V_{IN}$	Voltage Input Terminal. Bypass $V_{IN}$ , to AGND with a 0.1 $\mu F$ capacitor to improve noise immunity.
3	6	$\overline{FAULT}$	Fault Logic Output, open-drain. Tie $\overline{FAULT}$ to the positive logic supply with a 3.3k $\Omega$ resistor. Referenced to DGND.
4	7	DGND	Digital Ground. Ground reference level for the external positive logic, $\overline{FAULT}$ , and ENABLE. DGND can vary up to $\pm 5V$ with respect to AGND to accommodate differential ground voltages in large systems.
5	10	ENABLE	ENABLE Input. Turns on and off the internal FET. ENABLE is a positive logic-level input referenced to DGND. Drive ENABLE high to enable $V_{OUT}$ . Drive ENABLE low to disable $V_{OUT}$ . Pulse ENABLE low to reset the MAX5911/MAX5912 after a latched fault condition occurs.
6	11	AGND	Analog Ground. Ground reference level for $V_{IN}$ , $V_{OUT}$ , and UVLO.
7	14	$V_{OUT}$	Voltage Output Terminal
8	15	UVLO	Undervoltage Lockout Input. Leave UVLO open circuit for default setting of -28V. Alternatively, UVLO can be connected to a resistive divider to set the lockout voltage (see the <i>Changing the Undervoltage Lockout Setting</i> section). The comparator threshold level is +1.258V with respect to $V_{IN}$ .
—	1, 2, 8, 9, 16	N.C.	No Connection. No internal connection.



# -48V Simple Swapper Hot-Swap Switches

MAX5911/MAX5912

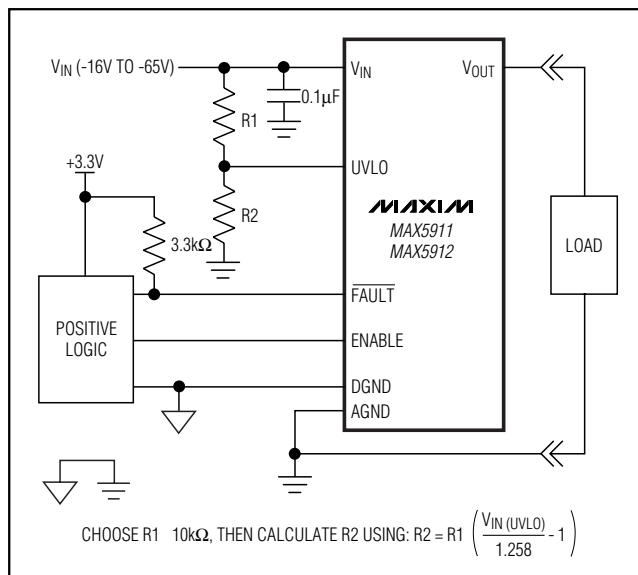


Figure 2. UVLO Voltage Set by an External Resistive Divider

## FAULT Output

The  $\overline{\text{FAULT}}$  output is open-drain and is pulled low if the MAX5911/MAX5912 detect an undervoltage fault, a thermal fault, a power-not-good fault, or a zero-current fault. See the *Normal Operation* section for specific details of fault operation. Connect  $\overline{\text{FAULT}}$  to the logic supply with a pullup resistor; 3.3kΩ is sufficient in most cases.

## Changing the Undervoltage Lockout Setting

The UVLO value defaults to -28V if the UVLO pin is left open circuit. The lockout voltage can be changed with a resistive divider. Connect the divider from  $V_{\text{IN}}$  to AGND, and connect the center node of the divider to the UVLO pin. Figure 2 shows an example circuit. Use  $R1 \leq 10\text{k}\Omega$ , then calculate R2 using:

$$R2 = R1 \times \left( \frac{V_{\text{IN(UVLO)}}}{1.258} - 1 \right)$$

where  $V_{\text{IN(UVLO)}}$  is the desired lockout voltage.

## Chip Information

TRANSISTOR COUNT: 1021

PROCESS: BiCMOS

heat dissipation properties, and always solder all of its  $V_{\text{IN}}$  pins to a large section of circuit board copper.

## Logic Control

The enable input responds to +3.3V logic signals and will force the internal FET off if it is pulled low. This feature allows the host to disconnect the load from the power bus if required. Additionally, all fault conditions that latch the internal FET off must be cleared by pulsing ENABLE low for at least 200ns, then reasserting ENABLE before normal operation can resume.

## GATE Connections

GATE connects to the gate of the internal N-channel power MOSFET. Normally this pin should be left open circuit. To slow down the voltage ramp at  $V_{\text{OUT}}$ , connect capacitors from GATE to  $V_{\text{OUT}}$  and  $V_{\text{IN}}$ . Size the capacitors so that the GATE to  $V_{\text{IN}}$  capacitor is ten times the size of the GATE to  $V_{\text{OUT}}$  capacitor. This technique to slow down the output voltage ramp will also cause the output discharge time to increase if the capacitor values exceed about 1nF. Additionally, this technique will cause the time delay for a power-not-good fault to increase.

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## Package Information

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:  
 1. D&E DO NOT INCLUDE MOLD FLASH  
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")  
 3. LEADS TO BE COPLANAR WITHIN .102mm (.004")  
 4. CONTROLLING DIMENSION: MILLIMETER  
 5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE  
 6. N = NUMBER OF PINS

**MAXIM**  
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 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150" TITLE

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21-0041 A DOCUMENT CONTROL NUMBER REV

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