



**THE DATASHEET OF  
VND830PTR-E**



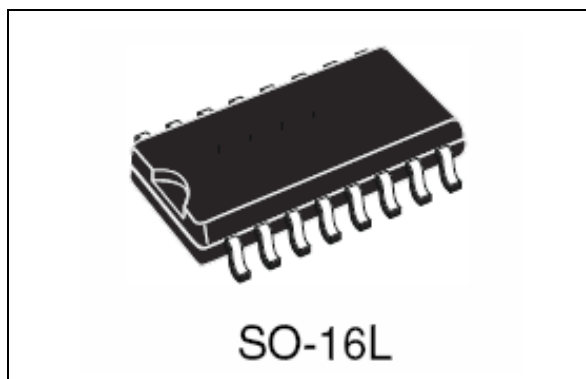
## Double channel high-side driver

### Features

Type	$R_{DS(on)}$	$I_{OUT}$	$V_{CC}$
VND830P-E	60 m $\Omega$ <sup>(1)</sup>	6 A <sup>(1)</sup>	36 V

1. Per each channel.

- ECOPACK<sup>®</sup>: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Very low standby current
- CMOS compatible input
- On-state open-load detection
- Off-state open-load detection
- Thermal shutdown protection and diagnosis
- Undervoltage shutdown
- Overvoltage clamp
- Output stuck to  $V_{CC}$  detection
- Load current limitation
- Reverse battery protection
- Electrostatic discharge protection



### Description

The VND830P-E is a monolithic device made by using STMicroelectronics<sup>™</sup> VIPower<sup>™</sup> M0-3 technology, intended for driving any kind of load with one side connected to ground.

Active  $V_{CC}$  pin voltage clamp protects the devices against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects open-load condition both is on-state and off-state. Output shorted to  $V_{CC}$  is detected in the off-state. Device automatically turns-off in case of ground pin disconnection.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
SO-16L	VND830P-E	VND830PTR-E

# Contents

<b>1</b>	<b>Block diagram and pin description</b>	<b>5</b>
<b>2</b>	<b>Electrical specifications</b>	<b>6</b>
2.1	Absolute maximum ratings	6
2.2	Thermal data	7
2.3	Electrical characteristics	7
2.4	Electrical characteristics curves	13
<b>3</b>	<b>Application information</b>	<b>16</b>
3.1	GND protection network against reverse battery	16
3.1.1	Solution 1: a resistor in the ground line (RGND only)	16
3.1.2	Solution 2: a diode (D <sub>GND</sub> ) in the ground line	17
3.2	Load dump protection	17
3.3	MCU I/O protection	17
3.4	Open-load detection in off-state	18
3.5	Maximum demagnetization energy	19
<b>4</b>	<b>Package and PCB thermal data</b>	<b>20</b>
4.1	SO-16L thermal data	20
<b>5</b>	<b>Package and packing information</b>	<b>23</b>
5.1	ECOPACK <sup>®</sup> packages	23
5.2	SO-16L package information	23
5.3	SO-16L packing information	25
<b>6</b>	<b>Revision history</b>	<b>26</b>

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Suggested connections for unused and not connected pins . . . . .	5
Table 3.	Absolute maximum ratings . . . . .	6
Table 4.	Thermal data (per island) . . . . .	7
Table 5.	Power output. . . . .	7
Table 6.	Protections . . . . .	8
Table 7.	V <sub>CC</sub> - output diode . . . . .	8
Table 8.	Status pin . . . . .	8
Table 9.	Switching (V <sub>CC</sub> = 13 V) . . . . .	9
Table 10.	Open-load detection . . . . .	9
Table 11.	Logic input . . . . .	9
Table 12.	Truth table. . . . .	10
Table 13.	Electrical transient requirements on V <sub>CC</sub> pin (part 1) . . . . .	11
Table 14.	Electrical transient requirements on V <sub>CC</sub> pin (part 2) . . . . .	11
Table 15.	Electrical transient requirements on V <sub>CC</sub> pin (part 3) . . . . .	11
Table 16.	Thermal parameters . . . . .	22
Table 17.	SO-16L mechanical data . . . . .	24
Table 18.	Document revision history . . . . .	26

## List of figures

Figure 1.	Block diagram . . . . .	5
Figure 2.	Configuration diagram (top view) . . . . .	5
Figure 3.	Current and voltage conventions . . . . .	7
Figure 4.	Switching time waveforms . . . . .	10
Figure 5.	Waveforms . . . . .	12
Figure 6.	Off-state output current . . . . .	13
Figure 7.	High level input current . . . . .	13
Figure 8.	Input clamp voltage . . . . .	13
Figure 9.	Status leakage current . . . . .	13
Figure 10.	Status low output voltage . . . . .	13
Figure 11.	Status clamp voltage . . . . .	13
Figure 12.	Overshoot shutdown . . . . .	14
Figure 13.	$I_{LIM}$ vs $T_{case}$ . . . . .	14
Figure 14.	Turn-on voltage slope . . . . .	14
Figure 15.	Turn-off voltage slope . . . . .	14
Figure 16.	On-state resistance vs $T_{case}$ . . . . .	14
Figure 17.	On-state resistance vs $V_{CC}$ . . . . .	14
Figure 18.	Input high level . . . . .	15
Figure 19.	Input low level . . . . .	15
Figure 20.	Open-load on-state detection threshold . . . . .	15
Figure 21.	Open-load off-state detection threshold . . . . .	15
Figure 22.	Input hysteresis voltage . . . . .	15
Figure 23.	Application schematic . . . . .	16
Figure 24.	Open-load detection in off-state . . . . .	18
Figure 25.	SO-16L maximum turn-off current versus load inductance . . . . .	19
Figure 26.	SO-16L PC board . . . . .	20
Figure 27.	$R_{thj-amb}$ vs PCB copper area in open box free air condition . . . . .	20
Figure 28.	SO-16 L thermal impedance junction ambient single pulse . . . . .	21
Figure 29.	Thermal fitting model of a quad channel HSD in SO-16L . . . . .	21
Figure 30.	SO-16L package dimensions . . . . .	23
Figure 31.	SO-16L tube shipment (no suffix) . . . . .	25
Figure 32.	Tape and reel shipment (suffix "TR") . . . . .	25

# 1 Block diagram and pin description

Figure 1. Block diagram

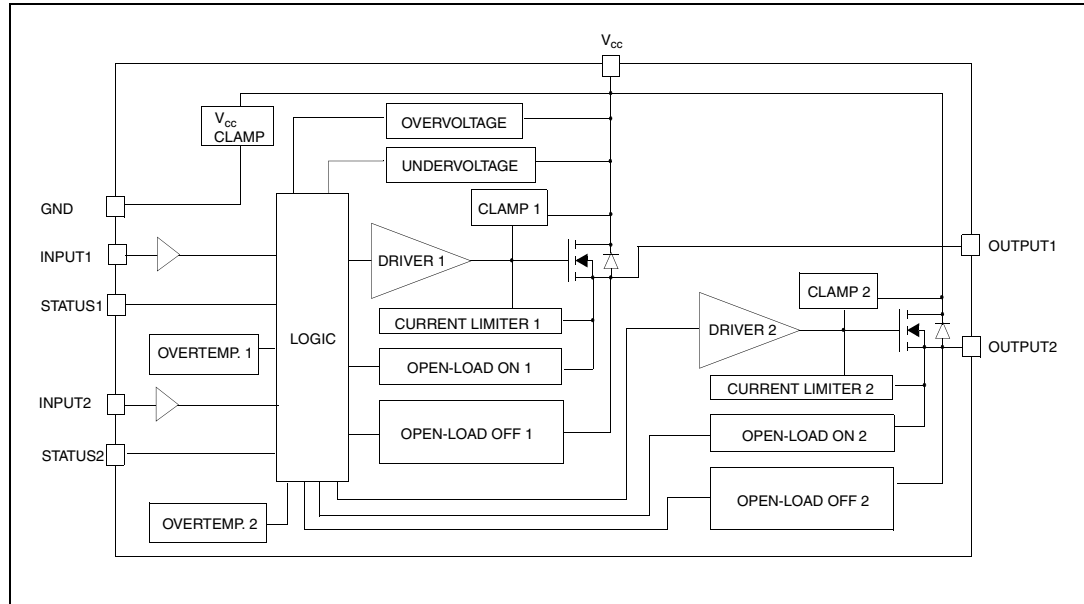


Figure 2. Configuration diagram (top view)

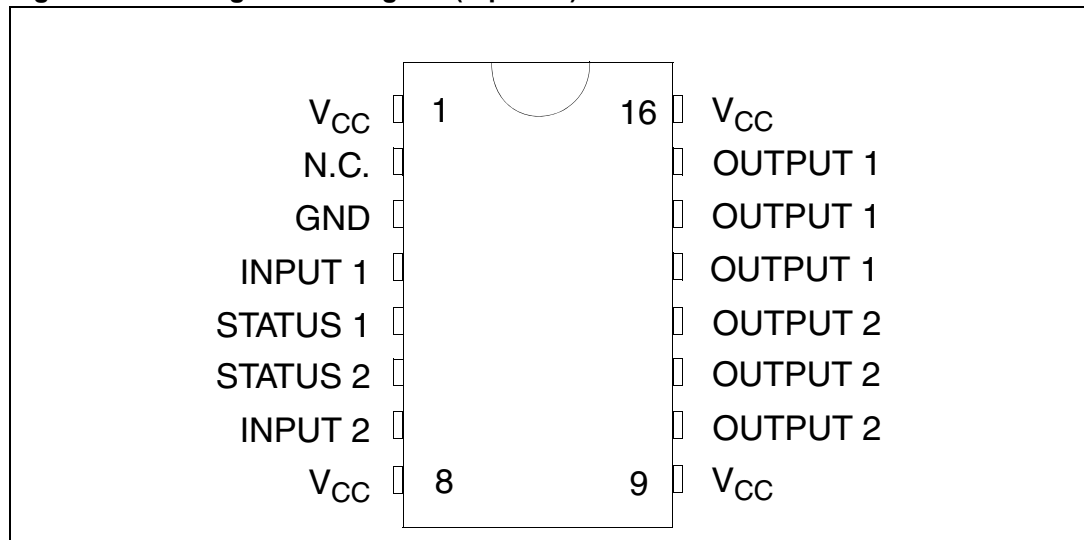


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground	-	X	-	Through 10 KΩ resistor

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	- 0.3	V
$-I_{GND}$	DC reverse ground pin current	- 200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	- 6	A
$I_{IN}$	DC input current	+/- 10	mA
$I_{STAT}$	DC status current	+/- 10	mA
$V_{ESD}$	Electrostatic discharge (Human Body Model: R=1.5 K $\Omega$ ; C = 100 pF)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- $V_{CC}$	5000	V
$E_{MAX}$	Maximum switching energy (L = 1.8 mH; $R_L = 0 \Omega$ ; $V_{bat} = 13.5 V$ ; $T_{jstart} = 150 \text{ }^\circ\text{C}$ ; $I_L = 9 A$ )	102	mJ
$P_{tot}$	Power dissipation $T_{lead} = 25 \text{ }^\circ\text{C}$	8.3	W
$T_j$	Junction operating temperature	Internally limited	$^\circ\text{C}$
$T_C$	Case operating temperature	- 40 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$

## 2.2 Thermal data

**Table 4. Thermal data (per island)**

Symbol	Parameter	Value		Unit
$R_{thj-lead}$	Thermal resistance junction-lead (max)	15		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (max)	65 <sup>(1)</sup>	48 <sup>(2)</sup>	°C/W

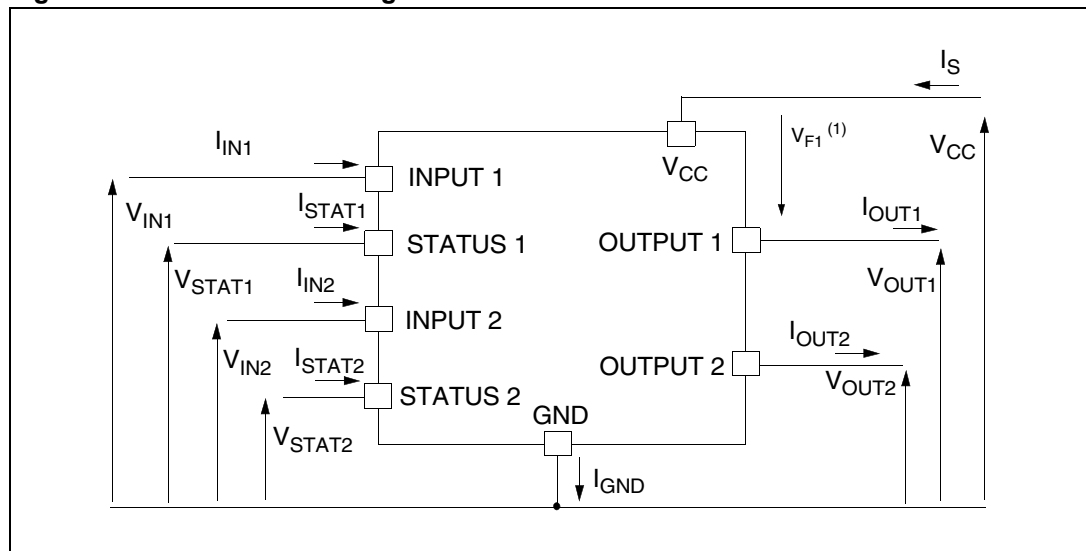
1. When mounted on a standard single-sided FR-4 board with 0.5 cm<sup>2</sup> of Cu (at least 35 μm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6 cm<sup>2</sup> of Cu (at least 35 μm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.

## 2.3 Electrical characteristics

Values specified in this section are for 8 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>j</sub> < 150 °C, unless otherwise stated.

(Per each channel)

**Figure 3. Current and voltage conventions**



1.  $V_{Fn} = V_{CCn} - V_{OUTn}$  during reverse battery condition.

**Table 5. Power output**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}^{(1)}$	Operating supply voltage		5.5	13	36	V
$V_{USD}^{(1)}$	Undervoltage shutdown		3	4	5.5	V
$V_{OV}^{(1)}$	Overvoltage shutdown		36			V
$R_{ON}$	On-state resistance	$I_{OUT} = 2\text{ A}; T_j = 25\text{ °C}$ $I_{OUT} = 2\text{ A}; V_{CC} > 8\text{ V}$			60 120	mΩ mΩ

**Table 5. Power output (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_S^{(1)}$	Supply current	Off-state; $V_{CC} = 13\text{ V}$ ; $V_{IN} = V_{OUT} = 0\text{ V}$		12	40	$\mu\text{A}$
		Off-state; $V_{CC} = 13\text{ V}$ ; $V_{IN} = V_{OUT} = 0\text{ V}$ ; $T_j = 25^\circ\text{C}$		12	25	$\mu\text{A}$
		On-state; $V_{CC} = 13\text{ V}$ ; $V_{IN} = 5\text{ V}$ ; $I_{OUT} = 0\text{ A}$		5	7	$\text{mA}$
$I_{L(\text{off}1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$	0		50	$\mu\text{A}$
$I_{L(\text{off}2)}$	Off-state output current	$V_{IN} = 0\text{ V}$ ; $V_{OUT} = 3.5\text{ V}$	-75		0	$\mu\text{A}$
$I_{L(\text{off}3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 125^\circ\text{C}$			5	$\mu\text{A}$
$I_{L(\text{off}4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 25^\circ\text{C}$			3	$\mu\text{A}$

1. Per device.

**Table 6. Protections<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{TSD}$	Shutdown temperature		150	175	200	$^\circ\text{C}$
$T_R$	Reset temperature		135			$^\circ\text{C}$
$T_{hyst}$	Thermal hysteresis		7	15		$^\circ\text{C}$
$T_{SDL}$	Status delay in overload conditions	$T_j > T_{TSD}$			20	$\mu\text{s}$
$I_{lim}$	Current limitation	$V_{CC} = 13\text{ V}$	6	9	15	$\text{A}$
		$5.5\text{ V} < V_{CC} < 36\text{ V}$			15	$\text{A}$
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 2\text{ A}$ ; $L = 6\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	$\text{V}$

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

**Table 7.  $V_{CC}$  - output diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$-I_{OUT} = 1.3\text{ A}$ ; $T_j = 150^\circ\text{C}$	-	-	0.6	$\text{V}$

**Table 8. Status pin**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{STAT}$	Status low output voltage	$I_{STAT} = 1.6\text{ mA}$			0.5	$\text{V}$
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT} = 5\text{ V}$			10	$\mu\text{A}$
$C_{STAT}$	Status pin input capacitance	Normal operation; $V_{STAT} = 5\text{ V}$			100	$\text{pF}$

**Table 8. Status pin (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>SCL</sub>	Status clamp voltage	I <sub>STAT</sub> = 1 mA	6	6.8	8	V
		I <sub>STAT</sub> = -1 mA		-0.7		V

**Table 9. Switching (V<sub>CC</sub> = 13 V)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	R <sub>L</sub> = 6.5 Ω from V <sub>IN</sub> rising edge to V <sub>OUT</sub> = 1.3 V	-	30	-	μs
t <sub>d(off)</sub>	Turn-off delay time	R <sub>L</sub> = 6.5 Ω from V <sub>IN</sub> falling edge to V <sub>OUT</sub> = 11.7 V	-	30	-	μs
dV/dt <sub>(on)</sub>	Turn-on voltage slope	R <sub>L</sub> = 6.5 Ω from V <sub>OUT</sub> = 1.3 V to V <sub>OUT</sub> = 10.4 V	-	See Figure 14	-	V/μs
dV/dt <sub>(off)</sub>	Turn-off voltage slope	R <sub>L</sub> = 6.5 Ω from V <sub>OUT</sub> = 11.7 V to V <sub>OUT</sub> = 1.3 V	-	See Figure 15	-	V/μs

**Table 10. Open-load detection**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I <sub>OL</sub>	Open-load on-state detection threshold	V <sub>IN</sub> = 5 V	50	100	200	mA
t <sub>DOL(on)</sub>	Open-load on-state detection delay	I <sub>OUT</sub> = 0 A			200	μs
V <sub>OL</sub>	Open-load off-state voltage detection threshold	V <sub>IN</sub> = 0 V	1.5	2.5	3.5	V
t <sub>DOL(off)</sub>	Open-load detection delay at turn-off				1000	μs

**Table 11. Logic input**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Input low level				1.25	V
I <sub>IL</sub>	Low level input current	V <sub>IN</sub> = 1.25 V	1			μA
V <sub>IH</sub>	Input high level		3.25			V
I <sub>IH</sub>	High level input current	V <sub>IN</sub> = 3.25 V			10	μA
V <sub>hyst</sub>	Input hysteresis voltage		0.5			V
V <sub>ICL</sub>	Input clamp voltage	I <sub>IN</sub> = 1 mA	6	6.8	8	V
		I <sub>IN</sub> = -1 mA		-0.7		V

Figure 4. Switching time waveforms

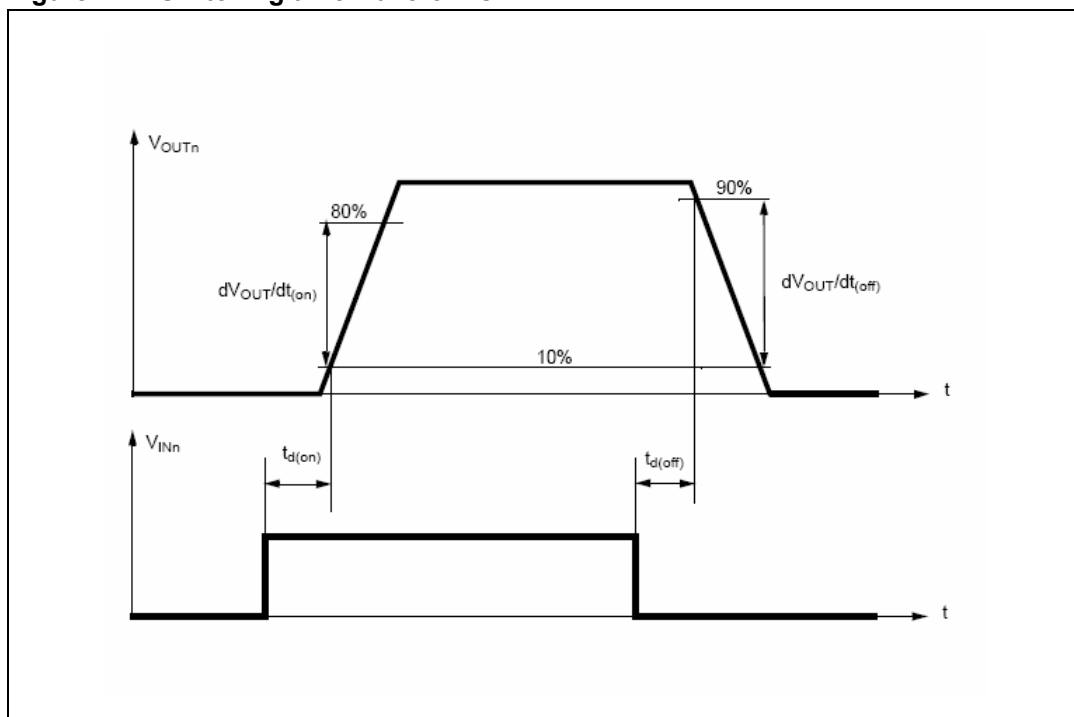


Table 12. Truth table

Conditions	Input	Output	Sense
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_j < T_{TSD})$ H $(T_j > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output voltage $> V_{OL}$	L	H	L
	H	H	H
Output current $< I_{OL}$	L	L	H
	H	H	L

Table 13. Electrical transient requirements on V<sub>CC</sub> pin (part 1)

ISO T/R 7637/1 test pulse	Test levels				Delays and impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms, 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms, 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs, 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs, 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

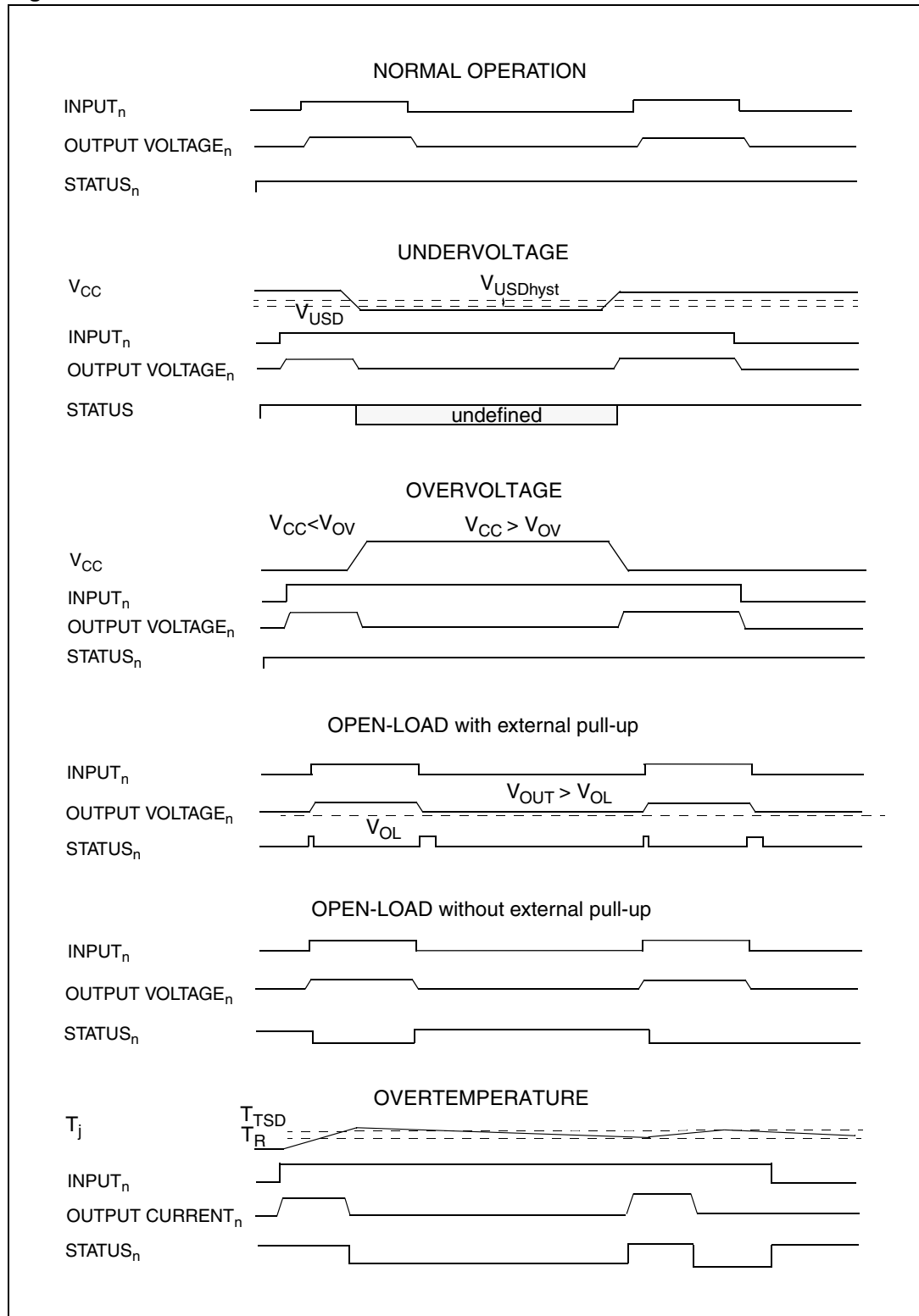
Table 14. Electrical transient requirements on V<sub>CC</sub> pin (part 2)

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 15. Electrical transient requirements on V<sub>CC</sub> pin (part 3)

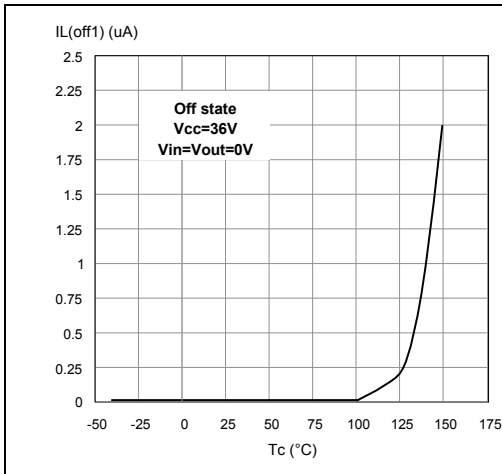
Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 5. Waveforms

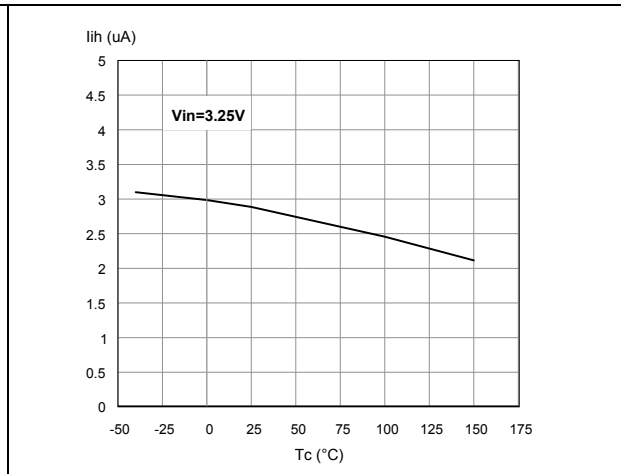


## 2.4 Electrical characteristics curves

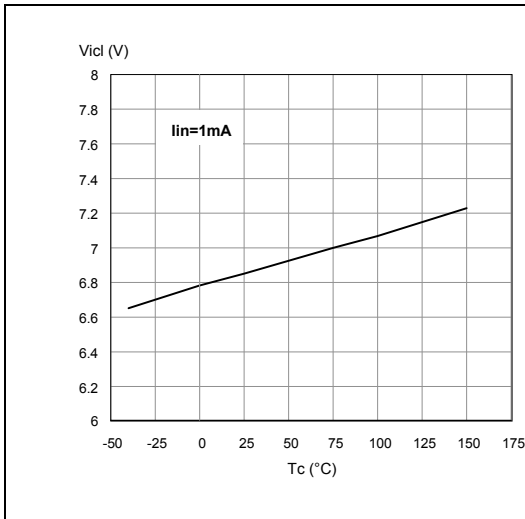
**Figure 6. Off-state output current**



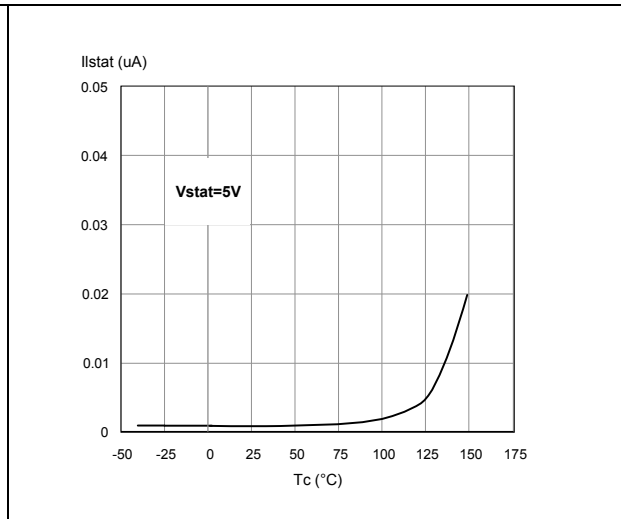
**Figure 7. High level input current**



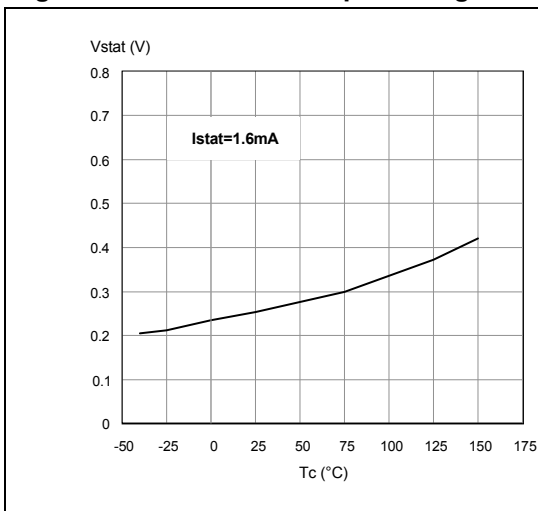
**Figure 8. Input clamp voltage**



**Figure 9. Status leakage current**



**Figure 10. Status low output voltage**



**Figure 11. Status clamp voltage**

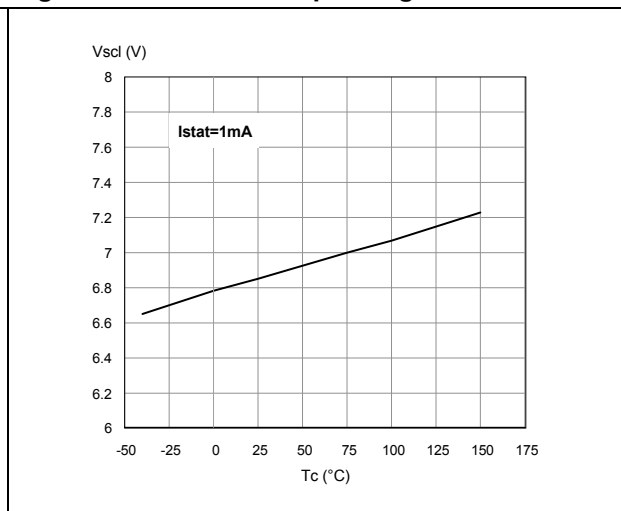


Figure 12. Overvoltage shutdown

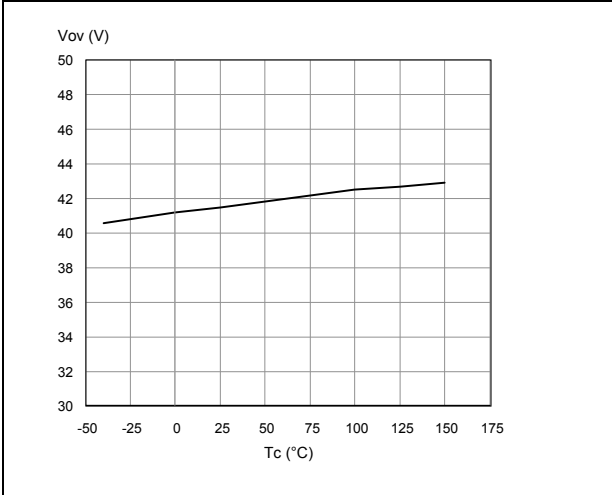


Figure 13.  $I_{LIM}$  vs  $T_{case}$

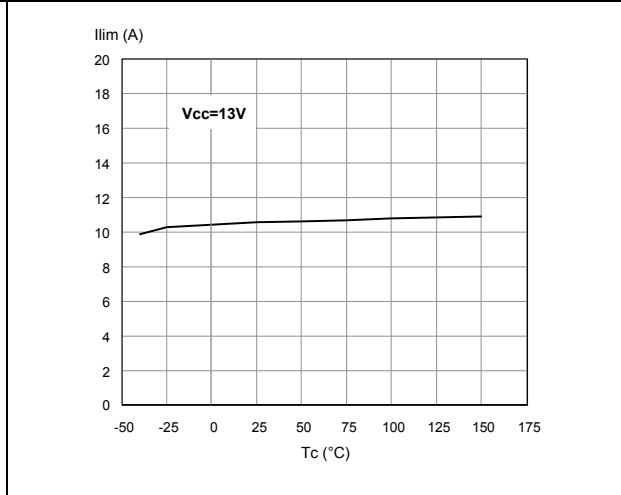


Figure 14. Turn-on voltage slope

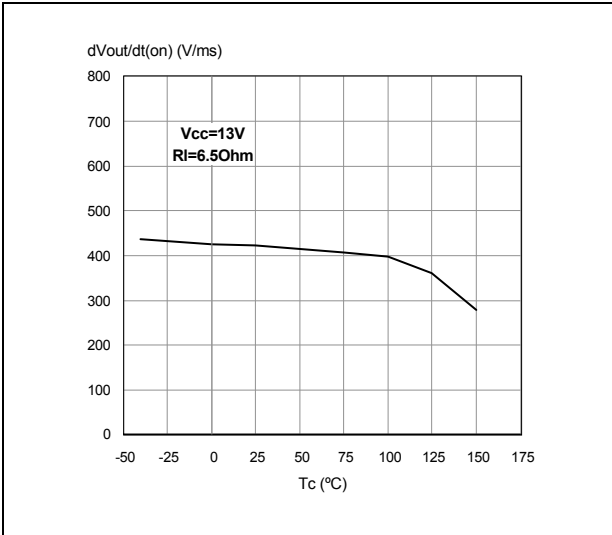


Figure 15. Turn-off voltage slope

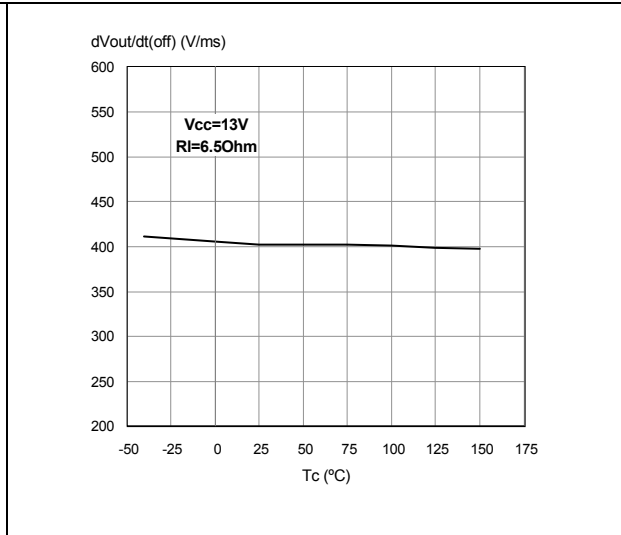


Figure 16. On-state resistance vs  $T_{case}$

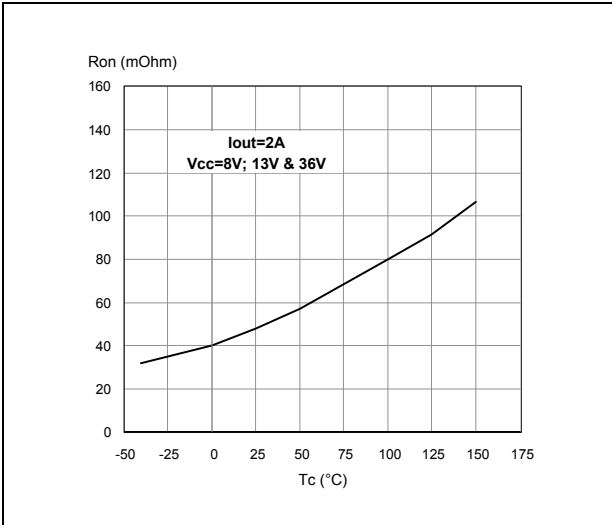


Figure 17. On-state resistance vs  $V_{CC}$

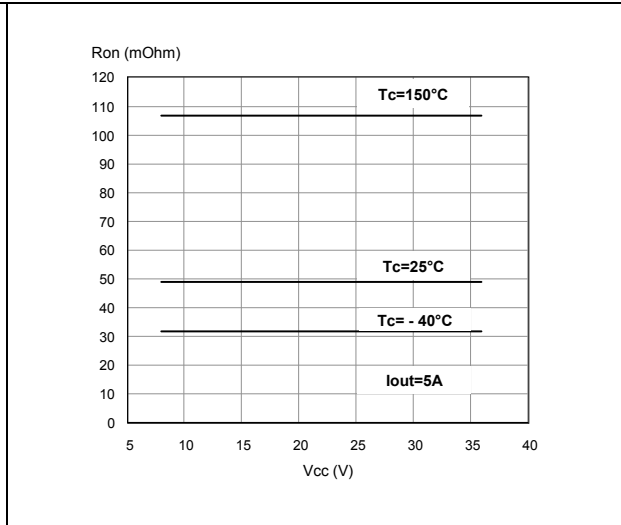


Figure 18. Input high level

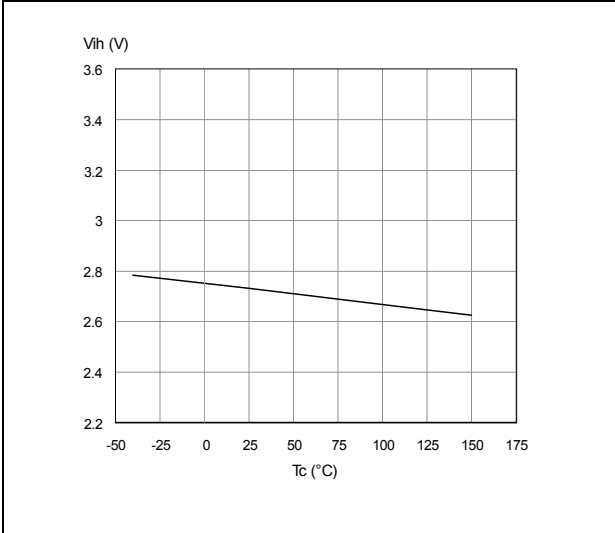


Figure 19. Input low level

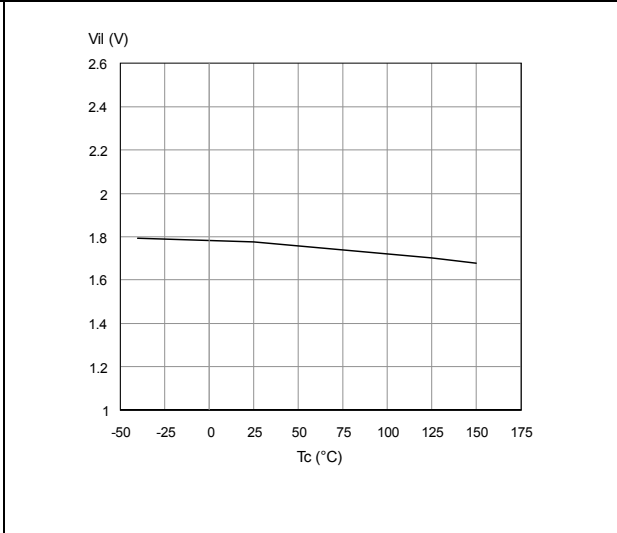


Figure 20. Open-load on-state detection threshold

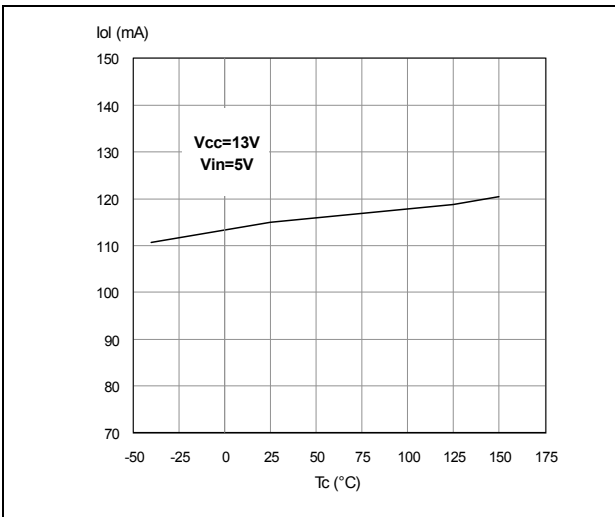


Figure 21. Open-load off-state detection threshold

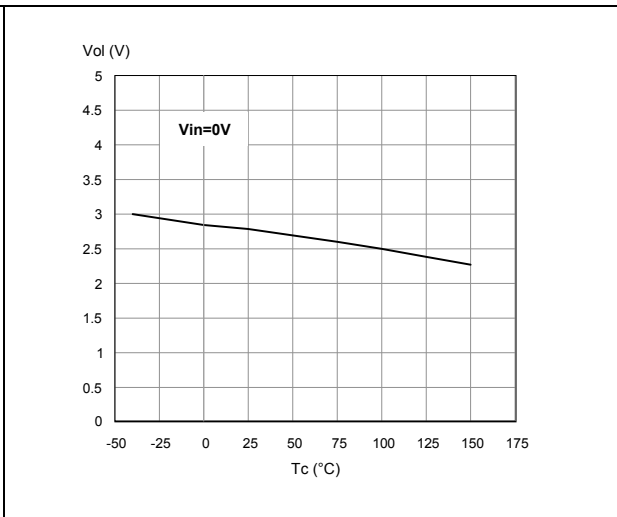
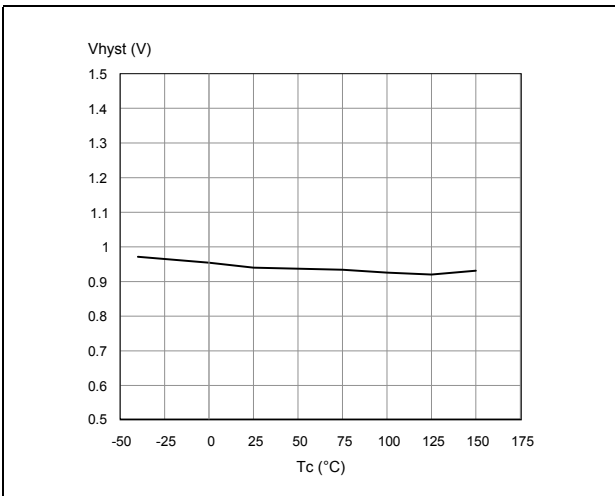
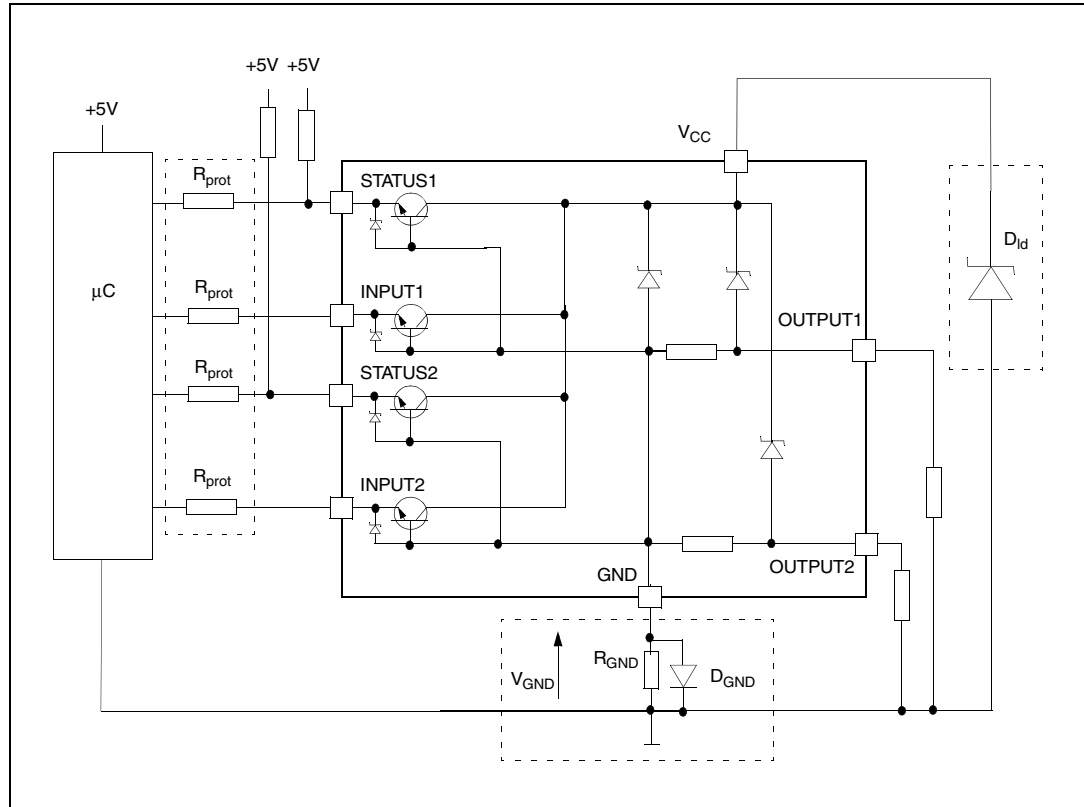


Figure 22. Input hysteresis voltage



### 3 Application information

Figure 23. Application schematic



#### 3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

##### 3.1.1 Solution 1: a resistor in the ground line ( $R_{GND}$ only)

This can be used with any type of load.

The following shows how to dimension the  $R_{GND}$  resistor:

1.  $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power dissipation in  $R_{GND}$  (when  $V_{CC} < 0$  during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not common with the device ground, then the  $R_{GND}$  produces a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using [Section 3.1.2](#) described below.

### 3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND} = 1 \text{ k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device is driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network produce a shift (~600 mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  maximum DC rating. The same applies if the device is subjected to transients on the  $V_{CC}$  line that are greater than those shown in [Table 13](#).

## 3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins are pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the microcontroller I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

### Example

For the following conditions:

$$V_{CCpeak} = -100 \text{ V}$$

$$I_{latchup} \geq 20 \text{ mA}$$

$$V_{OH\mu C} \geq 4.5 \text{ V}$$

$$5 \text{ k}\Omega \leq R_{prot} \leq 65 \text{ k}\Omega.$$

The recommended values are:

$$R_{prot} = 10 \text{ k}\Omega$$

### 3.4 Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor ( $R_{PU}$ ) connected between OUTPUT pin and a positive supply voltage ( $V_{PU}$ ) like the +5 V line used to supply the microprocessor.

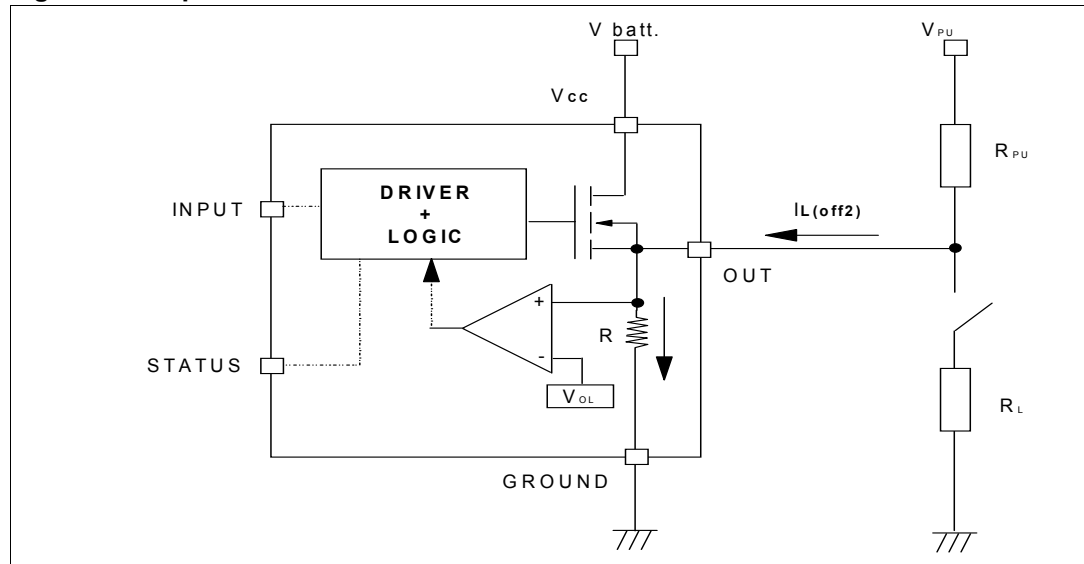
The external resistor has to be selected according to the following requirements:

1. No false open-load indication when load is connected: in this case it needs to avoid  $V_{OUT}$  to be higher than  $V_{OLmin}$ ; this results in the following condition  $V_{OUT} = (V_{PU} / (R_L + R_{PU}))R_L < V_{OLmin}$ .
2. No misdetection when load is disconnected: in this case the  $V_{OUT}$  has to be higher than  $V_{OLmax}$ ; this results in the following condition  $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$ .

Because  $I_{S(OFF)}$  may significantly increase if  $V_{out}$  is pulled high (up to several mA), the pull-up resistor  $R_{PU}$  should be connected to a supply that is switched OFF when the module is in standby.

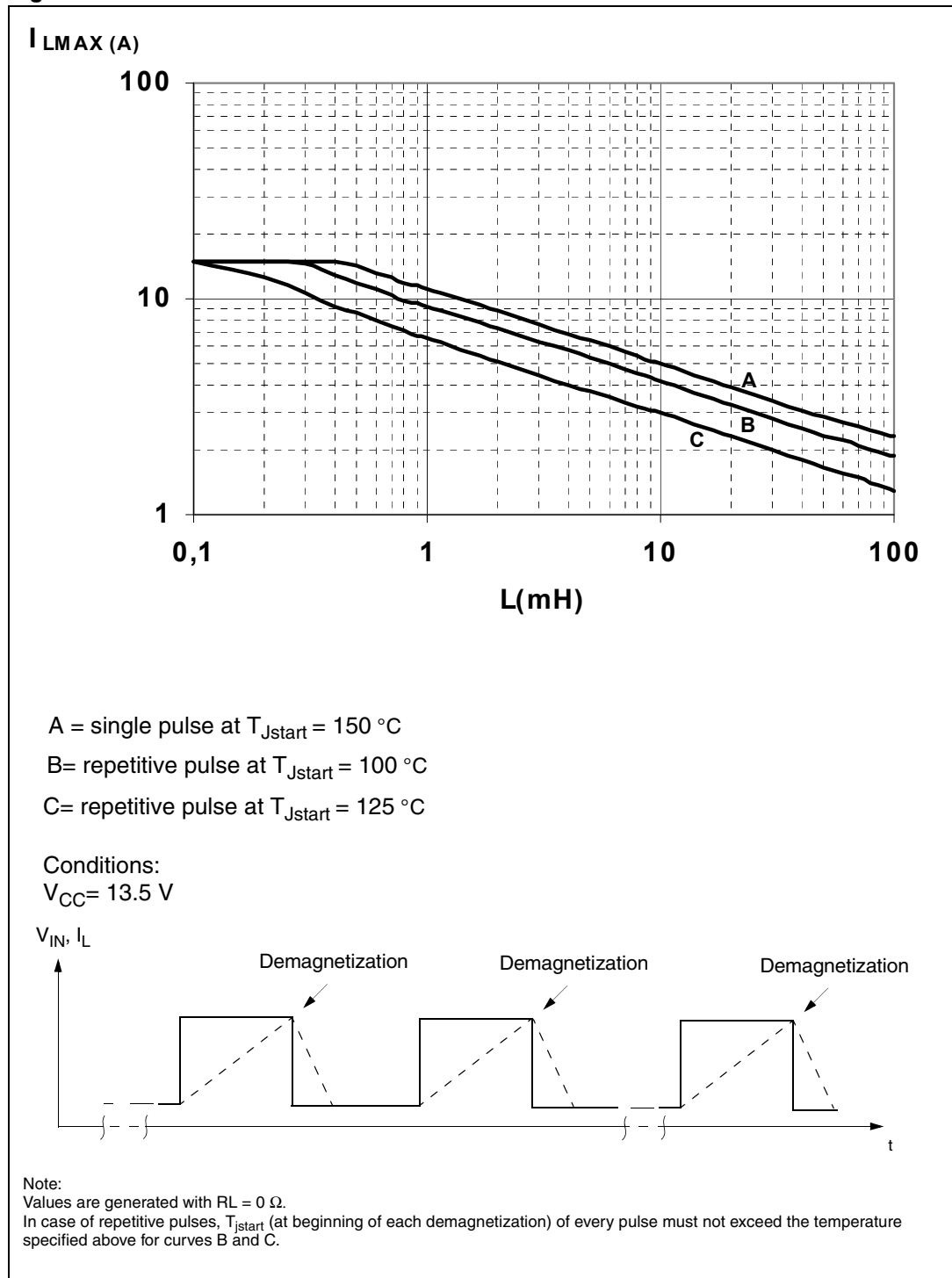
The values of  $V_{OLmin}$ ,  $V_{OLmax}$  and  $I_{L(off2)}$  are available in [Chapter 2: Electrical specifications](#).

**Figure 24. Open-load detection in off-state**



### 3.5 Maximum demagnetization energy

Figure 25. SO-16L maximum turn-off current versus load inductance



## 4 Package and PCB thermal data

### 4.1 SO-16L thermal data

Figure 26. SO-16L PC board<sup>(1)</sup>

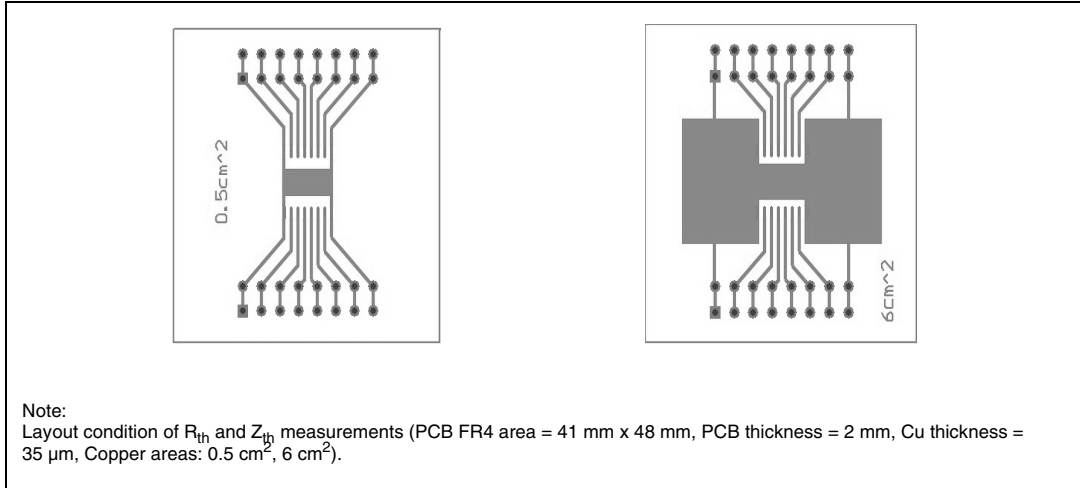


Figure 27.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

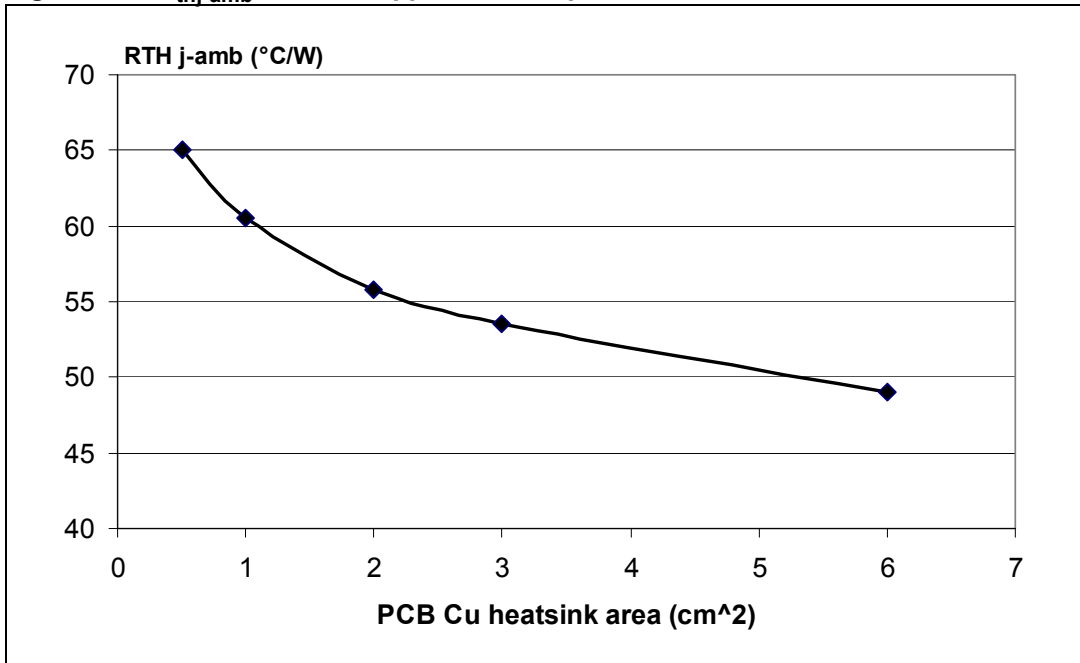
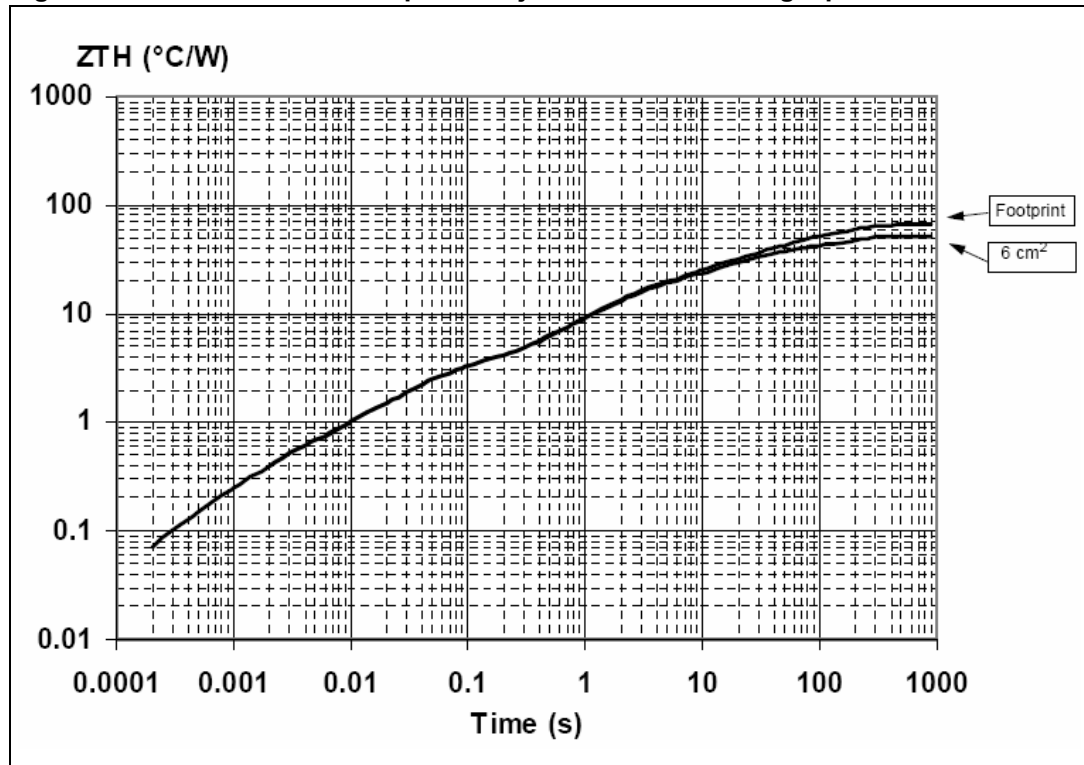


Figure 28. SO-16 L thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 29. Thermal fitting model of a quad channel HSD in SO-16L

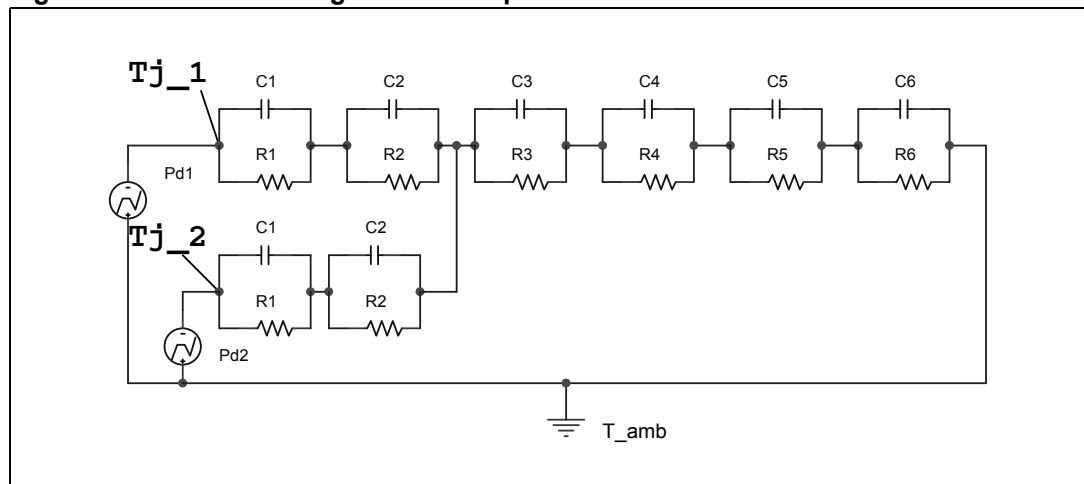


Table 16. Thermal parameters

Area/ island (cm <sup>2</sup> )	Footprint	6
R1 (°C/W)	0.05	
R2 (°C/W)	0.3	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.001	
C2 (W.s/°C)	5.00E-03	
C3 (W.s/°C)	0.02	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	1	
C6 (W.s/°C)	3	5

## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 5.2 SO-16L package information

Figure 30. SO-16L package dimensions

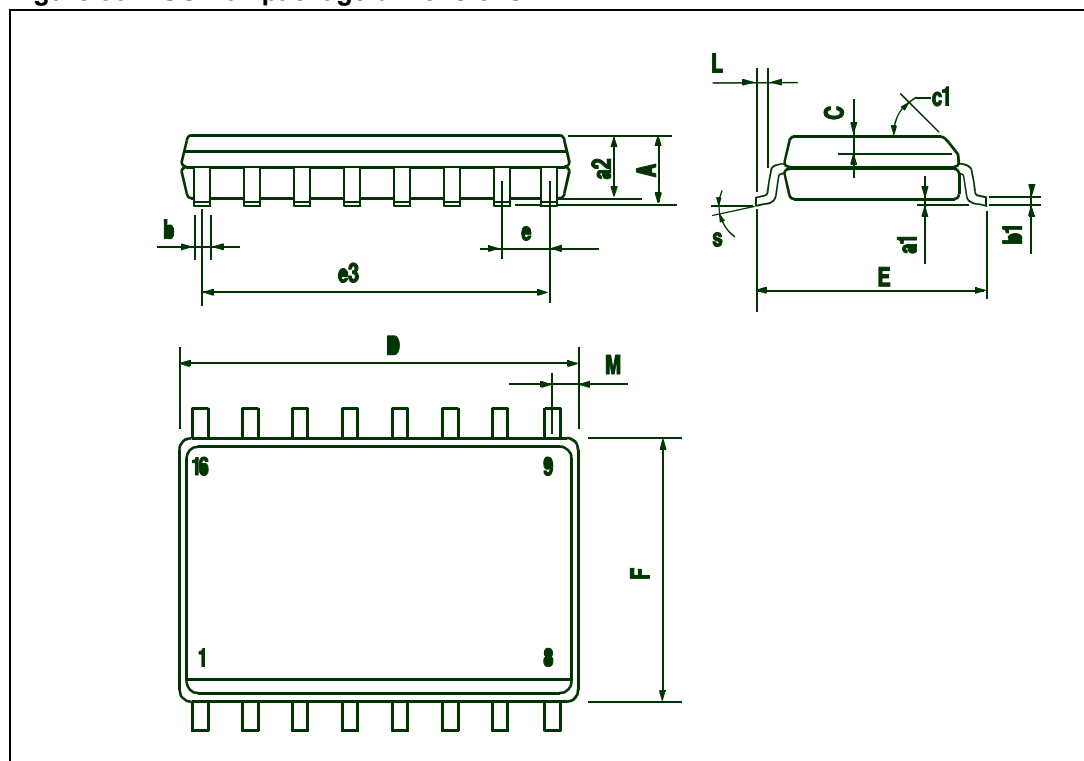


Table 17. SO-16L mechanical data

DIM.	mm.		
	Min.	Typ.	Max.
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		
D	10.1		10.5
E	10.0		10.65
e		1.27	
e3		8.89	
F	7.4		7.6
L	0.5		1.27
M			0.75
S	8° (max.)		

### 5.3 SO-16L packing information

Figure 31. SO-16L tube shipment (no suffix)

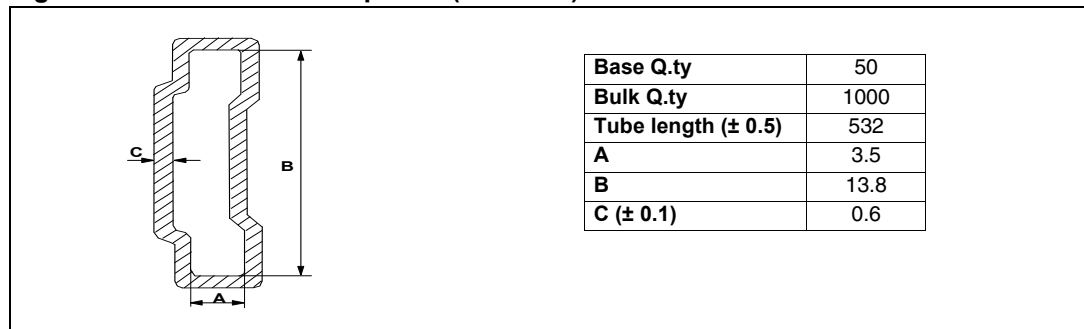
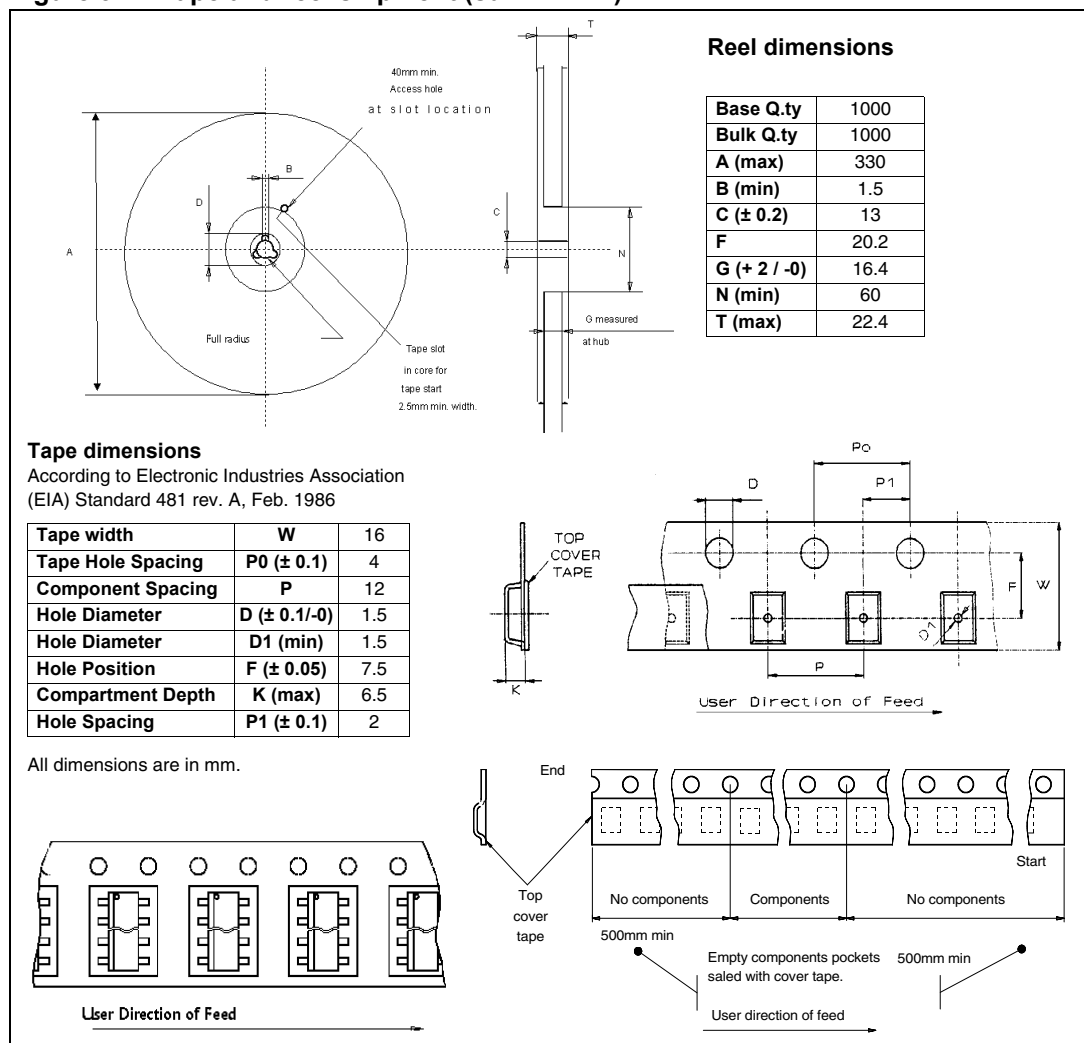


Figure 32. Tape and reel shipment (suffix “TR”)



## 6 Revision history

**Table 18. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
25-May-2010	1	Initial release.
22-Sep-2010	2	Changed document status from preliminary data to datasheet.
19-Sep-2013	3	Updated Disclaimer

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved


STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View VND830PTR-E on WIN SOURCE](#)
-  [STMicroelectronics Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management