



**THE DATASHEET OF
LP8556TMX-E09/NOPB**



LP8556 High-Efficiency LED Backlight Driver For Tablets

1 Features

- High-efficiency DC/DC boost converter with integrated 0.19-Ω power MOSFET and three switching frequency options: 312 kHz, 625 kHz, and 1250 kHz
- 2.7-V to 36-V Boost switch input voltage range supports multi-cell Li-Ion batteries (2.7-V to 20-V V_{DD} input range)
- 7-V to 43-V Boost switch output voltage range supports as few as 3 WLEDs in series per channel and as many as 12
- Configurable channel count (1 to 6)
- Up to 50 mA per channel
- PWM and / or I²C brightness control
- Phase-shift PWM mode reduces audible noise
- Adaptive dimming for higher LED drive optical efficiency
- Programmable edge-rate control and spread spectrum scheme minimize switching noise and improve EMI performance
- LED fault (short and open) detection, UVLO, TSD, OCP, and OVP (up to 6 threshold options)
- Available in tiny 20-pin, 0.4-mm pitch DSBGA package and 24-pin, 0.5-mm pitch WQFN package

2 Applications

LED backlights for tablet LCDs

3 Description

The LP8556 device is a white-LED driver featuring an asynchronous boost converter and six high precision current sinks that can be controlled by a PWM signal or an I²C master.

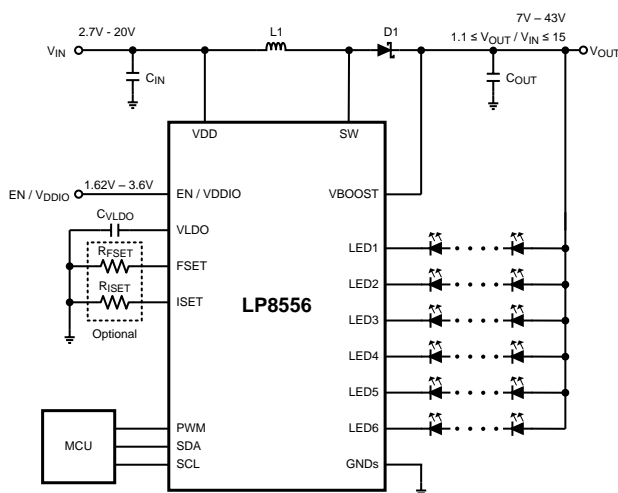
The boost converter uses adaptive output voltage control for setting the optimal LED driver voltages as low as 7 V and as high as 43 V. This feature minimizes the power consumption by adjusting the output voltage to the lowest sufficient level under all conditions. The converter can operate at three switching frequencies: 312 kHz, 625 kHz, and 1250 kHz, which can be set with an external resistor or pre-configured via EPROM. Programmable slew rate control and spread spectrum scheme minimize switching noise and improve EMI performance.

LED current sinks can be set with the PWM dimming resolution of up to 15 bits. Proprietary adaptive dimming mode allows higher system power saving. In addition, phase shifted LED PWM dimming allows reduced audible noise and smaller boost output capacitors.

The LP8556 device has a full set of fault-protection features that ensure robust operation of the device and external components. The set consists of input undervoltage lockout (UVLO), thermal shutdown (TSD), overcurrent protection (OCP), up to 6 levels of overvoltage protection (OVP), LED open and short detection.

The LP8556 device operates over the ambient temperature range of -30°C to +85°C. It is available in space-saving 20-pin DSBGA and 24-pad WQFN packages.

Simplified Schematic



Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE |
|-------------|------------|--------------------------|
| LP8556 | DSBGA (20) | 2.401 mm × 1.74 mm (MAX) |
| | WQFN (24) | 4.00 mm × 4.00 mm (NOM) |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

| Changes from Revision K (March 2019) to Revision L | Page |
|---|-------------|
| • Deleted 03H register from Table 9 | 32 |
| • Deleted 8.6.1.4 Identification section from the Register Bit Explanations | 33 |

| Changes from Revision J (January 2018) to Revision K | Page |
|--|-------------|
| • Added separate ESD Rating for the WQFN package - changed from "±2000" to "±1000" | 6 |

| Changes from Revision I (March 2016) to Revision J | Page |
|--|-------------|
| • Added content in VBOOST_RANGE description of CFG9E | 38 |

| Changes from Revision H (December 2014) to Revision I | Page |
|---|-------------|
| • Changed "25 mA" to "23 mA" - E00, E08 and E09 SQ rows, E09, E11 TME rows | 3 |
| • Changed <i>Handing Ratings</i> table to <i>ESD Ratings</i> | 6 |
| • Added updated <i>Thermal Information</i> | 7 |
| • Changed "8" to "10" in PWMres row | 9 |
| • Changed subtracted 1 from bit value of all Table 4 " f_{PWM} [Hz] (Resolution)" entries | 20 |
| • Changed subtracted 1 from bit value of all Table 5 " f_{PWM} [Hz] (Resolution)" entries except 2402 | 21 |
| • Changed subtracted 1 from bit value of all Table 11 " f_{PWM} [Hz] (Resolution)" entries | 45 |
| • Changed "via EPROM" in Table 13 title to "With an External Resistor" | 46 |
| • Changed subtracted 1 from bit values of all Table 13 " f_{PWM} [Hz] (Resolution)" entries except 2402 | 46 |

Changes from Revision G (November 2013) to Revision H
Page

| | |
|--|---|
| <ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>Handling Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
|--|---|

Changes from Revision E (August 2013) to Revision G
Page

| | |
|--|----------------------|
| <ul style="list-style-type: none"> Changed Description of "1=" for OCP row in Fault table, STATUS Register Section..... Changed A7h values for E02, E03, E04, E06, E07, E09, E11 DSGBA EPROM Bit Explanations tables Deleted E00, E01, E08, E10, E12, E13 columns and A8H row from 3 EPROM Bit Explanations table..... Changed values for E00, E08, E09 WQFN EPROM Settings table..... | 34 36 36 37 |
|--|----------------------|

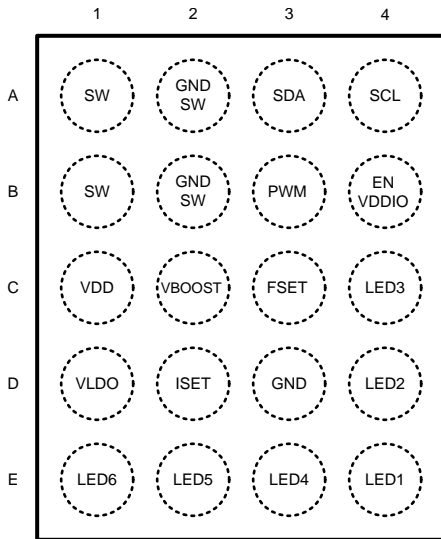
5 Device Options

| ORDERABLE DEVICE ⁽¹⁾ | PACKAGE TYPE | DEVICE OPTION | LED CHANNEL COUNT | MAXIMUM LED CURRENT | BOOST OUTPUT VOLTAGE RANGE |
|---|--------------|---|---|---------------------|-------------------------------------|
| LP8556SQ-E00/NOPB LP8556SQE-E00/NOPB LP8556SQX-E00/NOPB | WQFN | "PWM Only" – Recommended for systems without an I ² C master. | 5 | 23 mA | 16 V to 34.5 V |
| LP8556SQ-E08/NOPB LP8556SQE-E08/NOPB LP8556SQX-E08/NOPB | | | 4 | | |
| LP8556SQ-E09/NOPB LP8556SQE-E09/NOPB LP8556SQX-E09/NOPB | | | 6 | | |
| LP8556TME-E02/NOPB LP8556TMX-E02/NOPB | DSBGA | "PWM and I ² C" - Recommended for systems with an I ² C master. | 6 | 25 mA | 16 V to 30 V |
| LP8556TME-E03/NOPB LP8556TMX-E03/NOPB | | "PWM Only" – Recommended for systems without an I ² C master. | 5 | 20 mA | 16 V to 34.5 V |
| LP8556TME-E04/NOPB LP8556TMX-E04/NOPB | | | 6 | 20 mA | 16 V to 25 V |
| LP8556TME-E05/NOPB LP8556TMX-E05/NOPB | | "Non-programmed" – This option is for evaluation purposes only. | Can be programmed to any available. | 25 mA | Can be programmed to any available. |
| LP8556TME-E06/NOPB LP8556TMX-E06/NOPB | | "PWM Only" – Recommended for systems without an I ² C master. | 5 | 25 mA | 16 V to 39 V |
| LP8556TME-E07/NOPB LP8556TMX-E07/NOPB | | | 4 | 20 mA | 12.88 V to 30 V |
| LP8556TME-E09/NOPB LP8556TMX-E09/NOPB | | | 6 | 23 mA | 16 V to 34.5 V |
| LP8556TME-E11/NOPB LP8556TMX-E11/NOPB | | | "PWM and I ² C" - Recommended for systems with an I ² C master. | 3 | 23 mA |

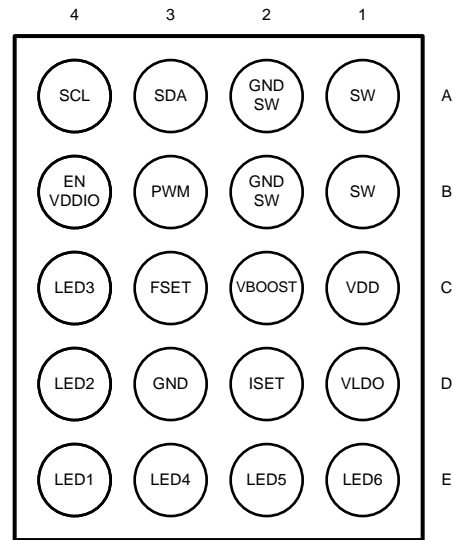
(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the TI website at www.ti.com.

6 Pin Configuration and Functions

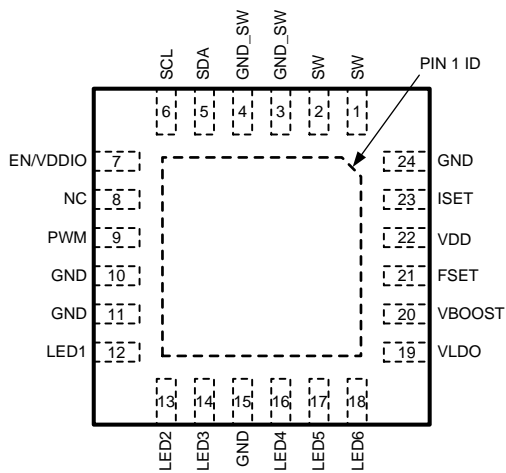
**YFQ Package
20-Pin DSBGA
Top View**



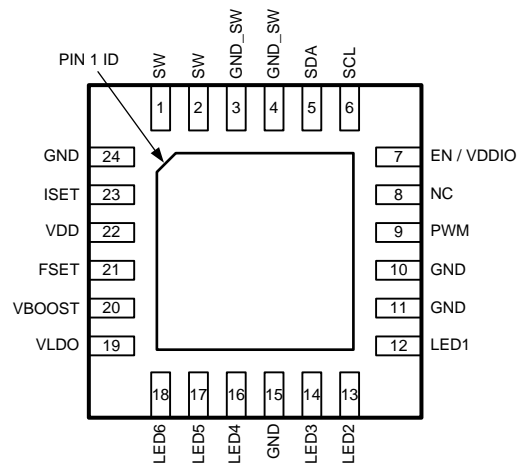
**YFQ Package
20-Pin DSBGA
Bottom View**



**RTW Package
24-Pin WQFN
Top View**



**RTW Package
24-Pin WQFN
Bottom View**



Pin Functions

| PIN | | | TYPE ⁽¹⁾ | DESCRIPTION |
|--------|---------------------|------------|---------------------|--|
| DSBGA | WQFN | NAME | | |
| A1, B1 | 1, 2 | SW | A | A connection to the drain terminal of the integrated power MOSFET. |
| A2, B2 | 3, 4 | GND_SW | G | A connection to the source terminal of the integrated power MOSFET. |
| A3 | 5 | SDA | I/O | I ² C data input/output pin |
| A4 | 6 | SCL | I | I ² C clock input pin |
| B3 | 9 | PWM | I | PWM dimming input. Supply a 75-Hz to 25-kHz PWM signal to control dimming. This pin must be connected to GND if unused. |
| B4 | 7 | EN / VDDIO | P | Dual-purpose pin serving both as a chip enable and as a power supply reference for PWM, SDA, and SCL inputs. Drive this pin with a logic gate capable of sourcing a minimum of 1 mA. |
| C1 | 22 | VDD | P | Device power supply pin. Provide 2.7-V to 20-V supply to this pin. This pin is an input of the internal LDO regulator. The output of the internal LDO is what powers the device. |
| C2 | 20 | VBOOST | A | Boost converter output pin. The internal feedback (FB) and overvoltage protection (OVP) circuitry monitors the voltage on this pin. Connect the converter output capacitor bank close to this pin. |
| C3 | 21 | FSET | A | A connection for setting the boost frequency and PWM output dimming frequency by using an external resistor. Connect a resistor, R _{FSET} , between this pin and the ground reference (see Table 5). This pin may be left floating if PWM_FSET_EN = 0 AND BOOST_FSET_EN = 0 (see Table 10). |
| C4 | 14 | LED3 | A | LED driver - current sink terminal. If unused, it may be left floating. |
| D1 | 19 | VLDO | P | Internal LDO output pin. Connect a capacitor, C _{VLDO} , between this pin and the ground reference. |
| D2 | 23 | ISET | A | A connection for the LED current set resistor. Connect a resistor, R _{ISET} , between this pin and the ground reference. This pin may be left floating if ISET_EN = 0 (see Table 10). |
| D3 | 10, 11, 15, 24, DAP | GND | I | Ground pin. |
| D4 | 13 | LED2 | A | LED driver - current sink pin. If unused, it may be left floating. |
| E1 | 18 | LED6 | A | LED driver - current sink pin. If unused, it may be left floating. |
| E2 | 17 | LED5 | A | LED driver - current sink pin. If unused, it may be left floating. |
| E3 | 16 | LED4 | A | LED driver - current sink pin. If unused, it may be left floating. |
| E4 | 12 | LED1 | A | LED driver - current sink pin. If unused, it may be left floating. |
| — | 8 | NC | — | No Connect pin. |

(1) A: Analog Pin, G: Ground Pin, P: Power Pin, I: Digital Input Pin, I/O: Digital Input/Output Pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

| | MIN | MAX | UNIT |
|---|------|------------|------|
| V _{DD} | -0.3 | 24 | V |
| Voltage on Logic Pins (SCL, SDA, PWM) | -0.3 | 6 | |
| Voltage on Analog Pins (VLDO, EN / VDDIO) | -0.3 | 6 | |
| Voltage on Analog Pins (FSET, ISET) | -0.3 | VLDO + 0.3 | |
| V (LED1...LED6, SW, VBOOST) | -0.3 | 50 | |
| Junction Temperature (T _{J-MAX}) ⁽³⁾ | | 125 | °C |
| Maximum Lead Temperature (Soldering) | | 260 | °C |
| Storage temperature, T _{stg} | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability, see the *Electrical Characteristics* tables.
- (2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} - (R_{θJA} × P_{D-MAX}).

7.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, DSBGA Package ⁽¹⁾ | ±2000 |
| | | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, WQFN Package ⁽¹⁾ | ±1000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|--------------------------------------|------|-----|------|
| VDD | 2.7 | 20 | V |
| EN / VDDIO | 1.62 | 3.6 | V |
| V (LED1...LED6, SW, VBOOST) | 0 | 48 | V |
| Junction temperature, T _J | -30 | 125 | °C |
| Ambient temperature, T _A | -30 | 85 | °C |

- (1) All voltages are with respect to the potential at the GND pins.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LP8556 | | UNIT |
|-------------------------------|--|-------------|------------|------|
| | | YFQ (DSBGA) | RTW (WQFN) | |
| | | 20 PINS | 24 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 66.2 | 35.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.5 | 32.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 15.1 | 13.7 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter | 1.9 | 0.3 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter | 15.0 | 13.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | 3.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

Unless otherwise specified: $V_{DD} = 12\text{ V}$, $EN / V_{DDIO} = 1.8\text{ V}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|---|-----------------|------|------|---------------|
| V_{DDIO} | Supply voltage for digital I/Os | | 1.62 | | 3.6 | V |
| V_{DD} | Input voltage for the internal LDO | | 2.7 | | 20 | V |
| I_{DD} | Standby supply current | EN / VDDIO = 0 V, LDO disabled, $-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | | | 1.6 | μA |
| | Normal mode supply current | LDO enabled, boost disabled | | 0.9 | 1.5 | mA |
| | | LDO enabled, boost enabled, no load | | | 2.2 | |
| f_{OSC} | Internal oscillator frequency accuracy | | -4% | | 4% | |
| | | $-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | -7% | | 7% | |
| V_{LDO} | LDO output voltage | $V_{DD} \geq 3.1\text{ V}$ | 2.95 | 3.05 | 3.15 | V |
| | | $2.7\text{ V} \leq V_{DD} < 3.1\text{ V}$ | $V_{DD} - 0.05$ | | | |
| T_{TSD} | Thermal shutdown threshold | See ⁽³⁾ | | 150 | | °C |
| T_{TSD_hyst} | Thermal shutdown hysteresis | | | 20 | | °C |

(1) All voltages are with respect to the potential at the GND pins.

(2) Minimum (MIN) and Maximum (MAX) limits are verified by design, test, or statistical analysis. Typical numbers are for information only.

(3) Verified by design and not tested in production.

7.6 Electrical Characteristics — Boost Converter

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|--|---|------------------------------------|--------------------------|------------|------|---|
| R _{DS_ON} | Switch ON resistance | I _{SW} = 0.5A | | 0.19 | | Ω | |
| V _{BOOST_MIN} | Boost minimum output voltage | VBOOST_RANGE = 0 VBOOST_RANGE = 1 | | 7 16 | | V | |
| V _{BOOST_MAX} | Boost maximum output voltage | VBOOST_MAX = 100, VBOOST_RANGE = 0 | 19 | 21 | 22 | V | |
| | | VBOOST_MAX = 101, VBOOST_RANGE = 0 | 24.0 | 25 | 27 | | |
| | | VBOOST_MAX = 110, VBOOST_RANGE = 0 | 28.0 | 30 | 32 | | |
| | | VBOOST_MAX = 111, VBOOST_RANGE = 0 | 32 | 34 | 37 | | |
| | | VBOOST_MAX = 010, VBOOST_RANGE = 1 | 17.9 | 21 | 23.1 | V | |
| | | VBOOST_MAX = 011, VBOOST_RANGE = 1 | 22.8 | 25 | 27.2 | | |
| VBOOST_MAX = 100, VBOOST_RANGE = 1 | 27.8 | 30 | 31.5 | | | | |
| VBOOST_MAX = 101, VBOOST_RANGE = 1 | 32.7 | 34.5 | 36.6 | | | | |
| VBOOST_MAX = 110, VBOOST_RANGE = 1 | 37.2 | 39 | 40.8 | | | | |
| VBOOST_MAX = 111, VBOOST_RANGE = 1 | 41.8 | 43 | 44.2 | | | | |
| I _{LOAD_MAX} | Maximum continuous output load current | V _{IN} = 3 V, V _{OUT} = 18 V | | 220 | | mA | |
| | | V _{IN} = 3 V, V _{OUT} = 24 V | | 160 | | | |
| | | V _{IN} = 3 V, V _{OUT} = 30 V | | 120 | | | |
| V _{OUT} /V _{IN} | Conversion ratio ⁽²⁾ | f _{SW} = 625 kHz | | | 15 | | |
| | | f _{SW} = 1250 kHz | | | 12 | | |
| f _{SW} | Switching frequency | BOOST_FREQ = 00 BOOST_FREQ = 01 BOOST_FREQ = 10 | | 312 625 1250 | | kHz | |
| V _{OVP} | Overvoltage protection voltage | VBOOST_RANGE = 1 | | V _{BOOST} + 1.6 | | V | |
| V _{UVLO} | V _{IN} undervoltage lockout threshold | UVLO_EN = 1 | | | | V | |
| | | UVLO_TH = 0, falling UVLO_TH = 1, falling | | 2.5 5.2 | | | |
| V _{UVLO_hyst} | V _{UVLO} hysteresis | V _{UVLO} [rising] V _{UVLO} [falling] | UVLO_TH = 0 UVLO_TH = 1 | 50 100 | | mV | |
| t _{PULSE} | Switch minimum pulse width | No load | | 50 | | ns | |
| t _{STARTUP} | Start-up time | See ⁽³⁾ | | 8 | | ms | |
| I _{SW_LIM} | SW pin current limit ⁽⁴⁾ | IBOOST_LIM_2X = 0 | IBOOST_LIM = 00 | 0.66 | 0.9 | 1.16 | A |
| | | | IBOOST_LIM = 01 | 0.88 | 1.2 | 1.40 | |
| | | | IBOOST_LIM = 10 | 1.12 | 1.5 | 1.73 | |
| | | | IBOOST_LIM = 11 | 1.35 | 1.8 | 2.07 | |
| | | IBOOST_LIM_2X = 1 | IBOOST_LIM = 00 | | 1.6 | | A |
| | | | IBOOST_LIM = 01 IBOOST_LIM = 10 | | 2.1 2.6 | | |
| ΔV _{SW} / t _{off_on} | SW pin slew rate during OFF to ON transition | EN_DRV3 = 0 AND EN_DRV2 = 0 | | 3.7 | | V/ns | |
| | | EN_DRV3 = 0 AND EN_DRV2 = 1 | | 5.3 | | | |
| | | EN_DRV3 = 1 AND EN_DRV2 = 1 | | 7.5 | | | |
| ΔV _{SW} / t _{on_off} | SW pin slew rate during ON to OFF transition | EN_DRV3 = 0 AND EN_DRV2 = 0 | | 1.9 | | V/ns | |
| | | EN_DRV3 = 0 AND EN_DRV2 = 1 | | 4.4 | | | |
| | | EN_DRV3 = 1 AND EN_DRV2 = 1 | | 4.8 | | | |
| Δt _{ON} / t _{SW} | Peak-to-peak switch ON time deviation to SW period ratio (spread spectrum feature) | SSCLK_EN = 1 | | 1% | | | |

(1) Minimum (MIN) and Maximum (MAX) limits are verified by design, test, or statistical analysis. Typical numbers are for information only.

(2) Verified by design and not tested in production.

(3) Start-up time is measured from the moment boost is activated until the V_{BOOST} crosses 90% of its target value.

(4) 1.8 A is the maximum I_{SW_LIM} supported with the DSBGA package. For applications requiring the I_{SW_LIM} to be greater than 1.8 A and up to 2.6 A, WQFN package should be considered.

7.7 Electrical Characteristics — LED Driver

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|---|--|--------------|------|------|---------------|
| $I_{LED_LEAKAGE}$ | Leakage current | Outputs LED1...LED6, $V_{OUT} = 48\text{ V}$ | | 0.1 | 1 | μA |
| I_{LED_MAX} | Maximum sink current LED1...LED6 | | | 50 | | mA |
| I_{LED} | LED current accuracy ⁽²⁾ | Output current set to 23 mA | -3% | 1% | 3% | |
| | | Output current set to 23 mA, $-30^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ | -4% | 1% | 4% | |
| I_{MATCH} | Matching | Output current set to 23 mA | | 0.5% | | |
| PWM_{DUTY} | LED PWM output pulse duty cycle ⁽³⁾ | $100\text{ Hz} < f_{PWM} \leq 200\text{ Hz}$ | 0.02% | | 100% | |
| | | $200\text{ Hz} < f_{PWM} \leq 500\text{ Hz}$ | 0.02% | | 100% | |
| | | $500\text{ Hz} < f_{PWM} \leq 1\text{ kHz}$ | 0.02% | | 100% | |
| | | $1\text{ kHz} < f_{PWM} \leq 2\text{ kHz}$ | 0.04% | | 100% | |
| | | $2\text{ kHz} < f_{PWM} \leq 5\text{ kHz}$ | 0.1% | | 100% | |
| | | $5\text{ kHz} < f_{PWM} \leq 10\text{ kHz}$ | 0.2% | | 100% | |
| | | $10\text{ kHz} < f_{PWM} \leq 20\text{ kHz}$ | 0.4% | | 100% | |
| | | $20\text{ kHz} < f_{PWM} \leq 30\text{ kHz}$ $30\text{ kHz} < f_{PWM} \leq 39\text{ kHz}$ | 0.6% 0.8% | | 100% | |
| f_{LED} | PWM output frequency | $PWM_FREQ = 1111$ | | 38.5 | | kHz |
| V_{SAT} | Saturation voltage ⁽⁴⁾ | Output current set to 23 mA | | 200 | | mV |

- (1) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.
- (2) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUT1 to OUT6), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: $(MAX-AVG)/AVG$ and $(AVG-MIN)/AVG$. The largest number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts. Note that some manufacturers have different definitions in use.
- (3) Verified by design and not tested in production.
- (4) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1 V.

7.8 Electrical Characteristics — PWM Interface⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--|--|-----|-----|--------|---------------|
| f_{PWM} | PWM frequency range ⁽²⁾ | | 75 | | 25 000 | Hz |
| t_{MIN_ON} | Minimum pulse ON time | | | 1 | | μs |
| t_{MIN_OFF} | Minimum pulse OFF time | | | 1 | | |
| $t_{STARTUP}$ | Turnon delay from standby to backlight on | PWM input active, VDDIO pin transitions from 0 V to 1.8 V | | 10 | | ms |
| t_{STBY} | Turnoff delay | PWM input low time for turnoff | | 50 | | ms |
| PWM_{RES} | PWM input resolution | $f_{IN} < 9\text{ kHz}$ | | 10 | | bits |

- (1) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis. Typical numbers are for information only.
- (2) Verified by design and not tested in production.

7.9 Electrical Characteristics — Logic Interface ⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------|---|-----|-------------|-------------|------|
| LOGIC INPUTS (PWM, SDA, SCL) | | | | | | |
| V _{IL} | Input low level | -30°C ≤ T _A ≤ 85°C | | | 0.3 × VDDIO | V |
| V _{IH} | Input high level | -30°C ≤ T _A ≤ 85°C | | 0.7 × VDDIO | | V |
| I _I | Input current | (V _{DDIO} = 0 V or 3.6 V), (V _I = 0 V or 3.6 V), -30°C ≤ T _A ≤ 85°C | -1 | | 1 | μA |
| LOGIC OUTPUTS (SDA) | | | | | | |
| V _{OL} | Output low level | I _{OUT} = 3 mA (pull-up current) | | 0.3 | | V |
| | | I _{OUT} = 3 mA (pull-up current), -30°C ≤ T _A ≤ 85°C | | 0.3 | 0.4 | |
| I _L | Output leakage current | V _{OUT} = 5 V, -30°C ≤ T _A ≤ 85°C | -1 | | 1 | μA |

(1) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis. Typical numbers are for information only.

7.10 I²C Serial Bus Timing Parameters (SDA, SCL)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|------------------------|-----|------|
| f _{SCL} | Clock frequency | | 400 | kHz |
| 1 | Hold time (repeated) START condition | 0.6 | | μs |
| 2 | Clock low time | 1.3 | | μs |
| 3 | Clock high time | 600 | | ns |
| 4 | Setup time for a repeated START condition | 600 | | ns |
| 5 | Data hold time | 50 | | ns |
| 6 | Data set-up time | 100 | | ns |
| 7 | Rise time of SDA and SCL | 20 + 0.1C _b | 300 | ns |
| 8 | Fall time of SDA and SCL | 15 + 0.1C _b | 300 | ns |
| 9 | Setup time for STOP condition | 600 | | ns |
| 10 | Bus-free time between a STOP and a START condition | 1.3 | | μs |
| C _b | Capacitive load parameter for each bus line load of 1 pF corresponds to 1 ns. | 10 | 200 | ns |

(1) Verified by design and not tested in production.

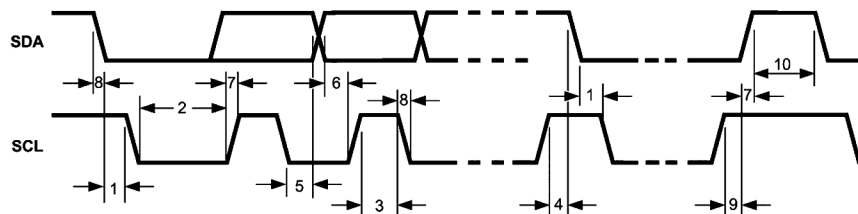
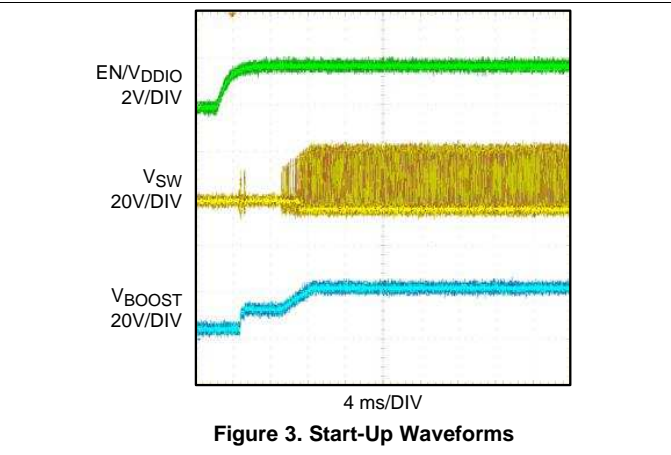
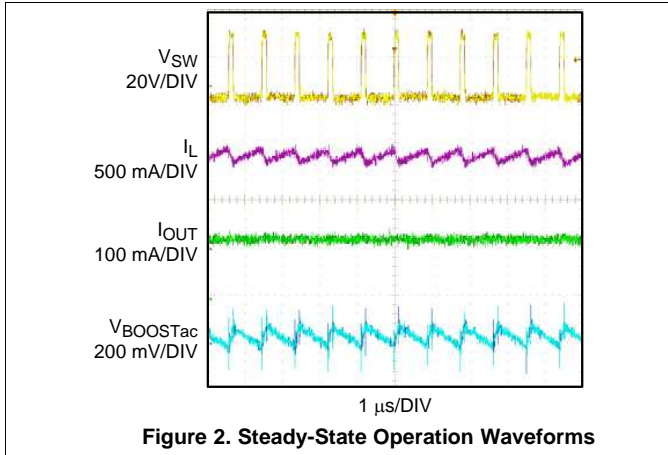


Figure 1. I²C-Compatible Timing

7.11 Typical Characteristics

Unless otherwise specified: $V_{IN} = 3.8\text{ V}$, $C_{VLDO} = 10\ \mu\text{F}$, $L1 = 4.7\ \mu\text{H}$, $C_{IN} = 2.2\ \mu\text{F}$, $C_{OUT} = 4.7\ \mu\text{F}$, $f_{SW} = 1.25\ \text{MHz}$.



8 Detailed Description

8.1 Overview

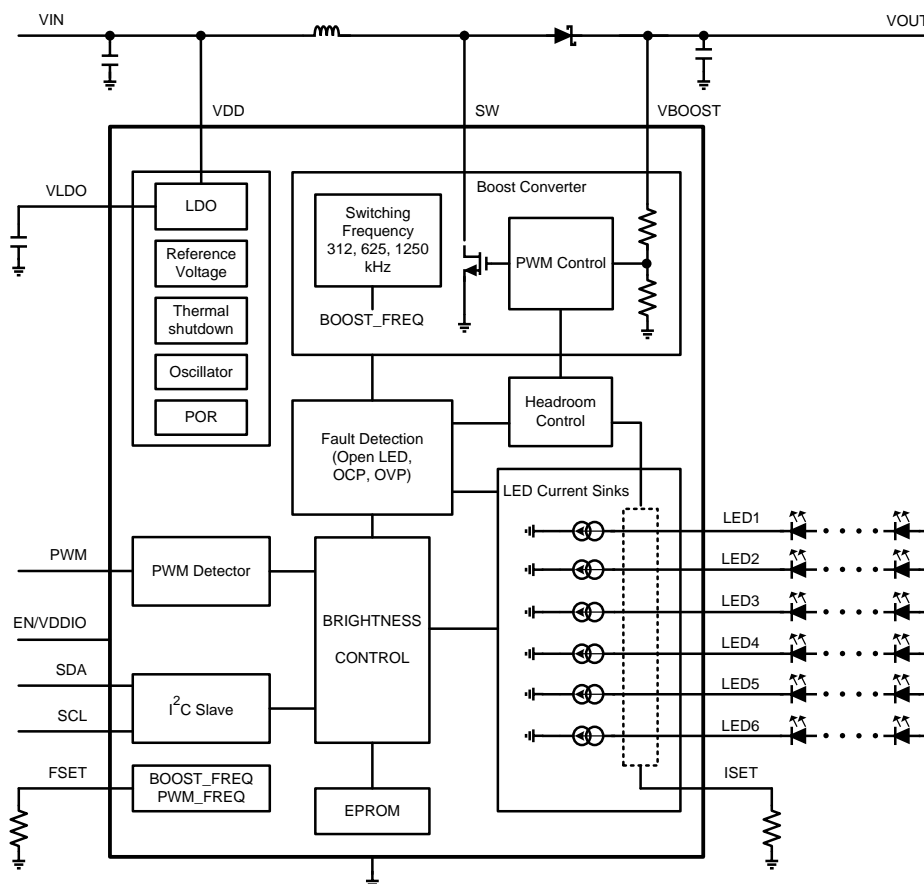
LP8556 is a white LED driver featuring an asynchronous boost converter and six high-precision current sinks that can be controlled by a PWM signal or an I²C master.

The boost converter uses adaptive output voltage control for setting the optimal LED driver voltages as high as 43 V. This feature minimizes the power consumption by adjusting the voltage to the lowest sufficient level under all conditions. The converter can operate at three switching frequencies: 312, 625, and 1250 kHz pre-configured via EPROM or can be set through an external resistor. Programmable slew rate control and spread spectrum scheme minimize switching noise and improve EMI performance.

LED current sinks can be set with the PWM dimming resolution of up to 15 bits. Proprietary adaptive dimming mode allows higher system power saving. In addition, phase shifted LED PWM dimming allows reduced audible noise and smaller boost output capacitors.

The LP8556 device has a full set of safety features that ensure robust operation of the device and external components. The set consists of input undervoltage lockout, thermal shutdown, overcurrent protection, up to six levels of overvoltage protection, LED open, and short detection.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Boost Converter

8.3.1.1 Boost Converter Operation

The LP8556 boost DC-DC converter generates a 7-V to approximately 43-V of boost output voltage from a 2.7-V to 36-V boost input voltage. The boost output voltage minimum, maximum value and range can be set digitally by pre-configuring EPROM memory (VBOOST_RANGE, VBOOST, and VBOOST_MAX fields).

The converter is a magnetic switching PWM mode DC-DC boost converter with a current limit. It uses CPM (current programmed mode) control, where the inductor current is measured and controlled with the feedback. During start-up, the soft-start function reduces the peak inductor current. The LP8556 has an internal 20-MHz oscillator which is used for clocking the boost. Figure 4 shows the boost block diagram.

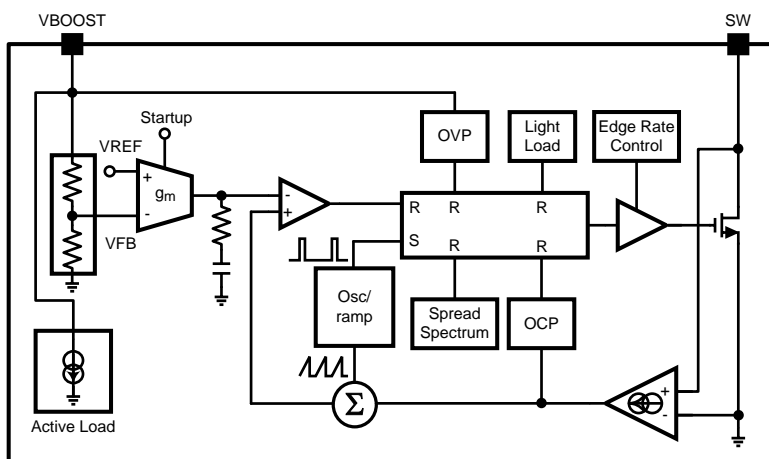


Figure 4. LP8556 Boost Converter Block Diagram

8.3.1.2 Setting Boost Switching Frequency

The LP8556 boost converter switching frequency can be set either by an external resistor (BOOST_FSET_EN = 1 selection), R_{FSET} , or by pre-configuring EPROM memory with the choice of boost frequency (BOOST_FREQ field). Table 1 summarizes setting of the switching frequency. Note that the R_{FSET} is shared for setting the PWM dimming frequency in addition to setting the boost switching frequency. Setting the boost switching frequency and PWM dimming frequency using an external resistor is separately shown in Table 5.

Table 1. Configuring Boost Switching Frequency via EPROM

| R_{FSET} [Ω] | BOOST_FSET_EN | BOOST_FREQ[1:0] | f_{sw} [kHz] |
|-------------------------|---------------|-----------------|--------------------|
| don't care | 0 | 00 | 312 |
| don't care | 0 | 01 | 625 |
| don't care | 0 | 10 | 1250 |
| don't care | 0 | 11 | undefined |
| See ⁽¹⁾ | 1 | don't care | See ⁽¹⁾ |

(1) See Table 5.

8.3.1.3 Output Voltage Control

The LP8556 device supports two modes of controlling the boost output voltage: Adaptive Boost Voltage Control (see [Adaptive Control](#)) and Manual Boost Output Control (see [Manual Control](#)).

8.3.1.3.1 Adaptive Control

LP8556 supports a mode of output voltage control called Adaptive Boost Control mode. In this mode, the voltage at the LED pins is periodically monitored by the control loop and adaptively adjusted to the optimum value based on the comparator thresholds set using LED_DRIVER_HEADROOM, LED_COMP_HYST, BOOST_STEP_UP, BOOST_STEP_DOWN fields in the EPROM. Settings under LED_DRIVER_HEADROOM along with LED_COMP_HYST fields determine optimum boost voltage for a given condition. Boost voltage is raised if the voltage measured at any of the LED strings falls below the threshold setting determined with LED_DRIVER_HEADROOM field. Likewise, boost voltage is lowered if the voltage measured at any of the LED strings is above the combined setting determined under LED_DRIVER_HEADROOM and LED_COMP_HYST fields. LED_COMP_HYST field serves to fine tune the headroom voltage for a given peak LED current. The boost voltage up/down step size can be controlled with the BOOST_STEP_UP and BOOST_STEP_DN fields.

The initial boost voltage is configured with the VBOOST field. This field also sets the minimum boost voltage. The VBOOST_MAX field sets the maximum boost voltage. When an LED pin is open, the monitored voltage never has enough headroom, and the adaptive mode control loop keeps raising the boost voltage. The VBOOST_MAX field allows the boost voltage to be limited to stay under the voltage rating of the external components.

NOTE

Only LED strings that are enabled are monitored and PS_MODE field determines which LED strings are enabled.

The adaptive mode is selected using ADAPTIVE bit set to 1 (CFG_A EPROM Register) and is the recommended mode of boost control.

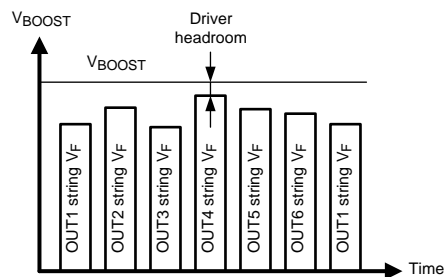


Figure 5. Boost Adaptive Control Principle

8.3.1.3.2 Manual Control

User can control the boost output voltage with the VBOOST EPROM field when adaptive mode is not used. [Equation 1](#) shows the relationship between the boost output voltage and the VBOOST field.

$$V_{\text{BOOST}} = V_{\text{BOOST_MIN}} + 0.42 \times V_{\text{BOOST}}[\text{dec}] \quad (1)$$

The expression is only valid when the calculated values are between the minimum boost output voltage and the maximum boost output voltage. The minimum boost output voltage is set with the VBOOST_RANGE field. The maximum boost output voltage is set with the VBOOST_MAX EPROM field.

8.3.1.4 EMI Reduction

The LP8556 device features two EMI reduction schemes.

The first scheme, Programmable Slew Rate Control, uses a combination of three drivers for boost switch. Enabling all three drivers allows boost switch on/off transition times to be the shortest. On the other hand, enabling just one driver allows boost switch on/off transition times to be the longest. The longer the transition times, the lower the switching noise on the SW pin. Note that the shortest transition times bring the best efficiency as the switching losses are the lowest.

EN_DRV2 and EN_DRV3 bits in the EPROM determine the boost switch driver configuration. Refer to the SW pin slew rate parameter listed under *Electrical Characteristics — Boost Converter* for the slew rate options.

The second EMI reduction scheme is the spread spectrum. This scheme deliberately spreads the frequency content of the boost switching waveform, which inherently has a narrow bandwidth, makes the bandwidth of the switching waveform wider, and ultimately reduces its EMI spectral density.

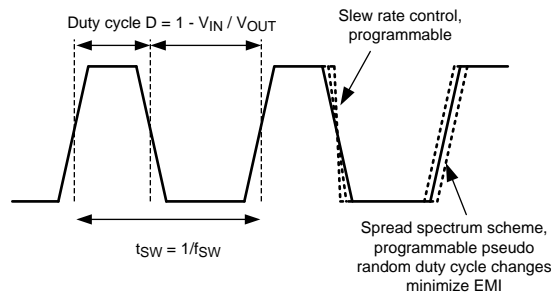


Figure 6. Principles of EMI Reduction Scheme

8.3.2 Brightness Control

LP8556 enables various methods of brightness control. The brightness can be controlled using an external PWM signal or the Brightness register accessible by users via an I²C interface or both. How these two input sources are selected and combined is set by the BRT_MODE EPROM bits and described in *BRT_MODE = 00* through *BRT_MODE = 11*, Figure 7, and Table 2. The LP8556 can also be preconfigured via EPROM memory to allow direct and unaltered brightness control by an external PWM signal. This mode of operation is obtained by setting PWM_DIRECT EPROM bit to 1 (CFG5[7] = 1).

8.3.2.1 BRT_MODE = 00

With BRT_MODE = 00, the LED output is controlled by the PWM input duty cycle. The PWM detector block measures the duty cycle at the PWM pin and uses this 16-bit value to generate an internal to the device PWM data. Before the output is generated, the PWM data goes through the PWM curve-shaper block. Then, the data goes into the adaptive dimming function which determines the range of the PWM and Current control as described in *Output Dimming Schemes*. The outcome of the adaptive dimming function is 12-bit current and/or up to 6 PWM output signals. The current is then passed through the non-linear compensation block while the output PWM signals are channeled through the dither block.

8.3.2.2 BRT_MODE = 01

With BRT_MODE = 01, the PWM output is controlled by the PWM input duty cycle and the Brightness register. The PWM detector block measures the duty cycle at the PWM pin and uses this 16-bit value to generate the PWM data. Before the output is generated, the PWM data is first multiplied with BRT[7:0] register, then it goes through the PWM Curve Shaper block. Then, the data goes into the Adaptive Dimming function which determines the range of the PWM and Current control as described in *Output Dimming Schemes*. The outcome of the Adaptive Dimming function is 12-bit current and/or up to 6 PWM output signals. The current is then passed through the non-linear compensation block while the output PWM signals are channeled through the Dither block.

8.3.2.3 BRT_MODE = 10

With BRT_MODE = 10, the PWM output is controlled only by the Brightness register. From BRT[7:0] register, the data goes through the PWM Curve Shaper block. Then, the data goes into the Adaptive Dimming function which determines the range of the PWM and Current control as described in [Output Dimming Schemes](#). The outcome of the Adaptive Dimming function is 12-bit Current and / or up to 6 PWM output signals. The current is then passed through the non-linear compensation block while the output PWM signals are channeled through the Dither block.

8.3.2.4 BRT_MODE = 11

With BRT_MODE = 11, the PWM control signal path is similar to the path when BRT_MODE = 01 except that the PWM input signal is multiplied with BRT[7:0] data after the Curve-Shaper block.

Table 2. Brightness Control Methods Truth Table

| PWM_DIRECT | BRT_MODE [1:0] | BRIGHTNESS CONTROL SOURCE | OUTPUT ILED FORM |
|------------|----------------|--|--|
| 0 | 00 | External PWM signal | Adaptive. See Output Dimming Schemes |
| 0 | 01 | External PWM signal and Brightness Register (multiplied before Curve Shaper) | |
| 0 | 10 | Brightness Register | |
| 0 | 11 | External PWM signal and Brightness Register (multiplied after Curve Shaper) | |
| 1 | don't care | External PWM signal | Same as the external PWM input |

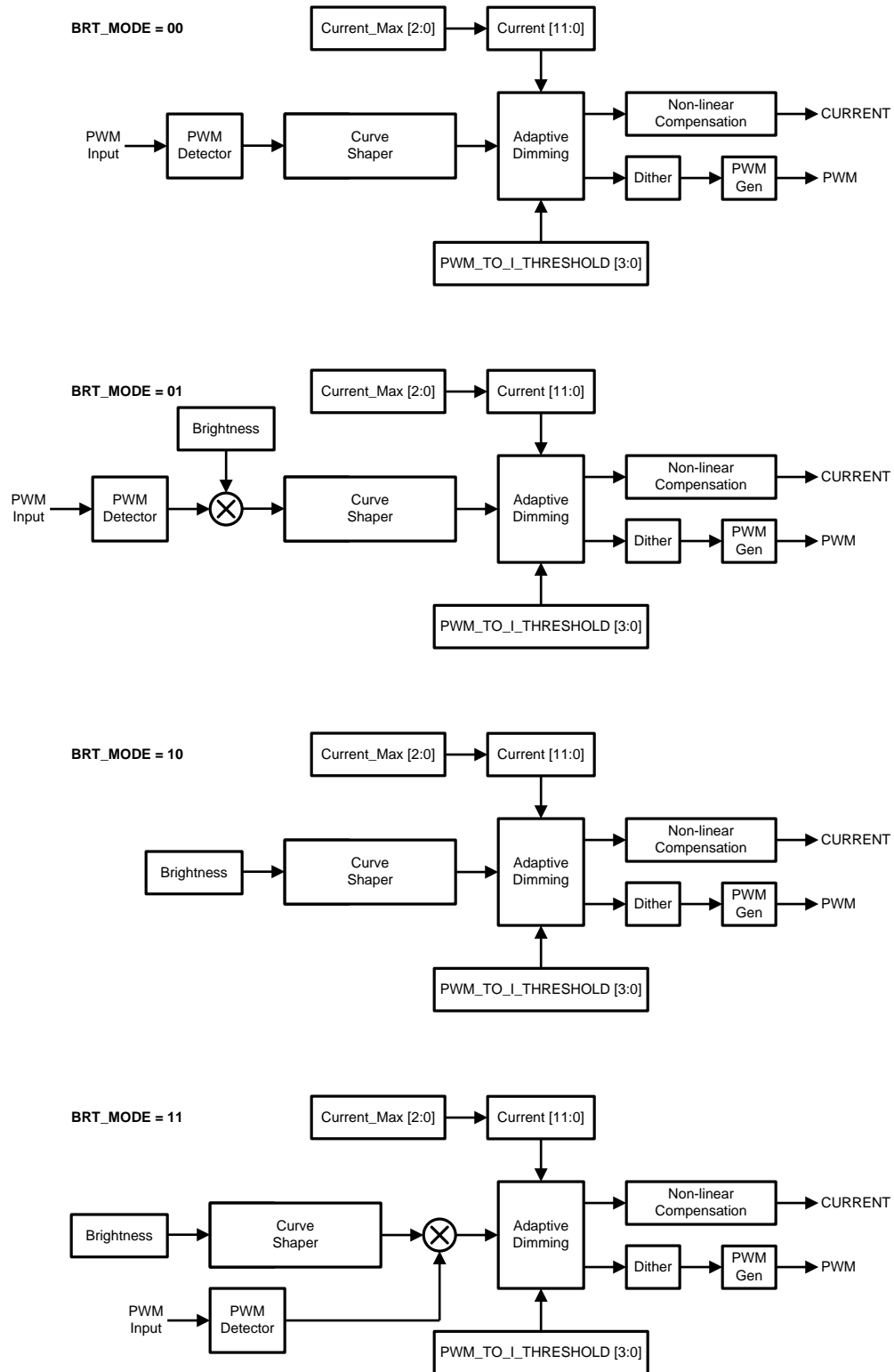


Figure 7. Brightness Control Signal Path Block Diagrams

8.3.2.5 Output Dimming Schemes

The LP8556 device supports three types of output dimming control methods: PWM Control, Pure Current Control and Adaptive Dimming (Hybrid PWM and Current) Control.

8.3.2.5.1 PWM Control

PWM control is the traditional way of controlling the brightness using PWM of the outputs with the same LED current across the entire brightness range. Brightness control is achieved by varying the duty cycle proportional to the input PWM. PWM frequency is set either using an external set resistor (R_{FSET}) or using the PWM_FREQ EPROM field. The maximum LED current is set by using an external set Resistor (R_{ISET}), CURRENT, and CURRENT_MAX EPROM bits. PWM frequency can also be set by simply using the CURRENT and CURRENT_MAX EPROM bits.

NOTE

The output PWM signal is de-coupled and generated independent of the input PWM signal eliminating display flicker issues and allowing better noise immunity.

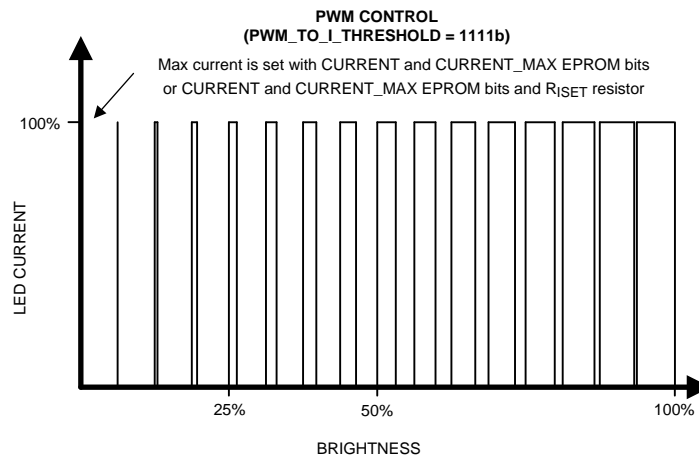


Figure 8. PWM Only Output Dimming Scheme

8.3.2.5.2 Pure Current Control

In Pure Current Control mode, brightness control is achieved by changing the LED current proportionately from maximum value to a minimum value across the entire brightness range. Like in PWM Control mode, the maximum LED current is set by using an external set Resistor (R_{ISET}), CURRENT, and CURRENT_MAX EPROM bits. The maximum LED current can also be set by just using the CURRENT and CURRENT_MAX EPROM bits. Current resolution in this mode is 12 bits.

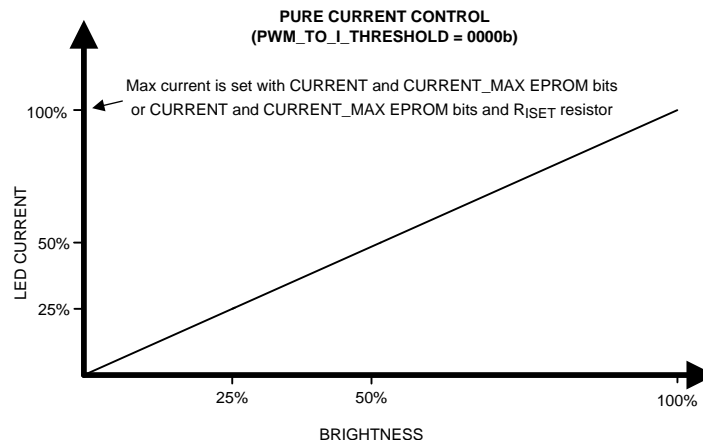


Figure 9. Pure Current or Analog Output Dimming Scheme

8.3.2.5.3 Adaptive Control

Adaptive dimming control combines PWM Control and Pure Current Control dimming methods. With the adaptive dimming, it is possible to achieve better optical efficiency from the LEDs compared to pure PWM control while still achieving smooth and accurate control at low brightness levels. Current resolution in this mode is 12 bits. Switch point from Current to PWM control can be set with the PWM_TO_I_THRESHOLD EPROM field from 0% to 100% of the brightness range to get good compromise between good matching of the LEDs brightness/white point at low brightness and good optical efficiency.

PWM frequency is set either using an external set Resistor (R_{FSET}) or using the PWM_FREQ EPROM bits. The maximum LED current is set either by using an external set Resistor (R_{ISET}), CURRENT, and CURRENT_MAX EPROM bits. Or the maximum LED current may be set using the CURRENT and CURRENT_MAX EPROM bits.

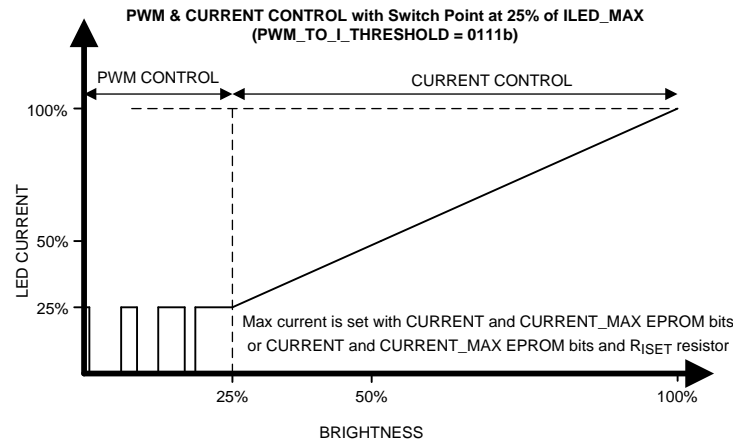


Figure 10. Adaptive Output Dimming Scheme

8.3.2.6 Setting Full-Scale LED Current

The maximum or full-scale LED current is set either using an external set Resistor (R_{ISET}), CURRENT, and CURRENT_MAX EPROM bits or just by using the CURRENT and CURRENT_MAX EPROM bits. Table 3 summarizes setting of the full-scale LED current.

Table 3. Setting Full-Scale LED Current

| R_{ISET} [Ω] | ISET_EN | CURRENT_MAX | CURRENT[11:0] | FULL-SCALE ILED [mA] |
|-------------------------|---------|-------------|---------------|----------------------|
| don't care | 0 | 000 | FFFh | 5 |
| don't care | 0 | 001 | FFFh | 10 |
| don't care | 0 | 010 | FFFh | 15 |
| don't care | 0 | 011 | FFFh | 20 |
| don't care | 0 | 100 | FFFh | 23 |
| don't care | 0 | 101 | FFFh | 25 |
| don't care | 0 | 110 | FFFh | 30 |
| don't care | 0 | 111 | FFFh | 50 |
| don't care | 0 | 000 - 111 | 001h - FFFh | See ⁽¹⁾ |
| 24k | 1 | 000 | FFFh | 5 |
| 24k | 1 | 001 | FFFh | 10 |
| 24k | 1 | 010 | FFFh | 15 |
| 24k | 1 | 011 | FFFh | 20 |
| 24k | 1 | 100 | FFFh | 23 |
| 24k | 1 | 101 | FFFh | 25 |
| 24k | 1 | 110 | FFFh | 30 |
| 24k | 1 | 111 | FFFh | 50 |
| 12k - 100k | 1 | 000 - 111 | 001h - FFFh | See ⁽¹⁾ |

(1) See CFG0.

8.3.2.7 Setting PWM Dimming Frequency

LP8556 PWM dimming frequency can be set by an external resistor, R_{FSET} , or by pre-configuring EPROM Memory (CFG5 register, PWM_FREQ[3:0] bits). [Table 4](#) summarizes setting of the PWM dimming frequency. Note that .

NOTE

The R_{FSET} is shared for setting the boost switching frequency, too. Setting the boost switching frequency and PWM dimming frequency using an external resistor is shown in [Table 5](#).

Table 4. Configuring PWM Dimming Frequency via EPROM

| R_{FSET} [k Ω] | PWM_FSET_EN | PWM_FREQ[3:0] | f_{PWM} [Hz] (Resolution) |
|--------------------------|---------------|---------------|-----------------------------|
| don't care | 0 | 0000 | 4808 (11-bit) |
| | | 0001 | 6010 (10-bit) |
| | | 0010 | 7212 (10-bit) |
| | | 0011 | 8414 (10-bit) |
| | | 0100 | 9616 (10-bit) |
| | | 0101 | 12020 (9-bit) |
| | | 0110 | 13222 (9-bit) |
| | | 0111 | 14424 (9-bit) |
| | | 1000 | 15626 (9-bit) |
| | | 1001 | 16828 (9-bit) |
| | | 1010 | 18030 (9-bit) |
| | | 1011 | 19232 ((9-bit) |
| | | 1100 | 24040 (8-bit) |
| | | 1101 | 28848 (8-bit) |
| 1110 | 33656 (8-bit) | | |
| 1111 | 38464 (8-bit) | | |
| See ⁽¹⁾ | 1 | don't care | See ⁽¹⁾ |

(1) See [Table 5](#).

Table 5. Setting Switching and PWM Dimming Frequency With an External Resistor

| R_{FSET} [Ω] (Tolerance) | f_{SW} [kHz] | f_{PWM} [Hz] (Resolution) |
|--------------------------------------|----------------|-----------------------------|
| Floating or FSET pin pulled HIGH | 1250 | 9616 (10-bit) |
| 470k - 1M ($\pm 5\%$) | 312 | 2402 (12-bit) |
| 300k, 330k ($\pm 5\%$) | 312 | 4808 (11-bit) |
| 200k ($\pm 5\%$) | 312 | 6010 (10-bit) |
| 147k, 150k, 154k, 158k ($\pm 1\%$) | 312 | 9616 (10-bit) |
| 121k ($\pm 1\%$) | 312 | 12020 (9-bit) |
| 100k ($\pm 1\%$) | 312 | 14424 (9-bit) |
| 86.6k ($\pm 1\%$) | 312 | 16828 (9-bit) |
| 75.0k ($\pm 1\%$) | 312 | 19232 (9-bit) |
| 63.4k ($\pm 1\%$) | 625 | 2402 (12-bit) |
| 52.3k, 53.6k ($\pm 1\%$) | 625 | 4808 (11-bit) |
| 44.2k, 45.3k ($\pm 1\%$) | 625 | 6010 (10-bit) |
| 39.2k ($\pm 1\%$) | 625 | 9616 (10-bit) |
| 34.0k ($\pm 1\%$) | 625 | 12020 (9-bit) |
| 30.1k ($\pm 1\%$) | 625 | 14424 (9-bit) |
| 26.1k ($\pm 1\%$) | 625 | 16828 (9-bit) |
| 23.2k ($\pm 1\%$) | 625 | 19232 (9-bit) |
| 20.5k ($\pm 1\%$) | 1250 | 2402 (12-bit) |
| 18.7k ($\pm 1\%$) | 1250 | 4808 (11-bit) |
| 16.5k ($\pm 1\%$) | 1250 | 6010 (10-bit) |
| 14.7k ($\pm 1\%$) | 1250 | 9616 (10-bit) |
| 13.0k ($\pm 1\%$) | 1250 | 12020 (9-bit) |
| 11.8k ($\pm 1\%$) | 1250 | 14424 (9-bit) |
| 10.7k ($\pm 1\%$) | 1250 | 16828 (9-bit) |
| 9.76k ($\pm 1\%$) | 1250 | 19232 (9-bit) |
| FSET pin shorted to GND | 1250 | Same as PWM input |

8.3.2.8 Phase Shift PWM Scheme

Phase shift PWM scheme allows delaying the time when each LED driver is active. When the LED drivers are not activated simultaneously, the peak load current from the boost output is greatly decreased. This reduces the ripple seen on the boost output and allows smaller output capacitors. Reduced ripple also reduces the output ceramic capacitor audible ringing. PSPWM scheme also increases the load frequency seen on the boost output six times and therefore transfers the possible audible noise to the frequencies outside of the audible range.

Description of the PSPWM mode is seen in [Table 6](#). PSPWM mode is set with <PS_MODE[2:0]> bits.

Table 6. LED String Configuration

| PS_MODE[2:0] | WAVEFORMS | CONNECTION |
|--|---|------------|
| 000 | <p>Phase Delay 60 degrees Cycle Time $1/(f_{PWM})$</p> | |
| 6 LED strings with 60 degree phase shift. One driver for each LED string. | | |
| 001 | <p>Phase Delay 72 degrees Cycle Time $1/(f_{PWM})$</p> | |
| 5 LED strings with 72 degree phase shift. One driver for each LED string. (Driver #6 not used). | | |

Table 6. LED String Configuration (continued)

| PS_MODE[2:0] | WAVEFORMS | CONNECTION |
|--------------|--|---|
| 010 | <p>Phase Delay 90 degrees Cycle Time $1/(f_{PWM})$</p> | <p>VBOOST</p> <p>4 LED strings with 90 degree phase shift. One driver for each LED string. (Drivers #5 and #6 not used).</p> |
| 011 | <p>Phase Delay 120 degrees Cycle Time $1/(f_{PWM})$</p> | <p>VBOOST</p> <p>3 LED strings with 120 degree phase shift. One driver for each LED string. (Drivers #4, #5 and #6 not used).</p> |
| 100 | <p>Phase Delay 180 degrees Cycle Time $1/(f_{PWM})$</p> | <p>VBOOST</p> <p>2 LED strings with 180 degree phase shift. One driver for each LED string. (Drivers #3, #4, #5 and #6 not used).</p> |

Table 6. LED String Configuration (continued)

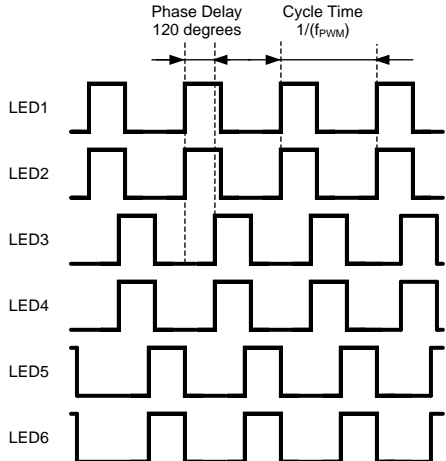
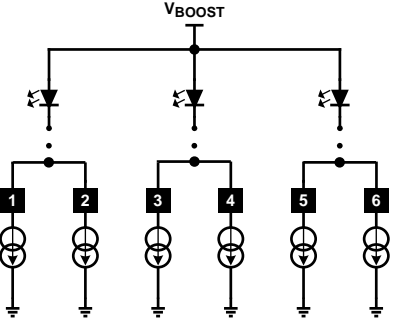
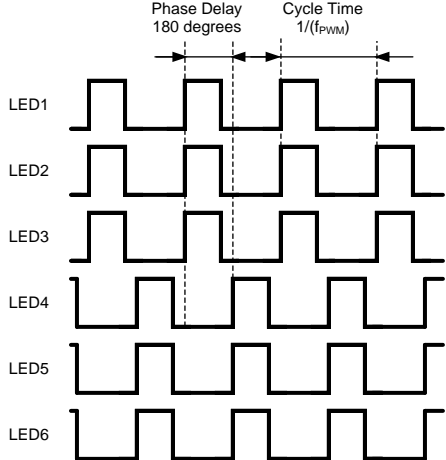
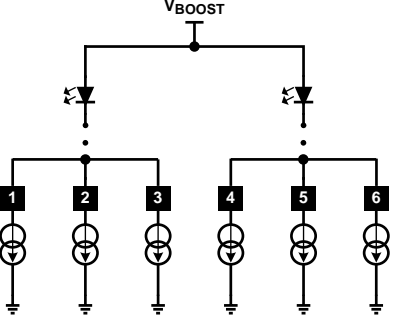
| PS_MODE[2:0] | WAVEFORMS | CONNECTION |
|--|--|--|
| 101 |  |  |
| <p>3 LED strings with 120 degree phase shift. Two drivers for each LED string. (Drivers 1&2, 3&4 and 5&6 are tied and with the same phase).</p> | | |
| 110 |  |  |
| <p>2 LED strings with 180 degree phase shift. Three drivers for each LED string. (Drivers 1&2&3 and 4&5&6 are tied and with the same phase).</p> | | |

Table 6. LED String Configuration (continued)

| PS_MODE[2:0] | WAVEFORMS | CONNECTION |
|--|-----------|------------|
| 111 | | |
| <p>1 LED string driven by all six drivers. (All drivers are tied and with the same phase).</p> | | |

8.3.2.9 Slope and Advanced Slope

Transition time between two brightness values can be programmed with EPROM bits <PWM_SLOPE[2:0]> from 0 to 500 ms. Same slope time is used for sloping up and down. With advanced slope the brightness changes can be made more pleasing to a human eye.

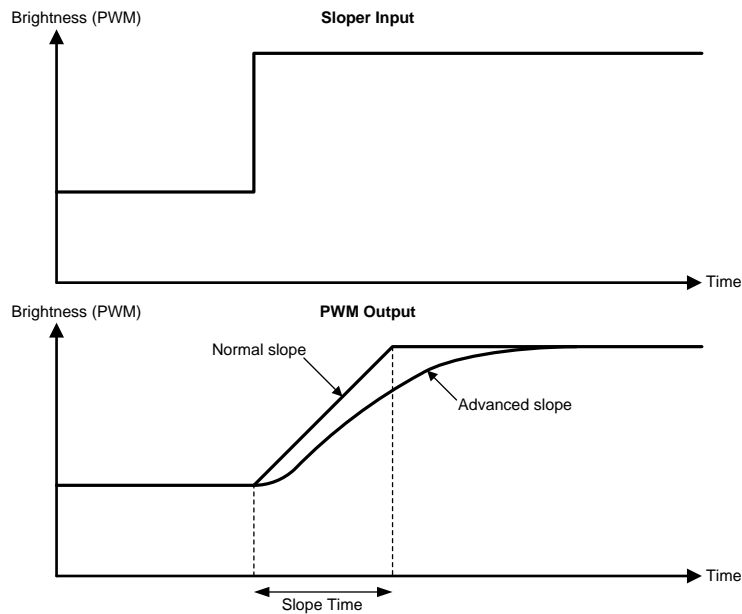


Figure 11. Sloper Operation

8.3.2.10 Dithering

Special dithering scheme can be used during brightness changes and in steady state condition. It allows increased resolution and smaller average steps size during brightness changes. Dithering can be programmed with EPROM bits <DITHER[1:0]> from 0 to 3 bits. <STEADY_DITHER> EPROM bit sets whether the dithering is used also in steady state or only during slopes. Example below is for 1-bit dithering. For 3-bit dithering, every 8th pulse is made 1 LSB longer to increase the average value by 1/8th.

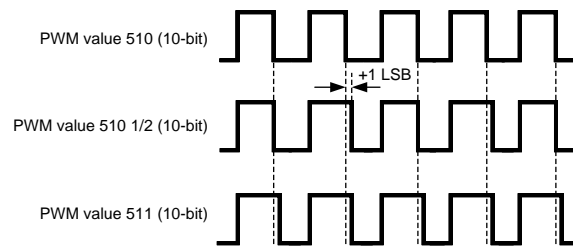


Figure 12. Example of the Dithering, 1-bit Dither, 10-bit Resolution

8.3.3 Fault Detection

LP8556 has fault detection for LED open and short conditions, UVLO, overcurrent, and thermal shutdown. The cause for the fault can be read from status register. Reading the fault register also resets the fault.

8.3.3.1 LED Fault Detection

With LED fault detection, the voltages across the LED drivers are constantly monitored. Shorted or open LED strings are detected.

8.3.3.1.1 Open Detect

The logic uses the LOW comparators and the requested boost voltage to detect the OPEN condition. If the logic is asking the boost for the maximum allowed voltage and a LOW comparator is asserted, then the OPEN bit is set in the STATUS register (ADDR = 02h). In normal operation, the adaptive headroom control loop raises the requested boost voltage when the LOW comparator is asserted. If it has raised it as high as it can and an LED string still needs more voltage, then it is assumed to be disconnected from the boost voltage (open or grounded). The actual boost voltage is not part of the OPEN condition decision; only the requested boost voltage and the LOW comparators.

8.3.3.1.2 Short Detect

The logic uses all three comparators (HIGH, MID and LOW) to detect the SHORT condition. When the MID and LOW comparators are de-asserted, the headroom control loop considers that string to be optimized - enough headroom, but not excessive. If at least one LED string is optimized and at least one other LED string has its HIGH comparator asserted, then the SHORT condition is detected. It is important to note that the SHORT condition requires at least two strings for detection: one in the optimized headroom zone (LOW/MID/HIGH comparators all de-asserted) and one in the excessive headroom zone (HIGH comparator asserted).

Fault is cleared by reading the fault register.

8.3.3.2 Undervoltage Detection

The LP8556 device has detection for too-low V_{IN} voltage. Threshold level for the voltage is set with EPROM register bits as shown in [Table 7](#).

Table 7. UVLO Truth Table

| UVLO_EN | UVLO_TH | THRESHOLD (V) |
|---------|------------|---------------|
| 0 | don't care | OFF |
| 1 | 0 | 2.5 |
| 1 | 1 | 5.2 |

When undervoltage is detected the LED outputs and the boost shuts down, and the corresponding fault bit is set in the fault register. The LEDs and the boost start again when the voltage has increased above the threshold level. Hysteresis is implemented to threshold level to avoid continuous triggering of fault when threshold is reached.

Fault is cleared by setting the EN / VDDIO pin low or by reading the fault register.

8.3.3.3 Overcurrent Protection

LP8556 has detection for too-high loading on the boost converter. When overcurrent fault is detected, the boost shuts down and the corresponding fault bit is set in the fault register. The boost starts again when the current has dropped below the OCP threshold.

Fault is cleared by reading the fault register.

8.3.3.4 Thermal Shutdown

If the LP8556 reaches thermal shutdown temperature (150°C) the LED outputs and boost shut down to protect it from damage. The device re-activates when temperature drops below 130°C.

Fault is cleared by reading the fault register.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The device is in shutdown mode when the EN/VDDIO input is low. Current consumption in this mode from VDD pin is $< 1.6 \mu\text{A}$.

8.4.2 Active Mode

In active mode the backlight is enabled either with setting the ON register bit high (BRTMODE = 0 1, 10, 11) or by activating PWM input (BRTMODE=00). The powers supplying the VDD and EN/VDDIO pins must be present. Brightness is controlled with I²C writes to brightness registers or by changing PWM input duty cycle (operation without I²C control). Configuration registers are not accessible in Active mode to prevent damage to the device by accidental writes. Current consumption from VDD pin this mode is typically 2.2 mA when boost is enabled and LEDs are not drawing any current.

8.5 Programming

8.5.1 I²C-Compatible Serial Bus Interface

8.5.1.1 Interface Bus Overview

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the ICs connected to the bus. The two interface lines are the Serial Data Line (SDA) and the Serial Clock Line (SCL). These lines must be connected to a positive supply via a pull-up resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the SCL. The LP8556 can operate as an I²C slave.

8.5.1.2 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock SCL. Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

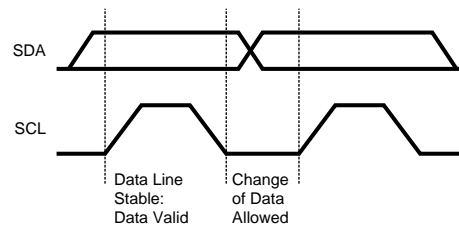


Figure 13. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

Programming (continued)

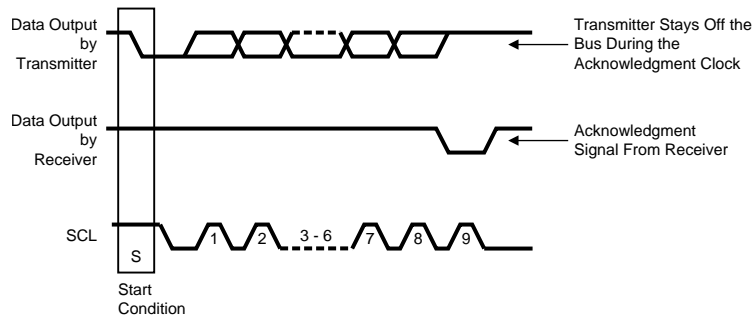


Figure 14. Start and Stop

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

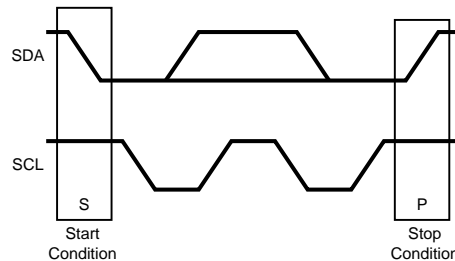


Figure 15. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

8.5.1.3 Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

8.5.1.4 Acknowledge After Every Byte Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

Programming (continued)

8.5.1.5 Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP8556 operates as a slave device with 7-bit address combined with data direction bit. Slave address is 2Ch as 7-bit or 58h for write and 59h for read in 8-bit format.

Before any data is transmitted, the master transmits the slave I.D. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the 8th bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

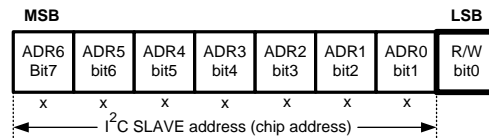


Figure 16. I²C Chip Address (0x2C)

8.5.1.6 Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master sends further data bytes the control register address is incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

8.5.1.7 Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address is incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

Programming (continued)

Table 8. Data Read and Write Cycles

| | ADDRESS MODE |
|------------|--|
| Data Read | <Start Condition> <Slave Address><r/w = 0>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> ... additional reads from subsequent register address possible <Stop Condition> |
| Data Write | <Start Condition> <Slave Address><r/w='0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] ... additional writes to subsequent register address possible <Stop Condition> |

<>Data from master [] Data from slave

8.5.1.8 Register Read and Write Detail

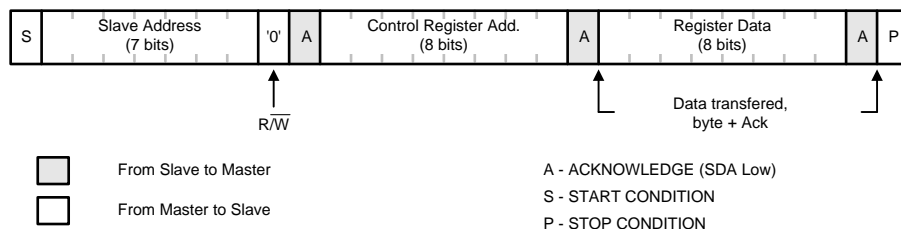


Figure 17. Register Write Format

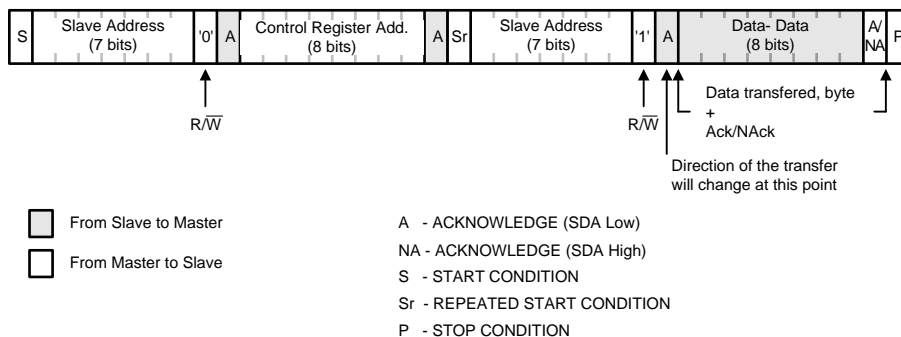


Figure 18. Register Read Format

8.6 Register Maps

Table 9. Register Map

| ADDR | REGISTER | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | RESET |
|------|--------------------|----------|-------|---------|-----------|-----|----------|-----|--------|-----------|
| 00H | Brightness Control | BRT[7:0] | | | | | | | | 0000 0000 |
| 01H | Device Control | FAST | | | | | BRT_MODE | | BL_CTL | 0000 0000 |
| 02H | Status | OPEN | SHORT | VREF_OK | VBOOST_OK | OVP | OC | TSD | UVLO | 0000 0000 |
| 04H | Direct Control | LED | | | | | | | | 0000 0000 |
| 16H | LED Enable | LED_EN | | | | | | | | 0011 1111 |

Table 10. EPROM Memory Map

| ADDR | REGISTER | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------|--------------------|-------------|--------------|----------|-----------------|-----------------|----------------------|-------------|
| 98H | CFG98 | IBOOST_LIM_2X | RESERVED | | | RESERVED | | | |
| 9EH | CFG9E | RESERVED | | VBOOST_RANGE | RESERVED | HEADROOM_OFFSET | | | |
| A0H | CFG0 | CURRENT_LSB | | | | | | | |
| A1H | CFG1 | PDET_STDBY | CURRENT_MAX | | | CURRENT_MSB | | | |
| A2H | CFG2 | RESERVED | | UVLO_EN | UVLO_TH | BL_ON | ISET_EN | BOOST_FSET_EN | PWM_FSET_EN |
| A3H | CFG3 | RESERVED | SLOPE | | | FILTER | | PWM_INPUT_HYSTERESIS | |
| A4H | CFG4 | PWM_TO_I_THRESHOLD | | | | RESERVED | STEADY_DITHER | DITHER | |
| A5H | CFG5 | PWM_DIRECT | PS_MODE | | | PWM_FREQ | | | |
| A6H | CFG6 | BOOST_FREQ | | VBOOST | | | | | |
| A7H | CFG7 | RESERVED | | EN_DRV3 | EN_DRV2 | RESERVED | | IBOOST_LIM | |
| A8H | CFG8 | RESERVED | | RESERVED | | RESERVED | | RESERVED | |
| A9H | CFG9 | VBOOST_MAX | | | JUMP_EN | JUMP_THRESHOLD | | JUMP_VOLTAGE | |
| AAH | CFG9A | SSCLK_EN | RESERVED | RESERVED | | ADAPTIVE | DRIVER_HEADROOM | | |
| ABH | CFG9B | RESERVED | | | | | | | |
| ACH | CFG9C | RESERVED | | | | RESERVED | | | |
| ADH | CFG9D | RESERVED | | | | | | | |
| AEH | CFG9E | STEP_UP | | STEP_DN | | LED_FAULT_TH | | LED_COMP_HYST | |
| AFH | CFG9F | REVISION | | | | | | | |

8.6.1 Register Bit Explanations

8.6.1.1 Brightness Control

Address 00h

Reset value 0000 0000b

| BRIGHTNESS CONTROL REGISTER | | | | | | | |
|-----------------------------|-----|--------|-------------------------------------|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BRT[7:0] | | | | | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| BRT | 7:0 | R/W | Backlight PWM 8-bit linear control. | | | | |

8.6.1.2 Device Control

Address 01h

Reset value 0000 0000b

| DEVICE CONTROL REGISTER | | | | | | | |
|-------------------------|-----|--------|--|---|---------------|---|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FAST | | | | | BRT_MODE[1:0] | | BL_CTL |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| FAST | 7 | | Skip refresh of trim and configuration registers from EPROMs when exiting the low power STANDBY mode. 0 = read EPROMs before returning to the ACTIVE state 1 = only read EPROMs once on initial power-up. | | | | |
| BRT_MODE | 2:1 | R/W | Brightness source mode Figure 7 00b = PWM input only 01b = PWM input and Brightness register (combined before shaper block) 10b = Brightness register only 11b = PWM input and Brightness register (combined after shaper block) | | | | |
| BL_CTL | 0 | R/W | Enable backlight when Brightness Register is used to control brightness (BRT_MODE = 10). 0 = Backlight disabled and chip turned off 1 = Backlight enabled and chip turned on This bit has no effect when PWM pin control is selected for brightness control (BRT_MODE = 00). In this mode the state of PWM pin enable or disables the chip. | | | | |

8.6.1.3 Status

Address 02h

Reset value 0000 0000b

| FAULT REGISTER | | | | | | | |
|----------------|-------|---------|--|-----|-----|-----|------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OPEN | SHORT | VREF_OK | VBOOST_OK | OVP | OCP | TSD | UVLO |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| OPEN | 7 | R | LED open fault detection 0 = No fault 1 = LED open fault detected. The value is not latched. | | | | |
| SHORT | 6 | R | LED short fault detection 0 = No fault 1 = LED short fault detected. The value is not latched. | | | | |
| VREF_OK | 5 | R | Internal VREF node monitor status 1 = VREF voltage is OK. | | | | |
| VBOOST_OK | 4 | R | Boost output voltage monitor status 0 = Boost output voltage has not reached its target ($V_{BOOST} < V_{target} - 2.5V$) 1 = Boost output voltage is OK. The value is not latched. | | | | |
| OVP | 3 | R | Overvoltage protection 0 = No fault 1 = Overvoltage condition occurred. Fault is cleared by reading the register 02h. | | | | |
| OCP | 2 | R | Over current protection 0 = No fault 1 = Overcurrent condition occurred. Fault bit is cleared by reading this register. | | | | |
| TSD | 1 | R | Thermal shutdown 0 = No fault 1 = Thermal fault generated, 150°C reached. Boost converter and LED outputs are disabled until the temperature has dropped down to 130°C. Fault is cleared by reading this register. | | | | |
| UVLO | 0 | R | Undervoltage detection 0 = No fault 1 = Undervoltage detected on the V_{DD} pin. Boost converter and LED outputs are disabled until V_{DD} voltage is above the UVLO threshold voltage. Threshold voltage is set with EPROM bits. Fault is cleared by reading this register. | | | | |

8.6.1.4 Direct Control

Address 04h

Reset value 0000 0000b

| DIRECT CONTROL REGISTER | | | | | | | |
|-------------------------|-----|--------|---|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | OUT[5:0] | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| OUT | 5:0 | R/W | Direct control of the LED outputs 0 = Normal operation. LED output are controlled with the adaptive dimming block 1 = LED output is forced to 100% PWM. | | | | |

8.6.1.5 LED String Enable

Address 16h

Reset value 0011 1111b

| TEMP LSB REGISTER | | | | | | | |
|-------------------|-----|--------|--|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LED_EN[5:0] | | | | | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| LED_EN | 5:0 | R/W | Bits 5:0 correspond to LED Strings 6:1 respectively. Bit value 1 = LED String Enabled Bit value 0 = LED String Disabled Note: To disable string(s), it is recommended to disable higher order string(s). For example, for 5-string configuration, disable 6th String. For 4-string configuration, disable 6th and 5th string. These bits are ANDed with the internal LED enable bits that are generated with the PS_MODE logic. | | | | |

8.6.2 EPROM Bit Explanations

8.6.2.1 LP8556TM (DSBGA) Configurations and Pre-Configured EPROM Settings

| ADDRESS | LP8556-E02 | LP8556-E03 | LP8556-E04 | LP8556-E05 ⁽¹⁾ |
|---------|------------|------------|------------|---------------------------|
| 98h[7] | 0b | 0b | 0b | 0b |
| 9Eh | 22h | 24h | 24h | 22h |
| A0h | FFh | FFh | FFh | |
| A1h | 5Fh | BFh | 3Fh | |
| A2h | 20h | 28h | 2Fh | |
| A3h | 5Eh | 5Eh | 5Eh | |
| A4h | 72h | 72h | 72h | |
| A5h | 04h | 14h | 04h | |
| A6h | 80h | 80h | 80h | |
| A7h | F7h | F7h | F7h | |
| A9h | 80h | A0h | 60h | |
| AAh | 0Fh | 0Fh | 0Fh | |
| ABh | 00h | 00h | 00h | |
| ACh | 00h | 00h | 00h | |
| ADh | 00h | 00h | 00h | |
| A Eh | 0Fh | 0Fh | 0Fh | |
| AFh | 05h | 03h | 03h | |

(1) LP8556-E05 is a device option with un-configured EPROM settings. This option is for users that desire programming the device by themselves. Bits 98h[7] and 9Eh[5] are always pre-configured.

8.6.2.2 LP8556TM (DSBGA) Configurations and Pre-configured EPROM Settings Continued

| ADDRESS | LP8556-E06 | LP8556-E07 | LP8556-E09 | LP8556-E11 |
|---------|------------|------------|------------|------------|
| 98h[7] | 0b | 0b | 0b | 0b |
| 9Eh | 22h | 04h | 22h | 02h |
| A0h | FFh | FFh | FFh | FFh |
| A1h | DBh | BFh | CFh | 4Fh |
| A2h | 2Fh | 0Dh | 2Fh | 20h |
| A3h | 02h | 02h | 02h | 03h |
| A4h | 72h | 72h | 72h | 12h |
| A5h | 14h | 20h | 04h | 3Ch |
| A6h | 40h | 4Eh | 80h | 40h |
| A7h | F7h | F6h | F7h | F4h |
| A9h | DBh | C0h | A0h | 80h |
| AAh | 0Fh | 0Fh | 0Fh | 0Fh |
| ABh | 00h | 00h | 00h | 00h |
| ACh | 00h | 00h | 00h | 00h |
| ADh | 00h | 00h | 00h | 00h |
| A Eh | 0Fh | 0Fh | 0Eh | 0Fh |
| AFh | 05h | 03h | 05h | 01h |

8.6.2.3 LP8556SQ (WQFN) Configurations and Pre-configured EPROM Settings

| ADDRESS | LP8556-E00 | LP8556-E08 | LP8556-E09 |
|---------|------------|------------|------------|
| 98h[7] | 1b | 1b | 1b |
| 9Eh | 22h | 22h | 22h |
| A0h | FFh | FFh | FFh |
| A1h | CFh | CFh | CFh |
| A2h | 2Fh | 2Fh | 2Fh |
| A3h | 5Eh | 5Eh | 02h |
| A4h | 72h | 72h | 72h |
| A5h | 14h | 24h | 04h |
| A6h | 80h | 80h | 80h |
| A7h | F6h | F6h | F6h |
| A9h | A0h | A0h | A0h |
| AAh | 0Fh | 0Fh | 0Fh |
| ABh | 00h | 00h | 00h |
| ACh | 00h | 00h | 00h |
| ADh | 00h | 00h | 00h |
| A Eh | 0Fh | 0Fh | 0Fh |
| AFh | 01h | 01h | 01h |

8.6.2.4 CFG98

Address 98h

| CFG98 REGISTER | | | | | | | |
|----------------|-----|--------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IBOOST_LIM_2X | | | | | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| IBOOST_LIM_2X | 7 | R/W | Select the inductor current limit range. When IBOOST_LIM_2X = 0, the inductor current limit can be set to 0.9 A, 1.2 A, 1.5 A or 1.8 A. When IBOOST_LIM_2X = 1, the inductor current limit can be set to 1.6 A, 2.1 A, or 2.6 A . This option is supported only on WQFN package and not on DSBGA package. See ⁽¹⁾ . | | | | |

- (1) 1.8 A is the maximum I_{SW_LIM} supported with the DSBGA package. For applications requiring the I_{SW_LIM} to be greater than 1.8 A and up to 2.6 A, WQFN package should be considered.

8.6.2.5 CFG9E

Address 9Eh

| CFG9E REGISTER | | | | | | | |
|-----------------|-----|--------|--|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBOOST_RANGE | | | HEADROOM_OFFSET | | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| VBOOST_RANGE | 5 | R/W | Select VBOOST range. When VBOOST_RANGE = 0, the output voltage range is from 7 V to 34 V When VBOOST_RANGE = 1, the output voltage range is from 16 V to 43 V In applications with an output voltage higher than 16 V, VBOOST_RANGE = 1 is preferred. | | | | |
| HEADROOM_OFFSET | 3:0 | R/W | LED driver headroom offset. This adjusts the LOW comparator threshold together with LED_HEADROOM bits and contributes to the MID comparator threshold. 0000 = 460 mV 0001 = 390 mV 0010 = 320 mV 0100 = 250 mV 1000 = 180 mV | | | | |

8.6.2.6 CFG0

Address A0h

| CFG0 REGISTER | | | | | | | |
|------------------|-----|------------------------------|--|---|------------------------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CURRENT_LSB[7:0] | | | | | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| CURRENT_LSB | 7:0 | R/W | The 8-bits in this register (LSB) along the 4-bits defined in CFG1 Register (MSB) allow LED current to be set in 12-bit fine steps. These 12-bits further scale the maximum LED current set using CFG1 Register, CURRENT_MAX bits (denoted as I _{MAX}). If ISET_EN = 0, the LED current is defined with the bits as shown below. If ISET_EN = 1, then the external resistor connected to the ISET pin scales the LED current as shown below. | | | | |
| | | | | | ISET_EN = 0 | ISET_EN = 1 | |
| | | | 0000 0000 0000 | | 0A | 0A | |
| | | | 0000 0000 0001 | | $(1/4095) \times I_{MAX}$ | $(1/4095) \times I_{MAX} \times 20,000 \times 1.2V / R_{ISET}$ | |
| | | | 0000 0000 0010 | | $(2/4095) \times I_{MAX}$ | $(2/4095) \times I_{MAX} \times 20,000 \times 1.2V / R_{ISET}$ | |
| | | | ... | | ... | ... | |
| | | | 0111 1111 1111 | | $(2047/4095) \times I_{MAX}$ | $(2047/4095) \times I_{MAX} \times 20,000 \times 1.2V / R_{ISET}$ | |
| | | | ... | | ... | ... | |
| | | | 1111 1111 1101 | | $(4093/4095) \times I_{MAX}$ | $(4093/4095) \times I_{MAX} \times 20,000 \times 1.2V / R_{ISET}$ | |
| | | | 1111 1111 1110 | | $(4094/4095) \times I_{MAX}$ | $(4094/4095) \times I_{MAX} \times 20,000 \times 1.2V / R_{ISET}$ | |
| 1111 1111 1111 | | $(4095/4095) \times I_{MAX}$ | $(4095/4095) \times I_{MAX} \times 20,000 \times 1.2V / R_{ISET}$ | | | | |

8.6.2.7 CFG1

Address A1h

| CFG1 REGISTER | | | | | | | |
|---------------|------------------|--------|--|-------------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PDET_STDBY | CURRENT_MAX[2:0] | | | CURRENT_MSB[11:8] | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| PDET_STDBY | 7 | R/W | Enable Standby when PWM input is constant low (approx. 50 ms timeout). | | | | |
| CURRENT_MAX | 6:4 | R/W | Set Maximum LED current as shown below. This maximum current is scaled as described in the CFG0 Register. 000 = 5 mA 001 = 10 mA 010 = 15 mA 011 = 20 mA 100 = 23 mA 101 = 25 mA 110 = 30 mA 111 = 50 mA | | | | |
| CURRENT_MSB | 3:0 | R/W | These bits form the 4 MSB bits for LED Current as described in CFG0 Register. | | | | |

8.6.2.8 CFG2

Address A2h

| CFG2 REGISTER | | | | | | | |
|---------------|-----|---------|--|-------|---------|---------------|-------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | UVLO_EN | UVLO_TH | BL_ON | ISET_EN | BOOST_FSET_EN | PWM_FSET_EN |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| RESERVED | 7:6 | R/W | | | | | |
| UVLO_EN | 5 | R/W | Undervoltage lockout protection enable. | | | | |
| UVLO_TH | 4 | R/W | UVLO threshold levels: 0 = 2.5 V 1 = 5.2 V | | | | |
| BL_ON | 3 | R/W | Enable backlight. This bit must be set for PWM only control. 0 = Backlight disabled. This selection is recommended for systems with an I ² C master. With an I ² C master, the backlight can be controlled by writing to the register 01h. 1 = Backlight enabled. This selection is recommended for systems with PWM only control. | | | | |
| ISET_EN | 2 | R/W | Enable LED current set resistor. 0 = Resistor is disabled and current is set with CURRENT and CURRENT_MAX EPROM register bits. 1 = Resistor is enabled and current is set with the R _{ISET} resistor AND CURRENT AND CURRENT_MAX EPROM register bits. | | | | |
| BOOST_FSET_EN | 1 | R/W | Enable configuration of the switching frequency via FSET pin. 0 = Configuration of the switching frequency via FSET pin is disabled. The switching frequency is set with BOOST_FREQ EPROM register bits. 1 = Configuration of the switching frequency via FSET pin is enabled. | | | | |
| PWM_FSET_EN | 0 | R/W | Enable configuration of the PWM dimming frequency via FSET pin. 0 = Configuration of the switching frequency via FSET pin is disabled. The switching frequency is set with PWM_FREQ EPROM register bits. 1 = Configuration of the PWM dimming frequency via FSET pin is enabled. | | | | |

8.6.2.9 CFG3

Address A3h

| CFG3 REGISTER | | | | | | | |
|----------------------|------------|--------|---|-------------|---|---------------------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | SLOPE[2:0] | | | FILTER[1:0] | | PWM_INPUT_HYSTERESIS[1:0] | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| RESERVED | 7 | R/W | | | | | |
| SLOPE | 6:4 | R/W | Select brightness change transition duration 000 = 0 ms (immediate change) 001 = 1 ms 010 = 2 ms 011 = 50 ms 100 = 100 ms 101 = 200 ms 110 = 300 ms 111 = 500 ms | | | | |
| FILTER | 3:2 | R/W | Select brightness change transition filtering strength 00 = No filtering 01 = light smoothing 10 = medium smoothing 11 = heavy smoothing | | | | |
| PWM_INPUT_HYSTERESIS | 1:0 | R/W | PWM input hysteresis function. 00 = OFF 01 = 1-bit hysteresis with 13-bit resolution 10 = 1-bit hysteresis with 12-bit resolution 11 = 1-bit hysteresis with 8-bit resolution | | | | |

8.6.2.10 CFG4

Address A4h

| CFG4 REGISTER | | | | | | | |
|-------------------------|-----|--------|---|----------|---------------|-------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PWM_TO_I_THRESHOLD[3:0] | | | | RESERVED | STEADY_DITHER | DITHER[1:0] | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| PWM_TO_I_THRESHOLD | 7:4 | R/W | Select switch point between PWM and pure current dimming 0000 = current dimming across entire range 0001 = switch point at 10% of the maximum LED current. 0010 = switch point at 12.5% of the maximum LED current. 0011 = switch point at 15% of the maximum LED current. 0100 = switch point at 17.5% of the maximum LED current. 0101 = switch point at 20% of the maximum LED current. 0110 = switch point at 22.5% of the maximum LED current. 0111 = switch point at 25% of the maximum LED current. This is a recommended selection. 1000 = switch point at 33.33% of the maximum LED current. 1001 = switch point at 41.67% of the maximum LED current. 1010 = switch point at 50% of the maximum LED current. 1011 to 1111 = PWM dimming across entire range | | | | |
| RESERVED | 3 | R/W | | | | | |
| STEADY_DITHER | 2 | R/W | Dither function method select: 0 = Dither only on transitions 1 = Dither at all times | | | | |
| DITHER | 1:0 | R/W | Dither function control 00 = Dithering disabled 01 = 1-bit dithering 10 = 2-bit dithering 11 = 3-bit dithering | | | | |

8.6.2.11 CFG5

Address A5h

| CFG5 REGISTER | | | | | | | | |
|---------------|-----|--------------|---|---|---------------|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| PWM_DIRECT | | PS_MODE[2:0] | | | PWM_FREQ[3:0] | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | | |
| PWM_DIRECT | 7 | R/W | Intended for certain test mode purposes. When enabled, the entire pipeline is bypassed and PWM output is connected with PWM input. | | | | | |
| PS_MODE | 6:4 | R/W | Select PWM output phase configuration: 000 = 6-phase, 6 drivers (0°, 60°, 120°, 180°, 240°, 320°) 001 = 5-phase, 5 drivers (0°, 72°, 144°, 216°, 288°, OFF) 010 = 4-phase, 4 drivers (0°, 90°, 180°, 270°, OFF, OFF) 011 = 3-phase, 3 drivers (0°, 120°, 240°, OFF, OFF, OFF) 100 = 2-phase, 2 drivers (0°, 180°, OFF, OFF, OFF, OFF) 101 = 3-phase, 6 drivers (0°, 0°, 120°, 120°, 240°, 240°) 110 = 2-phase, 6 drivers (0°, 0°, 0°, 180°, 180°, 180°) 111 = 1-phase, 6 drivers (0°, 0°, 0°, 0°, 0°, 0°) | | | | | |
| PWM_FREQ | 3:0 | R/W | 0h = 4,808 Hz (11-bit) 1h = 6,010 Hz (10-bit) 2h = 7,212 Hz (10-bit) 3h = 8,414 Hz (10-bit) 4h = 9,616 Hz (10-bit) 5h = 12,020 Hz (9-bit) 6h = 13,222 Hz (9-bit) 7h = 14,424 Hz (9-bit) 8h = 15,626 Hz (9-bit) 9h = 16,828 Hz (9-bit) Ah = 18,030 Hz (9-bit) Bh = 19,232 Hz (9-bit) Ch = 24,040 Hz (8-bit) Dh = 28,848 Hz (8-bit) Eh = 33,656 Hz (8-bit) Fh = 38,464 Hz(8-bit) | | | | | |

8.6.2.12 CFG6

Address A6h

| CFG6 REGISTER | | | | | | | |
|-----------------|-----|-------------|--|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BOOST_FREQ[1:0] | | VBOOST[5:0] | | | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| BOOST_FREQ | 7:6 | R/W | Set boost switching frequency when BOOST_FSET_EN = 0. 00 = 312 kHz 01 = 625 kHz 10 = 1250 kHz 11 = undefined | | | | |
| VBOOST | 5:0 | R/W | Boost output voltage. When ADAPTIVE = 1, this is the boost minimum and initial voltage. | | | | |

8.6.2.13 CFG7

Address A7h

| CFG7 REGISTER | | | | | | | |
|---------------|-----|---------|--|----------|---|-----------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | EN_DRV3 | EN_DRV2 | RESERVED | | IBOOST_LIM[1:0] | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| RESERVED | 7:6 | | | | | | |
| EN_DRV3 | 5 | R/W | Selects boost driver strength to set boost slew rate. See EMI Reduction for more detail. 0 = Driver3 disabled 1 = Driver3 enabled | | | | |
| EN_DRV2 | 4 | R/W | Selects boost driver strength to set boost slew rate. See EMI Reduction for more detail. 0 = Driver2 disabled 1 = Driver2 enabled | | | | |
| RESERVED | 3:2 | R/W | | | | | |
| IBOOST_LIM | 1:0 | R/W | Select boost inductor current limit (IBOOST_LIM_2X = 0 / IBOOST_LIM_2X = 1) 00 = 0.9 A / 1.6 A 01 = 1.2 A / 2.1 A 10 = 1.5 A / 2.6 A 11 = 1.8 A / not permitted | | | | |

8.6.2.14 CFG9

Address A9h

| CFG9 REGISTER | | | | | | | |
|-----------------|-----|--------|---|---------------------|---|-------------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBOOST_MAX[2:0] | | | JUMP_EN | JUMP_THRESHOLD[1:0] | | JUMP_VOLTAGE[1:0] | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| VBOOST_MAX | 7:5 | R/W | Select the maximum boost voltage (typ values) (VBOOST_RANGE = 0 / VBOOST_RANGE = 1) 010 = NA / 21 V 011 = NA / 25 V 100 = 21 V / 30 V 101 = 25 V / 34.5 V 110 = 30 V / 39 V 111 = 34 V / 43 V | | | | |
| JUMP_EN | 4 | R/W | Enable JUMP detection on the PWM input. | | | | |
| JUMP_THRESHOLD | 3:2 | R/W | Select JUMP threshold: 00 = 10% 01 = 30% 10 = 50% 11 = 70% | | | | |
| JUMP_VOLTAGE | 1:0 | R/W | Select JUMP voltage: 00 = 0.5 V 01 = 1 V 10 = 2 V 11 = 4 V | | | | |

8.6.2.15 CFGA

Address AAh

| CFG9 REGISTER | | | | | | | |
|-----------------|----------|----------|--|----------|----------------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SSCLK_EN | RESERVED | RESERVED | | ADAPTIVE | DRIVER_HEADROOM[2:0] | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| SSCLK_EN | 7 | R/W | Enable spread spectrum function | | | | |
| RESERVED | 6 | R/W | | | | | |
| RESERVED | 5:4 | R/W | | | | | |
| ADAPTIVE | 3 | R/W | Enable adaptive boost control | | | | |
| DRIVER_HEADROOM | 2:0 | R/W | LED driver headroom control. This sets the LOW comparator threshold and contributes to the MID comparator threshold. 000 = HEADROOM_OFFSET + 875 mV 001 = HEADROOM_OFFSET + 750 mV 010 = HEADROOM_OFFSET + 625 mV 011 = HEADROOM_OFFSET + 500 mV 100 = HEADROOM_OFFSET + 375 mV 101 = HEADROOM_OFFSET + 250 mV 110 = HEADROOM_OFFSET + 125 mV 111 = HEADROOM_OFFSET mV | | | | |

8.6.2.16 CFGE

Address AEh

| CFGF REGISTER | | | | | | | |
|---------------|-----|--------------|---|-------------------|---|--------------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STEP_UP[1:0] | | STEP_DN[1:0] | | LED_FAULT_TH[2:0] | | LED_COMP_HYST[1:0] | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| STEP_UP | 7:6 | R/W | Adaptive headroom UP step size 00 = 105 mV 01 = 210 mV 10 = 420 mV 11 = 840 mV | | | | |
| STEP_DN | 5:4 | R/W | Adaptive headroom DOWN step size 00 = 105 mV 01 = 210 mV 10 = 420 mV 11 = 840 mV | | | | |
| LED_FAULT_TH | 3:2 | R/W | LED headroom fault threshold. This sets the HIGH comparator threshold. 00 = 5 V 01 = 4 V 10 = 3 V 11 = 2 V | | | | |
| LED_COMP_HYST | 1:0 | R/W | LED headrom comparison hysteresis. This sets the MID comparator threshold. 00 = DRIVER_HEADROOM + 1000 mV 01 = DRIVER_HEADROOM + 750 mV 10 = DRIVER_HEADROOM + 500 mV 11 = DRIVER_HEADROOM + 250 mV | | | | |

8.6.2.17 CFGF

Address AFh

| CFGF REGISTER | | | | | | | |
|---------------|-----|--------|---------------------------------|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVISION | | | | | | | |
| NAME | BIT | ACCESS | DESCRIPTION | | | | |
| REV | 7:0 | R/W | EPROM Settings Revision ID code | | | | |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Using LP8556 With I²C Host

9.1.1.1 Setting Boost Switching and PWM Dimming Frequencies

Boost switching and PWM dimming frequencies can be set via EEPROM when BOOST_FSET_EN = 0 and PWM_FSET_EN = 0. Available options are shown in [Table 11](#) and [Table 12](#).

Table 11. Configuring Boost Switching Frequency via EPROM

| BOOST_FSET_EN | BOOST_FREQ[1:0] | f_{sw} [kHz] |
|---------------|-----------------|----------------|
| 0 | 00 | 312 |
| 0 | 01 | 625 |
| 0 | 10 | 1250 |
| 0 | 11 | Reserved |

Table 12. Configuring PWM Dimming Frequency via EPROM

| PWM_FSET_EN | PWM_FREQ[3:0] | f_{PWM} [Hz] (Resolution) |
|-------------|---------------|-----------------------------|
| 0 | 0000 | 4808 (11-bit) |
| 0 | 0001 | 6010 (10-bit) |
| 0 | 0010 | 7212 (10-bit) |
| 0 | 0011 | 8414 (10-bit) |
| 0 | 0100 | 9616 (10-bit) |
| 0 | 0101 | 12020 (9-bit) |
| 0 | 0110 | 13222 (9-bit) |
| 0 | 0111 | 14424 (9-bit) |
| 0 | 1000 | 15626 (9-bit) |
| 0 | 1001 | 16828 (9-bit) |
| 0 | 1010 | 18030 (9-bit) |
| 0 | 1011 | 19232 (9-bit) |
| 0 | 1100 | 24040 (8-bit) |
| 0 | 1101 | 28848 (8-bit) |
| 0 | 1110 | 33656 (8-bit) |
| 0 | 1111 | 38464 (8-bit) |

9.1.1.2 Setting Full-Scale LED Current

The LED current per output is configured by programming the CURRENT_MAX and CURRENT registers when ISET_EN = 0. Available options are shown below.

Table 13. Setting Full-Scale LED Current with EEPROM

| ISET_EN | CURRENT_MAX | CURRENT[11:0] | FULL-SCALE ILED [mA] |
|---------|-------------|---------------|-------------------------------|
| 0 | 0 | FFFh | 5 |
| 0 | 1 | FFFh | 10 |
| 0 | 10 | FFFh | 15 |
| 0 | 11 | FFFh | 20 |
| 0 | 100 | FFFh | 23 |
| 0 | 101 | FFFh | 25 |
| 0 | 110 | FFFh | 30 |
| 0 | 111 | FFFh | 50 |
| 0 | 000 – 111 | 001h – FFFh | (CURRENT/4095) × CURRENT_IMAX |

9.1.2 Using LP8556 With Configuration Resistors and IO Pins

9.1.2.1 Setting Boost Switching and PWM Dimming Frequencies

Boost switching and PWM dimming frequencies can be set via resistor when BOOST_FSET_EN = 1 and PWM_FSET_EN = 1. Available options are shown in [Table 14](#).

Table 14. Configuring PWM Dimming Frequency With an External Resistor

| RFSET [kΩ] (TOLERANCE) | f _{sw} [kHz] BOOST_FSET_EN = 1 | f _{PWM} [Hz] (RESOLUTION) PWM_FSET_EN = 1 |
|----------------------------------|--|---|
| Floating or FSET pin pulled HIGH | 1250 | 9616 (10-bit) |
| 470 k - 1 M (±5%) | 312 | 2402 (12-bit) |
| 300 k, 330 k (±5%) | 312 | 4808 (11-bit) |
| 200 k (±5%) | 312 | 6010 (10-bit) |
| 147 k, 150k, 154 k, 158k (±1%) | 312 | 9616 (10-bit) |
| 121 k (±1%) | 312 | 12020 (9-bit) |
| 100 k (±1%) | 312 | 14424 (9-bit) |
| 86.6 k (±1%) | 312 | 16828 (9-bit) |
| 75 k (±1%) | 312 | 19232 (9-bit) |
| 63.4 k (±1%) | 625 | 2402 (12-bit) |
| 52.3 k, 53.6 k (±1%) | 625 | 4808 (11-bit) |
| 44.2k, 45.3 k (±1%) | 625 | 6010 (10-bit) |
| 39.2 k (±1%) | 625 | 9616 (10-bit) |
| 34 k (±1%) | 625 | 12020 (9-bit) |
| 30.1k (±1%) | 625 | 14424 (9-bit) |
| 26.1 k (±1%) | 625 | 16828 (9-bit) |
| 23.2 k (±1%) | 625 | 19232 (9-bit) |
| 20.5 k (±1%) | 1250 | 2402 (12-bit) |
| 18.7 k (±1%) | 1250 | 4808 (11-bit) |
| 16.5k (±1%) | 1250 | 6010 (10-bit) |
| 14.7 k (±1%) | 1250 | 9616 (10-bit) |
| 13 k (±1%) | 1250 | 12020 (9-bit) |
| 11.8k (±1%) | 1250 | 14424 (9-bit) |
| 10.7 k (±1%) | 1250 | 16828 (9-bit) |
| 9.76 k (±1%) | 1250 | 19232 (9-bit) |
| FSET pin shorted to GND | 1250 | Same as PWM input frequency |

9.1.2.2 Setting Full-Scale LED Current

The LED current per output is configured by ISET resistor when ISET_EN=1. In this mode the CURRENT_IMAX and CURRENT registers can also further scale the LED current. Available options are shown in Table 15.

Table 15. Setting Full-Scale LED Current with ISET Resistor

| RISET [Ω] | ISET_EN | CURRENT_MAX | CURRENT[11:0] | FULL-SCALE ILED [mA] |
|--------------|---------|-------------|---------------|--|
| 24 k | 1 | 0 | FFFh | 5 |
| 24 k | 1 | 1 | FFFh | 10 |
| 24 k | 1 | 10 | FFFh | 15 |
| 24 k | 1 | 11 | FFFh | 20 |
| 24 k | 1 | 100 | FFFh | 23 |
| 24 k | 1 | 101 | FFFh | 25 |
| 24 k | 1 | 110 | FFFh | 30 |
| 24 k | 1 | 111 | FFFh | 50 |
| 12 k – 100 k | 1 | 000–111 | 001h–FFFh | $(CURRENT/4095) \times IMAX \times 20,000 \times 1.2 V / R_{ISET}$ |

9.2 Typical Application

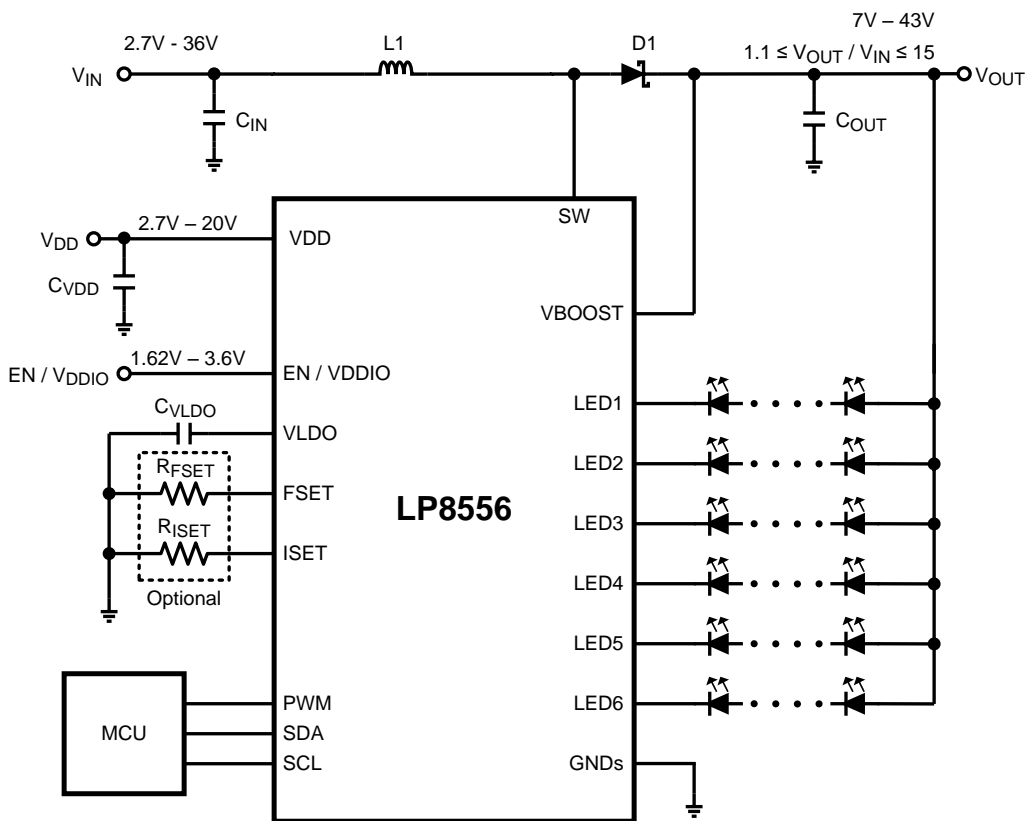


Figure 19. LP8556 Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

Table 16. Recommended Inductance

| f_{sw} | MIN | TYP | MAX | UNIT |
|----------|-----|-----|-----|---------|
| 1250 | 3.3 | | 22 | μ H |
| 625 | 6.8 | | 68 | μ H |
| 312 | 10 | | 100 | μ H |

Table 17. Recommended Output Capacitance

| f_{sw} | MIN | TYP | MAX | UNIT |
|----------|-----|-----|-----|---------|
| 1250 | 4.7 | | | μ F |
| 625 | 4.7 | | | μ F |
| 312 | 10 | | | μ F |

9.2.2 Detailed Design Procedure

9.2.2.1 Recommended Inductance for the Boost Power Stage

Assumes 20 mA as the maximum LED current per string and 3.3 V as the maximum LED forward voltage.

| NUMBER OF LED STRINGS | NUMBER OF LEDS PER STRING | BOOST INPUT VOLTAGE RANGE | L1 INDUCTANCE | | |
|-----------------------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|
| | | | $f_{sw} = 1250$ kHz | $f_{sw} = 625$ kHz | $f_{sw} = 312$ kHz |
| 6 | 6 | 2.7 V - 4.4 V | 3.3 μ H - 6.8 μ H | 6.8 μ H - 15 μ H | 10 μ H - 33 μ H |
| | | 5.4 V - 8.8 V | 10 μ H - 22 μ H | 22 μ H - 47 μ H | 47 μ H - 100 μ H |
| 6 | 8 | 2.7 V - 4.4 V | 4.7 μ H - 10 μ H | 10 μ H - 15 μ H | 22 μ H - 33 μ H |
| | | 5.4 V - 8.8 V | 10 μ H - 22 μ H | 22 μ H - 68 μ H | 47 μ H - 100 μ H |
| 4 | 10 | 5.4 V - 8.8 V | 6.8 μ H - 22 μ H | 22 μ H - 47 μ H | 47 μ H - 100 μ H |
| 4 | 12 | 5.4 V - 8.8 V | 10 μ H - 22 μ H | 22 μ H - 47 μ H | 33 μ H - 100 μ H |

9.2.2.2 Recommended Capacitances for the Boost and LDO Power Stages⁽¹⁾

| SWITCHING FREQUENCY [kHz] | C_{IN} [μ F] | C_{OUT} [μ F] | C_{VLDO} [μ F] |
|---------------------------|---------------------|----------------------|-----------------------|
| 1250 | 2.2 | 4.7 | 10 |
| 625 | 2.2 | 4.7 | 10 |
| 312 | 4.7 | 10 | 10 |

(1) Capacitance of Multi-Layer Ceramic Capacitors (MLCC) can change significantly with the applied DC voltage. Use capacitors with good capacitance versus DC bias characteristics. In general, MLCC in bigger packages have lower capacitance de-rating than physically smaller capacitors.

9.2.3 Application Curves

Unless otherwise specified: $V_{IN} = 3.8\text{ V}$, $C_{VLD0} = 10\ \mu\text{F}$, $L_1 = 4.7\ \mu\text{H}$, $C_{IN} = 2.2\ \mu\text{F}$, $C_{OUT} = 4.7\ \mu\text{F}$, $f_{SW} = 1.25\ \text{MHz}$

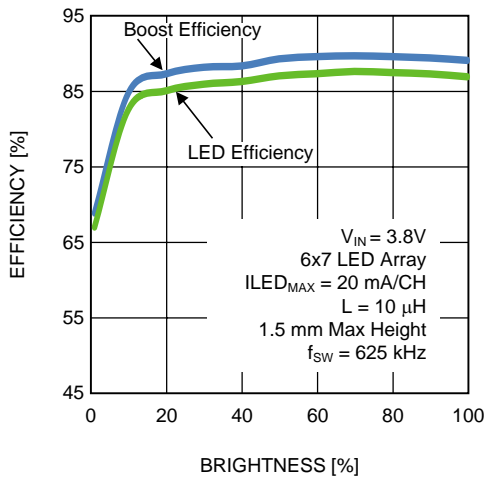


Figure 20. Boost and LED Drive Efficiency

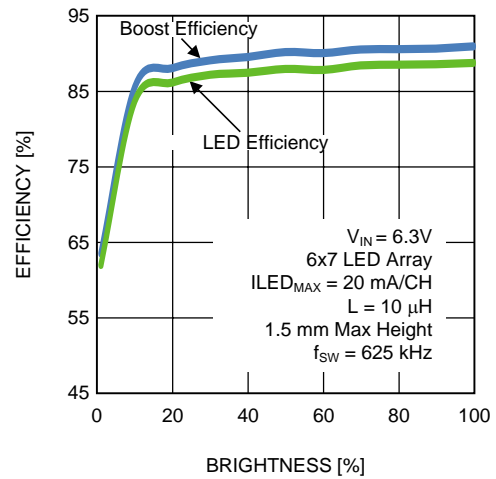


Figure 21. Boost and LED Drive Efficiency

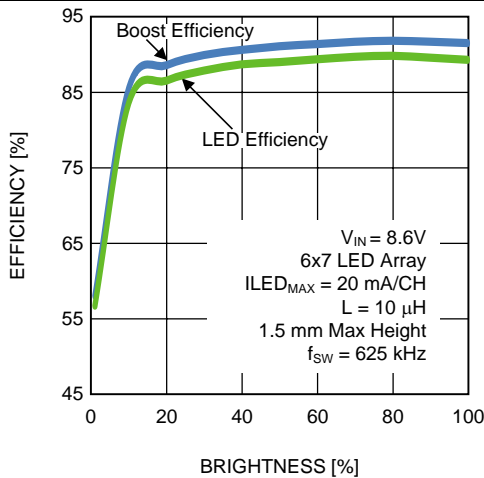


Figure 22. Boost and LED Drive Efficiency

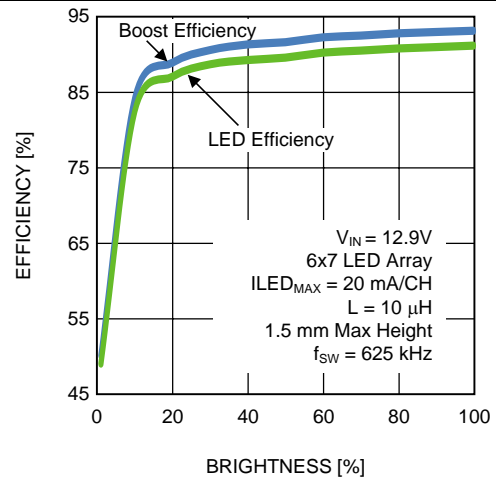


Figure 23. Boost and LED Drive Efficiency

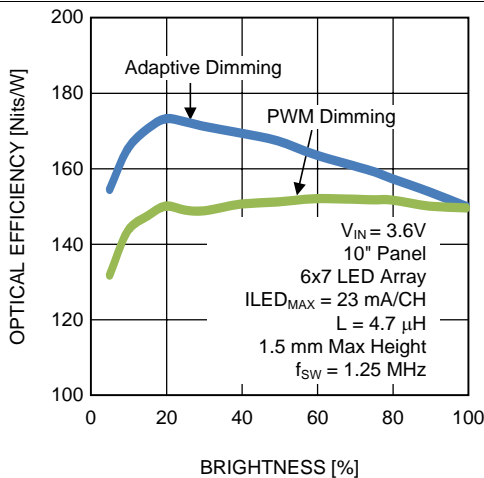


Figure 24. Optical Efficiency

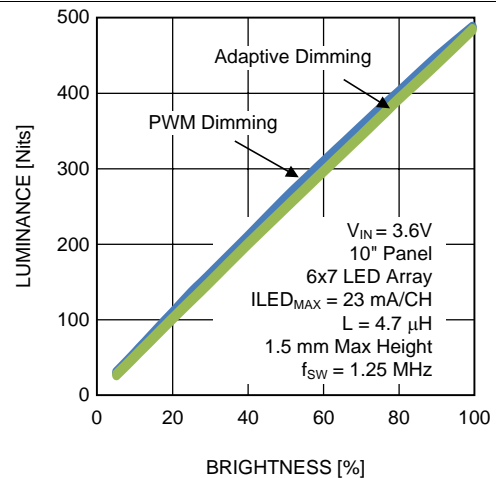


Figure 25. Luminance as a Function of Brightness

Unless otherwise specified: $V_{IN} = 3.8\text{ V}$, $C_{VLDO} = 10\ \mu\text{F}$, $L_1 = 4.7\ \mu\text{H}$, $C_{IN} = 2.2\ \mu\text{F}$, $C_{OUT} = 4.7\ \mu\text{F}$, $f_{SW} = 1.25\ \text{MHz}$

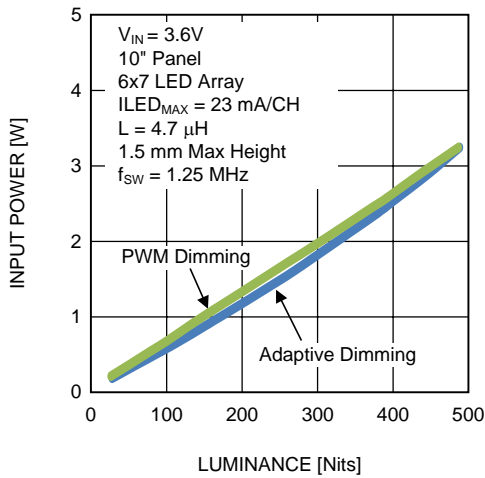


Figure 26. Input Power as a Function of Brightness

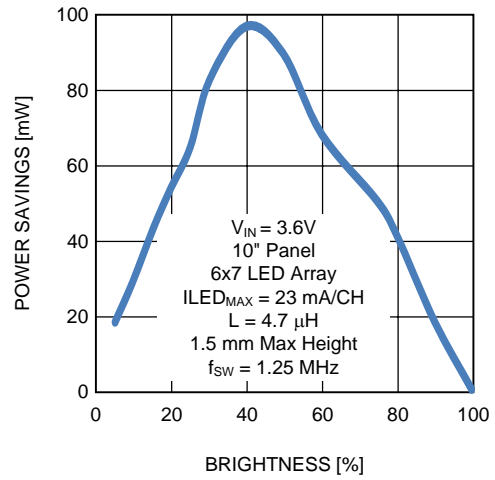


Figure 27. Power Savings With Adaptive Dimming when Compared to PWM Dimming

10 Power Supply Recommendations

The device is designed to operate from a VDD input voltage supply range from 2.7 V to 20 V. This input supply must be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition (start-up or rapid brightness change). The resistance of the input supply rail must be low enough that the input current transient does not cause drop high enough in the LP8556 supply voltage that can cause false UVLO fault triggering.

If the input supply is located more than a few inches from the LP8556 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. Depending on device EEPROM configuration and usage case the boost converter is configured to operate optimally with certain input voltage range.

11 Layout

11.1 Layout Guidelines

[Figure 28](#) and [Figure 29](#) follow proper layout guidelines and should be used as a guide for laying out the LP8556 circuit.

The LP8556 inductive boost converter has a high switched voltage at the SW pin, and a step current through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling ($I = C \times dV/dt$). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW and VBOOST pins due to parasitic inductance in the step current conducting path ($V = L \times di/dt$). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise.

The following list details the main (layout sensitive) areas of the device inductive boost converter in order of decreasing importance:

1. Boost Output Capacitor Placement

- Because the output capacitor is in the path of the inductor current discharge path, there is a high-current step from 0 to IPEAK each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the diodes cathode, through COUT, and back into the LP8556 GND pin contributes to voltage spikes ($V_{SPIKE} = LP_ \times di/dt$) at SW and OUT. These spikes can potentially over-voltage the SW and VBOOST pins, or feed through to GND. To avoid this, COUT+ must be connected as close to the cathode of the Schottky diode as possible, and COUT– must be connected as close to the LP8556 GND bumps as possible. The best placement for COUT is on the same layer as the LP8556 to avoid any vias that can add excessive series inductance.

2. Schottky Diode Placement

- In the device boost circuit the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode has a high-current step from 0 to IPEAK each time the switch turns off and the diode turns on. Any inductance in series with the diode causes a voltage spike ($V_{SPIKE} = LP_ \times di/dt$) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to VOUT and through the output capacitor, into GND. Connecting the anode of the diode as close to the SW pin as possible, and connecting the cathode of the diode as close to COUT+ as possible reduces the inductance (LP_) and minimize these voltage spikes.

3. Boost Input/VDD Capacitor Placement

- The LP8556 input capacitor filters the inductor current ripple and the internal MOSFET driver currents. The inductor current ripple can add input voltage ripple due to any series resistance in the input power path. The MOSFET driver currents can add voltage spikes on the input due to the inductance in series with the VIN/VDD and the input capacitor. Close placement of the input capacitor to the VDD pin and to the GND pin is critical because any series inductance between VIN/VDD and CIN+ or CIN– and GND can create voltage spikes that could appear on the VIN/VDD supply line and GND.
- Close placement of the input capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LP8556, forms a series RLC circuit. If the output resistance from the source is low enough, the circuit is underdamped and will have a resonant frequency (typically the case).
- Depending on the size of LS, the resonant frequency could occur below, close to, or above the switching frequency of the LP8556. This can cause the supply current ripple to be:

Layout Guidelines (continued)

- Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LP8556 switching frequency.
- Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency.
- Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency.

11.2 Layout Examples

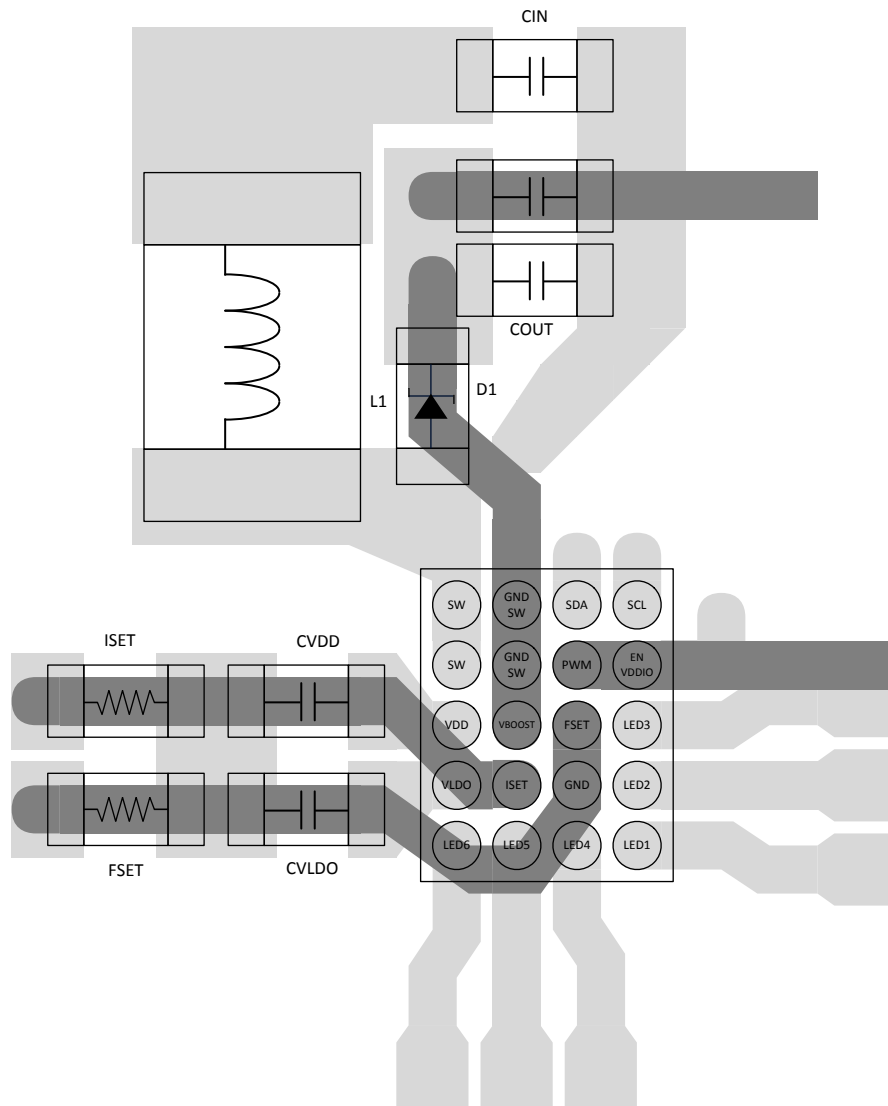


Figure 28. DSBGA Layout

Layout Examples (continued)

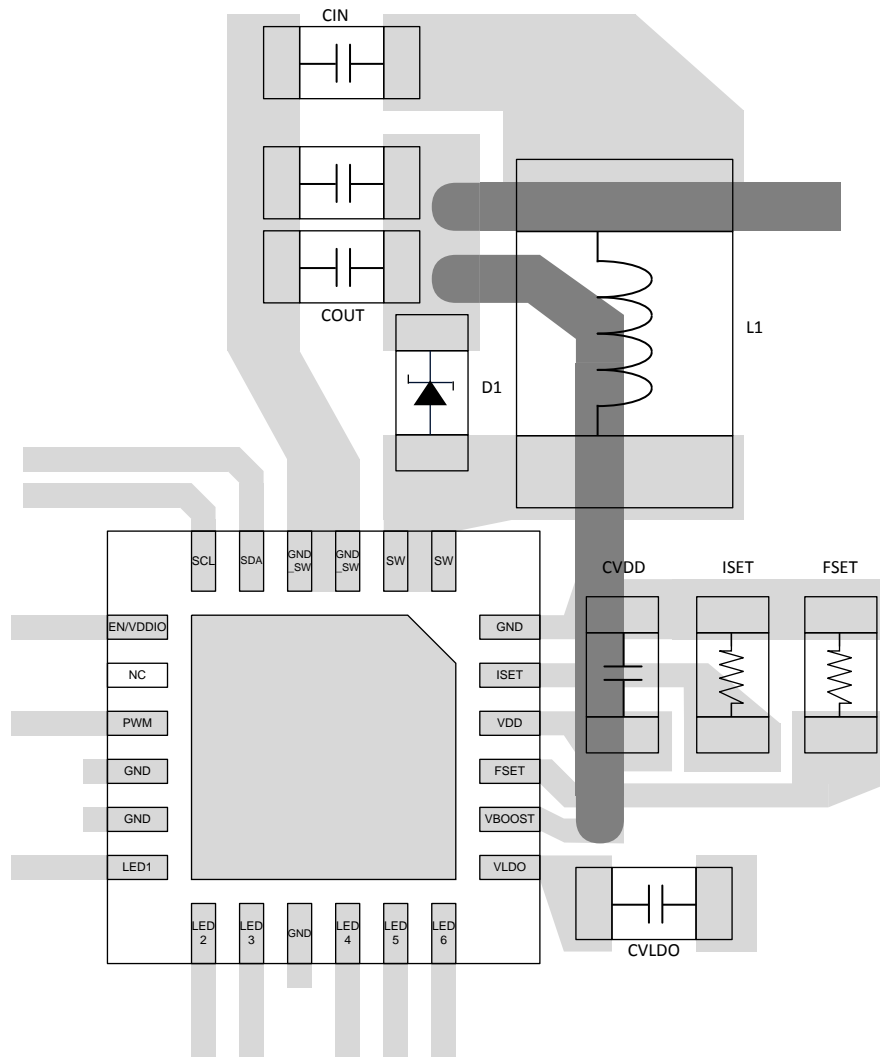


Figure 29. WQFN Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP8556SQ-E00/NOPB | ACTIVE | WQFN | RTW | 24 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -30 to 85 | L8556E0 | Samples |
| LP8556SQ-E08/NOPB | ACTIVE | WQFN | RTW | 24 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -30 to 85 | L8556E8 | Samples |
| LP8556SQ-E09/NOPB | ACTIVE | WQFN | RTW | 24 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -30 to 85 | L8556E9 | Samples |
| LP8556SQE-E00/NOPB | ACTIVE | WQFN | RTW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -30 to 85 | L8556E0 | Samples |
| LP8556SQE-E08/NOPB | ACTIVE | WQFN | RTW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -30 to 85 | L8556E8 | Samples |
| LP8556SQE-E09/NOPB | ACTIVE | WQFN | RTW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -30 to 85 | L8556E9 | Samples |
| LP8556SQX-E00/NOPB | ACTIVE | WQFN | RTW | 24 | 4500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -30 to 85 | L8556E0 | Samples |
| LP8556SQX-E08/NOPB | ACTIVE | WQFN | RTW | 24 | 4500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -30 to 85 | L8556E8 | Samples |
| LP8556SQX-E09/NOPB | ACTIVE | WQFN | RTW | 24 | 4500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -30 to 85 | L8556E9 | Samples |
| LP8556TME-E02/NOPB | ACTIVE | DSBGA | YFQ | 20 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E2 | Samples |
| LP8556TME-E03/NOPB | ACTIVE | DSBGA | YFQ | 20 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E3 | Samples |
| LP8556TME-E04/NOPB | ACTIVE | DSBGA | YFQ | 20 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E4 | Samples |
| LP8556TME-E05/NOPB | ACTIVE | DSBGA | YFQ | 20 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E5 | Samples |
| LP8556TME-E06/NOPB | ACTIVE | DSBGA | YFQ | 20 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E6 | Samples |
| LP8556TME-E09/NOPB | ACTIVE | DSBGA | YFQ | 20 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E9 | Samples |
| LP8556TME-E11/NOPB | ACTIVE | DSBGA | YFQ | 20 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 6E11 | Samples |
| LP8556TMX-E02/NOPB | ACTIVE | DSBGA | YFQ | 20 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E2 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP8556TMX-E03/NOPB | ACTIVE | DSBGA | YFQ | 20 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E3 | Samples |
| LP8556TMX-E04/NOPB | ACTIVE | DSBGA | YFQ | 20 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E4 | Samples |
| LP8556TMX-E05/NOPB | ACTIVE | DSBGA | YFQ | 20 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E5 | Samples |
| LP8556TMX-E06/NOPB | ACTIVE | DSBGA | YFQ | 20 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E6 | Samples |
| LP8556TMX-E09/NOPB | ACTIVE | DSBGA | YFQ | 20 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 56E9 | Samples |
| LP8556TMX-E11/NOPB | ACTIVE | DSBGA | YFQ | 20 | 3000 | Green (RoHS & no Sb/Br) | Call TI SNAGCU | Level-1-260C-UNLIM | -30 to 85 | 6E11 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

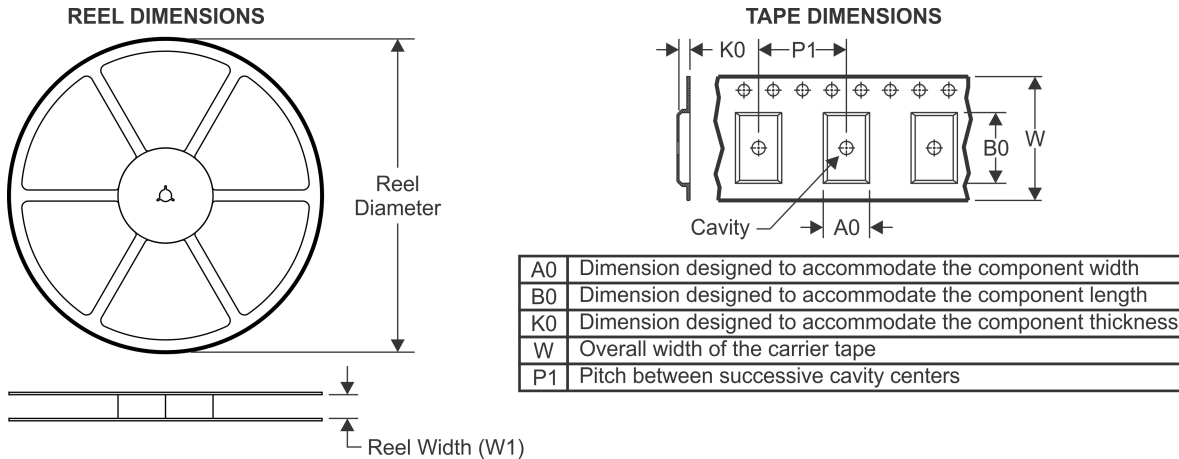
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

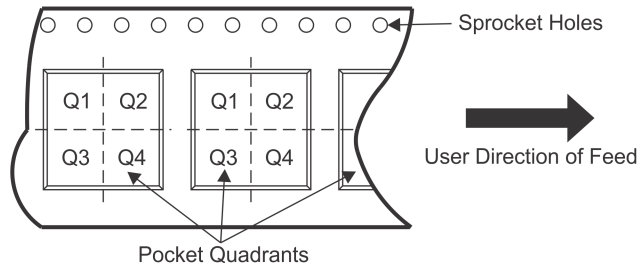
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TAPE AND REEL INFORMATION



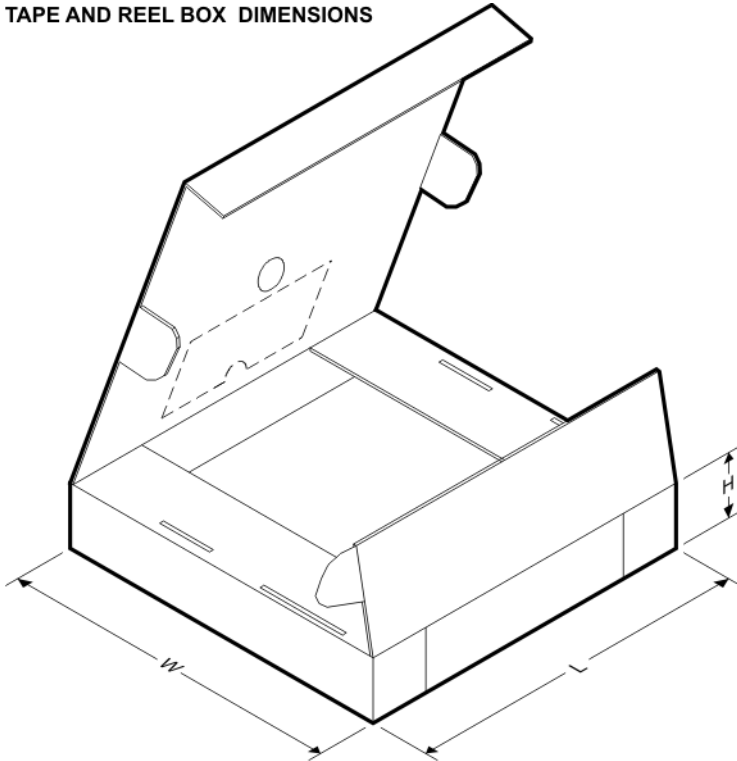
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP8556SQ-E00/NOPB | WQFN | RTW | 24 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP8556SQ-E08/NOPB | WQFN | RTW | 24 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP8556SQ-E09/NOPB | WQFN | RTW | 24 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP8556SQE-E00/NOPB | WQFN | RTW | 24 | 250 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP8556SQE-E08/NOPB | WQFN | RTW | 24 | 250 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP8556SQE-E09/NOPB | WQFN | RTW | 24 | 250 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP8556SQX-E00/NOPB | WQFN | RTW | 24 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP8556SQX-E08/NOPB | WQFN | RTW | 24 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP8556SQX-E09/NOPB | WQFN | RTW | 24 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP8556TME-E02/NOPB | DSBGA | YFQ | 20 | 250 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TME-E03/NOPB | DSBGA | YFQ | 20 | 250 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TME-E04/NOPB | DSBGA | YFQ | 20 | 250 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TME-E05/NOPB | DSBGA | YFQ | 20 | 250 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TME-E06/NOPB | DSBGA | YFQ | 20 | 250 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TME-E09/NOPB | DSBGA | YFQ | 20 | 250 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TME-E11/NOPB | DSBGA | YFQ | 20 | 250 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TMX-E02/NOPB | DSBGA | YFQ | 20 | 3000 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TMX-E03/NOPB | DSBGA | YFQ | 20 | 3000 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP8556TMX-E04/NOPB | DSBGA | YFQ | 20 | 3000 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TMX-E05/NOPB | DSBGA | YFQ | 20 | 3000 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TMX-E06/NOPB | DSBGA | YFQ | 20 | 3000 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TMX-E09/NOPB | DSBGA | YFQ | 20 | 3000 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |
| LP8556TMX-E11/NOPB | DSBGA | YFQ | 20 | 3000 | 178.0 | 8.4 | 1.83 | 2.49 | 0.76 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP8556SQ-E00/NOPB | WQFN | RTW | 24 | 1000 | 210.0 | 185.0 | 35.0 |
| LP8556SQ-E08/NOPB | WQFN | RTW | 24 | 1000 | 210.0 | 185.0 | 35.0 |
| LP8556SQ-E09/NOPB | WQFN | RTW | 24 | 1000 | 210.0 | 185.0 | 35.0 |
| LP8556SQE-E00/NOPB | WQFN | RTW | 24 | 250 | 210.0 | 185.0 | 35.0 |
| LP8556SQE-E08/NOPB | WQFN | RTW | 24 | 250 | 210.0 | 185.0 | 35.0 |
| LP8556SQE-E09/NOPB | WQFN | RTW | 24 | 250 | 210.0 | 185.0 | 35.0 |
| LP8556SQX-E00/NOPB | WQFN | RTW | 24 | 4500 | 367.0 | 367.0 | 35.0 |
| LP8556SQX-E08/NOPB | WQFN | RTW | 24 | 4500 | 367.0 | 367.0 | 35.0 |
| LP8556SQX-E09/NOPB | WQFN | RTW | 24 | 4500 | 367.0 | 367.0 | 35.0 |
| LP8556TME-E02/NOPB | DSBGA | YFQ | 20 | 250 | 210.0 | 185.0 | 35.0 |
| LP8556TME-E03/NOPB | DSBGA | YFQ | 20 | 250 | 210.0 | 185.0 | 35.0 |
| LP8556TME-E04/NOPB | DSBGA | YFQ | 20 | 250 | 210.0 | 185.0 | 35.0 |

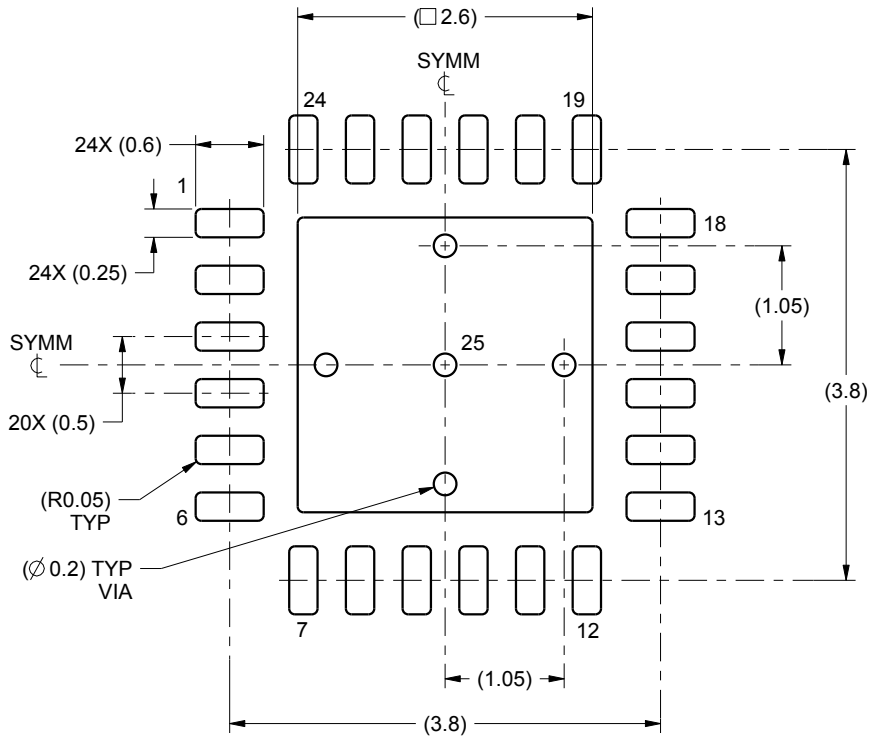
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP8556TME-E05/NOPB | DSBGA | YFQ | 20 | 250 | 210.0 | 185.0 | 35.0 |
| LP8556TME-E06/NOPB | DSBGA | YFQ | 20 | 250 | 210.0 | 185.0 | 35.0 |
| LP8556TME-E09/NOPB | DSBGA | YFQ | 20 | 250 | 210.0 | 185.0 | 35.0 |
| LP8556TME-E11/NOPB | DSBGA | YFQ | 20 | 250 | 210.0 | 185.0 | 35.0 |
| LP8556TMX-E02/NOPB | DSBGA | YFQ | 20 | 3000 | 210.0 | 185.0 | 35.0 |
| LP8556TMX-E03/NOPB | DSBGA | YFQ | 20 | 3000 | 210.0 | 185.0 | 35.0 |
| LP8556TMX-E04/NOPB | DSBGA | YFQ | 20 | 3000 | 210.0 | 185.0 | 35.0 |
| LP8556TMX-E05/NOPB | DSBGA | YFQ | 20 | 3000 | 210.0 | 185.0 | 35.0 |
| LP8556TMX-E06/NOPB | DSBGA | YFQ | 20 | 3000 | 210.0 | 185.0 | 35.0 |
| LP8556TMX-E09/NOPB | DSBGA | YFQ | 20 | 3000 | 210.0 | 185.0 | 35.0 |
| LP8556TMX-E11/NOPB | DSBGA | YFQ | 20 | 3000 | 210.0 | 185.0 | 35.0 |

EXAMPLE BOARD LAYOUT

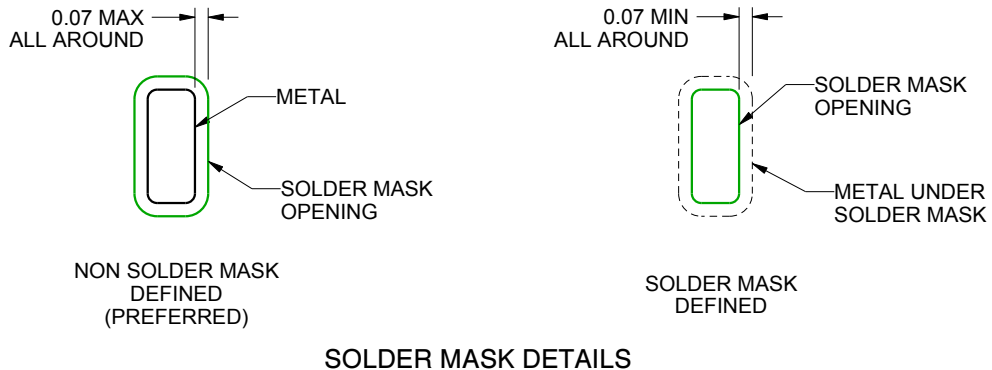
RTW0024A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

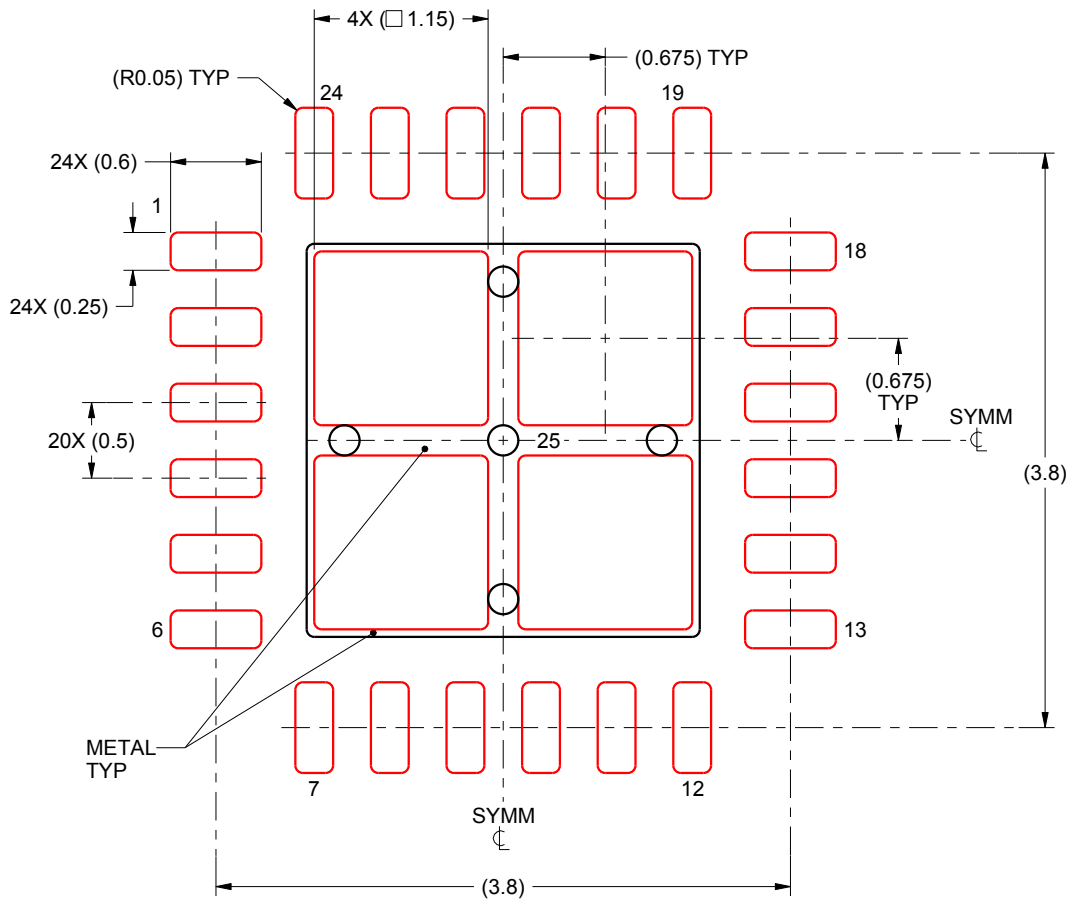
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RTW0024A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management