THE DATASHEET OF

IDT92HD71B7X5NLGXB3X8

www.win-source.net 0086-755-83957316

4-CHANNEL HD AUDIO CODEC OPTIMIZED FOR LOW POWER

92HD71B7

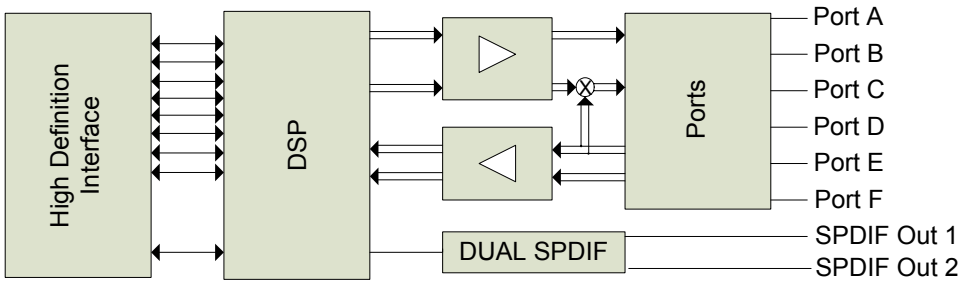
Description

The 92HD71B7 codec is a low power optimized, high fidelity, 4-channel audio codec compatible with Intel's High Definition (HD) Audio Interface. The 92HD71B7 codec provides stereo 24-bit resolution with sample rates up to 192kHz. Dual SPDIF provides connectivity to consumer electronic equipment that is WLP complaint. The 92HD71B7 provides high quality, HD Audio capability to notebook and business desktop PC applications.

Features

- **4 Channels (2 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
  - Supports full-duplex stereo audio and simultaneous VoIP
  - Provides a mono output for laptop sub-woofer
- **Microsoft WLP 3/4 premium logo compliant, as defined in WLP 3.09**
- **Optimized and flexible power management with pop/click mitigation**
- **2 independent S/PDIF Output converters for WLP compliant HDMI/SPDIF support.**
- **Support for 1.5V and 3.3V HDA signaling with runtime selection**
- **Digital microphone input (mono, stereo, or quad array)**
- **3 Adjustable VREF Out pins for microphone bias**
- **High performance analog mixer option**
- **6 analog ports**
- **Supports to 3 stereo microphone inputs**
- **Two-pin volume up/down control**
- **Digital PC Beep to all outputs**
- **Integrated headphone amp**
- **Jack insertion detection**
- **Sample rates up to 192kHz**
- **+3.3 V, +4 V, +4.75 V and +5 V analog power supply options**
- **48-pin QFP and 48-pad QFN RoHS packages**

Block Diagram



Software Support

- Intuitive graphical user interface that allows configurability and preference settings
- SKPI (Kernel Processing Interface)
  - Enables plug-ins that can operate globally on all audio streams of the system
- 12 band fully parametric equalizer (SKPI plug-in)
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- Dynamics Processing (SKPI plug-in)
  - Enables improved voice articulation
  - Compressor/limiter allows higher average noise level without resonances
- IDT Vista APO wrapper
  - Enables multiple APOs to be used with the IDT Driver
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- Dynamic Stream Switching
  - Improved multi-streaming user experience with less support calls
- Dolby PC Entertainment Experience Logo Program
  - Dolby Home Theater™ (HT)
  - Dolby Sound Room™ (SR)
- Dolby Technologies
  - Dolby Headphone™, Dolby Virtual Speaker™
  - Dolby ProLogic II™, Dolby ProLogic IIx™
  - Dolby Digital Live™ (DDL)
- Maxx Player™ from Waves
- WOW™ and Tru Surround™ from SRS

TABLE OF CONTENTS

1. DESCRIPTION 5
1.1. Overview 5
1.2. Orderable Part numbers 6
1.3. Block Diagram 6
1.4. Detailed Description 7
1.4.1. Low-voltage High Definition Audio Link Signaling 7
1.4.2. Port Functionality 7
1.4.3. Port Characteristics 7
1.4.4. Jack Detect 8
1.4.5. SPDIF Output 8
1.4.6. Mono Output 9
1.4.7. Analog Mixer 10
1.4.8. Input Multiplexers 10
1.4.9. ADC Multiplexers 10
1.4.10. Power Management 10
1.4.11. Multi-channel capture 11
1.4.12. EAPD 12
1.4.13. Digital Microphone Support 13
1.4.14. Analog PC-Beep 18
1.4.15. Headphone Drivers 18
1.4.16. GPIO 18
1.4.17. External Volume Control 19
2. CHARACTERISTICS 21
2.1. Electrical Specifications 21
2.1.1. Absolute Maximum Ratings 21
2.1.2. Recommended Operating Conditions 21
2.2. 92HD71B7 5V, 4.75V, and 3.3V Analog Performance Characteristics 22
3. PORT CONFIGURATION 27
4. FUNCTIONAL BLOCK DIAGRAM 28
5. WIDGET INFORMATION AND SUPPORTED COMMAND VERBS 29
5.1. Widget List 92HD71B 30
6. PIN CONFIGURATION DEFAULT REGISTER SETTINGS 31
7. WIDGET INFORMATION 32
8. SUPPORTED VERBS AND COMMANDS 33
8.1. Root Node (NID = 00) 33
8.1.1. Root VendorID 33
8.1.2. Root RevID 33
8.2. AFG Node (NID = 01 34
8.2.1. AFG Reset 34
8.2.2. AFG NodeInfo 34
8.2.4. AFG AFGCap 35
8.2.3. AFG FGType 35
8.2.5. AFG PCMCap 36
8.2.6. AFG StreamCap 37
8.2.7. AFG InAmpCap 38
8.2.8. AFG PwrStateCap 38
8.2.10. AFG OutAmpCap 39
8.2.9. AFG GPIOCnt 39
8.2.12. AFG UnsolResp 40
8.2.11. AFG PwrState 40
8.2.13. AFG GPIO 41
8.2.14. AFG GPIOEn 42
8.2.15. AFG GPIODir 43

8.2.16. AFG GPIOWakeEn 44
8.2.17. AFG GPIOUnsol 46
8.2.18. AFG GPIOSticky 48
8.2.19. AFG SubID 49
8.2.20. AFG GPIOPIrty 49
8.2.21. AFG GPIODrive 50
8.2.22. AFG DMic 51
8.2.23. AFG Misc. (B3 revision and beyond only) 52
8.3. Port A Node (NID = 0A) 53
8.3.1. PortA WCap 53
8.3.2. PortA PinCap 54
8.3.3. PortA ConLst 55
8.3.4. PortA ConLstEntry0 55
8.3.5. PortA ConSelectCtrl 56
8.3.6. PortA PinWCntrl 56
8.3.7. PortA UnsolResp 57
8.3.8. PortA ChSense 57
8.3.9. PortA InAmpLeft 58
8.3.10. PortA InAmpRight 58
8.3.11. PortA ConfigDefault 59
8.4. PortB Node (NID = 0B) 60
8.4.1. PortB WCap 60
8.4.2. PortB PinCap 61
8.4.3. PortB PinWCntrl 62
8.4.4. PortB UnsolResp 63
8.4.5. PortB ChSense 64
8.4.6. PortB ConfigDefault 64
8.5. Port C Node (NID = 0C) 65
8.5.1. PortC WCap 65
8.5.2. PortC PinCap 67
8.5.3. PortC PinWCntrl 68
8.5.4. PortC UnsolResp 68
8.5.5. PortC ChSense 69
8.5.6. PortC ConfigDefault 69
8.6. Port D Node (NID = 0D) 71
8.6.1. PortD WCap 71
8.6.2. PortD PinCap 72
8.6.3. PortD ConLst 73
8.6.4. PortD ConLstEntry0 73
8.6.5. PortD ConSelectCtrl 74
8.6.6. PortD PinWCntrl 74
8.6.7. PortD UnsolResp 75
8.6.8. PortD ChSense 75
8.6.9. PortD InAmpLeft 76
8.6.10. PortD InAmpRight 76
8.6.11. PortD ConfigDefault 77
8.7. PortE Node (NID = 0E) 78
8.7.1. PortE WCap 78
8.7.2. PortE PinCap 79
8.7.3. PortE PinWCntrl 80
8.7.4. PortE UnsolResp 81
8.7.5. PortE ChSense 82
8.7.6. PortE ConfigDefault 82
8.8. PortF Node (NID = 0F) 83
8.8.1. PortF WCap 83

8.8.2. PortF PinCap 85
8.8.3. PortF ConLst 86
8.8.4. PortF ConLstEntry0 86
8.8.5. PortF ConSelectCtrl 87
8.8.6. PortF PinWCntrl 87
8.8.7. PortF UnsolResp 87
8.8.8. PortF ChSense 88
8.8.9. PortF InAmpLeft 88
8.8.10. PortF InAmpRight 89
8.8.11. PortF ConfigDefault 89
8.9. DAC0 Node (NID = 10) 91
8.9.1. DAC0 WCap 91
8.9.2. DAC0 Cnvtr 92
8.9.3. DAC0 OutAmpLeft 93
8.9.4. DAC0 OutAmpRight 93
8.9.5. DAC0 PwrState 94
8.9.6. DAC0 CnvtrID 94
8.9.7. DAC0 LR 95
8.10. DAC1 Node (NID = 11) 95
8.10.1. DAC1 WCap 95
8.10.2. DAC1 Cnvtr 97
8.10.3. DAC1 OutAmpLeft 98
8.10.4. DAC1 OutAmpRight 98
8.10.5. DAC1 PwrState 99
8.10.6. DAC1 CnvtrID 99
8.10.7. DAC1 LR 100
8.11. ADC0 Node (NID = 12) 100
8.11.1. ADC0 WCap 100
8.11.2. ADC0 ConLst 101
8.11.3. ADC0 ConLstEntry0 102
8.11.4. ADC0 Cnvtr 102
8.11.5. ADC0 ProcState 103
8.11.6. ADC0 PwrState 104
8.11.7. ADC0 CnvtrID 104
8.12. ADC1 Node (NID = 13) 105
8.12.1. ADC1 WCap 105
8.12.2. ADC1 ConLst 106
8.12.3. ADC1 ConLstEntry0 107
8.12.4. ADC1 Cnvtr 107
8.12.5. ADC1 ProcState 108
8.12.6. ADC1 PwrState 109
8.12.7. ADC1 CnvtrID 109
8.13. MonoOut Node (NID = 14) 110
8.13.1. MonoOut WCap 110
8.13.2. MonoOut PinCap 111
8.13.3. MonoOut ConLst 112
8.13.4. MonoOut ConLstEntry0 112
8.13.5. MonoOut PinWCntrl 113
8.13.6. MonoOut InAmpLeft 113
8.13.7. MonoOut ConfigDefault 114
8.14. MonoMux Node (NID = 15) 115
8.14.1. MonoMux WCap 115
8.14.2. MonoMux ConLst 116
8.14.3. MonoMux ConLstEntry0 117
8.14.4. MonoMux ConSelectCtrl 117

8.15. MonoMixer Node (NID = 16) 118
8.15.1. MonoMixer WCap 118
8.15.2. MonoMixer ConLst 119
8.15.3. MonoMixer ConLstEntry0 120
8.16. InputMixer Node (NID = 17) 120
8.16.1. InputMixer WCap 120
8.16.2. InputMixer ConLst 121
8.16.3. InputMixer ConLstEntry4 122
8.16.4. InputMixer ConLstEntry0 122
8.16.5. InputMixer InAmpCap 123
8.16.6. InputMixer InAmpLeft0 124
8.16.7. InputMixer InAmpRight0 124
8.16.8. InputMixer InAmpLeft1 125
8.16.9. InputMixer InAmpRight1 125
8.16.10. InputMixer InAmpLeft2 126
8.16.11. InputMixer InAmpRight2 126
8.16.12. InputMixer InAmpLeft3 127
8.16.13. InputMixer InAmpRight3 127
8.16.14. InputMixer InAmpLeft4 128
8.16.15. InputMixer InAmpRight4 128
8.17. DMic0 Node (NID = 18) 129
8.17.1. DMic0 WCap 129
8.17.2. DMic0 PinCap 130
8.17.3. DMic0 PinWCntrl 131
8.17.4. DMic0 OutAmpCap 131
8.17.5. DMic0 OutAmpLeft 132
8.17.6. DMic0 OutAmpRight 132
8.17.7. DMic0 ConfigDefault 133
8.18. DMic1 Node (NID = 19) 134
8.18.1. DMic1 WCap 134
8.18.2. DMic1 PinCap 135
8.18.3. DMic1 PinWCntrl 136
8.18.4. DMic1 OutAmpCap 137
8.18.5. DMic1 OutAmpLeft 138
8.18.6. DMic1 OutAmpRight 138
8.18.7. DMic1 ConfigDefault 138
8.19. InPort0Mux Node (NID = 1A) 140
8.19.1. InPort0Mux WCap 140
8.19.2. InPort0Mux ConLst 141
8.19.3. InPort0Mux ConLstEntry0 141
8.19.4. InPort0Mux ConSelectCtrl 142
8.19.5. InPort0Mux OutAmpCap 142
8.19.6. InPort0Mux OutAmpLeft 143
8.19.7. InPort0Mux OutAmpRight 143
8.20. InPort1Mux Node (NID = 1B) 144
8.20.1. InPort1Mux WCap 144
8.20.2. InPort1Mux ConLst 145
8.20.3. InPort1Mux ConLstEntry0 146
8.20.4. InPort1Mux ConSelectCtrl 146
8.20.5. InPort1Mux OutAmpCap 146
8.20.6. InPort1Mux OutAmpLeft 147
8.20.7. InPort1Mux OutAmpRight 148
8.21. ADC0Mux Node (NID = 1C) 148
8.21.1. ADC0Mux WCap 148
8.21.2. ADC0Mux ConLst 149

8.21.3. ADC0Mux ConLstEntry0 150
8.21.4. ADC0Mux ConSelectCtrl 150
8.21.5. ADC0Mux LR 151
8.21.6. ADC0Mux OutAmpCap 151
8.21.7. ADC0Mux OutAmpLeft 152
8.21.8. ADC0Mux OutAmpRight 153
8.22. ADC1Mux Node (NID = 1D) 153
8.22.1. ADC1Mux WCap 153
8.22.2. ADC1Mux ConLst 154
8.22.3. ADC1Mux ConLstEntry0 155
8.22.4. ADC1Mux ConSelectCtrl 155
8.22.5. ADC1Mux LR 156
8.22.6. ADC1Mux OutAmpCap 156
8.22.7. ADC1Mux OutAmpLeft 157
8.22.8. ADC1Mux OutAmpRight 158
8.23. Dig0Pin Node (NID = 1E) 158
8.23.1. Dig0Pin WCap 158
8.23.2. Dig0Pin PinCap 159
8.23.3. Dig0Pin ConLst 160
8.23.4. Dig0Pin ConLstEntry0 161
8.23.5. Dig0Pin PinWCntrl 161
8.23.6. Dig0Pin ConfigDefault 162
8.24. Dig1Pin Node (NID = 1F) 163
8.24.1. Dig1Pin WCap 163
8.24.2. Dig1Pin PinCap 165
8.24.3. Dig1Pin ConLst 166
8.24.4. Dig1Pin ConLstEntry0 166
8.24.5. Dig1Pin ConSelectCtrl 167
8.24.6. Dig1Pin PinWCntrl 167
8.24.7. Dig1Pin PwrState 167
8.24.8. Dig1Pin EAPD 168
8.24.9. Dig1Pin ConfigDefault 168
8.25. Dig2Pin Node (NID = 20) 170
8.25.1. Dig2Pin WCap 170
8.25.2. Dig2Pin PinCap 171
8.25.3. Dig2Pin ConLst 172
8.25.4. Dig2Pin ConLstEntry0 172
8.25.5. Dig2Pin PinWCntrl 173
8.25.6. Dig2Pin ConfigDefault 173
8.26. SPDIFOut0 Node (NID = 21) 175
8.26.1. SPDIFOut0 WCap 175
8.26.2. SPDIFOut0 PCMCap 176
8.26.3. SPDIFOut0 StreamCap 177
8.26.4. SPDIFOut0 Cnvtr 178
8.26.5. SPDIFOut0 CnvtrID 179
8.26.6. SPDIFOut0 DigCnvtr 179
8.27. SPDIFOut1 Node (NID = 22) 180
8.27.1. SPDIFOut1 WCap 180
8.27.2. SPDIFOut1 PCMCap 181
8.27.3. SPDIFOut1 StreamCap 182
8.27.4. SPDIFOut1 Cnvtr 183
8.27.5. SPDIFOut1 CnvtrID 184
8.27.6. SPDIFOut1 DigCnvtr 184
8.28. Dig0Mux Node (NID = 24) 185
8.28.1. Dig0Mux WCap 185

8.28.2. Dig0Mux ConLst 187
8.28.3. Dig0Mux ConLstEntry0 187
8.28.4. Dig0Mux ConSelectCtrl 188
8.29. Dig2Mux Node (NID = 25) 188
8.29.1. Dig2Mux WCap 188
8.29.2. Dig2Mux ConLst 189
8.29.3. Dig2Mux ConLstEntry0 190
8.29.4. Dig2Mux ConSelectCtrl 190
8.30. DigBeep Node (NID = 26) 191
8.30.1. DigBeep WCap 191
8.30.2. DigBeep OutAmpCap 192
8.30.3. DigBeep OutAmpLeft 192
8.30.4. DigBeep Gen 193
8.30.5. DigBeep Mode 194
8.31. AnaBeep Node (NID = 27) 194
8.31.1. AnaBeep WCap 194
8.31.2. AnaBeep PinCap 195
8.31.3. AnaBeep PinWCntrl 196
8.31.4. AnaBeep ConfigDefault 197
8.32. VolumeKnob Node (NID = 28) 198
8.32.1. VolumeKnob WCap 198
8.32.2. VolumeKnob VolKnobCap 199
8.32.3. VolumeKnob ConLst 199
8.32.4. VolumeKnob ConLstEntry0 200
8.32.5. VolumeKnob UnsolResp 200
8.32.6. VolumeKnob Cntrl 201
8.32.7. VolumeKnob Update 201
9. DISCLAIMER 203
10. PINOUTS 204
10.1. Pin Assignment 204
10.2. Pin Descriptions 205
11. PACKAGE OUTLINE AND PACKAGE DIMENSIONS 207
11.1. 48-Pad QFN Package 207
11.2. 48-Pin QFP Package 208
12. SOLDER REFLOW PROFILE 209
12.1. Standard Reflow Profile Data 209
12.2. Pb Free Process - Package Classification Reflow Temperatures 210
13. REVISION HISTORY 211

LIST OF FIGURES

Figure 1. 92HD71B7 Block Diagram 11
Figure 2. System Diagram 11
Figure 3. Multi-channel capture 17
Figure 4. Multi-channel timing diagram 17
Figure 5. Single Digital Microphone (data is ported to both left and right channels 20
Figure 6. Stereo Digital Microphone Configuration 21
Figure 7. Quad Digital Microphone Configuration 22
Figure 8. Volume Knob 25
Figure 9. Port Configuration 32
Figure 10. 92HD71B7 Functional Block Diagram 33
Figure 11. 92HD71B Widget Diagram 34
Figure 12. Pin Assignment 208
Figure 13. 48-pad QFN Package Drawing 211
Figure 14. 48-pin QFP Package Drawing 212
Figure 15. Solder Reflow Profile 213

LIST OF TABLES

Table 1. Analog Output Port Behavior 13
Table 2. Jack Detect 13
Table 3. SPDIF OUT 0 (Pin 48) Behavior 14
Table 4. SPDIF OUT 1 (Pin 45) Behavior 14
Table 5. Power Managemen 16
Table 7. EAPD Behavior 18
Table 8. Valid Digital Mic Configurations 18
Table 9. DMIC_CLK and DMIC_0,1 Operation During Power States 19
Table 10. GPIO Pin mapping and shared functions 23
Table 11. Electrical Specification: Maximum Ratings 26
Table 12. Recommended Operating Conditions 26
Table 13. 92HD71B7 5V, 4.75V, and 3.3V Analog Performance Characteristics 27
Table 14. High Definition Audio Widget 35
Table 15. Pin Configuration Default Settings 36
Table 16. Command Format for Verb with 4-bit Identifier 37
Table 17. Command Format for Verb with 12-bit Identifier 37
Table 18. Solicited Response Format 37
Table 19. Unsolicited Response Format 37
Table 20. Pin Description 209
Table 23. Standard Reflow Profile 213
Table 24. Pb-Free Process Reflow 214

1. DESCRIPTION

1.1. Overview

The 92HD71B is a family of high fidelity, 4-channel audio codecs compatible with the Intel High Definition (HD) Audio Interface. The 92HD71B codecs provide high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

92HD71B variants:

PartNumber	*DAC SNR*	*# of Ports*	*Digital Mixer*	*Hi-Perf. Analog Mixer*
92HD71B8	103	6	Yes	Yes
92HD71B7	95	6	Yes	Yes
92HD71B5	95	4	Yes	No

The higher performance and quality of IDT's audio solutions brings consumer electronics level performance to notebook and desktop PCs. 92HD71B7 is designed to meet or exceed premium logo requirements for Microsoft's Windows Logo Program (WLP) 3.09 and revision 4 as indicated in WLP 3.09.

The 92HD71B7 provides stereo 24- bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. The 92HD71B7 SPDIF outputs support sample rates of 192kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz. Additional sample rates are supported by the driver software.

The 92HD71B7 supports a wide range of mobile and desktop 4 channel configurations. The 2 independent SPDIF output interfaces provide connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. Simultaneous WLP compliant HDMI and SPDIF output is possible. All analog input pairs support LINE_IN and MIC.

MIC inputs can be programmed with 0/10/20/30dB boost. (40dB boost is available using the IDT driver.) For more advanced configurations, the 92HD71B7 has up to 8 General Purpose I/O (GPIO).

The port presence detect capabilities allow the codecs to detect when audio devices are connected to the codec. The fully parametric IDT SoftEQ can be initiated or disabled upon headphone jack removal and insertion for protection of notebook speakers.

The 92HD71B7 operates with a 3.3V digital supply and either 3.3V, 4V, 4.75V or 5V analog supply. It can also work with 1.5V and 3.3V HDA signaling; the correct signalling level is selected dynamically based on the power supply voltage on the DVDD-IO pin.

Available in a 48-pin QFP or QFN Environmental (ROHS) packages.

1.2. Orderable Part numbers

92HD71B7X5PRGXyyX	6port, 95dB, 5V, 48QFP
92HD71B7X5NLGXyyX	6port, 95dB, 5V, 48QFN
92HD71B7X3PRGXyyX	6port, 95dB, 3.3V, 48QFP
92HD71B7X3NLGXyyX	6port, 95dB, 3.3V, 48QFN

yy = silicon stepping/revision, contact sales for current data.
Add an “8” to the end for tape and reel delivery. Min/Mult order quantitiy 2ku.

1.3. Block Diagram

Figure 1. 92HD71B7 Block Diagram

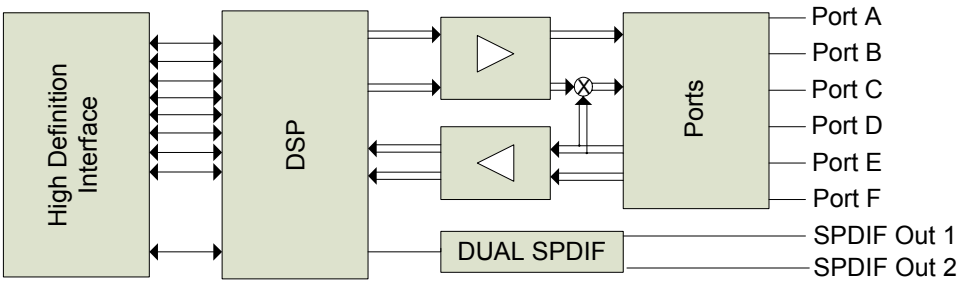
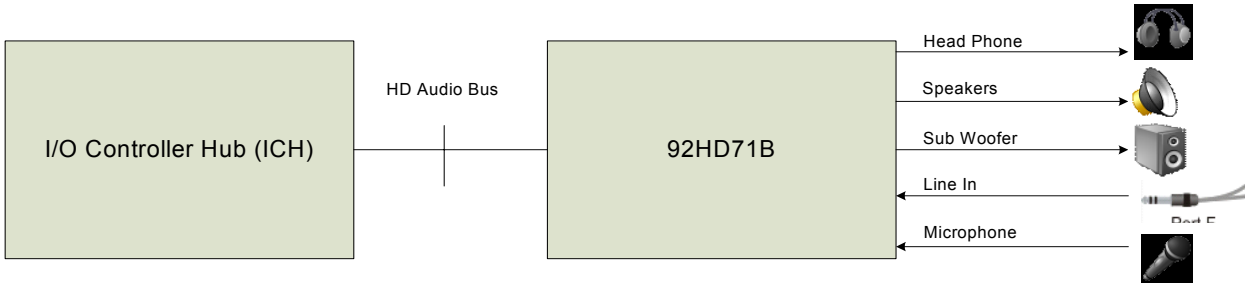


Figure 2. System Diagram



1.4. Detailed Description

1.4.1. Low-voltage High Definition Audio Link Signaling

The 92HD71B is compatible with either 1.5 V or 3.3 V High Definition Audio Link signaling; the voltage selection is performed dynamically based on the input voltage of DVDD_IO. Note that DVDD_IO is not a logic configuration pin but provides the digital power supply to be used for the High Definition Audio Link signals.

When in 1.5 V mode, the 92HD71B can correctly decode BITCLK, SYNC, RESET# and SDO because they operate at 1.5 V. Additionally, it will drive SDI_CODEC at 1.5 V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

1.4.2. Port Functionality

Single function (Input only / output only) ports allow for the highest possible performance.

- Port A supports
  - Headphone Out
  - Line Out
- Port D supports
  - Line Out
- Ports B and C support
  - Line In
  - Mic with 0/10/20/30/40 dB Mic boost[4]
- Mono Output cannot be reconfigured
- Port E supports
  - Line In
  - Mic with 0/10/20/30/40 dB Mic boost[4]
- Port F supports
  - Line Out

Note[4]: 40dB boost requires using the IDT driver. When the 40dB mic boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB MIC boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

1.4.3. Port Characteristics

Ports are designed to be dedicated inputs or outputs only. Universal (Bi-directional) jacks are not supported. Port A is designed to drive a set of 32 ohm (nominal) headphones or a 10K (nominal) load with on board shunt resistance as low as 20K ohms (typical - used to maintain coupling CAP bias.) Line Level outputs are intended to drive an external 10K speaker load (nominal) and an on board shunt resistor of 20-47K (nominal). However, applications may support load impedances of 5K ohms and above. Input ports are 47K impedance (nominal) at the pin.

DAC full scale outputs and intended full scale input levels are 1V rms. Line output ports and Head-on output ports on the 92HD71B7 may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing designs to use 92HD71B7, ensure that there are no conflicts between the output ports on 92HD71B7 and existing circuitry.

Table 1. Analog Output Port Behavior

AFG Power State	Output Enable	Mute	Port Behavior
D0-D2	1	0	Active - audio enabled
	1	1	Active - audio mute. Port drives silence
	0	-	Inactive -port is powered on (low output impedance) but drives silence only.
D3	-	-	Inactive (lower power) - Port keeps output coupling caps charged and has low output impedance (not necessarily the same as in D0) but consumes less power.

1.4.4. Jack Detect

Plugs inserted to a jack on Ports A, B, C, & D are detected using SENSE_A. Plugs inserted to a jack on Ports E & F are detected using SENSE_B. The following table summarizes the proper resistor tolerances for different analog supply voltages.

Table 2. Jack Detect

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance Pull-Up	Resistor Tolerance SENSE_A (If port D is used)	Resistor Tolerance SENSE_A (If port D is not used)	Resistor Tolerance SENSE_B
5V	1%	1%	1%	1%
4.75V	1%	1%	1%	1%
4V	0.50%	0.50%	1%	1%
3.3V	0.10%	0.10%	1%	1%

See reference design for more information on Jack Detect implementation.

1.4.5. SPDIF Output

All SPDIF Outputs can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

A second independant SPDIF Output is provided as an option for WLP compliant HDMI and SPDIF outputs. Its function is identical to the primary SPDIF output.

Table 3. SPDIF OUT 0 (Pin 48) Behavior

AFG Power State	RESET#	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
	De-Asserted (High)	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down enabled)
	De-Asserted (High)	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down enabled)
	De-Asserted (High)	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut0 data (internal pull-down enabled)

Table 4. SPDIF OUT 1 (Pin 45) Behavior

AFG Power State	RESET#	GPIO7 Enable	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
	De-Asserted (High)	Enabled	-	-	-	Active - Pin reflects GPIO7 configuration (internal pull-up enabled)
	De-Asserted (High)	Disabled	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut1 data (internal pull-down enabled)

1.4.6. Mono Output

The MONO Output is connected to pin 32 and has an independent mute (see the Widget listing for details). The MONO Output derives its input from the output of the summing node after the mono mux. The following sources are available for the mono pin:

DAC0 Output: When enabled (by using port connection list), both DAC0 Outputs are summed together.

DAC1 Output: When enabled (by using port connection list), both DAC1 Outputs are summed together.

Input Mixer: When enabled (by using mono mix connection list and DAC mixer), both mixer outputs are summed together.

The stereo inputs are scaled by -6dB and then summed to provide an output that is the average of the two inputs. The full scale output at mono out is designed to be about 0dBV. It is not possible to adjust to a +3dBV output level.

1.4.7. Analog Mixer

An analog mixer is available on the 92HD71B7. The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input.

The following inputs are available:

- DAC0
- DAC1
- Analog PC_Beep
- Inport0_Mux
- Inport1_Mux

1.4.8. Input Multiplexers

92HD71B7 implements 2 port input multiplexers. These multiplexers incorporate the microphone boost function (0, 10dB, 20dB, 30dB, and 40dB gain) as an output amp and allow a preselection of one of three possible inputs:

Port B

Port C

Port E

NOTE: Changing the Input multiplexer setting will affect both the analog mixer and the ADC.

1.4.9. ADC Multiplexers

92HD71B7 implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function (0 to +22.5dB gain in 1.5dB steps) as an output amp and allow a preselection of one of four possible inputs:

- DMIC 0
- DMIC1
- InPortMux (ADC0 selects inport0_mux / ADC1 selects inport1_mux)
- Mixer output

1.4.10. Power Management

The following table describes what functionality is active in each power state

The D3-default state is available for HD Audio compliance. The programmable values, exposed via vendor-specific settings, are under the IDT Device Driver control for further power reduction.

The default power state for the Audio Function Group after reset is D3-default..

Table 5. Power Managemen

D0	D1	D2[1]	D3	vendor specific	Function
On	Off	Off	Off	-	DAC
On	Off	Off	Off	-	D2S
On	Off	Off	Off	-	ADC
On	Off	Off	Off	-	ADC Volume Control
On	Off	Off	Off	-	Ref ADC
On	Off	Off	Off	-	Analog Clocks
On	On	Off	Off	-	VrefOut Pins
On	On	Off	Off	-	Input Boost
On	On	Off	Off	-	Analog mixer
On	On	Off	Off	-	Mixer Volumes
On	On	On	Low Drive[2]	Programmable	Lo Amp
On	On	On	Low Drive2	Programmable	HP Amps
On	On	On	Low Drive[3]	Programmable	VAG amp
On	On	On	On[4]	Programmable	Port Sense
On	On	On	On	Programmable[5]	Reference Bias generator
On	On	On	On	Programmable5	Reference Bandgap core
On	On	On	On[6]	-	AZ-Link

1.No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2.VAG is kept active when ports are disabled or in D2/D3. Ports A, D, F and mono may be powered down using vendor specific verbs.
3.VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
4. BITCLK must be active and both AVDD and DVDD must be available for Port Sense to operate.
5.Vendor specific bit for Ref Top controls VAG generator, Bandgap Reference, and Reference bias generator. Place part into D3 and power down all ports (using vendor specific verbs) before powering down Ref Top.
6.Obviously not active if BITCLK is not running (Controller in D3).

1.4.11. Multi-channel capture

The capability to assign multiple “ADC Converters” to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported and is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) must be used to create a multi-channel input stream. There are no restrictions regarding digital microphones.

The ADC Converters can be associated with a single stream as long the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries.” table.

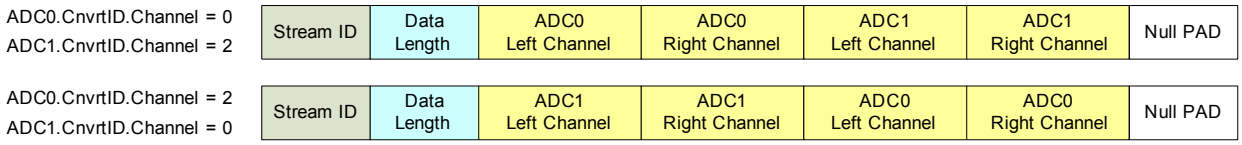
An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2 & 3 is shown below. A 4 Channel stream can be created by assigning the same non-zero

stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

Table 6: Example channel mapping

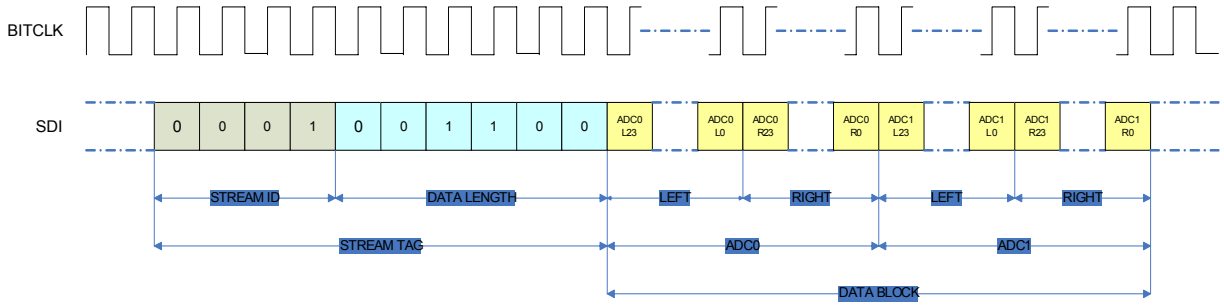
ADC1 CnvtrID	(NID = 0x08)	
	[3:0]	Ch = 2
ADC0 CnvtrID	(NID = 0x07)	
	[3:0]	Ch=0

Figure 3. Multi-channel capture



The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

Figure 4. Multi-channel timing diagram



1.4.12. EAPD

The EAPD pin (pin 47) also supports SPDIF and GPIO functions. The pin defaults to EAPD after power on reset and will remain in EAPD mode until either GPIO is enabled for pin 47 or the port I/O is enabled to support SPDIF. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up, and a 0 causes it to power down. When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value may remain 1. The default state of this pin is 0 (driving low) and a Pull-down prevents the line from floating high when the part is in reset.

Table 7. EAPD Behavior

AFG Power State	RESET#	GPIO Enable	Output Enable	EAPD Power State	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
	De-Asserted (High)	Enabled	-	-	Active - Pin reflects GPIO0 configuration (internal pull-up enabled)
	De-Asserted (High)	Disabled	Enabled	-	Active - Pin Drives SPDIFOut0/1 output (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D2-D3	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D0-D1	Active - Pin drives the value of the EAPD bit (internal pull-down enabled)

1.4.13. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0, DMIC1, and DMIC_CLK 3-pin interface. The DMIC0 and DMIC1 signals are inputs that carry individual channels of digital Mic data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the 24Mhz internal clock. The default frequency is 2.352Mhz.

92HD71B7 supports the following digital microphone configurations:

Table 8. Valid Digital Mic Configurations

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones

Table 8. Valid Digital Mic Configurations

Digital Mics	Data Sample	ADC Conn.	Notes
1	Single Edge	0, or 1	Available on either DMIC_0 or DMIC_1 Both ADC Channels produce data, may be in phase or out by 1/2 DMIC_CLK period depending upon external configuration and timing
2	Double Edge on either DMIC_0 or 1 OR Single Edge on DMIC_0 and 1	0, or 1	Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. If both DMIC_0 and DMIC_1 are used to support 2 digital microphones, 2 separate ADC units will be used, however, this configuration is not recommended since it consumes two stereo ADC resources.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0, or 1	Requires both DMIC_0 AND DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration
4	Double Edge	0, or 1	Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration

Table 9. DMIC_CLK and DMIC_0,1 Operation During Power States

Power State	DMIC Widget Enabled?	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D1	Yes	Clock Disabled	Input Disabled	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D2	Yes	Clock Disabled	Input Disabled	DMIC_CLK Remains Low
D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK Remains Low
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down

Figure 5. Single Digital Microphone (data is ported to both left and right channels

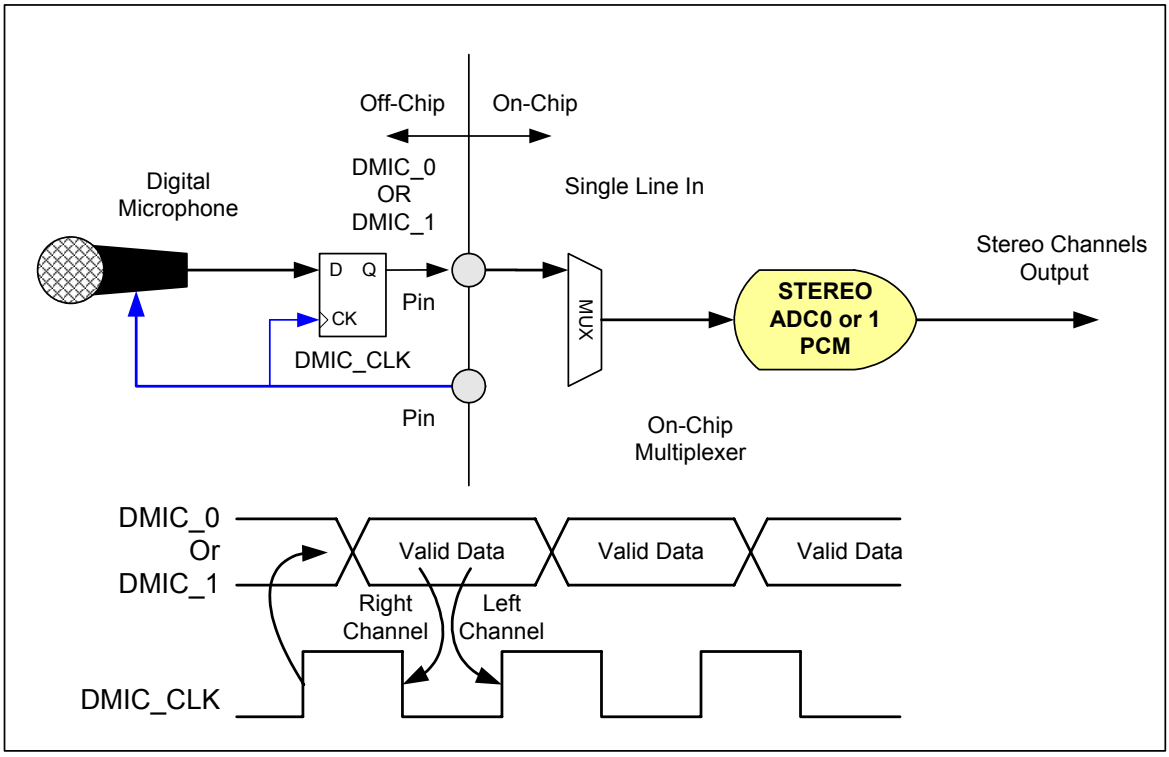
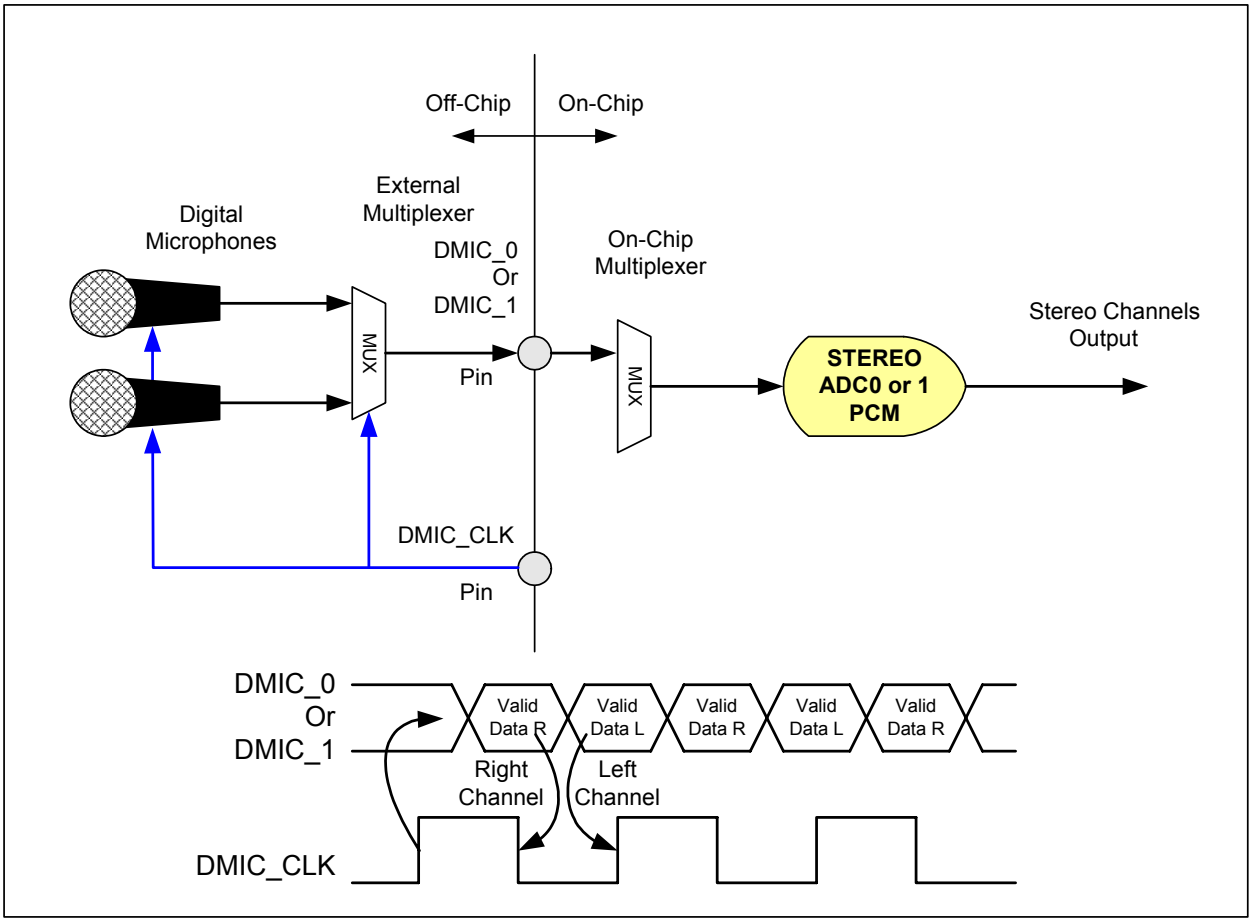
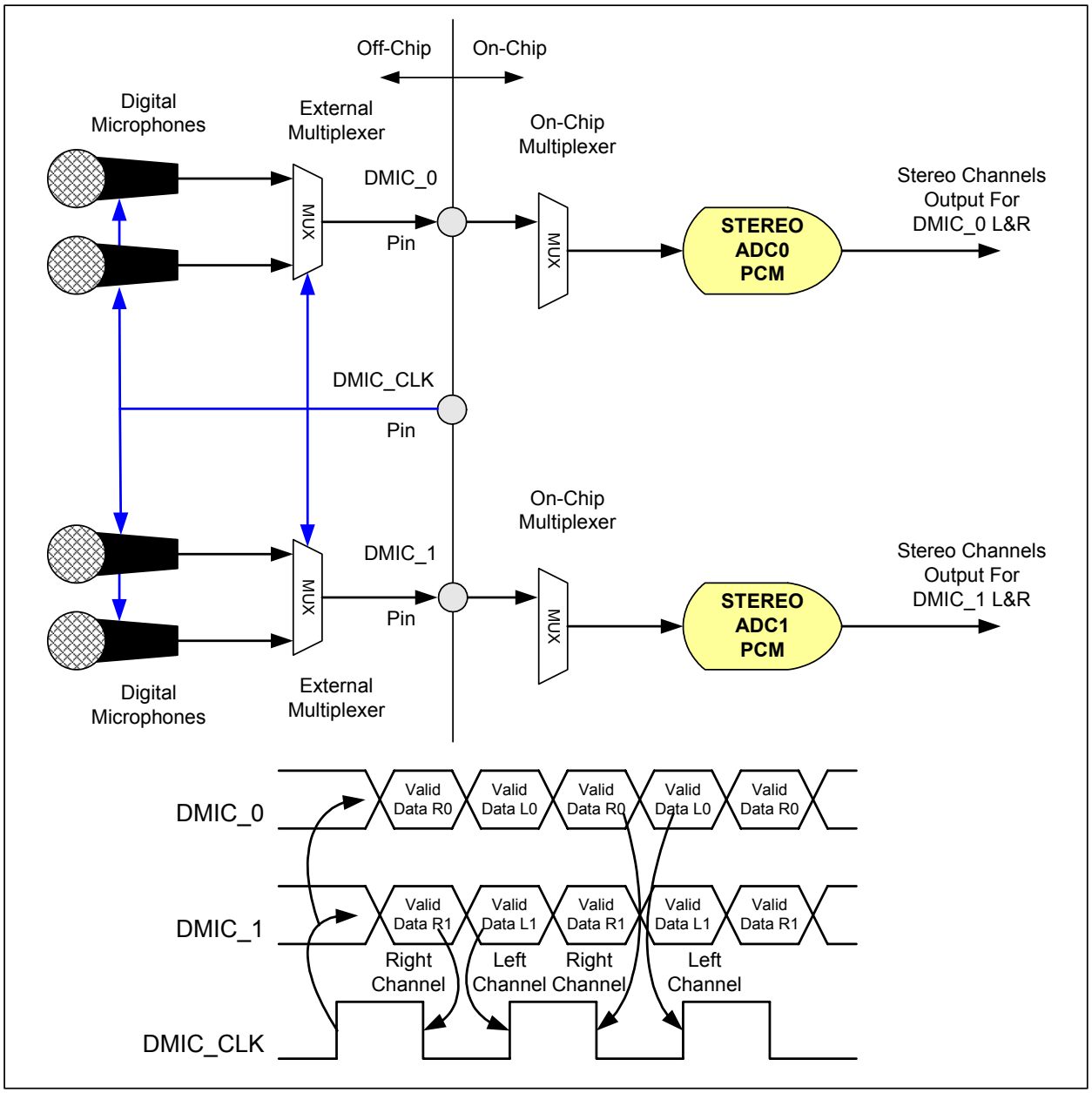


Figure 6. Stereo Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

Figure 7. Quad Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

1.4.14. Analog PC-Beep

92HD71B7 does not support automatic routing of the PC_Beep pin to all outputs when the link is in reset. Analog PC-Beep may be supported during Link Reset if the mixer is present and manually configured for pass-thru. Reset# must be high and Bit_Clk active. Analog PC_Beep is available as an input to the analog mixer.

1.4.15. Headphone Drivers

This product implements a +3dBV output option on headphone capable ports. (HP output and line output levels are defined as 1Vrms with an option to enable +3dBV FSOV using a vendor specific verb.)

1.4.16. GPIO

1.4.16.1. GPIO Pin mapping and shared functions.

Table 10. GPIO Pin mapping and shared functions

GPIO #	Pin	Supply	SPDIF In	SPDIF Out	GPI/O	GPI	GPO	VrefOut	ADAT	DMIC	VOL	Pull Up	Pull Down
1	2	DVDD			YES					YES	YES	50K (GPIO/VOL)	50K (DMIC)
2	4	DVDD			YES					YES	YES	50K (GPIO/VOL)	50K (DMIC)
3	30	AVDD			YES							50K[1]	
4	31	AVDD			YES			YES					
5	43	DVDD			YES							50K<superscript>1	
6	44	DVDD			YES							50K<superscript>1	
7	45	DVDD		YES	YES							50K (GPIO)	50K1 (SPDIF)
0	47	DVDD		YES	YES							50K (GPIO)	50K1 (SPDIF/EAPD)

1.Default condition.

1.4.16.2. Volume/Digital Microphone/GPIO Selection

To determine which function is actually enabled on pins2 and 4, the order of precedence is followed:

1) If the GPIOs are enabled, they override both Volume Control and Digital Mics

2) If the GPIOs are not enabled through the AFG, then at reset, the Volume control is enabled with the weak pull-up.

3) If BIOS or other software application enables either Digital Microphones inputs through the Configuration Default Register, the Volume is disconnected and the pull-ups are disconnected with the weak pull-downs enabled.

1.4.16.3. VRefOut/GPIO Selection

Two functions are available on pin 31. To determine which function is actually enabled, the order of precedence is followed:

1) If the GPIO4 function is enabled, it overrides VRefOut-E

2) If the GPIO4 function is not enabled through the AFG, then, at reset the VrefOut-E is enabled.

3) If using pin 31 as GPIO, make sure to incorporate a 10K ohm external pull-up to AVDD to prevent the pin from floating in GPI mode and to allow proper operation in open-drain GPO mode.

1.4.17. External Volume Control

92HD71B7 incorporates a 2-pin volume control interface. Volume up, down, and mute functions are easily implemented using 2 push-button switches. The CODEC provides internal pull-up resistors simplifying external CODEC circuitry. Also, repeat and direct modes of operation add flexibility to the interface. The typical usage model is for front panel master volume buttons on an entertainment PC, or case mounted hardware volume control for mobile platforms.

1.4.17.1. Theory of Operation

The codec monitors the volume up/down inputs for a change of state from high to low, and waits for the inputs to settle. If the inputs have not settled by the end of the de-bounce period, then the value at the end of the period is used. A 0 (low voltage) on the Down pin will decrement the volume register, while a 0 on the Up pin will increment the volume register. If both inputs are 0 at the same time, then the volume register will be set to its lowest value (mute). Pressing Up, Down, or both buttons at the same time when the volume control interface is in mute mode, will cause the part to un-mute.

The de-bounce / repeat rate is selectable from 2.5Hz to 20Hz in 2.5Hz increments using the Volume Knob VCSR0 verb (FE0) Rate bits (bits 2:0). This value is used for both de-bounce and repeat rates. The de-bounce period is the time that the CODEC waits for the inputs to settle, and the repeat rate is the rate at which the CODEC will increment/decrement the volume if a volume button is pushed and held. When a falling edge is detected on either one of the volume control pins, the codec will wait for (1/Rate) seconds for the input to settle. If the Continuous bit is set in the Volume Knob VCSR0 verb (bit 3), then the codec will wait for the de-bounce period to expire then repeatedly increment or decrement the volume register at the rate specified in the Rate bits until the button is released.

1.4.17.2. Modes of Operation

- DIRECT MODE
  - In Direct mode, the Volume Knob widget directly controls the volume of all of the DACs in the part. The volume in the Volume Knob widget acts as the master volume and limits the maximum volume for each of the DAC amplifiers. The amp gain for each of the DACs can also be adjusted using the DAC amplifiers. However, the actual gain for an individual DAC will be the sum of the Volume Knob volume and the DAC amplifier volume. For example, if the DAC amplifier gain is set to 0x7F (0dB) and the Volume Knob volume is set to 0x3F (-48dB) the resulting gain would be -48dB. If the combination of gains is less than -95.25dB

(the equivalent to a value of 0x0 for the DAC or Volume Knob volume settings) then the actual gain will be -95.25dB. For example, if the Volume Knob is set to 0x3F (-48dB) and the DAC amplifier volume is set to 0x1F (-72dB) then the DAC volume will be set to -95.25dB.

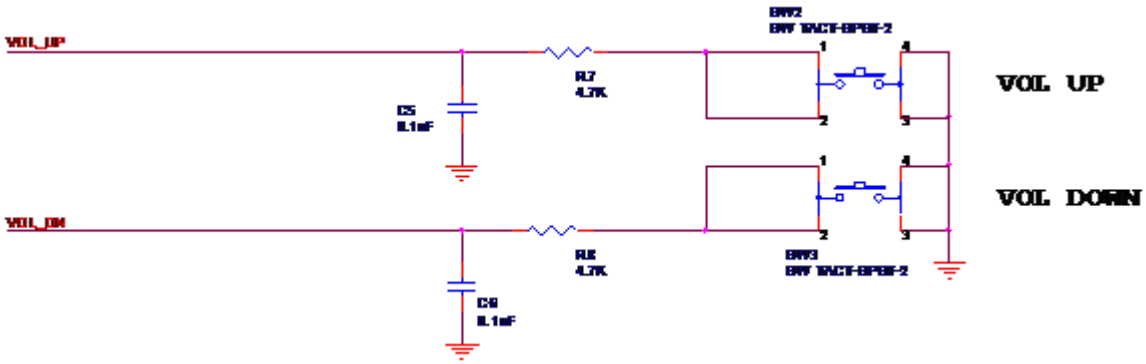
- Direct mode is enabled by setting bit 7 in the Volume Knob Cntrl verb (F0F). The volume is reflected in the Volume Knob Cntrl bits 6:0 and the step size is 0.75dB. In direct mode, software can read or write the volume in the Volume Knob widget.

- INDIRECT MODE
  - In indirect mode, the Volume Knob widget does not directly control the DAC amplifier gains. An event on the volume Up/Down pins will increment/decrement the value in the Volume Knob Cntrl verb (F0F) volume bits (bits 6:0) just as in Direct mode. However, instead of adjusting the DAC amplifier gain, an unsolicited response is generated (if enabled) and the control software must read the volume in the Volume Knob widget and take appropriate action. Indirect mode is particularly useful when it is undesirable to control all of the DAC amplifier volumes at the same time, or when implementing ADC volume control.
  - In indirect mode, there are only 128 volume levels in the Volume Knob Cntrl volume bits, the value will not go beyond the lower and upper limits (0x0 or 0x7F), and an unsolicited response will not be generated if an input event tries to go beyond these limits. Therefore, it is the responsibility of the controlling software to monitor the volume in the Volume Knob Widget and take appropriate action.
  - Indirect mode is enabled by clearing bit 7 in the Volume Knob Cntrl verb (F0F). The volume is reflected in the Volume Knob Cntrl bits 6:0 and the step size is 0.75dB. In direct mode, software can read or write the volume in the Volume Knob widget.

1.4.17.3. Hardware Implementation

The Volume Knob interface is comprised of two input pins, CODEC pins 2 and 4. Both pins have internal pull-up resistors, so only two push button switches are required for most implementations. Typically, a series resistor and shunt capacitor are used to help reduce noise and prevent damage from ESD and other potential faults. An example circuit is shown below.

Figure 8. Volume Knob



2. CHARACTERISTICS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 92HD71B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 11. Electrical Specification: Maximum Ratings

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0 ^{o}C to +70 ^{o}C
Storage temperature		-55 ^{o}C to +125 ^{o}C
Soldering temperature		Soldering temperature information for all available in the package section of this datasheet.

2.1.2. Recommended Operating Conditions

Table 12. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: With Supply Override Enable Bit set to force 5 V operation.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 4.5 V	4.51	4.75	4.99	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C
	T_{case} (48-QFN)			+95	°C

ESD: The 92HD71B is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the 92HD71B implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.2. 92HD71B7 5V, 4.75V, and 3.3V Analog Performance Characteristics

(Tambient = 25 ºC, AVdd = Supply ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 20Hz to 20KHz swept sinusoidal input; Sample Frequency = 48 kHz; 0 dB = 1 VRMS, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Table 13. 92HD71B7 5V, 4.75V, and 3.3V Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Digital to Analog Converters						
Resolution		All		24		Bits
Dynamic Range[1]: PCM to All Analog Outputs	-60dB FS signal level	5V 4.75V 3.3V	90 90 85	95 95 90	-	dB
SNR[2] - DAC to All Line-Out Ports	Analog Mixer Disabled, PCM data	5V 4.75V 3.3V	90 90 85	95 95 90		dB
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Disabled, -1dB FS Signal, PCM data	5V 4.75V 3.3V	80 80 80	83 82 84		dBr
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Disabled,-3dB FS Signal, PCM data	5V 4.75V 3.3V	80 80 80	83 82 84		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 10KΩ load, PCM data	5V 4.75V 3.3V	80 80 80	83 83 83		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, -1dB FS Signal, 10KΩ load, PCM data	5V 4.75V 3.3V	80 80 80	83 82 84		dBr
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, -3dB FS Signal, 10KΩ load, PCM data	5V 4.75V 3.3V	80 80 80	83 82 84		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 32Ω load, PCM data	5V 4.75V 3.3V	90 90 85	95 95 90		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, -1dB FS Signal, 32Ω load, PCM data	5V 4.75V 3.3V	70 68 68	78 76 73		dBr
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, -3dB FS Signal, 32Ω load, PCM data	5V 4.75V 3.3V	70 68 68	78 76 73		dBr

Table 13. 92HD71B7 5V, 4.75V, and 3.3V Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Any Analog Input (ADC) to DAC Crosstalk	10KHz Signal Frequency VREF_OUT=80%, BOOST=0dB, 10k load	All	-	-100	-	dB
Any Analog Input (ADC) to DAC Crosstalk	1KHz Signal Frequency VREF_OUT=80%, BOOST=0dB, 10k load	All	-	-100	-	dB
DAC L/R crosstalk	DAC to LO or HP 20-15KHz into 10KΩ load	All	65	75		dB
DAC L/R crosstalk	DAC to HP 20-15KHz into 32Ω load	All	65	70		dB
Gain Error	Analog Mixer Disabled	All			0.5	dB
Interchannel Gain Mismatch	Analog Mixer Disabled	All			0.5	dB
D/A Digital Filter Pass Band[4]		All	20	-	21,000	Hz
D/A Digital Filter Transition Band		All	21,000	-	31,000	Hz
D/A Digital Filter Stop Band		All	31,000	-	-	Hz
D/A Digital Filter Stop Band Rejection[5]		All	-100	-	-	dB
D/A Out-of-Band Rejection[6]		All	-55	-	-	dB
Group Delay (48KHz sample rate)		All	-	-	1	ms
Attenuation, Gain Step Size DIGITAL		All	-	0.75	-	dB
DAC Offset Voltage		All	-	10	20	mV
Deviation from Linear Phase		All	-	10	1	deg.
Analog Outputs						
Full Scale All Line-Outs + HP	DAC PCM Data	5V 4.75V 3.3V	1.00 1.00 0.707	1.07 1.07 0.758	-	Vrms
Full Scale All Line-Outs + HP	DAC PCM Data	5V 4.75V 3.3V	2.83 2.83 2.00	3.03 3.03 2.14	-	Vp-p
All Headphone Capable Outputs	32Ω load	5V 4.75V 3.3V	40 40 31	60 60 42	-	mW (peak)
Amplifier output impedance	Line Outputs Headphone Outputs	All		150 0.1		Ohms
Analog inputs						
Full Scale Input Voltage	0dB Boost @4.75V (input voltage required for 0dB FS output)	5V 4.75V 3.3V	1.00 1.00 0.707	1.03	-	Vrms
All Analog Inputs with boost	10dB Boost	5V 4.75V 3.3V	0.31	-	-	Vrms

Table 13. 92HD71B7 5V, 4.75V, and 3.3V Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
All Analog Inputs with boost	20dB Boost	5V 4.75V 3.3V	0.10	-	-	Vrms
All Analog Inputs with boost	30dB Boost	5V 4.75V 3.3V	0.03	-	-	Vrms
All Analog Inputs with boost	40dB Boost	5V 4.75V 3.3V	0.01	-	-	Vrms
Input Impedance		All	-	50	-	KΩ
Input Capacitance		All	-	15	-	pF
Analog Mixer						
SNR[2] - All Line-In to A D & F Line-Outs		5V 4.75V 3.3V	84	90		dB
THD+N[3] - All Line-In to A D & F Line-Out	0dBFS Input	5V 4.75V 3.3V	65	77		dBr
SNR[2] - DAC to All Line-Out Ports	Analog Mixer Enabled, PCM data	5V 4.75V 3.3V	88 86 83	90 88 85		dB
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Enabled, -1dB FS Signal, PCM data	5V 4.75V 3.3V	74 72 70	79 78 75		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Enabled, 10KΩ load, PCM data	5V 4.75V 3.3V	88 86 83	90 88 85		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Enabled, -1dB FS Signal, 10KΩ load, PCM data	5V 4.75V 3.3V	76 74 71	79 77 74		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Enabled, 32Ω load, PCM data	5V 4.75V 3.3V	86 84 81	89 87 84		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Enabled, -1dB FS Signal, 32Ω load, PCM data	5V 4.75V 3.3V	64 62 59	72 70 67		dBr
Attenuation, Gain Step Size ANALOG		All	-	1.5	-	dB
Gain Drift[7]		All	-	100	-	ppm/ºC
Analog to Digital Converter						
Resolution		All		24		Bits
Dynamic Range[1], All Analog Inputs to A/D	High Pass Filer Enabled, -60dB FS, No boost	5V 4.75V 3.3V	86 86 80	88 88 85		dB

Table 13. 92HD71B7 5V, 4.75V, and 3.3V Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
SNR[2] - All Analog Inputs to A/D	High Pass Filter enabled	5V 4.75V 3.3V	86 86 80	88 88 85		dB
THD+N All Analog Inputs to A/D	High Pass Filter enabled, -1dB FS signal level	5V 4.75V 3.3V	78 75 65	82 79 71		dBr
THD+N All Analog Inputs to A/D	High Pass Filter enabled, -3dB FS signal level	5V 4.75V 3.3V	78 78 65	83 83 73		dBr
Analog Frequency Response[8]		All	10	-	30,000	Hz
A/D Digital Filter Pass Band4		All	20	-	21,000	Hz
A/D Digital Filter Transition Band		All	21,000	-	31,000	Hz
A/D Digital Filter Stop Band		All	31,000	-	-	Hz
A/D Digital Filter Stop Band Rejection5		All	-100	-90	-	dB
Group Delay	48 KHz sample rate	All	-	-	1	ms
Any unselected analog Input to ADC Crosstalk	10KHz Signal Frequency VREF_OUT=80%, BOOST=0dB	All	-65	-80	-	dB
Any unselected analog Input to ADC Crosstalk	1KHz Signal Frequency VREF_OUT=80%, BOOST=0dB	All	-65	-85	-	dB
ADC L/R crosstalk	Any selected input to ADC 20-15Khz	All	-65	-73		dB
DAC to ADC crosstalk	Any DAC output to ADC 20-15Khz VREF_OUT=80%, BOOST=0dB, 32Ω load	All	-65	-78		dB
Spurious Tone Rejection[9]		All	-	-100	-	dB
Attenuation, Gain Step Size (analog)		All	-	1.5	-	dB
Gain Drift		All	-	100	-	ppm/ºC
Interchannel Gain Mismatch ADC		All	-	-	0.5	dB
40dB Mic Boost Enabled SNR	5mV Input	All		60		dB
40dB Mic Boost Enabled THD+N	5mV Input	All		55		dB
Power Supply[10]						
Power Supply Rejection Ratio	10kHz	All	-	-60	-	dB
Power Supply Rejection Ratio	1kHz	All	-	-70	-	dB
D0 Didd (Stereo Stream)	3.3V		-	43	-	mA
D0 Aidd (Stereo Stream)	5.0V, 4.75V, & 3.3V		-	31	-	mA
D0 Didd (All converters/ports enabled)	3.3V		-	39	-	mA
D0 Aidd (All converters/ports enabled)	5.0V, 4.75V, & 3.3V		-	53	-	mA

Table 13. 92HD71B7 5V, 4.75V, and 3.3V Analog Performance Characteristics

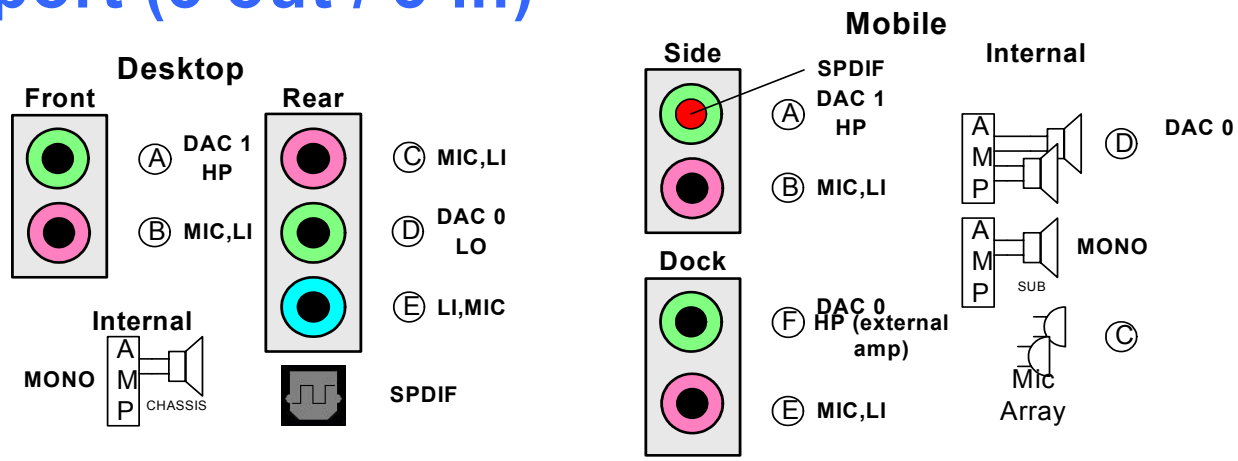
Parameter	Conditions	AVdd	Min	Typ	Max	Unit
D1 Didd	3.3V		-	13	-	mA
D1 Aidd	5.0V, 4.75V, & 3.3V		-	25	-	mA
D2 Didd	3.3V		-	13	-	mA
D2 Aidd	5.0V, 4.75V, & 3.3V		-	18	-	mA
D3 Didd	3.3V		-	10	-	mA
D3 Aidd	5.0V, 4.75V, & 3.3V		-	8	-	mA
Voltage Reference Outputs						
VREFOut[11]		All	-	0.5 X AVdd	-	V
VREFILT (VAG)		All		0.45 X AVdd		V
Phased Locked Loop						
PLL lock time		All		96	200	usec
PLL (or Azalia Bit CLK) 24MHz clock jitter		All		150	500	psec
ESD / Latchup						
Latch-up	As described in JESD78A Class II	All		70		degC
ESD - Human Body Model	As described in JESD22-A114-B	All	2K	3K		V
Charged Device Model	As described in JESD22-C101	All	500	1K		V

1.Dynamic Range is the ratio of the full scale signal to the noise output with a -60dBFS signal as defined in AES17 as SNR in the presence of signal and outlined in AES6id, measured “A weighted” over 20 Hz to 20 kHz bandwidth.
2.Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
3.THD+N ratio as defined in AES17 and outlined in AES6id,non-weighted, over 20 Hz to 20 kHz bandwidth.Results at the jack are dependent on external components and will likely be 1 - 2dB worse.
4.Peak-to-Peak Ripple over Passband meets ± 0.125dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.
5.Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
6.The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.
7.Gain drift is the change in analog volume control gain for each step across the supported 0 ^{o}C TO 70 ^{o}C temperature range referenced to the 25 ^{o}C gain value and specified in ppm per ^{o}C
8.± 1dB limits for Line Output & 0 dB gain, at -20dBV
9.Spurious tone rejection is tested with ADC dither enabled and compared to ADC performance without dither.
10.Does not include 32Ω load headphone power.
11.Can be set to 0.5 or 0.8 AVdd.

3. PORT CONFIGURATION

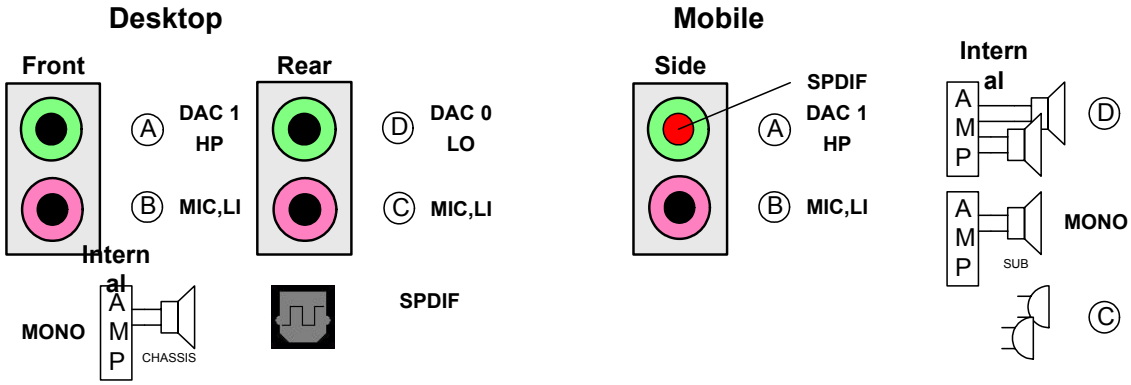
Figure 9. Port Configuration

6-port (3 out / 3 in)



2 stereo DACS / 2 stereo ADCs, dedicated inputs and outputs (no UJ) but inputs support line and mic functions. 4, 5, or 6 stereo ports + mono out. One or two SPDIF outputs. ONLY ONE HEADPHONE PORT Option for analog mixing of inputs. DAC output can be mixed with inputs for record or playback when mixer is present.
No volume control on mono output. Volume is the same as Port D.

4-port (2 out / 2 in)



4. FUNCTIONAL BLOCK DIAGRAM

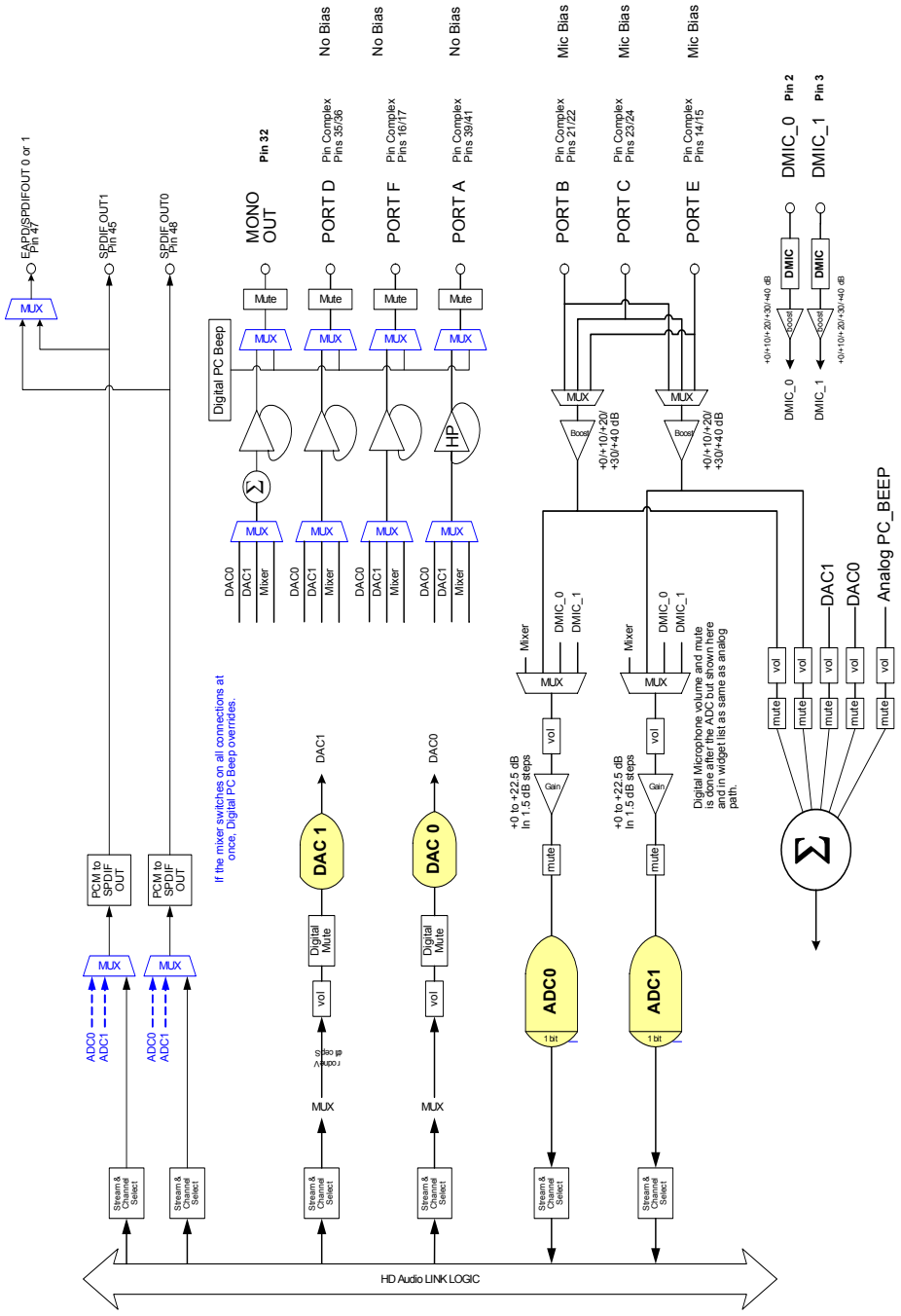


Figure 10. 92HD71B7 Functional Block Diagram

5. WIDGET INFORMATION AND SUPPORTED COMMAND VERBS

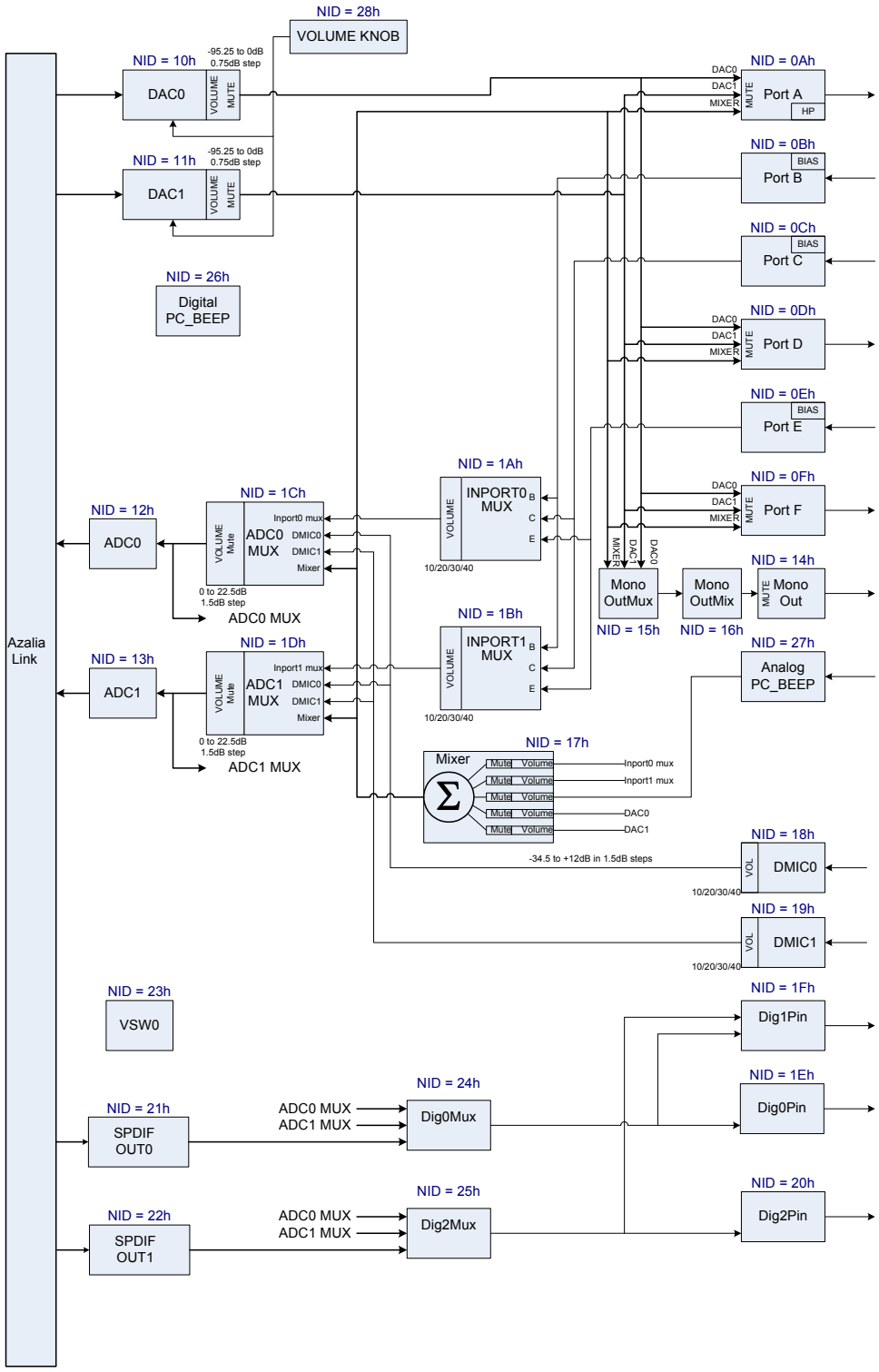


Figure 11. 92HD71B Widget Diagram

5.1. Widget List 92HD71B

Table 14. High Definition Audio Widget

ID	Widget Name	Description
00h	Root	Root Node
01h	AFG	Audio Function Group
0Ah	Port A	Port A Pin Widget (Configurable as HP, Line Out)
0Bh	Port B	Port B Pin Widget (Configurable as Line In, Mic)
0Ch	Port C	Port C Pin Widget (Configurable as Line In, Mic)
0Dh	Port D	Port D Pin Widget (Configurable as Line Out)
0Eh	Port E	Port E Pin Widget (Configurable as Line In, Mic)
0Fh	Port F	Port F Pin Widget (Configurable as Line Out)
10h	DAC0	Stereo Output Converter to DAC
11h	DAC1	Stereo Output Converter to DAC
12h	ADC0	Stereo Input Converter to ADC
13h	ADC1	Stereo Input Converter to ADC
14h	Port MonoOut	Port MonoOut Pin Widget (output only)
15h	MonoOutMux	Mono output source selector
16h	MonoOutMix	Port MonoOut Mixer
17h	Input Mixer	Input Mixer (Input Ports, DACs, Analog PC_Beep)
18h	DigMic0	Digital Microphone 0 Pin Widget
19h	DigMic1	Digital Microphone 1 Pin Widget
1Ah	InPort0Mux	Input port pre-select for ADC0 (also for mixer)
1Bh	InPort1Mux	input port pre-select for ADC1 (also for mixer)
1Ch	ADC0Mux	ADC0 Mux with volume and mute
1Dh	ADC1Mux	ADC1 Mux with volume and mute
1Eh	Dig0Pin	Digital Output Pin (pin48)
1Fh	Dig1Pin	EAPD and tertiary Digital Output Pin (pin 47)
20h	Dig2Pin	Secondary Digital Output Pin (Pin 45)
21h	SPDIFOut0	Stereo Output for SPDIF_Out
22h	SPDIFOut1	Second Stereo Output for SPDIF_Out
23h	Vendor Reserved	Vendor Reserved
24h	Dig0Mux	Digital Output mux for Dig0Pin
25h	Dig2Mux	Digital Output Mux for Dig2Pin
26h	PCBeep	Digital PC Beep
27h	AnalogBeep	Analog PC Beep Input Pin
28h	ExtVolume	External Volume Control

6. PIN CONFIGURATION DEFAULT REGISTER SETTINGS

The configuration default registers are 32-bit registers required for each pin widget. These registers are normally used by the CODEC driver to determine the configuration of jacks and devices attached to the CODEC. When the CODEC is powered on, these registers are loaded with the default values provided by IDT for typical system usage, and are loaded in a way that is compatible with the Microsoft Universal Audio Architecture (UAA) driver. The values can be overridden by IDT customers according to their system configuration. Table 15 shows the Pin Widget Configuration Default settings.

Table 15. Pin Configuration Default Settings

Pin Name	Port	Location	Device	Connection	Color	Misc	Assoc.	Seq
PortAPin	Connect to Jack 00b	Mainboard Front 2h	HP Out 2h	1/8 inch Jack 1h	Green 4h	Jack Detect Override=0	3h	0h
PortBPin	Connect to Jack 00b	Mainboard Front 2h	Mic In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override=0	4h	0h
PortCPin	Connect to Jack 00b	Mainboard Rear 1h	Mic In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override=0	2h	0h
PortDPin	Connect to Jack 00b	Mainboard Rear 1h	Line Out 0h	1/8 inch Jack 1h	Green 4h	Jack Detect Override=0	1h	0h
PortEPin	Connect to Jack 00b	Mainboard Rear 1h	Line In 8h	1/8 inch Jack 1h	Blue 3h	Jack Detect Override=0	2h	Eh
PortFPin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
MonoOutPin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
DigOutPin0	Connect to Jack 00b	Mainboard Rear 000001b	SPDIF Out 4h	optical 5h	Gray 2h	Jack Detect Override=0	5h	0h
DigOutPin1	Connect to Jack 10b	Internal 011000b	Digital Other Out 5h	Other Digital 6h	Unknown 0h	Jack Detect Override=0	6h	0h
DigOutPin2	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
DigMic0Pin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
DigMic1Pin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
Analog PC_BEEP Pin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h

7. WIDGET INFORMATION

Table 16. Command Format for Verb with 4-bit Identifier

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:16]	BITS [15:0]
Reserved	CODEC Address	NID	Verb ID (4-bit)	Payload Data (16-bit)

Table 17. Command Format for Verb with 12-bit Identifier

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:8]	BITS [7:0]
Reserved	CODEC Address	NID	Verb ID (12-bit)	Payload Data (8-bit)

There are two types of responses: Solicited and Unsolicited. Solicited responses are provided as a direct response to an issued command and will be provided in the frame immediately following the command. Unsolicited responses are provided by the CODEC independent of any command. Unsolicited responses are the result of CODEC events such as a jack insertion detection. The formats for Solicited Responses and Unsolicited Responses are shown in Tables 18 and 19 respectively. The “Tag” field in bits [31:28] of the Unsolicited Response identify the event.

Table 18. Solicited Response Format

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:0]
Valid (Valid = 1)	UnSol = 0	Reserved	Response

Table 19. Unsolicited Response Format

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:28]	BITS [27:0]
Valid (Valid = 1)	UnSol = 1	Reserved	Tag	Response

8. SUPPORTED VERBS AND COMMANDS

8.1. Root Node (NID = 00)

)

8.1.1. Root VendorID

	Verb ID	Payload	Response
Get	F00	00	See bitfield table.

8.1.1.1. Root VendorID

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Vendor	R	111D	Vendor ID.
[15.:8]	DeviceFix	R	76	Device ID=76B2h.
[7.:0]	DeviceProg	R	40	Device ID=76B2h.

8.1.2. Root RevID

	Verb ID	Payload	Response
Get	F00	02	See bitfield table.

8.1.2.1. Root RevID

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd	R	00	Reserved.
[23.:20]	Major	R	1	Compliant HDAudio spec major revision.
[19.:16]	Minor	R	0	Compliant HDAudio spec minor revision
[15.:12]	RevisionFix	R	0	Vendors rev number for this device.
[11.:8]	RevisionProg	R	1	Vendors rev number for this device.
[7.:4]	SteppingFix	R	0	Vendor RevID.
[3.:0]	SteppingProg	R	1	Vendor RevID.

8.1.2.2. Root NodeInfo

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:16]	StartNID	R	01	Starting node number (NID) of first function group
[15.:8]	Rsvd1	R	00	Reserved.
[7.:0]	TotalNodes	R	01	Total number of nodes

8.2. AFG Node (NID = 01

)

8.2.1. AFG Reset

	Verb ID	Payload	Response
Get			See bitfield table.

8.2.1.1. AFG Reset

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd1	R	000000	Reserved.
[7.:0]	Execute	W	00	Function Reset.

8.2.2. AFG NodeInfo

	Verb ID	Payload	Response
Get	F00	04	See bitfield table.

8.2.2.1. AFG NodeInfo

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:16]	StartNID	R	0A	Starting node number for function group subordinate nodes.

8.2.2.1. AFG NodeInfo

Bit	Bitfield Name	RW	Reset	Description
[15.:8]	Rsvd1	R	00	Reserved.
[7.:0]	TotalNodes	R	1F	Total number of nodes.

8.2.3. AFG FGType

	Verb ID	Payload	Response
Get	F00	05	See bitfield table.

8.2.3.1. AFG FGType

Bit	Bitfield Name	RW	Reset	Description
[31.:9]	Rsvd	R	000000	Reserved.
[8]	UnSol	R	1	Unsolicited response supported: 1 = yes 0 = no.
[7.:0]	NodeType	R	1	Function group type: 00h = Reserved; 01h = Audio Function Group; 02h = Vendor Defined Modem Function Group; 03h-7Fh = Reserved; 80h-FFh = Vendor Defined Function Group

8.2.4. AFG AFGCap

	Verb ID	Payload	Response
Get	F00	08	See bitfield table.

8.2.4.1. AFG AFGCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd3	R	00	Reserved.
[16]	BeepGen	R	1	Beep generator present: 1 = yes 0 = no.
[15.:12]	Rsvd2	R	0	Reserved.

8.2.4.1. AFG AFGCap

Bit	Bitfield Name	RW	Reset	Description
[11.:8]	InputDelay	R	D	Typical latency in frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link.
[7.:4]	Rsvd1	R	0	Reserved.
[3.:0]	OutputDelay	R	D	Typical latency in frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin.

8.2.5. AFG PCMCap

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

8.2.5.1. AFG PCMCap

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	000	Reserved.
[20]	B32	R	0	32 bit audio format support: 1 = yes 0 = no.
[19]	B24	R	1	24 bit audio format support: 1 = yes 0 = no.
[18]	B20	R	1	20 bit audio format support: 1 = yes 0 = no.
[17]	B16	R	1	16 bit audio format support: 1 = yes 0 = no.
[16]	B8	R	0	8 bit audio format support: 1 = yes 0 = no.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	R12	R	0	384kHz rate support: 1 = yes 0 = no.

8.2.5.1. AFG PCMCap

Bit	Bitfield Name	RW	Reset	Description
[10]	R11	R	1	192kHz rate support: 1 = yes 0 = no.
[9]	R10	R	1	176.4kHz rate support: 1 = yes 0 = no.
[8]	R9	R	1	96kHz rate support: 1 = yes 0 = no.
[7]	R8	R	1	88.2kHz rate support: 1 = yes 0 = no.
[6]	R7	R	1	48kHz rate support: 1 = yes 0 = no.
[5]	R6	R	1	44.1kHz rate support: 1 = yes 0 = no.
[4]	R5	R	0	32kHz rate support: 1 = yes 0 = no.
[3]	R4	R	0	22.05kHz rate support: 1 = yes 0 = no.
[2]	R3	R	0	16kHz rate support: 1 = yes 0 = no.
[1]	R2	R	0	11.025kHz rate support: 1 = yes 0 = no.
[0]	R1	R	0	8kHz rate support: 1 = yes 0 = no.

8.2.6. AFG StreamCap

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

8.2.6.1. AFG StreamCap

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	00000000	Reserved.
[2]	AC3	R	0	AC-3 formatted data support: 1 = yes 0 = no.
[1]	Float32	R	0	Float32 formatted data support: 1 = yes 0 = no.
[0]	PCM	R	1	PCM-formatted data support: 1 = yes 0 = no.

8.2.7. AFG InAmpCap

	Verb ID	Payload	Response
Get	F00	0D	See bitfield table.

8.2.7.1. AFG InAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	00	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	00	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

8.2.8. AFG PwrStateCap

	Verb ID	Payload	Response
Get	F00	0F	See bitfield table.

8.2.8.1. AFG PwrStateCap

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0000000	Reserved.
[3]	D3Sup	R	1	D3 power state support: 1 = yes 0 = no.
[2]	D2Sup	R	1	D2 power state support: 1 = yes 0 = no.
[1]	D1Sup	R	1	D1 power state support: 1 = yes 0 = no.
[0]	D0Sup	R	1	D0 power state support: 1 = yes 0 = no.

8.2.9. AFG GPIOCnt

	Verb ID	Payload	Response
Get	F00	11	See bitfield table.

8.2.9.1. AFG GPIOCnt

Bit	Bitfield Name	RW	Reset	Description
[31]	GPIWake	R	1	Wake capability. Assuming the Wake Enable Mask controls are enabled GPIOs configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin.
[30]	GPIUnsol	R	1	GPIO unsolicited response support: 1 = yes 0 = no.
[29.:24]	Rsvd	R	00	Reserved.
[23.:16]	NumGPIs	R	00	Number of GPI pins supported by function group.
[15.:8]	NumGPOs	R	00	Number of GPO pins supported by function group.
[7.:0]	NumGPIOs	R	08	Number of GPIO pins supported by function group.

8.2.10. AFG OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

8.2.10.1. AFG OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.

8.2.10.1. AFG OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[22.:16]	StepSize	R	02	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	7F	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	7F	Indicates which step is 0dB

8.2.11. AFG PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

8.2.11.1. AFG PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

8.2.12. AFG UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

8.2.12.1. AFG UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

8.2.13. AFG GPIO

	Verb ID	Payload	Response
Get	F15	00	See bitfield table.

8.2.13.1. AFG GPIO

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Data7	RW	0	Data for GPIO7. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[6]	Data6	RW	0	Data for GPIO6. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[5]	Data5	RW	0	Data for GPIO5. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22

8.2.13.1. AFG GPIO

Bit	Bitfield Name	RW	Reset	Description
[4]	Data4	RW	0	Data for GPIO4. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[3]	Data3	RW	0	Data for GPIO3. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[2]	Data2	RW	0	Data for GPIO2. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[1]	Data1	RW	0	Data for GPIO1. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[0]	Data0	RW	0	Data for GPIO0. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22

8.2.14. AFG GPIOEn

	Verb ID	Payload	Response
Get	F16	00	See bitfield table.

8.2.14.1. AFG GPIOEn

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mask7	RW	0	Enable for GPIO7: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[6]	Mask6	RW	0	Enable for GPIO6: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[5]	Mask5	RW	0	Enable for GPIO5: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[4]	Mask4	RW	0	Enable for GPIO4: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[3]	Mask3	RW	0	Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[2]	Mask2	RW	0	Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[1]	Mask1	RW	0	Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[0]	Mask0	RW	0	Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control

8.2.15. AFG GPIODir

	Verb ID	Payload	Response
Get	F17	00	See bitfield table.

8.2.15.1. AFG GPIODir

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Control7	RW	0	Direction control for GPIO7: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[6]	Control6	RW	0	Direction control for GPIO6: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[5]	Control5	RW	0	Direction control for GPIO5: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[4]	Control4	RW	0	Direction control for GPIO4: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[3]	Control3	RW	0	Direction control for GPIO3: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[2]	Control2	RW	0	Direction control for GPIO2: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[1]	Control1	RW	0	Direction control for GPIO1: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[0]	Control0	RW	0	Direction control for GPIO0: 0 = GPIO is configured as input; 1 = GPIO is configured as output

8.2.16. AFG GPIOWakeEn

	Verb ID	Payload	Response
Get	F18	00	See bitfield table.

8.2.16.1. AFG GPIOWakeEn

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	W7	RW	0	Wake enable for GPIO7: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[6]	W6	RW	0	Wake enable for GPIO6: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[5]	W5	RW	0	Wake enable for GPIO5: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[4]	W4	RW	0	Wake enable for GPIO4: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[3]	W3	RW	0	Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[2]	W2	RW	0	Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.

8.2.16.1. AFG GPIOWakeEn

Bit	Bitfield Name	RW	Reset	Description
[1]	W1	RW	0	Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[0]	W0	RW	0	Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.

8.2.17. AFG GPIOUnsol

	Verb ID	Payload	Response
Get	F19	00	See bitfield table.

8.2.17.1. AFG GPIOUnsol

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	EnMask7	RW	0	Unsolicited enable mask for GPIO7. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[6]	EnMask6	RW	0	Unsolicited enable mask for GPIO6. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.

8.2.17.1. AFG GPIOUnsol

Bit	Bitfield Name	RW	Reset	Description
[5]	EnMask5	RW	0	Unsolicited enable mask for GPIO5. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[4]	EnMask4	RW	0	Unsolicited enable mask for GPIO4. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[3]	EnMask3	RW	0	Unsolicited enable mask for GPIO3. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[2]	EnMask2	RW	0	Unsolicited enable mask for GPIO2. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[1]	EnMask1	RW	0	Unsolicited enable mask for GPIO1. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO1 is configured as input and changes state.
[0]	EnMask0	RW	0	Unsolicited enable mask for GPIO0. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO0 is configured as input and changes state.

8.2.18. AFG GPIOSticky

	Verb ID	Payload	Response
Get	F1A	00	See bitfield table.

8.2.18.1. AFG GPIOSticky

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mask7	RW	0	GPIO7 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[6]	Mask6	RW	0	GPIO6 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[5]	Mask5	RW	0	GPIO5 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[4]	Mask4	RW	0	GPIO4 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[3]	Mask3	RW	0	GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[2]	Mask2	RW	0	GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[1]	Mask1	RW	0	GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[0]	Mask0	RW	0	GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).

8.2.19. AFG SubID

	Verb ID	Payload	Response
Get	F20	00	See bitfield table.

8.2.19.1. AFG SubID

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Subsys3	RW	00	Subsystem ID (byte 3)
[23.:16]	Subsys2	RW	00	Subsystem ID (byte 2)
[15.:8]	Subsys1	RW	01	Subsystem ID (byte 1)
[7.:0]	Assembly	RW	00	Assembly ID (Not applicable to codec vendors).

8.2.20. AFG GPIOPIrty

	Verb ID	Payload	Response
Get	F70	00	See bitfield table.

8.2.20.1. AFG GPIOPIrty

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	GP7	RW	1	GPIO7 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[6]	GP6	RW	1	GPIO6 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected

8.2.20.1. AFG GPIOPIrty

Bit	Bitfield Name	RW	Reset	Description
[5]	GP5	RW	1	GPIO5 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[4]	GP4	RW	1	GPIO4 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[3]	GP3	RW	1	GPIO3 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[2]	GP2	RW	1	GPIO2 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[1]	GP1	RW	1	GPIO1 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[0]	GP0	RW	1	GPIO0 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected

8.2.21. AFG GPIODrive

	Verb ID	Payload	Response
Get	F71	00	See bitfield table.

8.2.21.1. AFG GPIODrive

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	OD7	RW	0	GPIO7 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[6]	OD6	RW	0	GPIO6 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[5]	OD5	RW	0	GPIO5 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[4]	OD4	RW	0	GPIO4 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[3]	OD3	RW	0	GPIO3 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[2]	OD2	RW	0	GPIO2 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[1]	OD1	RW	0	GPIO1 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[0]	OD0	RW	0	GPIO0 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open-drain (drive 0 float for 1).

8.2.22. AFG DMic

	Verb ID	Payload	Response
Get	F78	00	See bitfield table.

8.2.22.1. AFG DMic

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0000000	Reserved.
[3.:2]	PhAdj	RW	0	Selects what phase of the DMic clock the data should be latched: 0h = left data rising edge/right data falling edge; 1h = left data center of high/right data center of low; 2h = left data falling edge/right data rising edge; 3h = left data center of low/right data center of high
[1.:0]	Rate	RW	2	Selects the DMic clock rate: 0h = 4.704MHz; 1h = 3.528MHz; 2h = 2.352MHz; 3h = 1.176MHz.

8.2.23. AFG Misc. (B3 revision and beyond only)

	Verb ID	Payload	Response
Get	F7F	00	See bitfield table.

8.2.23.1. AFG Misc. (B3 revision and beyond only)

Bit	Bitfield Name	RW	Reset	Description
[31.:11]	Rsvd2	R	0000000	Reserved.
[10]	DMic1Mono	RW	0	Enable Mono Mode for DMIC1 0=disable, 1=enable mono mode *B3 revision and beyond only*
[9]	DMic0Mono	RW	0	Enable Mono Mode for DMIC0 0=disable, 1=enable mono mode *B3 revision and beyond only*
[8]	DMicSelect	RW	0	Digital Mic Select 0=DMic uses external pins 1=Volume knob uses external pins *B3 revision and beyond only*
[7.:0]	Rsvd1	R	0000000	Reserved.

8.3. Port A Node (NID = 0A)

8.3.1. PortA WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.3.1.1. PortA WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

8.3.1.1. PortA WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.3.2. PortA PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.3.2.1. PortA PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	0	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	1	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.

8.3.2.1. PortA PinCap

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.3.3. PortA ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.3.3.1. PortA ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

8.3.4. PortA ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.3.4.1. PortA ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	17	InputMixer Summing widget (0x17)
[15.:8]	ConL1	R	11	DAC1 Converter widget (0x11)
[7.:0]	ConL0	R	10	DAC0 Converter widget (0x10)

8.3.5. PortA ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.3.5.1. PortA ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.3.6. PortA PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.3.6.1. PortA PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	HPhnEn	RW	0	Headphone amp enable: 1 = enabled 0 = disabled.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	0	Reserved.

8.3.7. PortA UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

8.3.7.1. PortA UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

8.3.8. PortA ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

8.3.8.1. PortA ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:0]	Rsvd	R	0	Reserved.

8.3.9. PortA InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

8.3.9.1. PortA InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

8.3.10. PortA InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

8.3.10.1. PortA InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

8.3.11. PortA ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.3.11.1. PortA ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	02	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	2	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other

8.3.11.1. PortA ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Connection Type	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	4	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	3	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.4. PortB Node (NID = 0B)

8.4.1. PortB WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.4.1.1. PortB WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

8.4.1.1. PortB WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.4.2. PortB PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.4.2.1. PortB PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	17	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	0	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.4.3. PortB PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.4.3.1. PortB PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:3]	Rsvd1	R	0	Reserved.
[2.:0]	VRefEn	RW	0	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z; 001b= 50%; 010b= GND; 011b= Reserved; 100b= 80%; 101b= 100%; 110b= Reserved; 111b= Reserved

8.4.4. PortB UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

8.4.4.1. PortB UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

8.4.5. PortB ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

8.4.5.1. PortB ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:0]	Rsvd	R	0	Reserved.

8.4.6. PortB ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.4.6.1. PortB ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	02	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved

8.4.6.1. PortB ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[23.:20]	Device	RW	A	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	9	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	4	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.5. Port C Node (NID = 0C)

8.5.1. PortC WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.5.1.1. PortC WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.5.2. PortC PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.5.2.1. PortC PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	17	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	0	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.5.3. PortC PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.5.3.1. PortC PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:3]	Rsvd1	R	0	Reserved.
[2.:0]	VRefEn	RW	0	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z; 001b= 50%; 010b= GND; 011b= Reserved; 100b= 80%; 101b= 100%; 110b= Reserved; 111b= Reserved

8.5.4. PortC UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

8.5.4.1. PortC UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.

8.5.4.1. PortC UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

8.5.5. PortC ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

8.5.5.1. PortC ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:0]	Rsvd	R	0	Reserved.

8.5.6. PortC ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.5.6.1. PortC ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	1	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	A	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	9	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	2	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.6. Port D Node (NID = 0D)

8.6.1. PortD WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.6.1.1. PortD WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

8.6.1.1. PortD WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.6.2. PortD PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.6.2.1. PortD PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	0	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.

8.6.2.1. PortD PinCap

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.6.3. PortD ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.6.3.1. PortD ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

8.6.4. PortD ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.6.4.1. PortD ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	17	InputMixer Summing widget (0x17)
[15.:8]	ConL1	R	11	DAC1 Converter widget (0x11)
[7.:0]	ConL0	R	10	DAC0 Converter widget (0x10)

8.6.5. PortD ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.6.5.1. PortD ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.6.6. PortD PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.6.6.1. PortD PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	0	Reserved.

8.6.7. PortD UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

8.6.7.1. PortD UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

8.6.8. PortD ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

8.6.8.1. PortD ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:0]	Rsvd	R	0	Reserved.

8.6.9. PortD InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

8.6.9.1. PortD InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

8.6.10. PortD InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

8.6.10.1. PortD InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

8.6.11. PortD ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.6.11.1. PortD ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	1	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	0	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other

8.6.11.1. PortD ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	4	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	1	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.7. PortE Node (NID = 0E)

8.7.1. PortE WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.7.1.1. PortE WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

8.7.1.1. PortE WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.7.2. PortE PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.7.2.1. PortE PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	17	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	0	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.7.3. PortE PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.7.3.1. PortE PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:3]	Rsvd1	R	0	Reserved.
[2.:0]	VRefEn	RW	0	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z; 001b= 50%; 010b= GND; 011b= Reserved; 100b= 80%; 101b= 100%; 110b= Reserved; 111b= Reserved

8.7.4. PortE UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

8.7.4.1. PortE UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

8.7.5. PortE ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

8.7.5.1. PortE ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:0]	Rsvd	R	0	Reserved.

8.7.6. PortE ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.7.6.1. PortE ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	1	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved

8.7.6.1. PortE ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[23.:20]	Device	RW	8	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	3	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	2	Default assocation.
[3.:0]	Sequence	RW	E	Sequence.

8.8. PortF Node (NID = 0F)

8.8.1. PortF WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.8.1.1. PortF WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.8.2. PortF PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.8.2.1. PortF PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	0	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.8.3. PortF ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.8.3.1. PortF ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

8.8.4. PortF ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.8.4.1. PortF ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	17	InputMixer Summing widget (0x17)
[15.:8]	ConL1	R	11	DAC1 Converter widget (0x11)
[7.:0]	ConL0	R	10	DAC0 Converter widget (0x10)

8.8.5. PortF ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.8.5.1. PortF ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.8.6. PortF PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.8.6.1. PortF PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	0	Reserved.

8.8.7. PortF UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

8.8.7.1. PortF UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

8.8.8. PortF ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

8.8.8.1. PortF ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:0]	Rsvd	R	0	Reserved.

8.8.9. PortF InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

8.8.9.1. PortF InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

8.8.10. PortF InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

8.8.10.1. PortF InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

8.8.11. PortF ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.8.11.1. PortF ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	1	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	00	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	F	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	0	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	F	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.9. DAC0 Node (NID = 10)

8.9.1. DAC0 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.9.1.1. DAC0 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.

8.9.1.1. DAC0 WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.9.2. DAC0 Cnvtr

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.

8.9.2.1. DAC0 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.

8.9.2.1. DAC0 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

8.9.3. DAC0 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

8.9.3.1. DAC0 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.9.4. DAC0 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

8.9.4.1. DAC0 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.9.5. DAC0 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

8.9.5.1. DAC0 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

8.9.6. DAC0 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

8.9.6.1. DAC0 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

8.9.7. DAC0 LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

8.9.7.1. DAC0 LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

8.10. DAC1 Node (NID = 11)

8.10.1. DAC1 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.10.1.1. DAC1 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.10.2. DAC1 Cnvtr

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.

8.10.2.1. DAC1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

8.10.3. DAC1 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

8.10.3.1. DAC1 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.10.4. DAC1 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

8.10.4.1. DAC1 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.10.5. DAC1 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

8.10.5.1. DAC1 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

8.10.6. DAC1 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

8.10.6.1. DAC1 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

8.10.7. DAC1 LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

8.10.7.1. DAC1 LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

8.11. ADC0 Node (NID = 12)

8.11.1. ADC0 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.11.1.1. ADC0 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	1	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.

8.11.1.1. ADC0 WCap

Bit	Bitfield Name	RW	Reset	Description
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	1	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.11.2. ADC0 ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.11.2.1. ADC0 ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	01	Number of NID entries in connection list.

8.11.3. ADC0 ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.11.3.1. ADC0 ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	1C	ADC0Mux Selector widget (0x1C)

8.11.4. ADC0 Cnvtr

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.

8.11.4.1. ADC0 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

8.11.5. ADC0 ProcState

	Verb ID	Payload	Response
Get	F03	00	See bitfield table.

8.11.5.1. ADC0 ProcState

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	HPFOCDIS	RW	0	HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled.
[6.:2]	Rsvd1	R	00	Reserved.
[1.:0]	ADCHPFByp	RW	1	Processing State: 00b= bypass the ADC HPF ("off") 01b-11b= ADC HPF is enabled ("on" or "benign").

8.11.6. ADC0 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

8.11.6.1. ADC0 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

8.11.7. ADC0 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

8.11.7.1. ADC0 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

8.12. ADC1 Node (NID = 13)

8.12.1. ADC1 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.12.1.1. ADC1 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	1	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.

8.12.1.1. ADC1 WCap

Bit	Bitfield Name	RW	Reset	Description
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	1	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.12.2. ADC1 ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.12.2.1. ADC1 ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	01	Number of NID entries in connection list.

8.12.3. ADC1 ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.12.3.1. ADC1 ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	1D	ADC1Mux widget (0x1D)

8.12.4. ADC1 Cnvtr

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.

8.12.4.1. ADC1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved

8.12.4.1. ADC1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

8.12.5. ADC1 ProcState

	Verb ID	Payload	Response
Get	F03	00	See bitfield table.

8.12.5.1. ADC1 ProcState

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	HPFOCDIS	RW	0	HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled.
[6.:2]	Rsvd1	R	00	Reserved.
[1.:0]	ADCHPFByp	RW	1	Processing State: 00b= bypass the ADC HPF ("off") 01b-11b= ADC HPF is enabled ("on" or "benign").

8.12.6. ADC1 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

8.12.6.1. ADC1 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

8.12.7. ADC1 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

8.12.7.1. ADC1 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

8.13. MonoOut Node (NID = 14)

8.13.1. MonoOut WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.13.1.1. MonoOut WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

8.13.1.1. MonoOut WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	0	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.13.2. MonoOut PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.13.2.1. MonoOut PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	0	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.

8.13.2.1. MonoOut PinCap

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.13.3. MonoOut ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.13.3.1. MonoOut ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	01	Number of NID entries in connection list.

8.13.4. MonoOut ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.13.4.1. MonoOut ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	16	MonoMixer Summing widget

8.13.5. MonoOut PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.13.5.1. MonoOut PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	0	Reserved.

8.13.6. MonoOut InAmpLeft

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

8.13.6.1. MonoOut InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

8.13.7. MonoOut ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.13.7.1. MonoOut ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	1	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	00	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	F	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other

8.13.7.1. MonoOut ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	ConnectionType	RW	0	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	F	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.14. MonoMux Node (NID = 15)

8.14.1. MonoMux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.14.1.1. MonoMux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

8.14.1.1. MonoMux WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.14.2. MonoMux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.14.2.1. MonoMux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

8.14.3. MonoMux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.14.3.1. MonoMux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	17	Input Mixer widget (0x17)
[15.:8]	ConL1	R	11	DAC1 Converter widget (0x11)
[7.:0]	ConL0	R	10	DAC0 Converter widget (0x10)

8.14.4. MonoMux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.14.4.1. MonoMux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	0000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.15. MonoMixer Node (NID = 16)

8.15.1. MonoMixer WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.15.1.1. MonoMixer WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	2	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.

8.15.1.1. MonoMixer WCap

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	0	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.15.2. MonoMixer ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.15.2.1. MonoMixer ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	01	Number of NID entries in connection list.

8.15.3. MonoMixer ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.15.3.1. MonoMixer ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	15	MonoMux Selector widget (0x15)

8.16. InputMixer Node (NID = 17)

8.16.1. InputMixer WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.16.1.1. InputMixer WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	2	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.

8.16.1.1. InputMixer WCap

Bit	Bitfield Name	RW	Reset	Description
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.16.2. InputMixer ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.16.2.1. InputMixer ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	05	Number of NID entries in connection list.

8.16.3. InputMixer ConLstEntry4

	Verb ID	Payload	Response
Get	F02	04	See bitfield table.

8.16.3.1. InputMixer ConLstEntry4

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL7	R	00	Unused list entry.
[23.:16]	ConL6	R	00	Unused list entry.
[15.:8]	ConL5	R	00	Unused list entry.
[7.:0]	ConL4	R	1B	InPort1Mux Selector widget (0x1B). Uses InAmpLeft4/InAmpRight4 controls.

8.16.4. InputMixer ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.16.4.1. InputMixer ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	1A	InPort0Mux Selector widget (0x1A). Uses InAmpLeft3/InAmpRight3 controls.
[23.:16]	ConL2	R	27	AnaBeep Pin widget (0x27). Uses InAmpLeft2/InAmpRight2 controls.
[15.:8]	ConL1	R	11	DAC1 Converter widget (0x11). Uses InAmpLeft1/InAmpRight1 controls.
[7.:0]	ConL0	R	10	DAC0 Converter widget (0x10). Uses InAmpLeft0/InAmpRight0 controls.

8.16.5. InputMixer InAmpCap

	Verb ID	Payload	Response
Get	F00	0D	See bitfield table.

8.16.5.1. InputMixer InAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	05	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	1F	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	17	Indicates which step is 0dB

8.16.6. InputMixer InAmpLeft0

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

8.16.6.1. InputMixer InAmpLeft0

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.16.7. InputMixer InAmpRight0

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

8.16.7.1. InputMixer InAmpRight0

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.16.8. InputMixer InAmpLeft1

	Verb ID	Payload	Response
Get	B20	01	See bitfield table.

8.16.8.1. InputMixer InAmpLeft1

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.16.9. InputMixer InAmpRight1

	Verb ID	Payload	Response
Get	B00	01	See bitfield table.

8.16.9.1. InputMixer InAmpRight1

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.16.10. InputMixer InAmpLeft2

	Verb ID	Payload	Response
Get	B20	02	See bitfield table.

8.16.10.1. InputMixer InAmpLeft2

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.16.11. InputMixer InAmpRight2

	Verb ID	Payload	Response
Get	B00	02	See bitfield table.

8.16.11.1. InputMixer InAmpRight2

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.16.12. InputMixer InAmpLeft3

	Verb ID	Payload	Response
Get	B20	03	See bitfield table.

8.16.12.1. InputMixer InAmpLeft3

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.16.13. InputMixer InAmpRight3

	Verb ID	Payload	Response
Get	B00	03	See bitfield table.

8.16.13.1. InputMixer InAmpRight3

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.16.14. InputMixer InAmpLeft4

	Verb ID	Payload	Response
Get	B20	04	See bitfield table.

8.16.14.1. InputMixer InAmpLeft4

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.16.15. InputMixer InAmpRight4

	Verb ID	Payload	Response
Get	B00	04	See bitfield table.

8.16.15.1. InputMixer InAmpRight4

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

8.17. DMic0 Node (NID = 18)

8.17.1. DMic0 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.17.1.1. DMic0 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.

8.17.1.1. DMic0 WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.17.2. DMic0 PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.17.2.1. DMic0 PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VRefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	0	Output support: 1 = yes 0 = no.
[3]	HPhnDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.

8.17.2.1. DMic0 PinCap

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.17.3. DMic0 PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.17.3.1. DMic0 PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:0]	Rsvd1	R	00	Reserved.

8.17.4. DMic0 OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

8.17.4.1. DMic0 OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.

8.17.4.1. DMic0 OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[22.:16]	StepSize	R	27	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	03	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

8.17.5. DMic0 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

8.17.5.1. DMic0 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd1	R	00000000	Reserved.
[2.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.17.6. DMic0 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

8.17.6.1. DMic0 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd1	R	00000000	Reserved.
[2.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.17.7. DMic0 ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.17.7.1. DMic0 ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	1	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	00	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	F	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other

8.17.7.1. DMic0 ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	ConnectionType	RW	0	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	F	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.18. DMic1 Node (NID = 19)

8.18.1. DMic1 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.18.1.1. DMic1 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

8.18.1.1. DMic1 WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.18.2. DMic1 PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.18.2.1. DMic1 PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VRefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	0	Output support: 1 = yes 0 = no.
[3]	HPhnDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.18.3. DMic1 PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.18.3.1. DMic1 PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:0]	Rsvd1	R	00	Reserved.

8.18.4. DMic1 OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

8.18.4.1. DMic1 OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	27	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	03	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

8.18.5. DMic1 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

8.18.5.1. DMic1 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd1	R	00000000	Reserved.
[2.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.18.6. DMic1 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

8.18.6.1. DMic1 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd1	R	00000000	Reserved.
[2.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.18.7. DMic1 ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.18.7.1. DMic1 ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	1	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	00	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	F	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	0	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	F	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.19. InPort0Mux Node (NID = 1A)

8.19.1. InPort0Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.19.1.1. InPort0Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.

8.19.1.1. InPort0Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.19.2. InPort0Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.19.2.1. InPort0Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

8.19.3. InPort0Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.19.3.1. InPort0Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	0E	Port E Pin widget (0x0E)

8.19.3.1. InPort0Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[15.:8]	ConL1	R	0C	Port C Pin widget (0x0C)
[7.:0]	ConL0	R	0B	Port B Pin widget (0x0B)

8.19.4. InPort0Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.19.4.1. InPort0Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.19.5. InPort0Mux OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

8.19.5.1. InPort0Mux OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	27	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.

8.19.5.1. InPort0Mux OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[14.:8]	NumSteps	R	03	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

8.19.6. InPort0Mux OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

8.19.6.1. InPort0Mux OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd1	R	00000000	Reserved.
[2.:0]	Gain	RW	0	Amp gain step number (see OutAmpCap parameter pertaining to this widget).

8.19.7. InPort0Mux OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

8.19.7.1. InPort0Mux OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd1	R	00000000	Reserved.
[2.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.20. InPort1Mux Node (NID = 1B)

8.20.1. InPort1Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.20.1.1. InPort1Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.

8.20.1.1. InPort1Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.20.2. InPort1Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.20.2.1. InPort1Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

8.20.3. InPort1Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.20.3.1. InPort1Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	0E	Port E Pin widget (0x0E)
[15.:8]	ConL1	R	0C	Port C Pin widget (0x0C)
[7.:0]	ConL0	R	0B	Port B Pin widget (0x0B)

8.20.4. InPort1Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.20.4.1. InPort1Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.20.5. InPort1Mux OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

8.20.5.1. InPort1Mux OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	27	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	03	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

8.20.6. InPort1Mux OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

8.20.6.1. InPort1Mux OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd1	R	00000000	Reserved.
[2.:0]	Gain	RW	0	Amp gain step number (see OutAmpCap parameter pertaining to this widget).

8.20.7. InPort1Mux OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

8.20.7.1. InPort1Mux OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd1	R	00000000	Reserved.
[2.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.21. ADC0Mux Node (NID = 1C)

8.21.1. ADC0Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.21.1.1. ADC0Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.

8.21.1.1. ADC0Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParamOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.21.2. ADC0Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.21.2.1. ADC0Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	04	Number of NID entries in connection list.

8.21.3. ADC0Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.21.3.1. ADC0Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	19	DMic1 Pin widget (0x19)
[23.:16]	ConL2	R	18	DMic0 Pin widget (0x18)
[15.:8]	ConL1	R	17	InputMixer Summing widget (0x17)
[7.:0]	ConL0	R	1A	InPort0Mux Selector widget (0x1A)

8.21.4. ADC0Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.21.4.1. ADC0Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.21.5. ADC0Mux LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

8.21.5.1. ADC0Mux LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

8.21.6. ADC0Mux OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

8.21.6.1. ADC0Mux OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	05	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	0F	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

8.21.7. ADC0Mux OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

8.21.7.1. ADC0Mux OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:4]	Rsvd1	R	0	Reserved.
[3.:0]	Gain	RW	0	Amp gain step number (see OutAmpCap parameter pertaining to this widget).

8.21.8. ADC0Mux OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

8.21.8.1. ADC0Mux OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:4]	Rsvd1	R	0	Reserved.
[3.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.22. ADC1Mux Node (NID = 1D)

8.22.1. ADC1Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.22.1.1. ADC1Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

8.22.1.1. ADC1Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParamOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.22.2. ADC1Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.22.2.1. ADC1Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	04	Number of NID entries in connection list.

8.22.3. ADC1Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.22.3.1. ADC1Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	19	DMic1 Pin widget (0x19)
[23.:16]	ConL2	R	18	DMic0 Pin widget (0x18)
[15.:8]	ConL1	R	17	InputMixer Summing widget (0x17)
[7.:0]	ConL0	R	1B	InPort1Mux Selector widget (0x1B)

8.22.4. ADC1Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.22.4.1. ADC1Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.22.5. ADC1Mux LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

8.22.5.1. ADC1Mux LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

8.22.6. ADC1Mux OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

8.22.6.1. ADC1Mux OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	05	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	0F	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

8.22.7. ADC1Mux OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

8.22.7.1. ADC1Mux OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:4]	Rsvd1	R	0	Reserved.
[3.:0]	Gain	RW	0	Amp gain step number (see OutAmpCap parameter pertaining to this widget).

8.22.8. ADC1Mux OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

8.22.8.1. ADC1Mux OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:4]	Rsvd1	R	0	Reserved.
[3.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.23. Dig0Pin Node (NID = 1E)

8.23.1. Dig0Pin WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.23.1.1. Dig0Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

8.23.1.1. Dig0Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.23.2. Dig0Pin PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.23.2.1. Dig0Pin PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	0	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.23.3. Dig0Pin ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.23.3.1. Dig0Pin ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	01	Number of NID entries in connection list.

8.23.4. Dig0Pin ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.23.4.1. Dig0Pin ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	24	Dig0Mux Selector widget (0x24)

8.23.5. Dig0Pin PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.23.5.1. Dig0Pin PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	00	Reserved.

8.23.6. Dig0Pin ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.23.6.1. Dig0Pin ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	1	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved

8.23.6.1. Dig0Pin ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[23.:20]	Device	RW	4	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	5	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	2	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	5	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.24. Dig1Pin Node (NID = 1F)

8.24.1. Dig1Pin WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.24.1.1. Dig1Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.24.2. Dig1Pin PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.24.2.1. Dig1Pin PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	1	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	0	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.24.3. Dig1Pin ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.24.3.1. Dig1Pin ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	02	Number of NID entries in connection list.

8.24.4. Dig1Pin ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.24.4.1. Dig1Pin ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	25	Dig2Mux Selector widget (0x25)
[7.:0]	ConL0	R	24	Dig0Mux Selector widget (0x24)

8.24.5. Dig1Pin ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.24.5.1. Dig1Pin ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:1]	Rsvd	R	00000000	Reserved.
[0]	Index	RW	0	Connection select control index.

8.24.6. Dig1Pin PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.24.6.1. Dig1Pin PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	00	Reserved.

8.24.7. Dig1Pin PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

8.24.7.1. Dig1Pin PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget used for EAPD control in this case: 0h-1h = Pin drives the value of the EAPD control bit; 2h-3h = Pin tri-stated

8.24.8. Dig1Pin EAPD

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

8.24.8.1. Dig1Pin EAPD

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd2	R	00000000	Reserved.
[1]	Control	RW	0	EAPD value reflected on the EAPD pin: 0 = Power down external amplifier; 1 = Power up external amplifier
[0]	Rsvd1	R	0	Reserved.

8.24.9. Dig1Pin ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.24.9.1. Dig1Pin ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	2	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	18	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	5	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	6	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	6	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.25. Dig2Pin Node (NID = 20)

8.25.1. Dig2Pin WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.25.1.1. Dig2Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

8.25.1.1. Dig2Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.25.2. Dig2Pin PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.25.2.1. Dig2Pin PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	0	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.

8.25.2.1. Dig2Pin PinCap

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

8.25.3. Dig2Pin ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.25.3.1. Dig2Pin ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	01	Number of NID entries in connection list.

8.25.4. Dig2Pin ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.25.4.1. Dig2Pin ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	25	Dig2Mux Selector widget (0x25)

8.25.5. Dig2Pin PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.25.5.1. Dig2Pin PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	00	Reserved.

8.25.6. Dig2Pin ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.25.6.1. Dig2Pin ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	1	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	00	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	F	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	0	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	F	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.26. SPDIFOut0 Node (NID = 21)

8.26.1. SPDIFOut0 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.26.1.1. SPDIFOut0 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	4	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	1	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

8.26.1.1. SPDIFOut0 WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

8.26.2. SPDIFOut0 PCMCap

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

8.26.2.1. SPDIFOut0 PCMCap

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	000	Reserved.
[20]	B32	R	0	32 bit audio format support: 1 = yes, 0 = no.
[19]	B24	R	1	24 bit audio format support: 1 = yes, 0 = no.
[18]	B20	R	1	20 bit audio format support: 1 = yes, 0 = no.
[17]	B16	R	1	16 bit audio format support: 1 = yes, 0 = no.
[16]	B8	R	0	8 bit audio format support: 1 = yes, 0 = no.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	R12	R	0	384kHz rate support: 1 = yes, 0 = no.
[10]	R11	R	1	192kHz rate support: 1 = yes, 0 = no.
[9]	R10	R	1	176.4kHz rate support: 1 = yes, 0 = no.
[8]	R9	R	1	96kHz rate support: 1 = yes, 0 = no.
[7]	R8	R	1	88.2kHz rate support: 1 = yes, 0 = no.

8.26.2.1. SPDIFOut0 PCMCap

Bit	Bitfield Name	RW	Reset	Description
[6]	R7	R	1	48kHz rate support: 1 = yes, 0 = no.
[5]	R6	R	1	44.1kHz rate support: 1 = yes, 0 = no.
[4]	R5	R	0	32kHz rate support: 1 = yes, 0 = no.
[3]	R4	R	0	22.05kHz rate support: 1 = yes, 0 = no.
[2]	R3	R	0	16kHz rate support: 1 = yes, 0 = no.
[1]	R2	R	0	11.025kHz rate support: 1 = yes, 0 = no.
[0]	R1	R	0	8kHz rate support: 1 = yes, 0 = no.

8.26.3. SPDIFOut0 StreamCap

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

8.26.3.1. SPDIFOut0 StreamCap

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	00000000	Reserved.
[2]	AC3	R	1	AC-3 formatted data support: 1 = yes, 0 = no.
[1]	Float32	R	0	Float32 formatted data support: 1 = yes, 0 = no.
[0]	PCM	R	1	PCM-formatted data support: 1 = yes, 0 = no.

8.26.4. SPDIFOut0 Cnvtr

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.

8.26.4.1. SPDIFOut0 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	FrmtNonPCM	RW	0	Stream type: 1 = Non-PCM, 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

8.26.5. SPDIFOut0 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

8.26.5.1. SPDIFOut0 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off", 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).

8.26.6. SPDIFOut0 DigCnvtr

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table.

8.26.6.1. SPDIFOut0 DigCnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	Rsvd1	R	0	Reserved.
[14.:8]	CC	RW	00	CC: Category Code.
[7]	L	RW	0	L: Generation Level.
[6]	PRO	RW	0	PRO: Professional.
[5]	AUDIO	RW	0	/AUDIO: Non-Audio.
[4]	COPY	RW	0	COPY: Copyright.

8.26.6.1. SPDIFOut0 DigCnvtr

Bit	Bitfield Name	RW	Reset	Description
[3]	PRE	RW	0	PRE: Preemphasis.
[2]	VCFG	RW	0	VCFG: Validity Config.
[1]	V	RW	0	V: Validity.
[0]	DigEn	RW	0	Digital enable: 1 = converter enabled, 0 = converter disable.

8.27. SPDIFOut1 Node (NID = 22)

8.27.1. SPDIFOut1 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.27.1.1. SPDIFOut1 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	4	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes, 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes, 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital), 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes, 0 = no.

8.27.1.1. SPDIFOut1 WCap

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes, 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes, 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes, 0 = no.
[4]	FormatOvrd	R	1	Stream format override: 1 = yes, 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes, no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes, 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes, 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo), 0 = no (mono).

8.27.2. SPDIFOut1 PCMCap

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

8.27.2.1. SPDIFOut1 PCMCap

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	000	Reserved.
[20]	B32	R	0	32 bit audio format support: 1 = yes, 0 = no.
[19]	B24	R	1	24 bit audio format support: 1 = yes, 0 = no.
[18]	B20	R	1	20 bit audio format support: 1 = yes, 0 = no.
[17]	B16	R	1	16 bit audio format support: 1 = yes, 0 = no.

8.27.2.1. SPDIFOut1 PCMCap

Bit	Bitfield Name	RW	Reset	Description
[16]	B8	R	0	8 bit audio format support: 1 = yes, 0 = no.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	R12	R	0	384kHz rate support: 1 = yes, 0 = no.
[10]	R11	R	1	192kHz rate support: 1 = yes, 0 = no.
[9]	R10	R	1	176.4kHz rate support: 1 = yes, 0 = no.
[8]	R9	R	1	96kHz rate support: 1 = yes, 0 = no.
[7]	R8	R	1	88.2kHz rate support: 1 = yes, 0 = no.
[6]	R7	R	1	48kHz rate support: 1 = yes, 0 = no.
[5]	R6	R	1	44.1kHz rate support: 1 = yes, 0 = no.
[4]	R5	R	0	32kHz rate support: 1 = yes, 0 = no.
[3]	R4	R	0	22.05kHz rate support: 1 = yes, 0 = no.
[2]	R3	R	0	16kHz rate support: 1 = yes, 0 = no.
[1]	R2	R	0	11.025kHz rate support: 1 = yes, 0 = no.
[0]	R1	R	0	8kHz rate support: 1 = yes, 0 = no.

8.27.3. SPDIFOut1 StreamCap

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

8.27.3.1. SPDIFOut1 StreamCap

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	00000000	Reserved.
[2]	AC3	R	1	AC-3 formatted data support: 1 = yes, 0 = no.

8.27.3.1. SPDIFOut1 StreamCap

Bit	Bitfield Name	RW	Reset	Description
[1]	Float32	R	0	Float32 formatted data support: 1 = yes, 0 = no.
[0]	PCM	R	1	PCM-formatted data support: 1 = yes, 0 = no.

8.27.4. SPDIFOut1 Cnvtr

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.

8.27.4.1. SPDIFOut1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	FrmtNonPCM	RW	0	Stream type: 1 = Non-PCM, 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.

8.27.4.1. SPDIFOut1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

8.27.5. SPDIFOut1 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

8.27.5.1. SPDIFOut1 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off", 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).

8.27.6. SPDIFOut1 DigCnvtr

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table.

8.27.6.1. SPDIFOut1 DigCnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	Rsvd1	R	0	Reserved.
[14.:8]	CC	RW	00	CC: Category Code.
[7]	L	RW	0	L: Generation Level.
[6]	PRO	RW	0	PRO: Professional.
[5]	AUDIO	RW	0	/AUDIO: Non-Audio.
[4]	COPY	RW	0	COPY: Copyright.
[3]	PRE	RW	0	PRE: Preemphasis.
[2]	VCFG	RW	0	VCFG: Validity Config.
[1]	V	RW	0	V: Validity.
[0]	DigEn	RW	0	Digital enable: 1 = converter enabled, 0 = converter disable.

8.28. Dig0Mux Node (NID = 24)

8.28.1. Dig0Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.28.1.1. Dig0Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes, 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes, 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital), 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes, 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes, 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes, 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes, 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes, 0 = no.
[3]	AmpParamOvrd	R	0	Amplifier capabilities override: 1 = yes, no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes, 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes, 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo), 0 = no (mono).

8.28.2. Dig0Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.28.2.1. Dig0Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

8.28.3. Dig0Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.28.3.1. Dig0Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	1D	ADC1Mux Selector widget (0x1D)
[15.:8]	ConL1	R	1C	ADC0Mux Selector widget (0x1C)
[7.:0]	ConL0	R	21	SPDIFOut0 Converter widget (0x21)

8.28.4. Dig0Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.28.4.1. Dig0Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.29. Dig2Mux Node (NID = 25)

8.29.1. Dig2Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.29.1.1. Dig2Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes, 0 = no.

8.29.1.1. Dig2Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[10]	PwrCntrl	R	0	Power state support: 1 = yes, 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital), 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes, 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes, 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes, 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes, 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes, 0 = no.
[3]	AmpParamOvrd	R	0	Amplifier capabilities override: 1 = yes, no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes, 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes, 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo), 0 = no (mono).

8.29.2. Dig2Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.29.2.1. Dig2Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.

8.29.2.1. Dig2Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

8.29.3. Dig2Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.29.3.1. Dig2Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	1D	ADC1Mux Selector widget (0x1D)
[15.:8]	ConL1	R	1C	ADC0Mux Selector widget (0x1C)
[7.:0]	ConL0	R	22	SPDIFOut1 Converter widget (0x22)

8.29.4. Dig2Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

8.29.4.1. Dig2Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

8.30. DigBeep Node (NID = 26)

8.30.1. DigBeep WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.30.1.1. DigBeep WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd3	R	00	Reserved.
[23.:20]	Type	R	7	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:4]	Rsvd2	R	0	Reserved.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes, no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes, 0 = no.
[1.:0]	Rsvd1	R	0	Reserved.

8.30.2. DigBeep OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

8.30.2.1. DigBeep OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes, 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	17	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	03	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	03	Indicates which step is 0dB

8.30.3. DigBeep OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

8.30.3.1. DigBeep OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	0	Amp mute: 1 = muted, 0 = not muted.

8.30.3.1. DigBeep OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[6.:2]	Rsvd1	R	00	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

8.30.4. DigBeep Gen

	Verb ID	Payload	Response
Get	F0A	00	See bitfield table.

8.30.4.1. DigBeep Gen

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:0]	Divider	RW	00	Enable internal PC-Beep generation. Divider == 00h disables internal PC Beep generation and enables normal operation of the codec. Divider != 00h generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). This part can selectively generate tones with frequency = 48KHz * (257 - Divider) / 1024, yielding a linear range from 12kHz to 93.75Hz in steps of 46.875Hz. If the FreqShift bit is set, then the beep tones generated have frequency = 48KHz * (513 - Divider) / 1024, yielding a range of 24kHz to 12093.75Hz in steps of 46.875Hz.

8.30.5. DigBeep Mode

	Verb ID	Payload	Response
Get	FE0	00	See bitfield table.

8.30.5.1. DigBeep Mode

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	00000000	Reserved.
[1]	FreqShift	RW	0	Digital PCBeep frequency range shift (for linear mode only): 0 = 47Hz-12kHz, 1 = 12.047kHz-24kHz.
[0]	LinearSel	RW	0	Linear PCBeep frequency select. 0 = HD Audio Rev.1.0 frequencies ; 1 = linear frequencies

8.31. AnaBeep Node (NID = 27)

8.31.1. AnaBeep WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.31.1.1. AnaBeep WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

8.31.1.1. AnaBeep WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes, 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes, 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital), 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes, 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes, 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes, 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes, 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes, 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes, no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes, 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes, 0 = no.
[0]	Stereo	R	0	Stereo stream support: 1 = yes (stereo), 0 = no (mono).

8.31.2. AnaBeep PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

8.31.2.1. AnaBeep PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes, 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes, 0 = no); bit 4 = 80% support (1 = yes, 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes, 0 = no); bit 1 = 50% support (1 = yes, 0 = no); bit 0 = Hi-Z support (1 = yes, 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes, 0 = no.
[5]	InCap	R	1	Input support: 1 = yes, 0 = no.
[4]	OutCap	R	0	Output support: 1 = yes, 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes, 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes, 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes, 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes, 0 = no.

8.31.3. AnaBeep PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

8.31.3.1. AnaBeep PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled, 0 = disabled.
[4.:0]	Rsvd1	R	0	Reserved.

8.31.4. AnaBeep ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

8.31.4.1. AnaBeep ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	1	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)
[29.:24]	Location	RW	00	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	F	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other

8.31.4.1. AnaBeep ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	ConnectionType	RW	0	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	F	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

8.32. VolumeKnob Node (NID = 28)

8.32.1. VolumeKnob WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

8.32.1.1. VolumeKnob WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.

8.32.1.1. VolumeKnob WCap

Bit	Bitfield Name	RW	Reset	Description
[23.:20]	Type	R	6	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:0]	Rsvd1	R	0	Reserved.

8.32.2. VolumeKnob VolKnobCap

	Verb ID	Payload	Response
Get	F00	13	See bitfield table.

8.32.2.1. VolumeKnob VolKnobCap

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Delta	R	1	Indicates if software can write a base volume to the Volume Control Knob.
[6.:0]	NumSteps	R	7F	Number of gains steps (number of possible settings - 1).

8.32.3. VolumeKnob ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

8.32.3.1. VolumeKnob ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	02	Number of NID entries in connection list.

8.32.4. VolumeKnob ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

8.32.4.1. VolumeKnob ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	11	DAC1 Converter widget (0x11)
[7.:0]	ConL0	R	10	DAC0 Converter widget (0x10)

8.32.5. VolumeKnob UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

8.32.5.1. VolumeKnob UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled, 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

8.32.6. VolumeKnob Cntrl

	Verb ID	Payload	Response
Get	F0F	00	See bitfield table.

8.32.6.1. VolumeKnob Cntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Direct	RW	0	Direct = 1 causes the volume control to directly control the hardware volume of the slave amps. Direct = 0 causes unsolicited responses to be generated.
[6.:0]	Volume	RW	7F	Volume, specified in steps of amplifier gain

8.32.7. VolumeKnob Update

	Verb ID	Payload	Response
Get	FE0	00	See bitfield table.

8.32.7.1. VolumeKnob Update

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0000000	Reserved.
[3]	Continuous	RW	1	Allow continuous incrementing/decrementing of the volume knob value.
[2.:0]	Rate	RW	0	Volume knob update rate, for continuous mode and de-bouncing (0..7 = 2.5..20Hz, in increments of 2.5Hz)

9. DISCLAIMER

While the information presented herein has been checked for both accuracy and reliability, manufacturer assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements, are not recommended without additional processing by manufacturer. Manufacturer reserves the right to change any circuitry or specifications without notice. Manufacturer does not authorize or warrant any product for use in life support devices or critical medical instruments.

10. PINOUTS

10.1. Pin Assignment

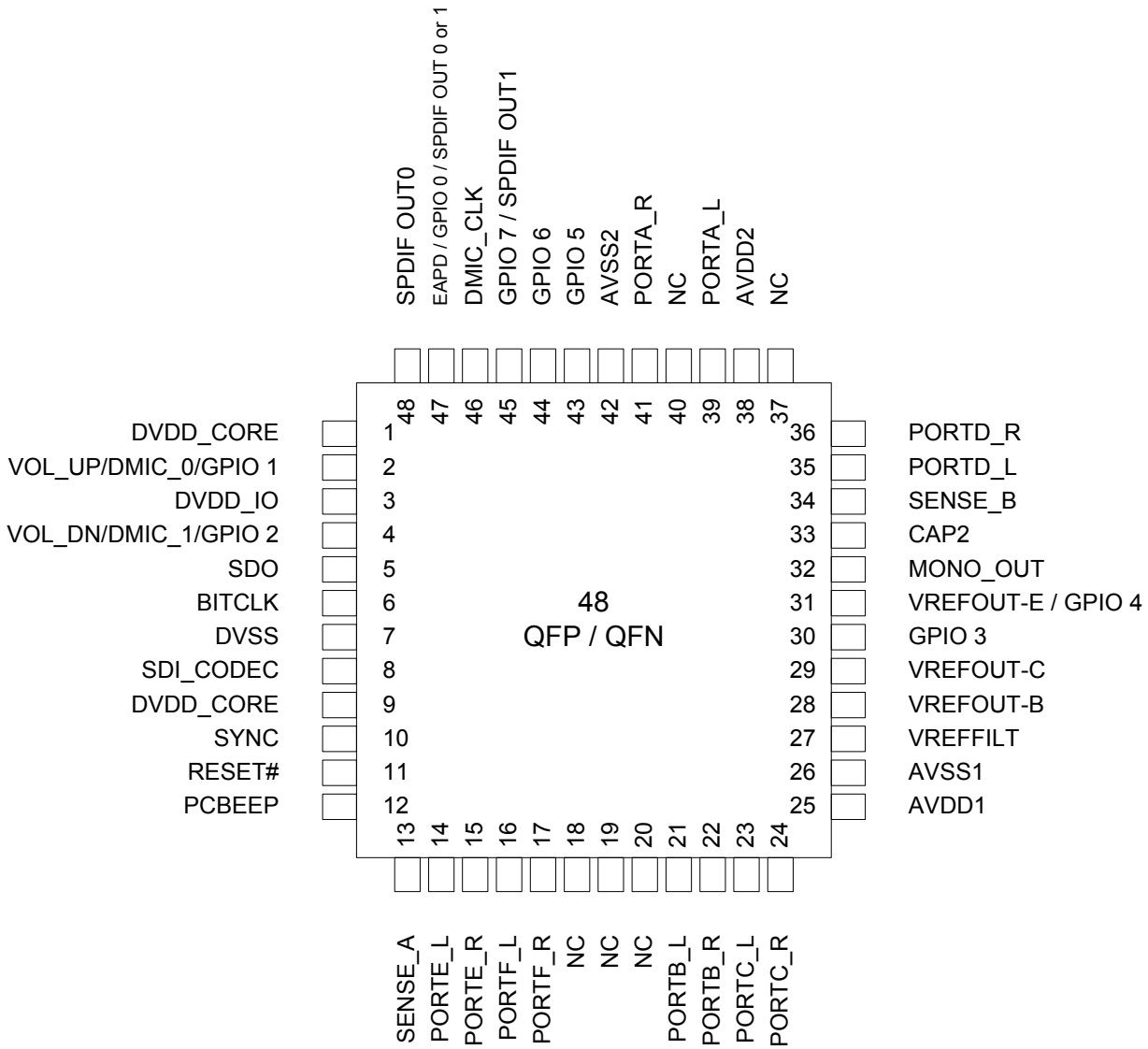


Figure 12. Pin Assignment

10.2. Pin Descriptions

Table 20. Pin Description

Pin No.	Pin Name	Pin Type	Internal Pull-up/ Pull-down	Pin Description
1	DVDD_CORE	I(Digital)	None	Digital Vdd = 3.3 V
2	Volume Up / DMIC0 / GPIO1	I/O(Digital)	50 KΩ pull-up with Volume or GPIO 50 KΩ pull-down with Digital Microphone	Volume Control or Digital Microphone 0 Input or General Purpose I/O
3	DVDD_IO	I(Digital)	None	Reference Voltage (1.5 V or 3.3 V)
4	Volume Down / DMIC1 / GPIO2	I/O(Digital)	50 KΩ pull-up with Volume or GPIO 50 KΩ pull-down with Digital Microphone	Volume Control or Digital Microphone 1 Input or General Purpose I/O
5	SDO	I/O(Digital)	None	HD Audio Serial Data output (inbound stream)
6	BITCLK	I(Digital)	None	HD Audio Bit Clock
7	DVSS	I(Digital)	None	Digital Ground
8	SDI_CODEC	O(Digital)	None	HD Audio Serial Data (outbound stream), audio module
9	DVDD_CORE	I(Digital)	None	Digital Vdd = 3.3 V
10	SYNC	I(Digital)	None	HD Audio Frame Sync
11	RESET#	I(Digital)	None	HD Audio Reset
12	PCBEEP	I(Analog)	None	PC Beep
13	SENSE_A	I(Analog)	None	Jack insertion detection Ports A, B, C, D
14	PORTE_L	I(Analog)	None	Port E Input Left
15	PORTE_R	I(Analog)	None	Port E Input Right
16	PORTF_L	O(Analog)	None	Port F Output Left
17	PORTF_R	O(Analog)	None	Port F Output Right
18	NC	-	None	No Connect
19	NC	-	None	No Connect
20	NC	-	None	No Connect
21	PORTB_L	I(Analog)	None	Port B Input Left
22	PORTB_R	I(Analog)	None	Port B Input Right
23	PORTC_L	I(Analog)	None	Port C Input Left
24	PORTC_R	I(Analog)	None	Port C Input Right

Table 20. Pin Description

Pin No.	Pin Name	Pin Type	Internal Pull-up/ Pull-down	Pin Description
25	AVDD1	I(Analog)	None	Analog Vdd = 5.0 V or 3.3 V
26	AVSS1	I(Analog)	None	Analog Ground
27	VREFFILT	O(Analog)	None	Analog Virtual Ground
28	VREFOUT-B	O(Analog)	None	Reference Voltage out drive (intended for microphone bias) for Port B
29	VREFOUT-C	O(Analog)	None	Reference Voltage out drive (intended for microphone bias) for Port C
30	GPIO3	I/O(Analog)	None	General Purpose I/O
31	VREFOUT-E / GPIO4	I/O(Analog)	None	Reference Voltage out drive (intended for microphone bias) for Port E or analog GPIO4
32	MONO_OUT	O(Analog)	None	Mono output of DAC0
33	CAP2	O(Analog)	None	ADC reference Capacitor
34	SENSE_A	I(Analog)	None	Jack insertion detection Ports E, F
35	PORT-D_L	O(Analog)	None	Port D Output Left
36	PORT-D_R	O(Analog)	None	Port D Output Right
37	NC	-	None	No Connect
38	AVDD2	I(Analog)	None	Analog Vdd = 5.0 V or 3.3 V
39	PORTA_L (HP)	O(Analog)	None	Port A Output Left
40	NC	-	None	No Connect
41	PORTA_R (HP)	O(Analog)	None	Port A Output Right
42	AVSS2	I(Analog)	None	Analog Ground
43	GPIO5	I/O (Digital)	50 KΩ pull-up	General Purpose I/O
44	GPIO6	I/O (Digital)	50 KΩ pull-up	General Purpose I/O
45	GPIO7 / SPDIFOUT1	I/O (Digital)	50 KΩ pull-down	General Purpose I/O or Second SPDIF output
46	DMIC_CLK	O(Digital)	50 KΩ pull-down	Digital Microphone Output Clock
47	GPIO0/EAPD/ SPDIF-OUT0or1	I/O(Digital)	50 KΩ pull-up	General Purpose I/O, EAPD, SPDIF Out
48	SPDIF-OUT0	O(Digital)	50 KΩ pull-down	SPDIF digital output

11. PACKAGE OUTLINE AND PACKAGE DIMENSIONS

Package dimensions are kept current with JEDEC Publication No. 95

11.1. 48-Pad QFN Package

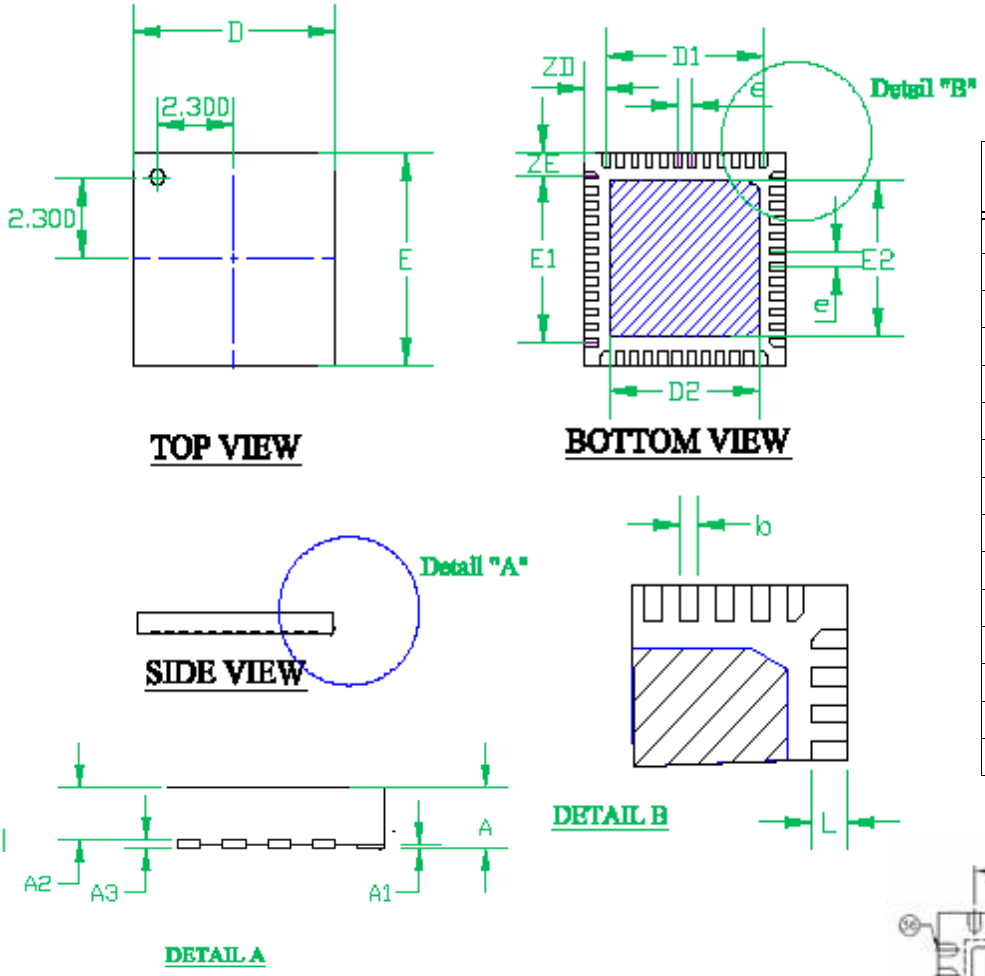


Table 21:

Key	QFN Dimensions in mm		
	Min	Nom	Max
A	0.80	0.90	1.0
A1	0.00	0.02	0.05
A3		0.20 REF	
D		7.00 BSC	
D1		5.50 BSC	
E		7.00 BSC	
E1		5.50 BSC	
L	0.35	0.40	0.45
e		0.50 BSC	
R		0.20-0.25	
b	0.18	0.25	0.30
D2	5.50	5.65	5.80
E2	5.50	5.65	5.80
ZD		0.75 BSC	
ZE		0.75 BSC	

Additional Approved Option

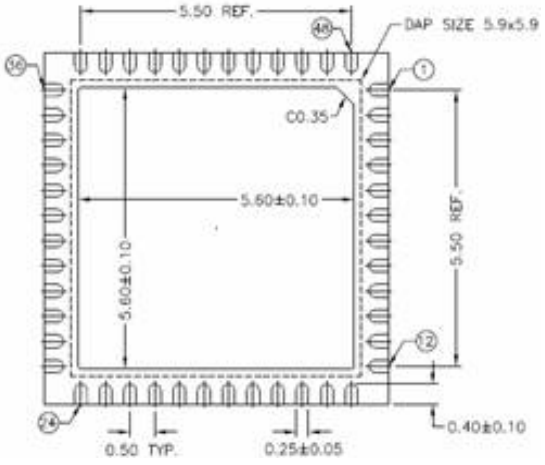


Figure 13. 48-pad QFN Package Drawing

11.2. 48-Pin QFP Package

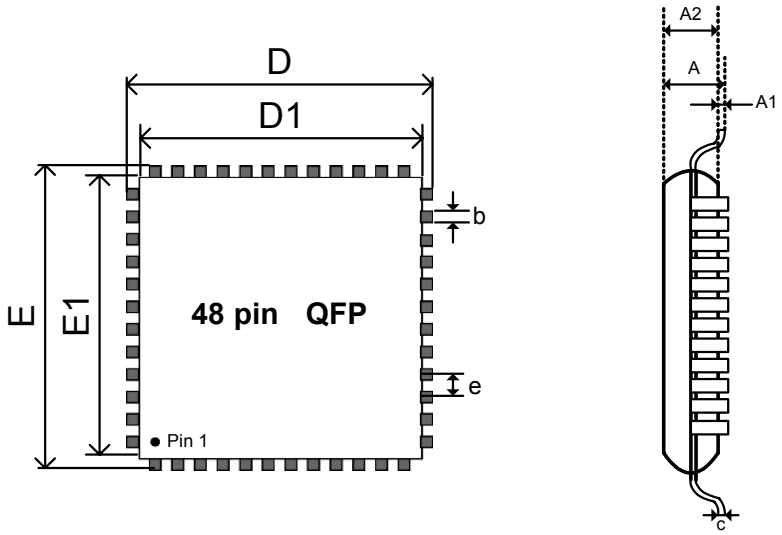


Table 22:

Key	QFP Dimensions in mm		
	Min	Nom	
A	1.40	1.50	
A1	0.05	0.10	
A2	1.35	1.40	
D	8.80	9.00	
D1	6.90	7.00	
E	8.80	9.00	
E1	6.90	7.00	
L	0.45	0.60	
e		0.50	
c	0.09	-	
b	0.17	0.22	

Figure 14. 48-pin QFP Package Drawing

12. SOLDER REFLOW PROFILE

12.1. Standard Reflow Profile Data

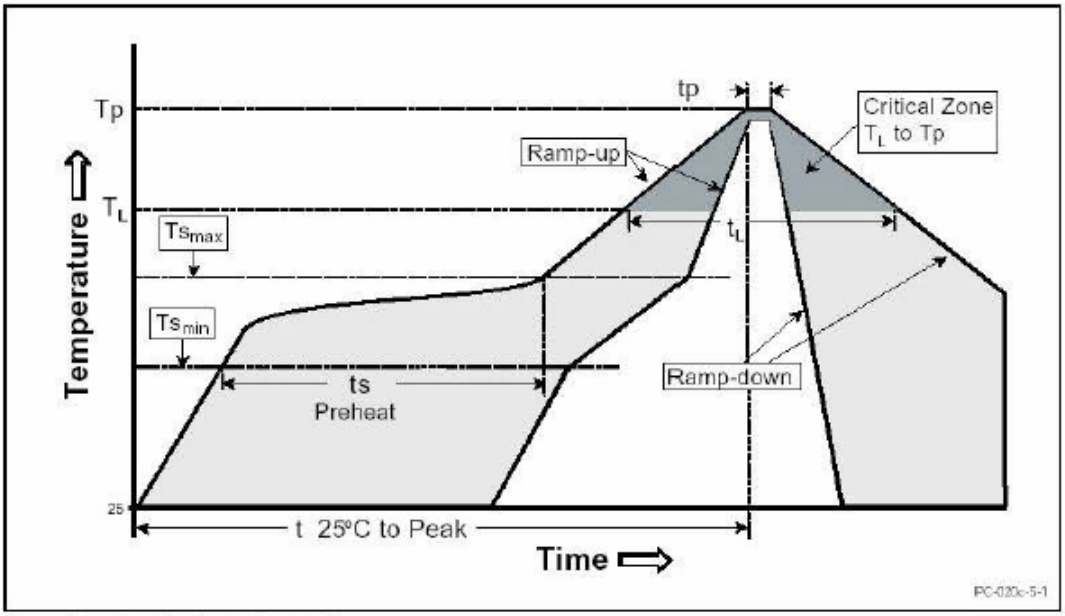
Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices" (www.jedec.org/download).

Table 23. Standard Reflow Profile

Profile Feature		Pb Free Assembly
Average Ramp-Up Rate (Ts_{max} - Tp)		3 °C / second max
Preheat:	Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (ts_{min} - ts_{max})	150 °C 200 °C 60 - 180 seconds
Time maintained above:	Temperature (T_L) Time (t_L)	217 °C 60 - 150 seconds
Peak / Classification Temperature (Tp)		See "Package Classification Reflow Temperatures" on page 215.
Time within 5 °C of actual Peak Temperature (tp)		20 - 40 seconds
Ramp-Down rate		6 °C / second max
Time 25 °C to Peak Temperature		8 minutes max
Note: All temperatures refer to topside of the package, measured on the package body surface.		

Figure 15. Solder Reflow Profile



12.2. Pb Free Process - Package Classification Reflow Temperatures

Table 24. Pb-Free Process Reflow

Package Type	MSL	Reflow Temperature
QFP 48-pin	3	260 ^{o}C
QFN 48-pad	3	260 ^{o}C

13. REVISION HISTORY

Revision	Date	Description of Change
0.8	March 21, 2007	Initial release
0.9	July 13, 2007	seperated B8, B7, B5 versions to individual datasheets, added orderable part numbers, updated performance and power numbers based on characterization, corrected I/O labeling in pin table
0.91	Sept 26, 2007	added feature bullet for GUI, corrected pin 34 from no connect to SENSE_B in pinout graphic and table, added 4 port confirguration diagram
0.92	Nov 14, 2007	Added AFG Misc widget, B3 silicon revision adds this functionality
1.0	January 23, 2008	Removed Preliminary and confidential, corrected all THD number unit to dBr. Performance numbers updated based on characterization. Latchup/ESD specifications clarified/updated.

Innovate with IDT audio for high fidelity. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
HA.CM@idt.com

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

© 2006 Integrated Device Technology, Inc. All rights reserved. Product specifications subject to change without notice. IDT and the IDT logo are trademarks of Integrated Device Technology, Inc. Accelerated Thinking is a service mark of Integrated Device Technology, Inc. All other brands, product names and marks are or may be trademarks or registered trademarks used to identify products or services of their respective owners.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View IDT92HD71B7X5NLGXB3X8 on WIN SOURCE
- IDT, Integrated Device Technology Inc Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management