



**THE DATASHEET OF
TC74AC573FW-ELP**



OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74AC573 is an advanced high speed CMOS OCTAL LATCH fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

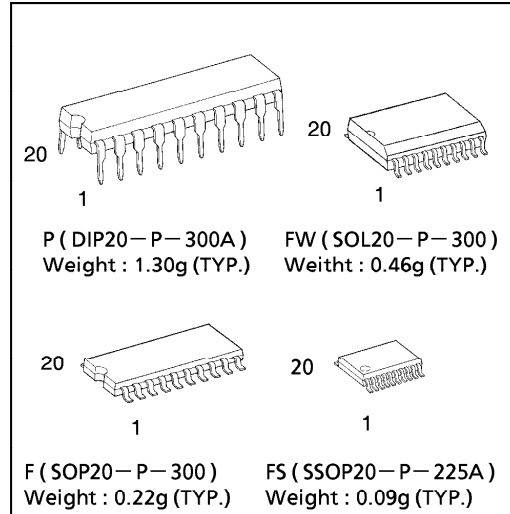
FEATURES :

- High Speed..... $t_{pd} = 6.0ns$ (typ.) at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 8\mu A$ (Max.) at $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24mA$ (Min.)
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... V_{CC} (opr) = $2V \sim 5.5V$
- Pin and Function Compatible with 74F573

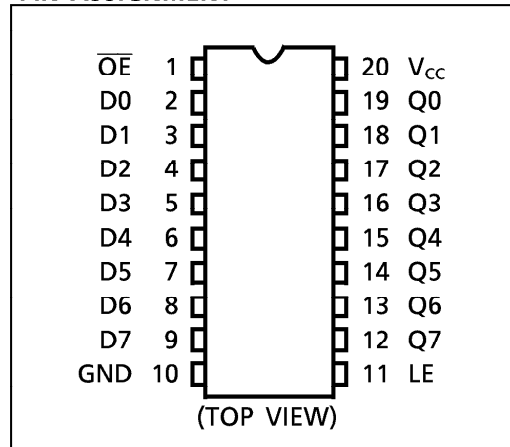
TRUTH TABLE

| INPUTS | | | OUTPUTS |
|--------|----|---|----------------|
| OE | LE | D | Q |
| H | X | X | Z |
| L | L | X | Q _n |
| L | H | L | L |
| L | H | H | H |

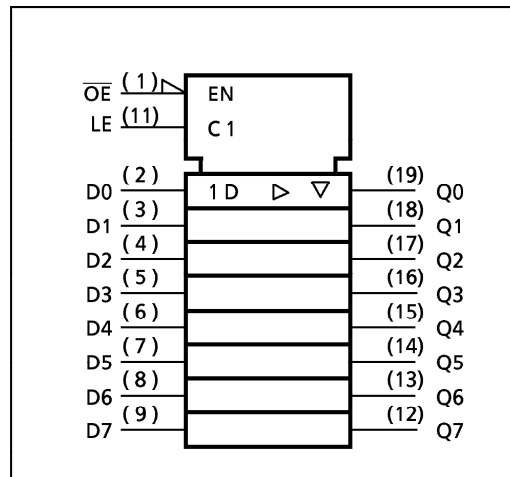
X : Don't Care
Z : High Impedance
Q_n: Q outputs are latched at the time when the LE input is taken to a low logic level.



PIN ASSIGNMENT



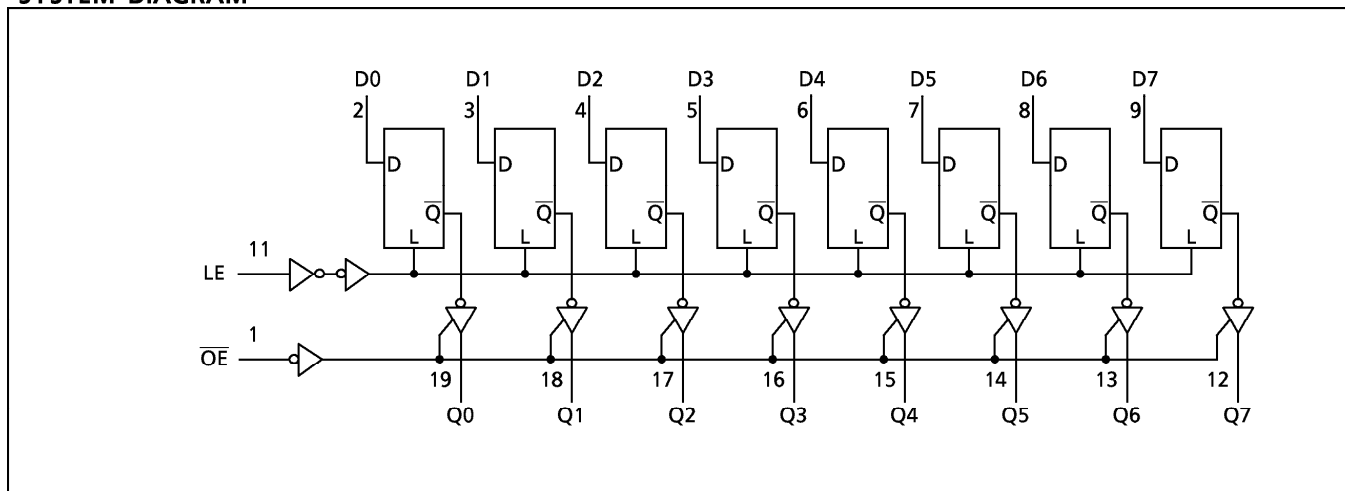
IEC LOGIC SYMBOL



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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|-----------------------------|-----------|-----------------------------|-------------|
| Supply Voltage Range | V_{CC} | -0.5~7.0 | V |
| DC Input Voltage | V_{IN} | -0.5~ $V_{CC} + 0.5$ | V |
| DC Output Voltage | V_{OUT} | -0.5~ $V_{CC} + 0.5$ | V |
| Input Diode Current | I_{IK} | ± 20 | mA |
| Output Diode Current | I_{OK} | ± 50 | mA |
| DC Output Current | I_{OUT} | ± 50 | mA |
| DC V_{CC} /Ground Current | I_{CC} | ± 200 | mA |
| Power Dissipation | P_D | 500 (DIP)* / 180 (SOP/SSOP) | mW |
| Storage Temperature | T_{stg} | -65~150 | $^{\circ}C$ |

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | VALUE | UNIT |
|--------------------------|-----------|---|-------------|
| Supply Voltage | V_{CC} | 2.0~5.5 | V |
| Input Voltage | V_{IN} | 0~ V_{CC} | V |
| Output Voltage | V_{OUT} | 0~ V_{CC} | V |
| Operating Temperature | T_{opr} | -40~85 | $^{\circ}C$ |
| Input Rise and Fall Time | dt/dV | 0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$) | ns/V |

DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | V _{CC} (V) | Ta = 25°C | | | Ta = -40~85°C | | UNIT | |
|--------------------------------------|-----------------|---|---|----------------------|-------------------|----------------------|----------------------|----------------------|----------------------|---|
| | | | | MIN. | TYP. | MAX. | MIN. | MAX. | | |
| High - Level Input Voltage | V _{IH} | | 2.0 3.0 5.5 | 1.50 2.10 3.85 | — — — | — — — | 1.50 2.10 3.85 | — — — | V | |
| Low - Level Input Voltage | V _{IL} | | 2.0 3.0 5.5 | — — — | — — — | 0.50 0.90 1.65 | — — — | 0.50 0.90 1.65 | V | |
| High - Level Output Voltage | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -50μA | 2.0 3.0 4.5 | 1.9 2.9 4.4 | 2.0 3.0 4.5 | — — — | 1.9 2.9 4.4 | — — — | V |
| | | | I _{OH} = -4mA I _{OH} = -24mA I _{OH} = -75mA* | 3.0 4.5 5.5 | 2.58 3.94 — | — — — | — — — | 2.48 3.80 3.85 | — — — | |
| | | | I _{OL} = 50μA | 2.0 3.0 4.5 | — — — | 0.0 0.0 0.0 | 0.1 0.1 0.1 | — — — | 0.1 0.1 0.1 | |
| Low - Level Output Voltage | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 12mA I _{OL} = 24mA I _{OL} = 75mA* | 3.0 4.5 5.5 | — — — | — — — | 0.36 0.36 — | — — — | 0.44 0.44 1.65 | V |
| | | | I _{OL} = 50μA | 2.0 3.0 4.5 | — — — | 0.0 0.0 0.0 | 0.1 0.1 0.1 | — — — | 0.1 0.1 0.1 | |
| | | | I _{OL} = 50μA | 2.0 3.0 4.5 | — — — | 0.0 0.0 0.0 | 0.1 0.1 0.1 | — — — | 0.1 0.1 0.1 | |
| 3 - State Output Off - State Current | I _{OZ} | V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND | 5.5 | — | — | ± 0.5 | — | ± 5.0 | μA | |
| Input Leakage Current | I _{IN} | V _{IN} = V _{CC} or GND | 5.5 | — | — | ± 0.1 | — | ± 1.0 | | |
| Quiescent Supply Current | I _{CC} | V _{IN} = V _{CC} or GND | 5.5 | — | — | 8.0 | — | 80.0 | | |

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

| PARAMETER | SYMBOL | TEST CONDITION | Ta = 25°C | | Ta = -40~85°C | | UNIT |
|--------------------------|--------------------|----------------|---------------------|-------|---------------|----|------|
| | | | V _{CC} (V) | LIMIT | LIMIT | | |
| Minimum Pulse Width (LE) | t _W (H) | | 3.3 ± 0.3 | 7.0 | 7.0 | ns | |
| | | | 5.0 ± 0.5 | 5.0 | 5.0 | | |
| Minimum Set - up Time | t _s | | 3.3 ± 0.3 | 7.0 | 7.0 | | |
| | | | 5.0 ± 0.5 | 4.0 | 4.0 | | |
| Minimum Hold Time | t _h | | 3.3 ± 0.3 | 1.0 | 1.0 | | |
| | | | 5.0 ± 0.5 | 1.0 | 1.0 | | |

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

| PARAMETER | SYMBOL | TEST CONDITION | Ta = 25°C | | | Ta = -40~85°C | | UNIT | |
|----------------------------------|--------------------------------------|----------------|---------------------|------|------|---------------|------|------|------|
| | | | V _{CC} (V) | MIN. | TYP. | MAX. | MIN. | | MAX. |
| Propagation Delay Time (LE-Q) | t _{pLH} t _{pHL} | | 3.3 ± 0.3 | — | 9.4 | 15.4 | 1.0 | 17.6 | ns |
| | | | 5.0 ± 0.5 | — | 6.6 | 9.9 | 1.0 | 11.3 | |
| Propagation Delay Time (Dn-Q) | t _{pLH} t _{pHL} | | 3.3 ± 0.3 | — | 9.4 | 16.0 | 1.0 | 18.2 | |
| | | | 5.0 ± 0.5 | — | 6.2 | 8.9 | 1.0 | 10.2 | |
| Output Enable Time | t _{pZL} t _{pZH} | | 3.3 ± 0.3 | — | 9.0 | 15.2 | 1.0 | 17.3 | |
| | | | 5.0 ± 0.5 | — | 6.3 | 9.2 | 1.0 | 10.5 | |
| Output Disable Time | t _{pLZ} t _{pHZ} | | 3.3 ± 0.3 | — | 7.0 | 12.3 | 1.0 | 14.0 | |
| | | | 5.0 ± 0.5 | — | 6.0 | 8.8 | 1.0 | 10.0 | |
| Input Capacitance | C _{IN} | | | — | 5 | 10 | — | 10 | pF |
| Output Capacitance | C _{OUT} | | | — | 10 | — | — | — | |
| Power Dissipation Capacitance | C _{PD} (1) | | | — | 32 | — | — | — | |

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

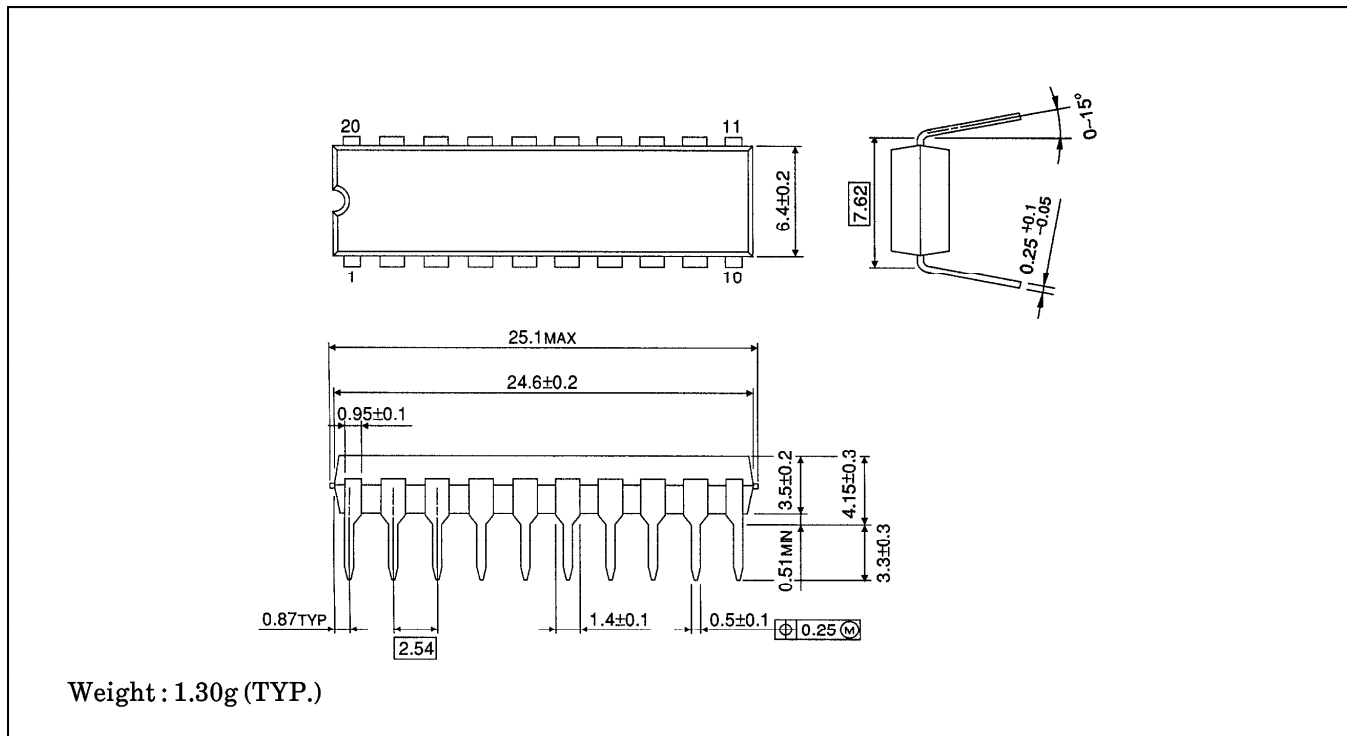
$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per Latch)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 21 + 11 \cdot n$$

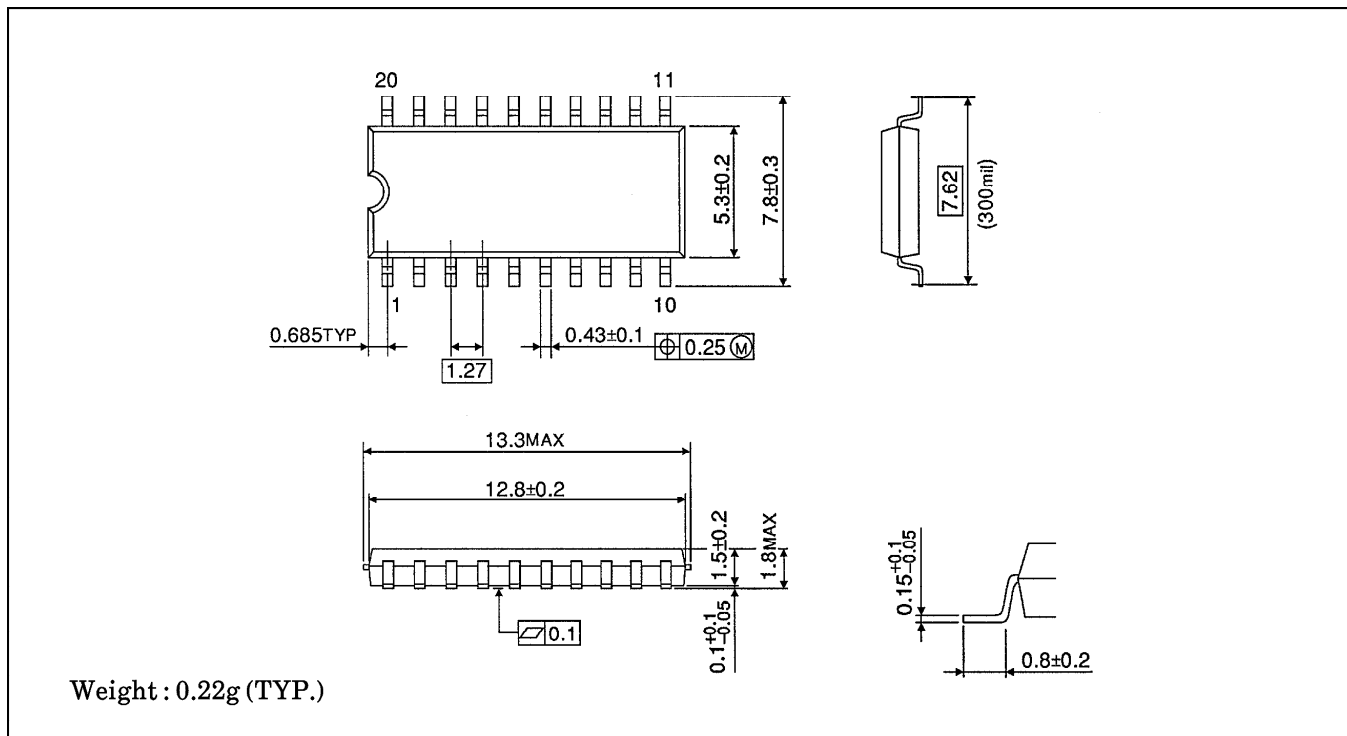
DIP 20PIN OUTLINE DRAWING (DIP20-P-300A)

Unit in mm



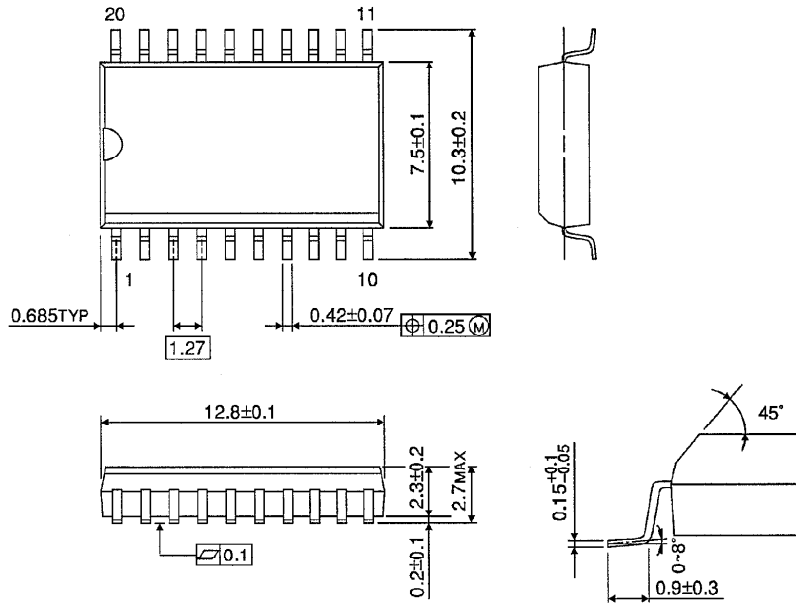
SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300)

Unit in mm



SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300)

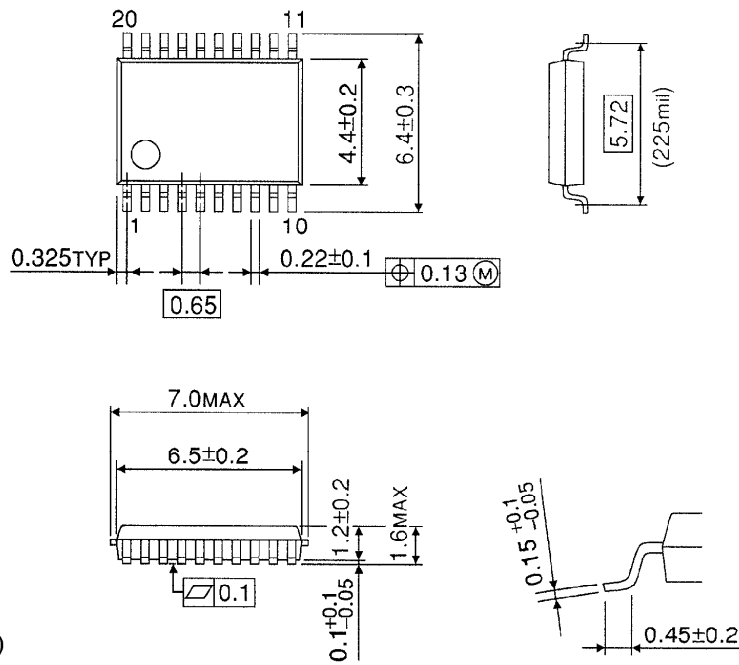
Unit in mm



Weight : 0.46g (TYP.)

SSOP 20PIN OUTLINE DRAWING (SSOP20-P-225A)

Unit in mm



Weight : 0.09g (TYP.)

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