



THE DATASHEET OF U4256BM-NFSG3



Frequency Synthesizer for Radio Tuning

Description

The U4256BM is a synthesizer IC for FM receiver and an AM up-conversion system in BICMOS technology. Together with the AM/FM IC U4255BM, it performs a complete AM/FM car radio front end, which is

recommended also for RDS (Radio Data System) applications. It is controlled by 3-wire bus and contains also switches and Digital to Analog Converters (DACs) for software controlled alignment of the AM/FM tuner.

Features

- Reference oscillator up to 15 MHz (tuned)
- Oscillator buffer output (for AM up/down conversion)
- Two programmable 16-bit dividers
- Fine-tuning steps possible
- Fast response time due to integrated loop push-pull stage
- 3-wire bus (enable, clock and data; 3 V and 5 V micro-controllers acceptable)
- Four programmable switching outputs (open drain)
- Three DACs for software controlled tuner alignment
- Low power consumption
- High S/N ratio
- Integrated band gap – only one supply voltage necessary

Block Diagram

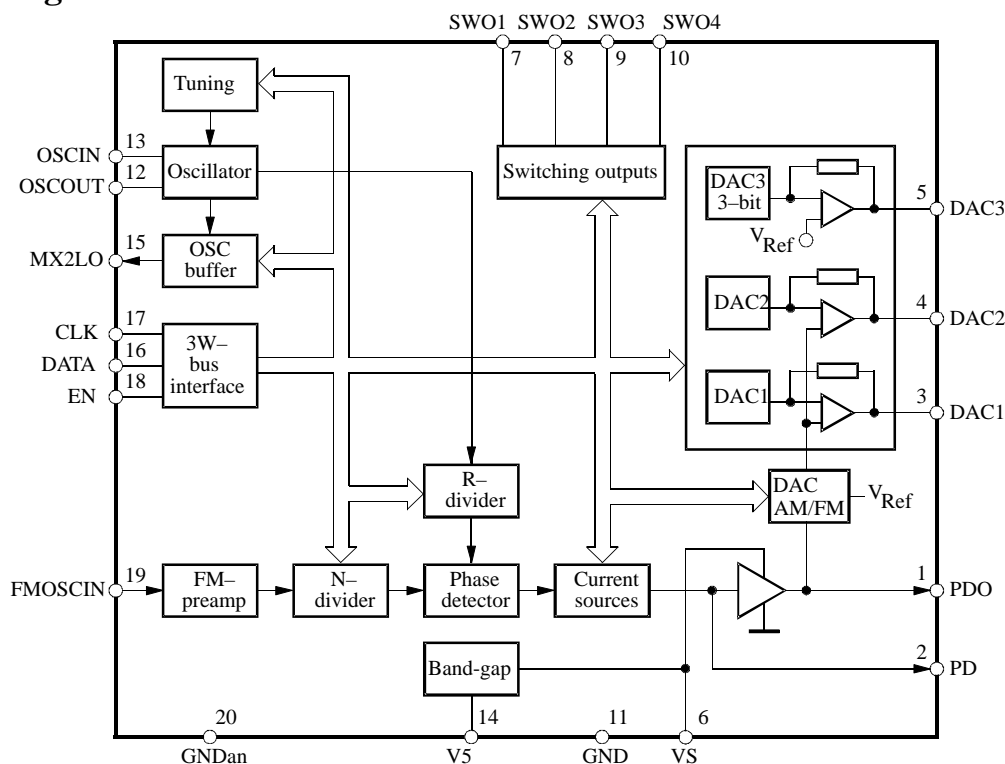


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U4256BM-NFS	SSO20	Tube
U4256BM-NFSG3	SSO20	Taped and reeled

Pin Description

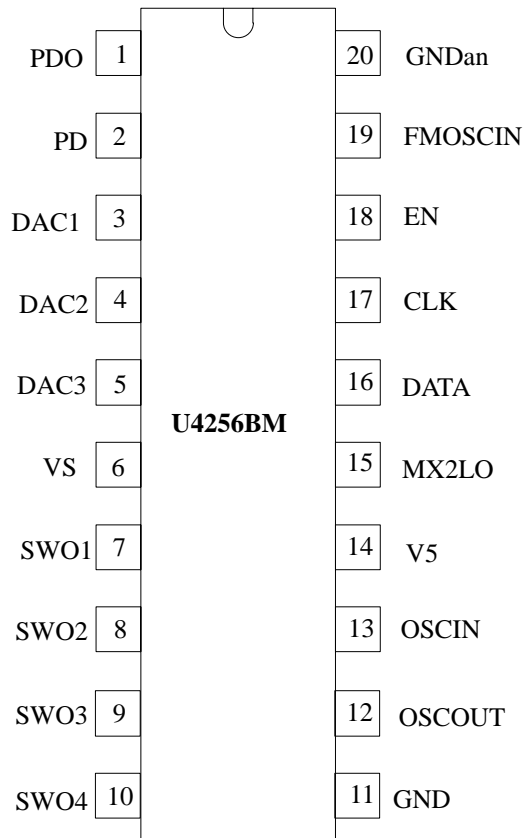


Figure 2. Pinning

Pin	Symbol	Function
1	PDO	Phase detector output
2	PD	Pulsed current output
3	DAC1	Digital-to-analog converter 1
4	DAC2	Digital-to-analog converter 2
5	DAC3	Digital-to-analog converter 3
6	VS	Supply voltage analog part
7	SWO1	Switching output 1
8	SWO2	Switching output 2
9	SWO3	Switching output 3
10	SWO4	Switching output 4
11	GND	Ground, digital part
12	OSCOUT	Reference oscillator output
13	OSCIN	Reference oscillator input
14	V5	Capacitor band gap
15	MX2LO	Oscillator buffer output
16	DATA	Data input
17	CLK	Clock
18	EN	Enable
19	FMOSCIN	FM-oscillator input
20	GNDan	Ground, analog part

Functional Description

For a tuned FM – broadcast receiver, the following parts are needed:

- voltage-controlled oscillator (VCO)
- antenna amplifier tuned circuit
- RF amplifier tuned circuit

Typical modern receivers with electronic tuning are tuned to the desired FM frequency by the frequency synthesizer IC U4256BM. The special design allows to build software-controlled tuner alignment systems. Two programmable DACs (Digital-to-Analog Converter) support the computer-controlled alignment. The output of the PLL is a tuning voltage which is connected to the VCO of the receiver IC. The output of the VCO is equal to the desired station frequency plus the IF (10.7 MHz). The RF and the oscillator signal (VCO) are both input to the mixer that translates the desired FM channel signal to the fixed IF signal. For FM, the double-conversion system of the receiver requires exactly 10.7 MHz for the first IF frequency, which determines the center frequency of the software-controlled integrated second IF filter.

If this oscillator tuning feature is not used, the internal capacities have to be switched off and the oscillator has to be operated with high-quality external capacities to ensure that the operational frequency is exactly 10.250 MHz.

When dimensioning the oscillator circuit, it is important that the additional capacities enable the oscillator to operate through its complete tracking range. The oscillating ability depends very strongly on the used crystal oscillator. Initializing the oscillator should be established without switching any additional capacities to guarantee that the oscillator starts to operate properly. Due to the lower quality of the integrated capacities compared to discrete capacities, the amount of the switched integrated capacities should always be minimized. (if necessary reduce tracking range or use another crystal oscillator)

The U4256BM has a very fast response time of maximum 800 μs (at 2 mA, fref = 100 kHz, measured on MPX signal). It performs a high signal to noise ratio.

Only one supply voltage is necessary, due to a integrated band gap.

Absolute Maximum Ratings

All voltages are referred to GND (Pin 11)

Parameters	Symbol	Value	Unit
Analog supply voltage Pin 6	V_S	8 to 15	V
Input voltage BUS Pins 16, 17 and 18	V_I	-0.3 to +12	V
Output current switches (see figure 10) Pins 7, 8, 9 and 10	I_O	-1 to +5	mA
Drain voltage switches Pins 7, 8, 9 and 10	V_{OD}	15	V
Ambient temperature range	T_{amb}	-40 to +85	°C
Storage temperature range	T_{stg}	-40 to +125	°C
Junction temperature	T_j	125	°C
Electrostatic handling	V_{ESD}	t.b.d.	V

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient when soldered to PCB	R_{thJA}	140	K/W

Operating Range

All voltages are referred to GND (Pin 11)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range Pin 6	V_S	8	8.5	14	V
Ambient temperature	T_{amb}	-40		+85	°C
Input frequency FMOSCIN Pin 19	f_{in}	70		160	MHz
Programmable N, R divider	SF	2		65535	
Crystal reference oscillator Pins 12 and 13	fXTAL	0.1		15	MHz

Electrical Characteristics

Test conditions (unless otherwise specified): $V_S = +8.5$ V, $T_{amb} = +25$ °C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage Pin 6						
Analog supply voltage		V_S	8	8.5	12	V
Supply current Pin 20						
Analog supply current		I_S	4.5	10	20	mA
OSCIN Pin 13						
Input voltage	f = 0.1 to 15 MHz	OSC	100			mV _{rms}
OSC buffer (MX2LO) Pin 15						
Output AC voltage	At Pin15: 47 pF and 1 kΩ	V_{MX2LO}	80	120	200	mV _{pp}
Output DC voltage		V_{MX2LO}	1.6	1.9	2.1	V
FMOSCIN Pin 19						
Input voltage	f = 70 to 120 MHz	FMOSC	40			mV _{rms}
	f = 120 to 160 MHz	FMOSC	150			mV _{rms}

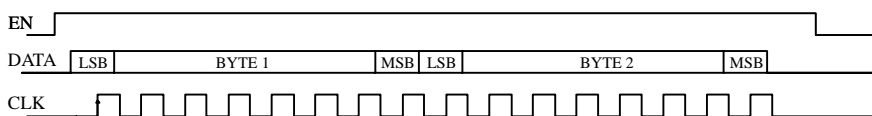
Electrical Characteristics (continued)

Test conditions (unless otherwise specified): $V_S = +8.5\text{ V}$, $T_{amb} = +25^\circ\text{C}$

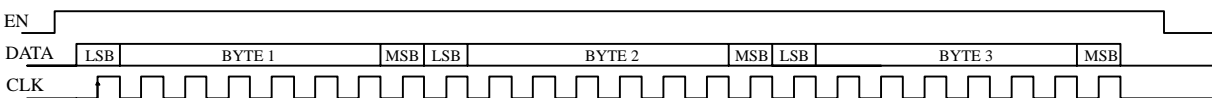
Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Pulsed current output PD						
Pin 2						
Output current Bit 71, 70 = '00'	PD = 2.5 V	± IPD	20	25	30	μA
Output current Bit 71, 70 = '001'			80	100	120	μA
Output current Bit 71, 70 = '10'			400	500	600	μA
Output current Bit 71, 70 = '11'			1600	2000	2400	μA
Leakage current	PD = 2.5 V	± IPDL			20	nA
PDO						
Pin 1						
Saturation voltage HIGH LOW	I = 15 mA	V_{PDOH} V_{PDOL}	0.1	0.2	$V_S - 0.5$ 0.4	V V
SWO1, SWO2, SWO3, SWO4 (open drain) Pins 7, 8, 9 and 10						
Output leakage current HIGH	V7,8,9,10 = 8.5 V	I_{SWOH}			100	nA
Output voltage LOW	I = 1 mA	V_{SWOL}		100	400	mV
DAC1, DAC2						
Pins 3 and 4						
Output current		$I_{DAC1,2}$			± 1	mA
Output voltage		$V_{DAC1,2}$	0.3		$V_S - 0.5$	V
Gain range (resolution 256 steps)			0.6		2.3	
Offset range (resolution 24 steps)			-0.6		0.7	V
DAC 3						
Pin 5						
Output current		I_{DAC3}			± 1	mA
Output voltage (resolution 16 steps)		V_{DAC3}	0.25		6	V

3-Wire Bus Description

16-bit command



24-bit command



e.g., Divider

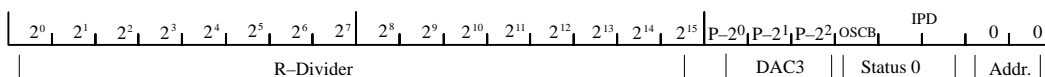


Figure 3. Pulse diagram

Data Transfer

A

MSB		Byte 3					LSB	MSB		BYTE 2					LSB	MSB		BYTE 1					LSB
ADDR		STATUS 0			DAC3			R - DIVIDER															
0	0	IPD		OSCB 0 = on, 1 = off	P-2 ²	P-2 ¹	P-2 ⁰	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
		B71	B70	B69	B68	B67	B66	B65	B64	B63	B62	B61	B60	B59	B58	B57	B56	B55	B54	B53	B52	B51	B50

B

MSB		Byte 3					LSB	MSB		BYTE 2					LSB	MSB		BYTE 1					LSB
ADDR		STATUS 1						N - DIVIDER															
0	1	0	AM=1 FM=0 DAC	SWO4 1=off, 0=on	SWO3 1=off, 0=on	SWO2 1=off, 0=on	SWO1 1=off, 0=on	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
		B35	B34	B33	B32	B31	B30	B29	B28	B27	B25	B24	B23	B22	B22	B21	B20	B19	B18	B17	B16	B15	B14

C

MSB		BYTE 2					LSB	MSB		BYTE 1					LSB
ADDR		DAC1 OFFSET						DAC1 GAIN							
0	0	O-2 ⁵	O-2 ⁴	O-2 ³	O-2 ²	O-2 ¹	O-2 ⁰	G-2 ⁷	G-2 ⁶	G-2 ⁵	G-2 ⁴	G-2 ³	G-2 ²	G-2 ¹	G-2 ⁰
		B49	B48	B47	B46	B45	B44	B43	B42	B41	B40	B39	B38	B37	B36

D

MSB		BYTE 2					LSB	MSB		BYTE 1					LSB
ADDR		DAC2 OFFSET						DAC2 GAIN							
0	1	O-2 ⁵	O-2 ⁴	O-2 ³	O-2 ²	O-2 ¹	O-2 ⁰	G-2 ⁷	G-2 ⁶	G-2 ⁵	G-2 ⁴	G-2 ³	G-2 ²	G-2 ¹	G-2 ⁰
		B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

E

MSB		BYTE 2					LSB	MSB		BYTE 1					LSB
ADDR		Oscillator tuning function						Not used							
1	0	8pF	32pF	16pF	8pF	4pF	2pF	1pF	0.5pF	X	X	X	X	X	X
		B85	B84	B83	B82	B81	B80	B79	B78	B77	B76	B75	B74	B73	B72

Timing Information

Parameters		Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
3-wire bus, ENABLE, DATA, CLOCK Pins 16, 17, 18							
Input voltage	HIGH		V_{BUSH}	2.0			V
	LOW		V_{BUSL}			1.0	V
Clock frequency						1.0	MHz
Period of CLK	HIGH		t_H	250			ns
	LOW		t_L	250			ns
Rise time EN, DATA, CLK			t_r			400	ns
Fall time EN, DATA, CLK			t_f			100	ns
Set-up time			t_s	100			ns
Hold time EN			t_{HEN}	250			ns
Hold time DATA			t_{HDA}	0			ns

Bus Timing

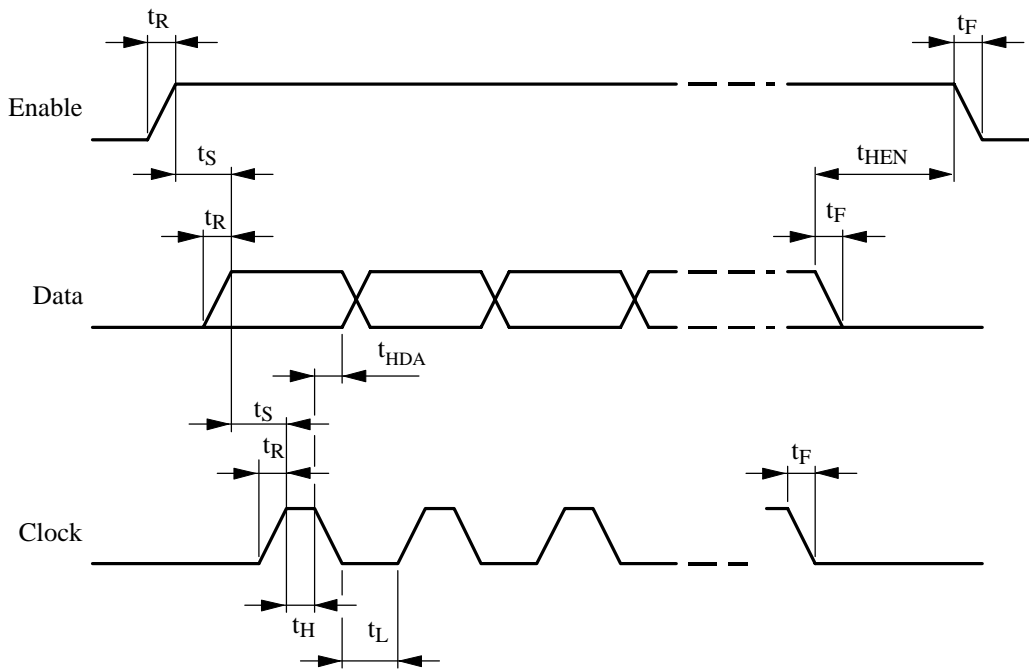


Figure 4. Bus timing

Bus Control

The charge-pump current can be chosen by setting the Bits 71 and 70 as following:

IPD (μA)	B71	B70
25	0	0
100	0	1
500	1	0
2000	1	1

The oscillator buffer output can be switched by the OSCB Bit as following (Bit 69):

MX2LO AC Voltage	B69
ON	0
OFF	1

The DAC3 output voltage can be controlled by the Bits P-2⁰ to P-2² (Bits 66 to 68) as following:

DAC3 Offset Approx.	B68	B67	B66
0.5 V	0	0	0
1.1 V	0	0	1
1.8 V	0	1	0
2.4 V	0	1	1
3.1 V	1	0	0
3.7 V	1	0	1
4.4 V	1	1	0
5.0 V	1	1	1

The switching output SWO1 to SWO4 can be controlled as following (Bits 30 to 33):

Switch Output	B29 + X
SWO _x = ON (switch to GND)	0
SWO _x = OFF	1

The DAC mode can be controlled by setting the Bit 34 as following:

DAC Mode	B34
FM	0
AM	1

The gains of DAC1 and DAC2 have a range of 0.7 x V(PDO) to 2.15 x V(PDO). V(PDO) is the PLL tuning voltage output. This range is divided into 256 steps. So one step is approximately (2.15-0.7)/256 = 5.664 m. The gain can be controlled by the Bits 36 to 43 (G-2⁰ to G-2⁷) as following:

Gain DAC1 Approx.	B43	B42	B41	B40	B39	B38	B37	B36
0.7	0	0	0	0	0	0	0	0
0.70566	0	0	0	0	0	0	0	1
0.71133	0	0	0	0	0	0	1	0
0.71699	0	0	0	0	0	0	1	1
...
1.00019	0	0	1	1	0	1	0	1
...
2.1386	1	1	1	1	1	1	0	1
2.14434	1	1	1	1	1	1	1	0
2.15	1	1	1	1	1	1	1	1

The offset of DAC1 has a range of 0.5 V to -0.6 V. This range is divided into 64 steps. So one step is approximately 1.1V/63 = 17.2 m. The offset can be controlled by the Bits 44 to 49 (O-2⁰ to O-2⁵) as following:

Offset DAC1 Approx. [V]	B49	B48	B47	B46	B45	B44
0.5	0	0	0	0	0	0
0.4828	0	0	0	0	0	1
0.4656	0	0	0	0	1	0
0.4484	0	0	0	0	1	1
...
-0.0156	0	1	1	1	1	0
...
0.5656	1	1	1	1	0	1
-0.5828	1	1	1	1	1	0
-0.6	1	1	1	1	1	1

The tuning capacity for the crystal oscillator has a range of 0.5 pF to 71.5 pF. The values are coded binary. The tuning can be controlled by the Bits 78 to 85 as following:

B85=0 pF	B85=1 pF	B84	B83	B82	B81	B80	B79	B78
0	8.0	1	1	1	1	1	1	1
0.5	8.5	1	1	1	1	1	1	0
1.0	9.0	1	1	1	1	1	0	1
1.5	19.5	1	1	1	1	1	0	0
...
63.0	71.0	0	0	0	0	0	0	0
63.5	71.5	0	0	0	0	0	0	0

The gain of DAC2 has a range of $0.7 \times V(\text{PDO})$ to $2.15 \times V(\text{PDO})$. $V(\text{PDO})$ is the PLL tuning voltage output. This range is divided into 256 steps. So one step is approximately $(2.15 - 0.7) / 256 = 5.664 \text{ m}$. The gain can be controlled by the bits 0 to 7 ($G-2^0$ to $G-2^7$) as following:

Gain DAC2 Approx.	B7	B6	B5	B4	B3	B2	B1	B0
0.7	0	0	0	0	0	0	0	0
0.70566	0	0	0	0	0	0	0	1
0.71133	0	0	0	0	0	0	1	0
0.71699	0	0	0	0	0	0	1	1
...
1.00019	0	0	1	1	0	1	0	1
...
2.1386	1	1	1	1	1	1	0	1
2.14434	1	1	1	1	1	1	1	0
2.15 m	1	1	1	1	1	1	1	1

The offset of DAC2 has a range of 0.5 to -0.6 . This range is divided into 64 steps. So one step is approximately $1.1\text{V}/63 = 17.2 \text{ m}$. The offset can be controlled by the Bits 8 to 13 ($O-2^0$ to $O-2^5$) as following:

Offset DAC2 Approx.	B13	B12	B11	B10	B9	B8
0.5	0	0	0	0	0	0
0.4828	0	0	0	0	0	1
0.4656	0	0	0	0	1	0
0.4484	0	0	0	0	1	1
...
-0.0156	0	1	1	1	1	0
...
0.5656	1	1	1	1	0	1
-0.5828	1	1	1	1	1	0
-0.6	1	1	1	1	1	1

Input / Output Interface Circuits

PDO

PDO is the loop amplifier output of the PLL. The bipolar output stage is a rail-to-rail amplifier.

PD

PD is the current charge pump output of the PLL. The current can be controlled by setting the Bits. The loop filter has to be designed corresponding to the chosen pump current and the internal reference frequency. A recommendation can be found in the application circuit.

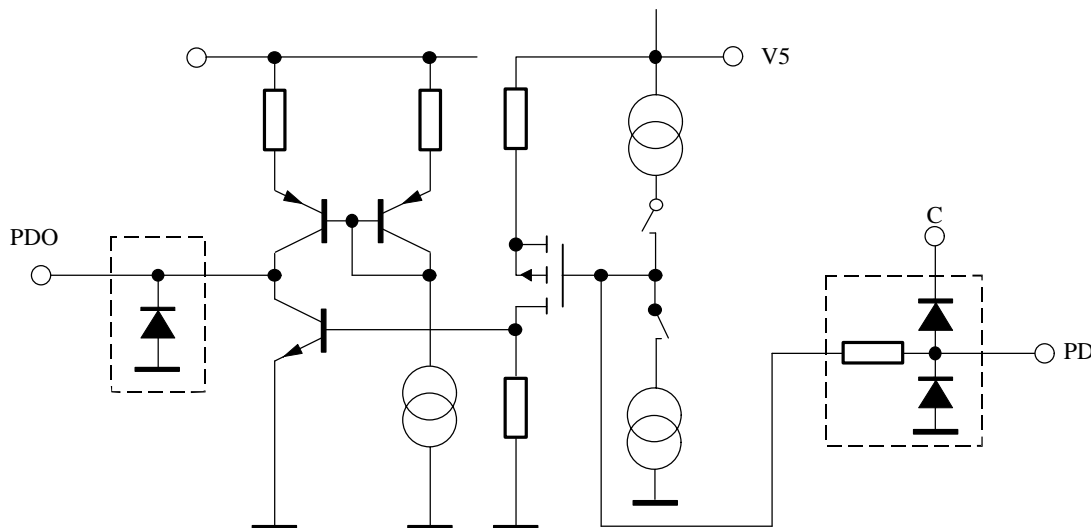


Figure 5.

FMOSCIN

FMOSCIN is the preamplifier input for the FM oscillator signal.

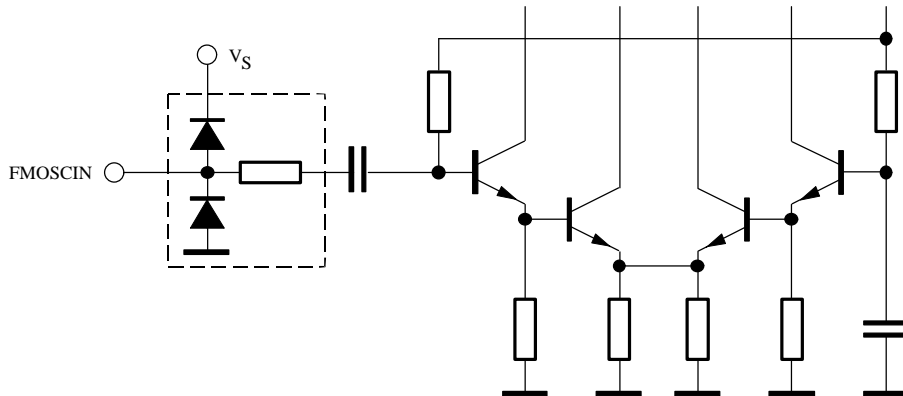


Figure 6.

MX2LO

MX2LO is the buffered output of the crystal oscillator. This signal can be used as a reference frequency for U4255BM.

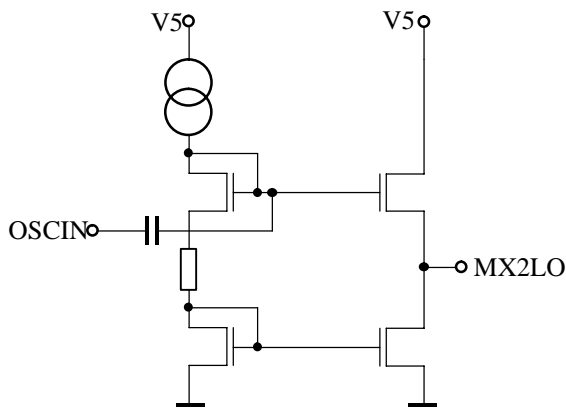


Figure 7.

EN, DATA, CLK

All functions can be controlled via a 3-wire bus consisting of ENABLE, DATA and CLOCK. The bus is designed for microcontrollers which operate with 3 V supply voltage. Details of the data transfer protocol are shown in the table 'Data Transfer'.

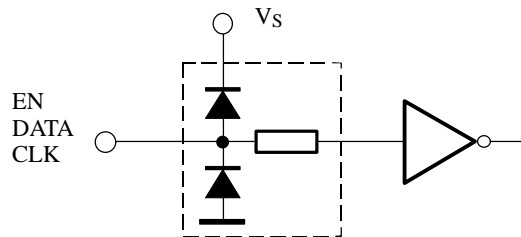


Figure 9.

DAC 1, 2 and 3

DAC 1 to 3 are the outputs for automatic tuner alignment.

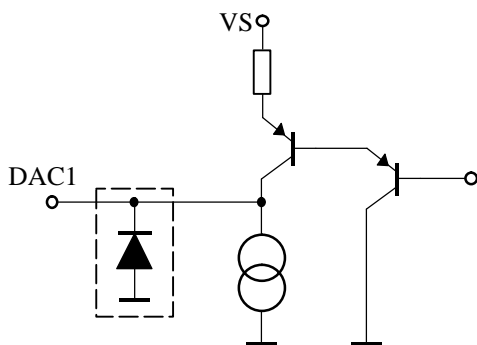


Figure 8.

SWO1, 2, 3 and 4

All switching outputs are 'open drain' and can be set and reset by software control. Details are described in the data transfer protocol.

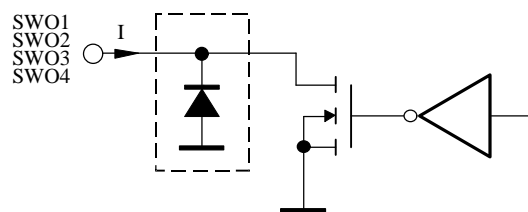


Figure 10.

OSCIN, OSCOUT

A crystal resonator (up to 15 MHz) is connected between OSCIN and OSCOUT in order to generate the reference frequency. By using the U4256BM in connection with U4255BM the crystal frequency must be 10.25 MHz. The complete application circuit is shown in figure 15. If a reference is available, it can be applied at OSCIN. The minimum voltage should be 100mVrms. In this case, pin OSCOUT has to be open.

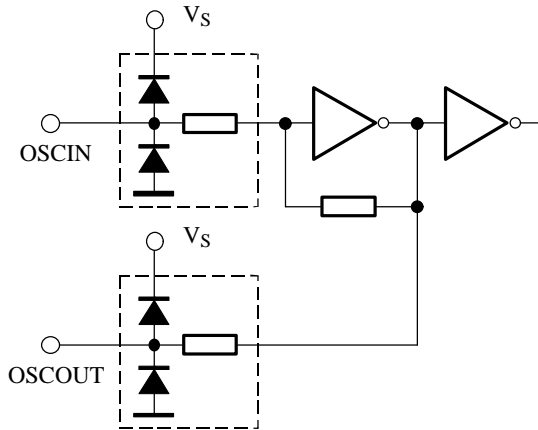


Figure 11.

Application Information

Function of DAC1, 2 in FM Mode

For automatic tuner alignment, the DAC1 and 2 of the U4256BM can be controlled by setting gain of VPDO and offset values. The following figure shows the principle of the operation. The gain is in the range of 0.7 to 2.15. The offset range is +0.5 V to -0.6 V. For alignment, DAC1 and 2 are connected to the varicaps of the preselection filters. For alignment, offset and gain is set for having the best tuner tracking.

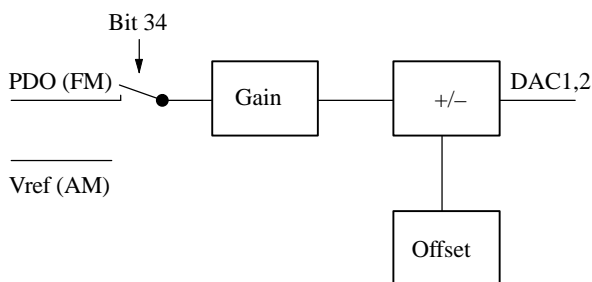


Figure 12.

Function of DAC1, 2 in AM Mode

If Bit 94 = 1, the DAC1, 2 can be used as standard DAC converters. The resolution of 8 bit is controlled via the gain bits in a range of approximately 0.5 V to 7 V, depending on the offset value.

FMOSCIN Sensitivity

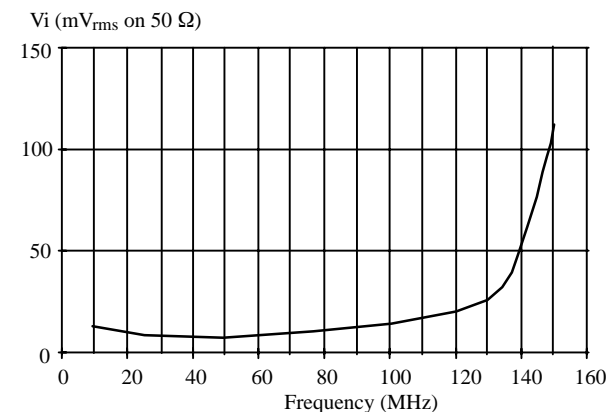


Figure 13.

Oscillator Tuning Function Schematic

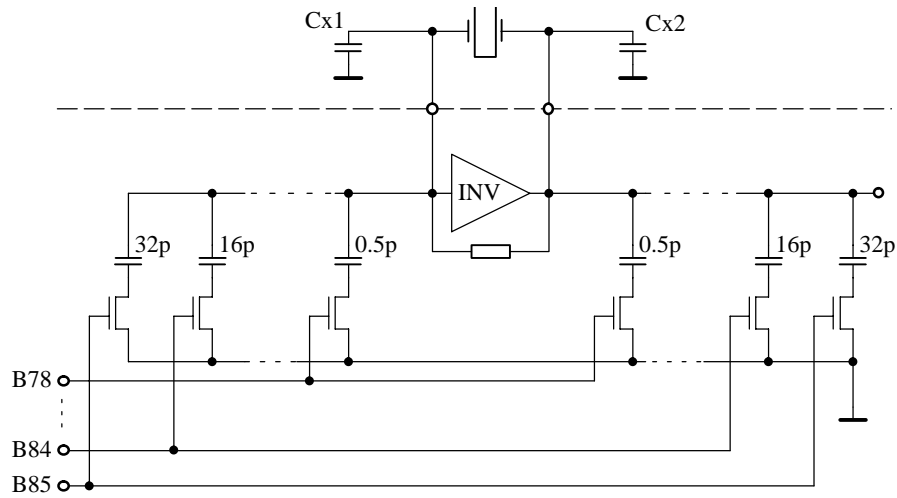


Figure 14.

Application Circuit

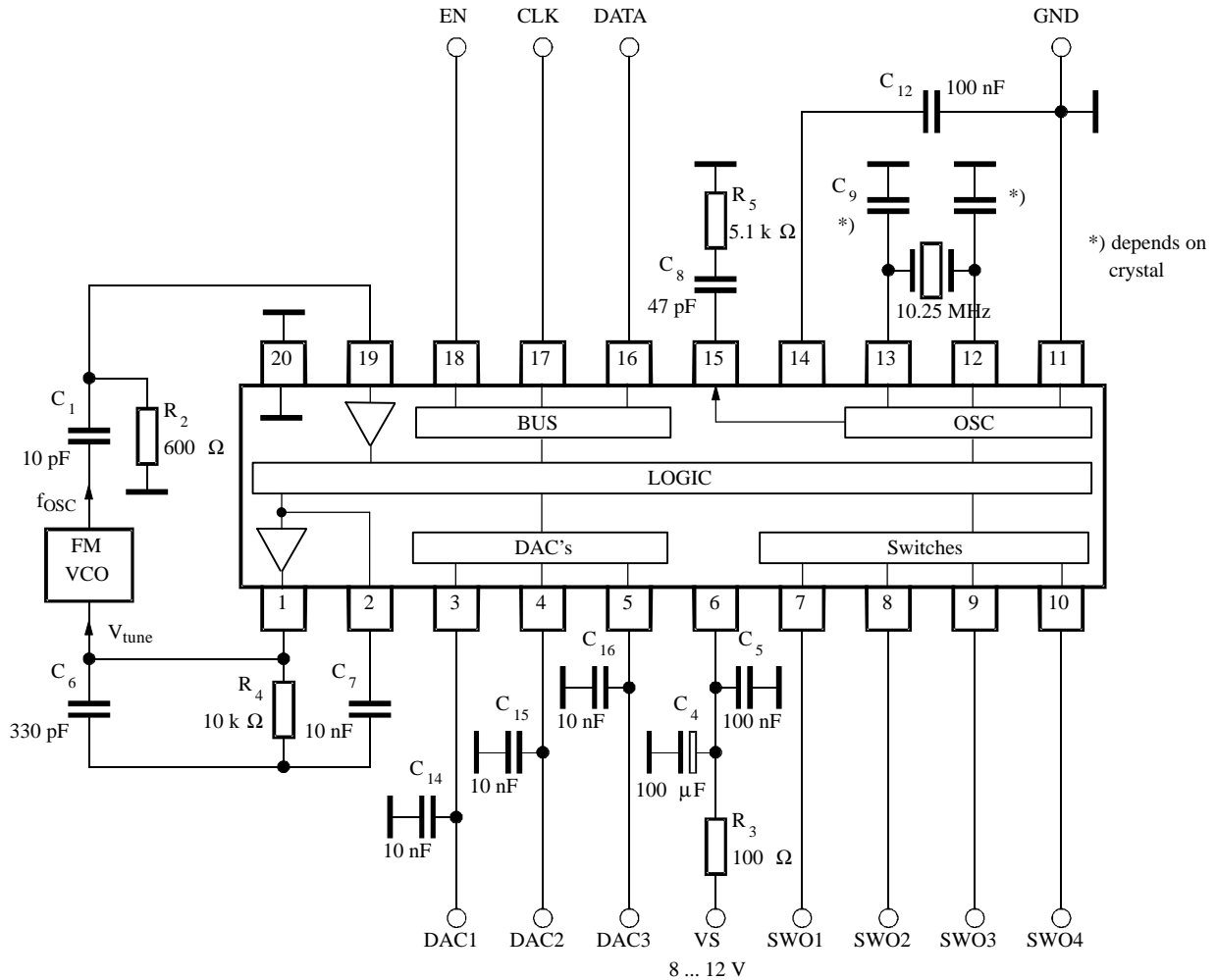
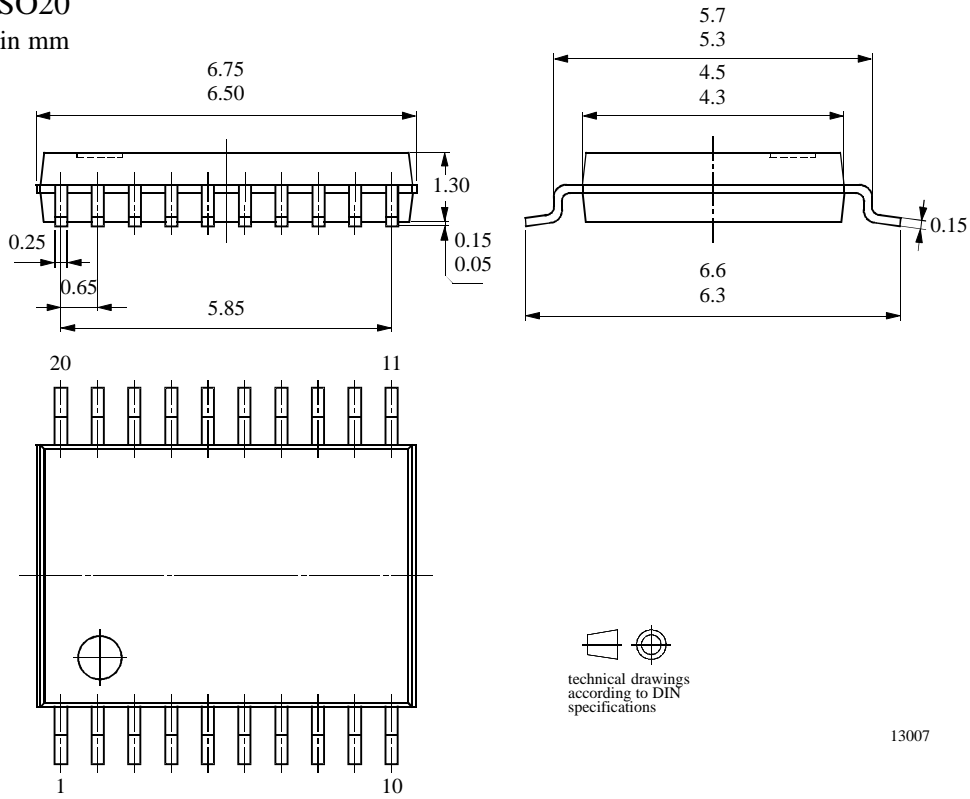


Figure 15. Application circuit

Package Information

Package SSO20
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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Data sheets can also be retrieved from the Internet: <http://www.atmel-wm.com>

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