



**THE DATASHEET OF
VN5E016MH-E**



16 mΩ high-side driver with analog current sense for automotive applications

Datasheet - production data



- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Overtemperature shutdown with auto restart (thermal shutdown)
- Reverse battery protected
- Electrostatic discharge protection

Features

Max supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28 V
Max on-state resistance (per ch.)	R_{ON}	16 mΩ
Current limitation (typ)	I_{LIMH}	73 A
Off-state supply current	I_S	2 μA ⁽¹⁾

1. Typical value with all loads connected.

- General
 - Inrush current active management by power limitation
 - Very low standby current
 - 3.0 V CMOS compatible inputs
 - Optimized electromagnetic emissions
 - Very low electromagnetic susceptibility
 - In compliance with the 2002/95/EC European directive
- Diagnostic functions
 - Proportional load current sense
 - High current sense precision for wide current range
 - Current sense disable
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation

Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VN5E016MH-E is a single channel high-side driver manufactured in the ST proprietary VIPower™ M0-5 technology and housed in the tiny HPak package. The VN5E016MH-E is designed to drive 12 V automotive grounded loads delivering protection, diagnostics and easy 3 V and 5 V CMOS compatible interface with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto restart and overvoltage active clamp.

A dedicated analog current sense pin is associated with every output channel in order to provide enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication and overtemperature indication.

The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS_DIS pin high to allow sharing of the external sense resistor with other similar devices.

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1 Block diagram and pin description

Figure 1. Block diagram

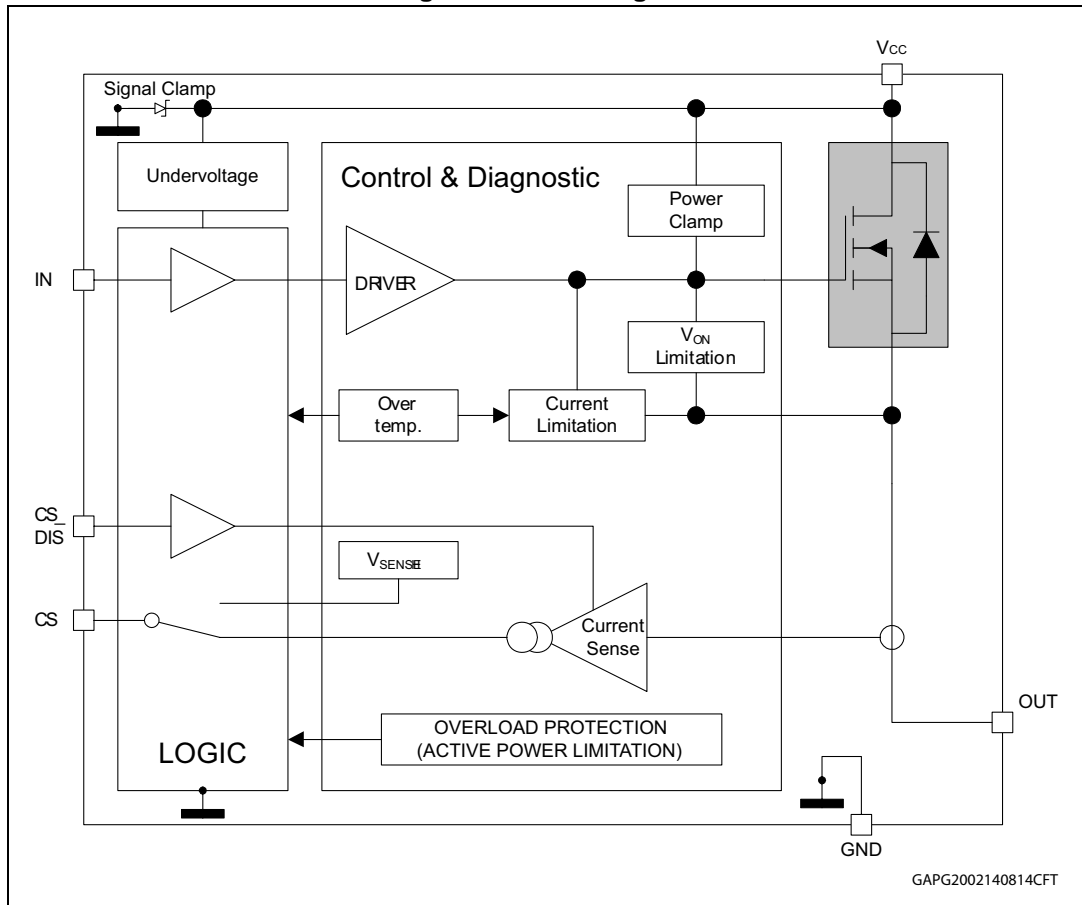


Table 1. Pin functions

Name	Function
V _{CC}	Battery connection
OUTPUT	Power output ⁽¹⁾
GND	Ground connection
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CURRENT SENSE	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

1. Pins 1 and 7 must be externally tied together.

Figure 2. Configuration diagram (top view) not in scale

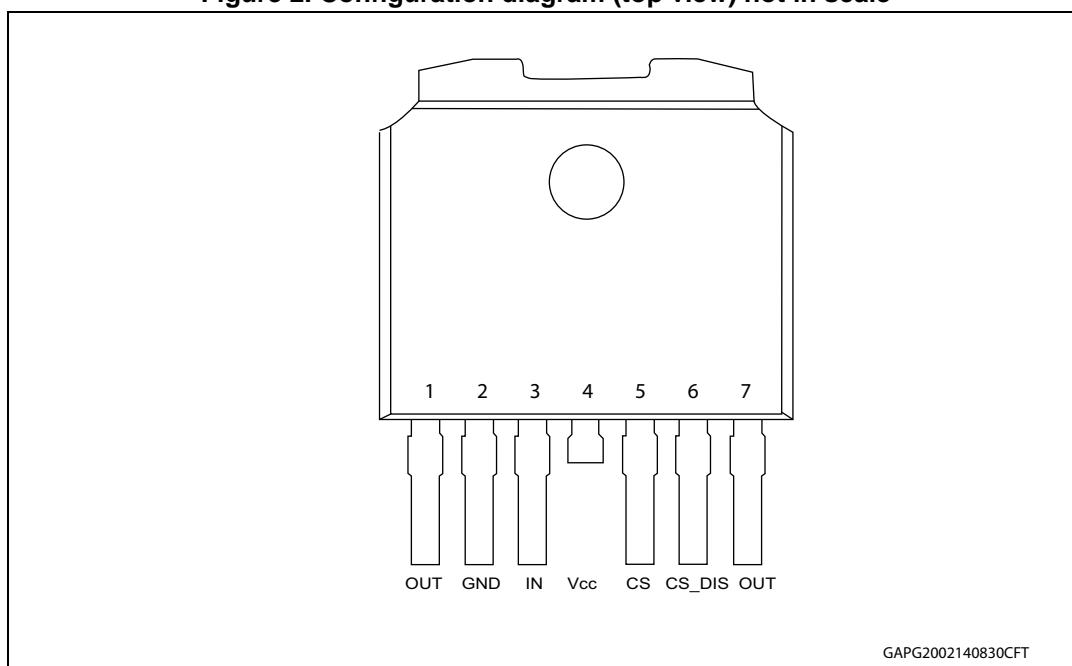
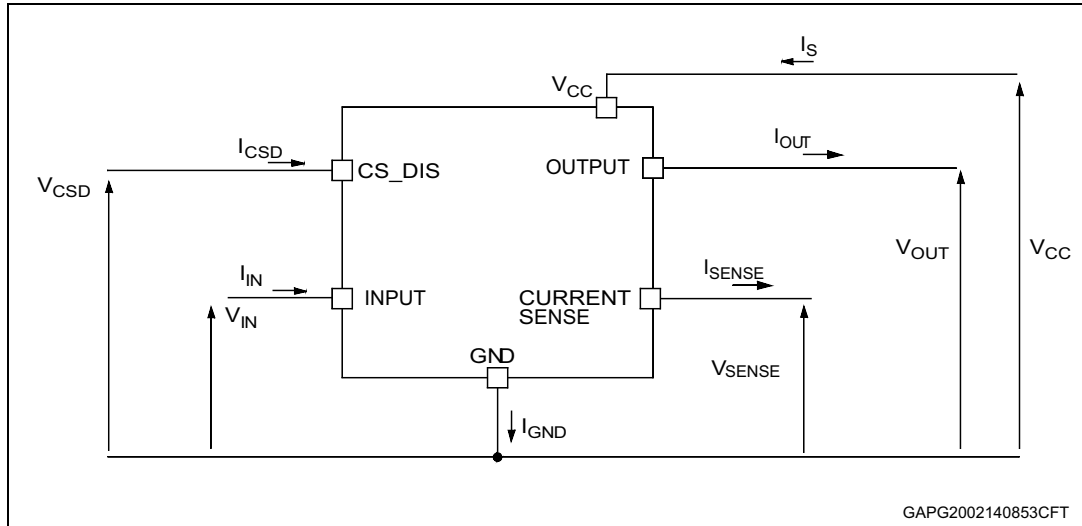


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	Output	Input	CS_DIS
Floating	Not allowed	X	X	X
To ground	Through 1 k Ω resistor	Through 22 k Ω resistor	Through 10 k Ω resistor	Through 10 k Ω resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
I_{GND}	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$V_{CSSENSE}$	Current sense maximum voltage ($V_{CC} > 0$)	$V_{CC}-41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 1.55\text{ mH}$; $R_L = 0\ \Omega$; $V_{bat} = 13.5\text{ V}$; $T_{jstart} = 150\text{ }^\circ\text{C}$; $I_{OUT} = I_{limL}(Typ.)$)	350	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V _{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF)		
	– Input	4000	V
	– Current sense	2000	V
	– CS_DIS	4000	V
	– Output	5000	V
	– V _{CC}	5000	V
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _j	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
R _{thj-case}	Thermal resistance junction-case	0.63	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	69.3	°C/W

2.3 Electrical characteristics

Values specified in this section are for $8\text{ V} < V_{CC} < 28\text{ V}$, $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	$I_{OUT} = 5\text{ A}; T_j = 25\text{ °C}$			16	m Ω
		$I_{OUT} = 5\text{ A}; T_j = 150\text{ °C}$			32	m Ω
		$I_{OUT} = 5\text{ A}; V_{CC} = 5\text{ V}; T_j = 25\text{ °C}$			20	m Ω
V_F	Output - V_{CC} diode voltage	$-I_{OUT} = 5\text{ A}; T_j = 150\text{ °C}$			0.7	V
V_{clamp}	Clamp voltage	$I_{CC} = 20\text{ mA}; I_{OUT} = 0\text{ A}$	41	46	52	V
I_S	Supply current	Off-state; $V_{CC} = 13\text{ V}; T_j = 25\text{ °C}; V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$		2	5	μA
		On-state; $V_{CC} = 13\text{ V}; V_{IN} = 5\text{ V}; I_{OUT} = 0\text{ A}$		1.5	3	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 13\text{ V}; T_j = 25\text{ °C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 13\text{ V}; T_j = 125\text{ °C}$	0		5	μA

Table 6. Switching ($V_{CC} = 13\text{ V}, T_j = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 2.6\ \Omega$ (see Figure 5)	—	15	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 2.6\ \Omega$ (see Figure 5)	—	45	—	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 2.6\ \Omega$	—	0.2	—	V/ μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 2.6\ \Omega$	—	0.2	—	V/ μs
W_{ON}	Switching energy losses at turn-on (t_{won})	$R_L = 2.6\ \Omega$ (see Figure 5)	—	1.4	—	mJ
W_{OFF}	Switching energy losses at turn-off (t_{won})	$R_L = 2.6\ \Omega$ (see Figure 5)	—	0.8	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD} = 0.9\text{ V}$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD} = 2.1\text{ V}$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD} = 1\text{ mA}$	5.5		7	V
		$I_{CSD} = -1\text{ mA}$		-0.7		V

Table 8. Protection and diagnostics (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	Short circuit current	$V_{CC} = 13\text{ V}$	54	73	108	A
		$5\text{ V} < V_{CC} < 28\text{ V}$			108	A
I_{limL}	Short circuit current during thermal cycling	$V_{CC} = 13\text{ V};$ $T_R < T_j < T_{TSD}$		18		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$
T_{RS}	Thermal reset of status		135			$^{\circ}\text{C}$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}\text{C}$
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT} = 2\text{ A}; V_{IN} = 0;$ $L = 6\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 0.5\text{ A};$ $T_j = -40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense ($8\text{ V} < V_{CC} < 18\text{ V}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.25\text{ A}$; $V_{SENSE} = 0.5\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	2836	6200	10444	
K_1	I_{OUT}/I_{SENSE}	$I_{OUT} = 5\text{ A}$; $V_{SENSE} = 0.5\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$ $T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	4306 4358	5200 5200	7004 6106	
$dK_1/K_1^{(1)}$	Current sense ratio drift	$I_{OUT} = 5\text{ A}$; $V_{SENSE} = 0.5\text{ V}$; $V_{CSD} = 0\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	- 11		+ 11	%
K_2	I_{OUT}/I_{SENSE}	$I_{OUT} = 10\text{ A}$; $V_{SENSE} = 4\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$ $T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	4608 4501	5040 5040	5926 5502	
$dK_2/K_2^{(1)}$	Current sense ratio drift	$I_{OUT} = 10\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{CSD} = 0\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	- 8		+ 8	%
K_3	I_{OUT}/I_{SENSE}	$I_{OUT} = 25\text{ A}$; $V_{SENSE} = 4\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$ $T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	4612 4566	4930 4930	5367 5168	
$dK_3/K_3^{(1)}$	Current sense ratio drift	$I_{OUT} = 25\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{CSD} = 0\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	- 4		+ 4	%
I_{SENSE0}	Analog sense leakage current	$I_{OUT} = 0\text{ A}$; $V_{SENSE} = 0\text{ V}$; $V_{CSD} = 5\text{ V}$; $V_{IN} = 0\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	0		1	μA
		$V_{CSD} = 0\text{ V}$; $V_{IN} = 5\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	0		2	μA
		$I_{OUT} = 2\text{ A}$; $V_{SENSE} = 0\text{ V}$; $V_{CSD} = 5\text{ V}$; $V_{IN} = 5\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$			1	μA
I_{OL}	Openload ON-state current detection threshold	$V_{IN} = 5\text{ V}$; $I_{SENSE} = 5\text{ } \mu\text{A}$	5		70	mA
V_{SENSE}	Max analog sense output voltage	$I_{OUT} = 18\text{ A}$; $R_{SENSE} = 3.9\text{ K}\Omega$	5			V
$V_{SENSEH}^{(2)}$	Analog sense output voltage in fault condition	$V_{CC} = 13\text{ V}$; $R_{SENSE} = 3.9\text{ K}\Omega$		8		V
$I_{SENSEH}^{(2)}$	Analog sense output current in fault condition	$V_{CC} = 13\text{ V}$; $V_{SENSE} = 5\text{ V}$		9		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	$V_{SENSE} < 4\text{ V}$; $1.5\text{ A} < I_{OUT} < 25\text{ A}$; $I_{SENSE} = 90\%$ of $I_{SENSE\text{ max}}$ (see Figure 4)		50	100	μs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	$V_{SENSE} < 4\text{ V}$; $1.5\text{ A} < I_{OUT} < 25\text{ A}$; $I_{SENSE} = 10\%$ of $I_{SENSE\text{ max}}$ (see Figure 4)		5	20	μs

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} < 4 V; 1.5 A < I _{OUT} < 25 A; I _{SENSE} = 90 % of I _{SENSE max} (see Figure 4)		270	600	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4V; I _{SENSE} = 90 % of I _{SENSEMAX} ; I _{OUT} = 90 % of I _{OUTMAX} ; I _{OUTMAX} = 3 A (see Figure 7)			280	μs
t _{DSENSE2L}	Delay response time from falling edge of INPUT pin	V _{SENSE} < 4 V; 1.5 A < I _{OUT} < 25 A; I _{SENSE} = 10 % of I _{SENSE max} (see Figure 4)		100	250	μs

1. Parameter guaranteed by design, it is not tested.
2. Fault condition includes: power limitation and overtemperature.

Figure 4. Current sense delay characteristics

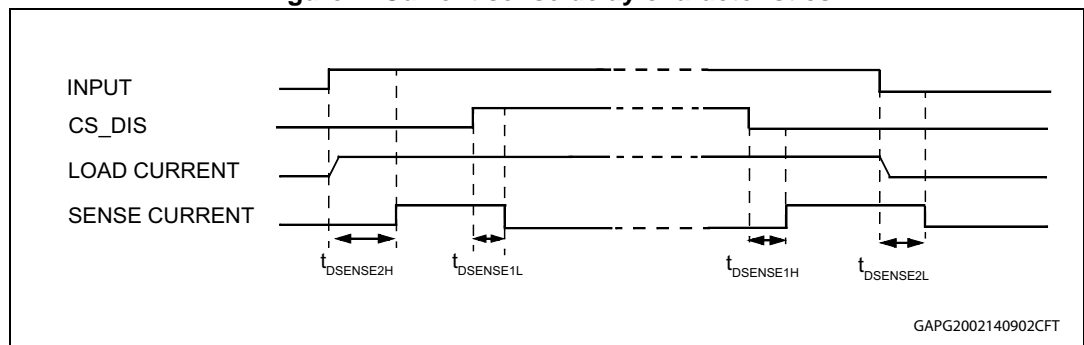


Figure 5. Switching characteristics

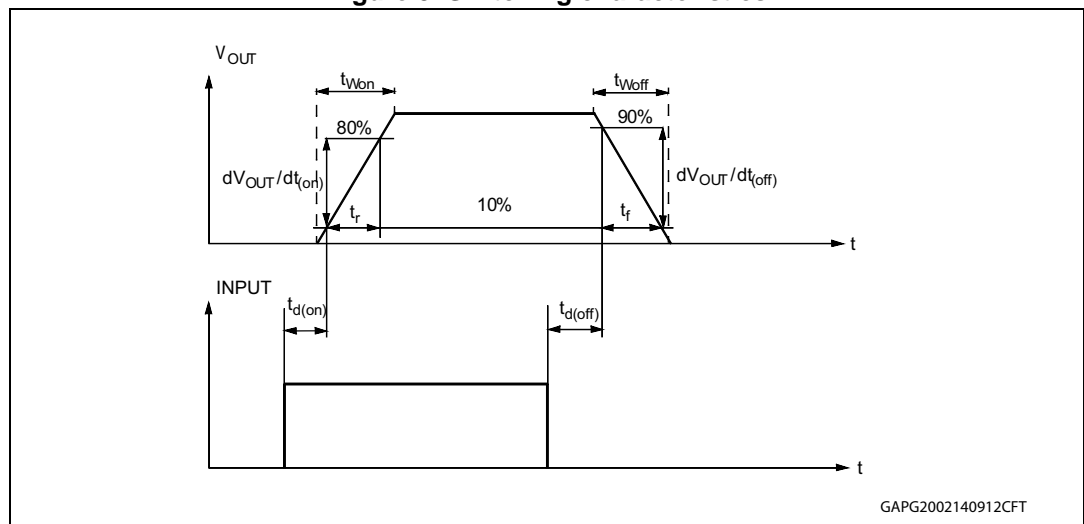


Figure 6. Output voltage drop limitation

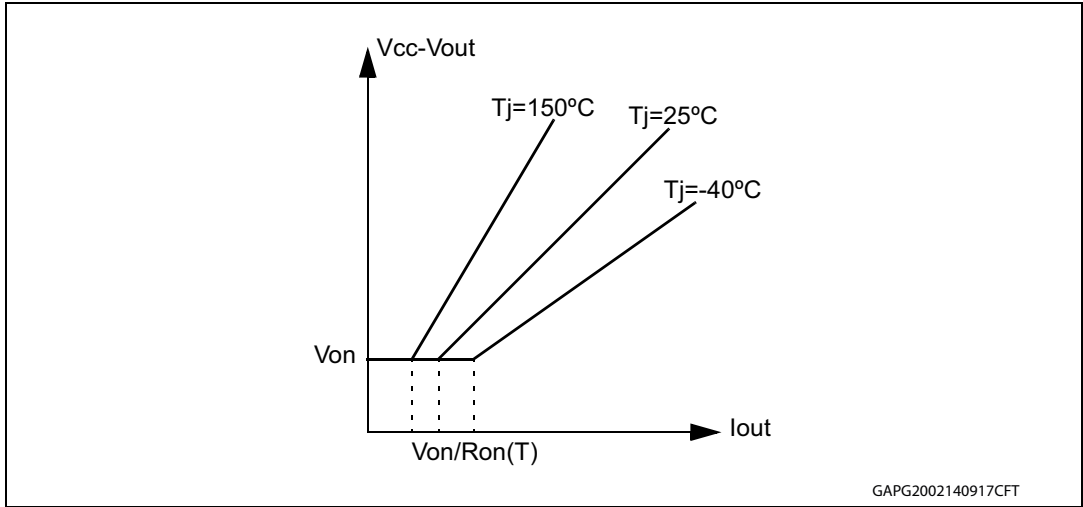


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

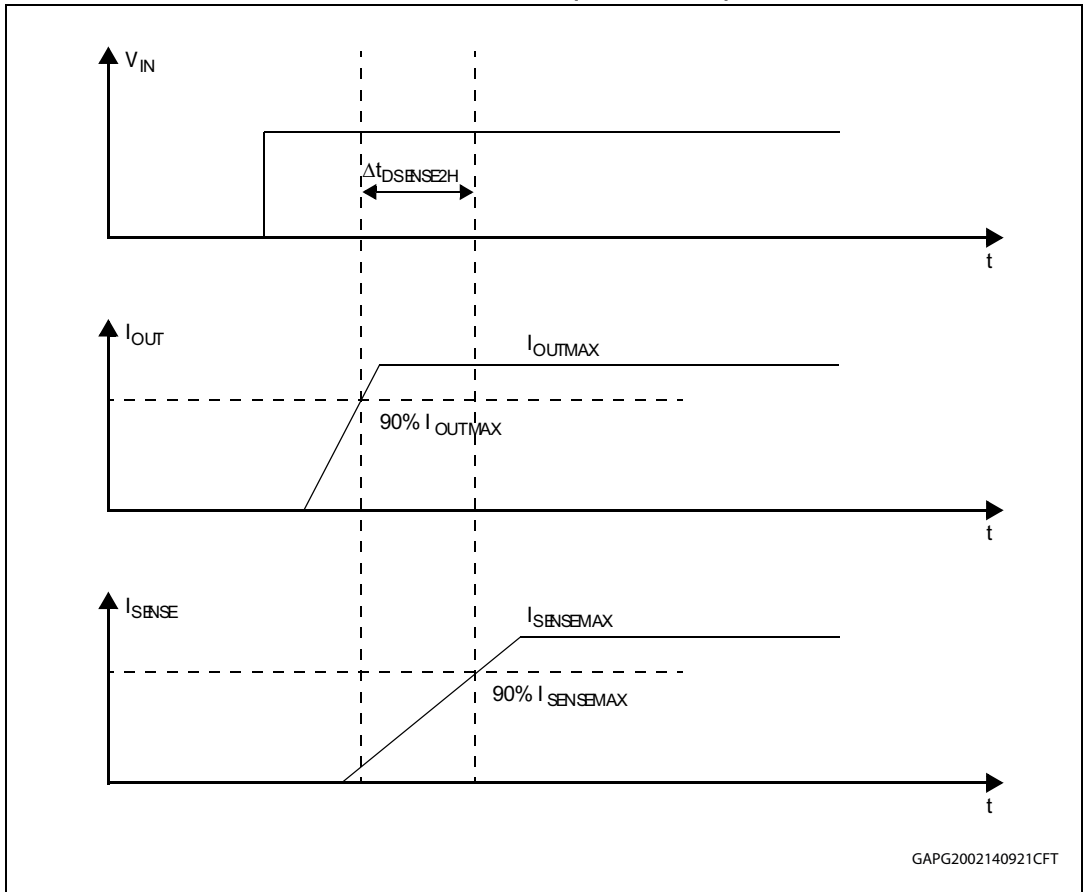


Figure 8. I_{OUT}/I_{SENSE} vs I_{OUT}

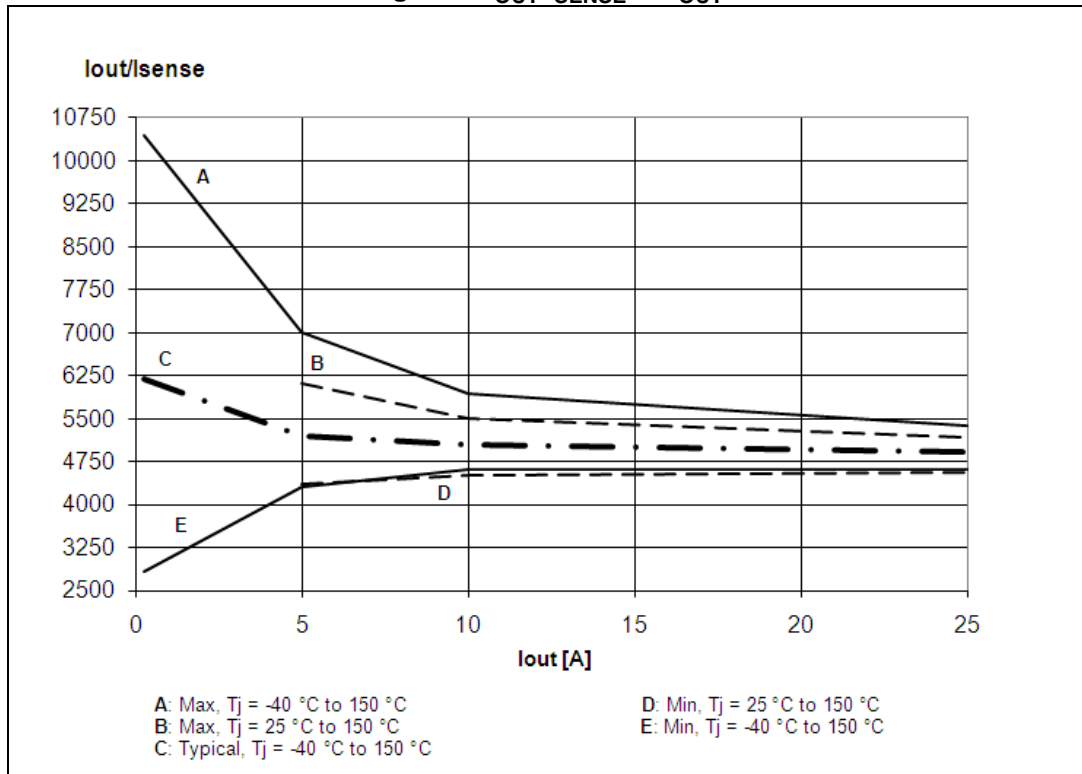
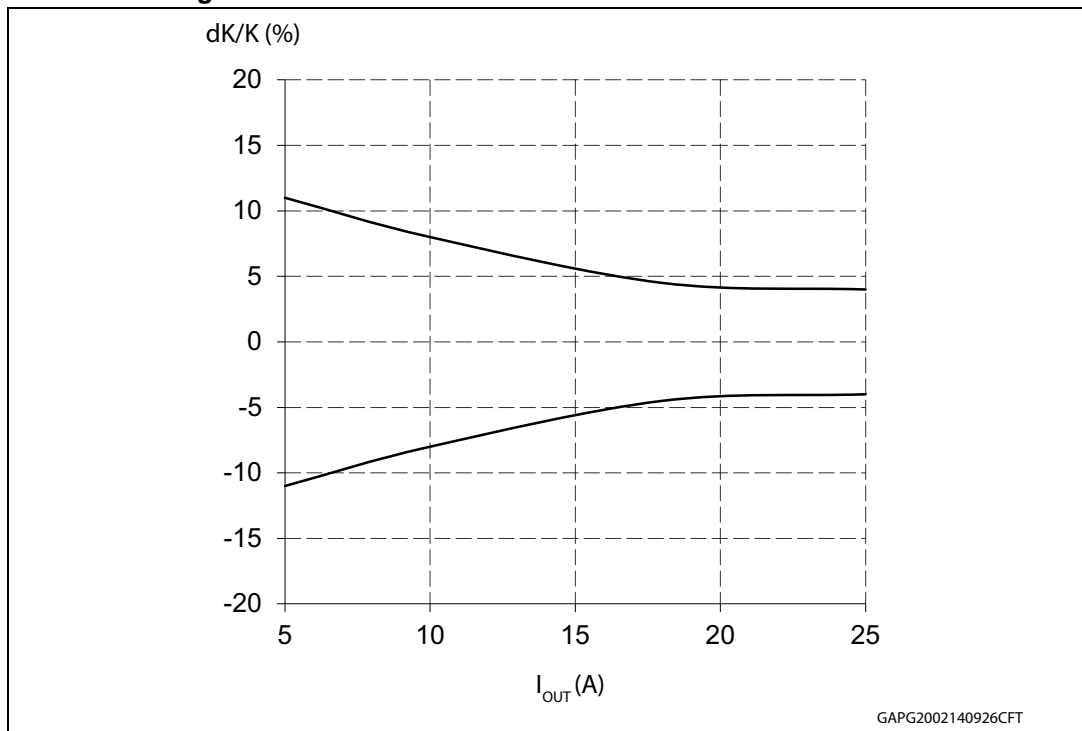


Figure 9. Maximum current sense ratio drift vs load current



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1. Parameter guaranteed by design; it is not tested.

Table 10. Truth table

Conditions	Input	Output	Sense ($V_{CSD} = 0\text{ V}$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overload	H	X (no power limitation)	Nominal
	H	Cycling (power limitation)	V_{SENSEH}
Short circuit to GND (power limitation)	L	L	0
	H	L	V_{SENSEH}
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 11. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1μs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01Ω
5b ⁽¹⁾	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 12. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b

2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 13. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 10. Normal operation

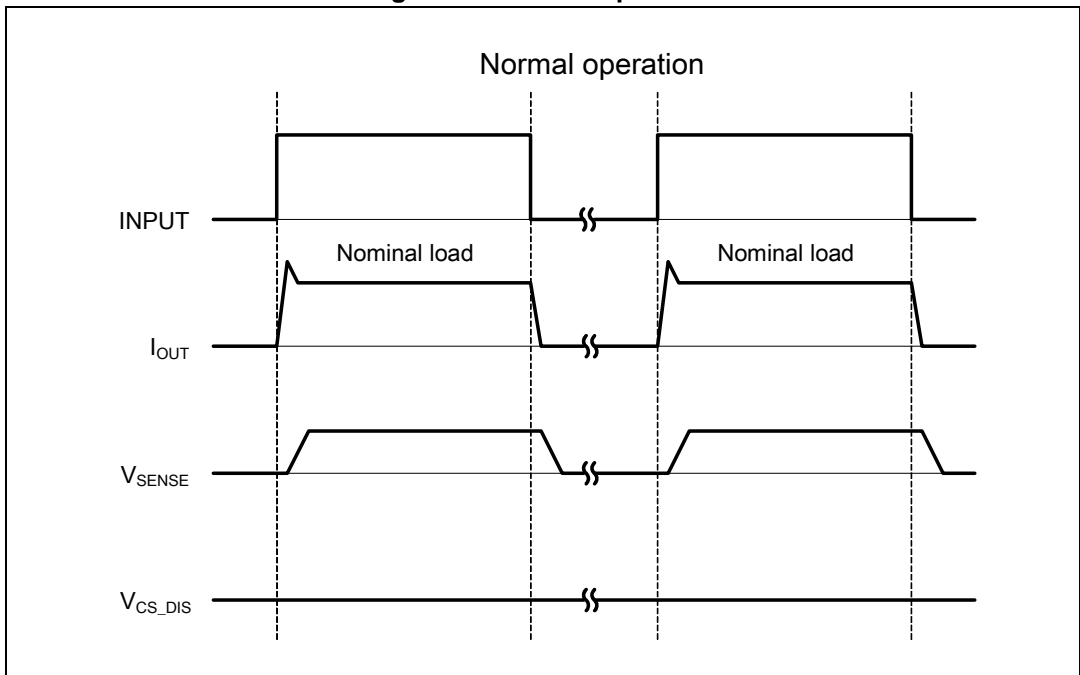


Figure 11. Overload or short to GND

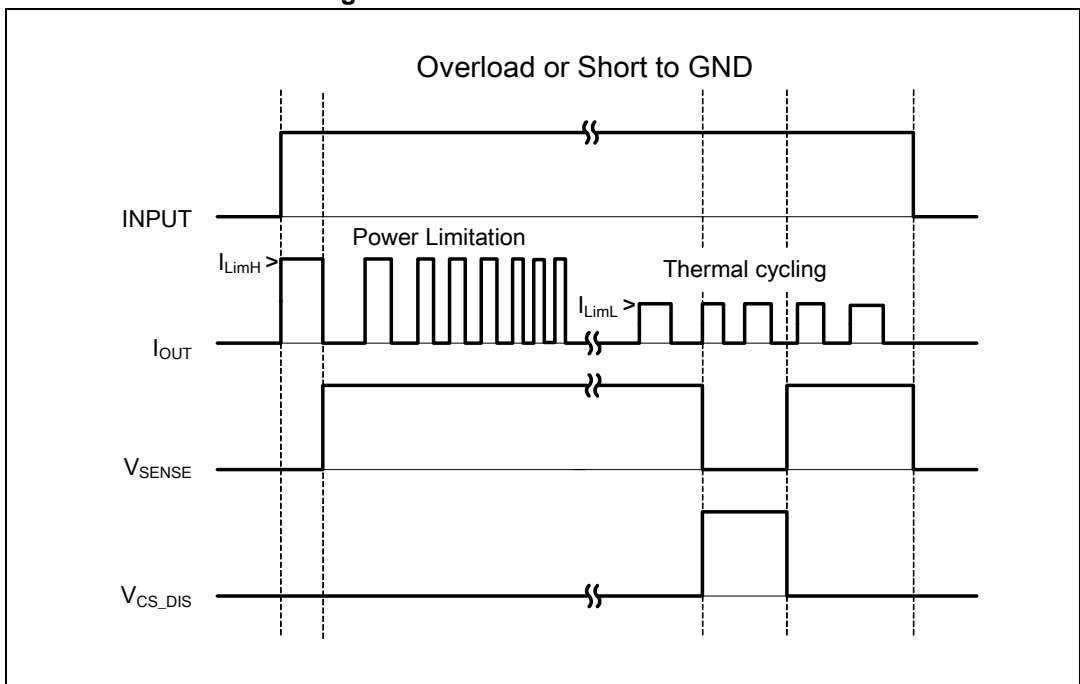


Figure 12. Intermittent overload

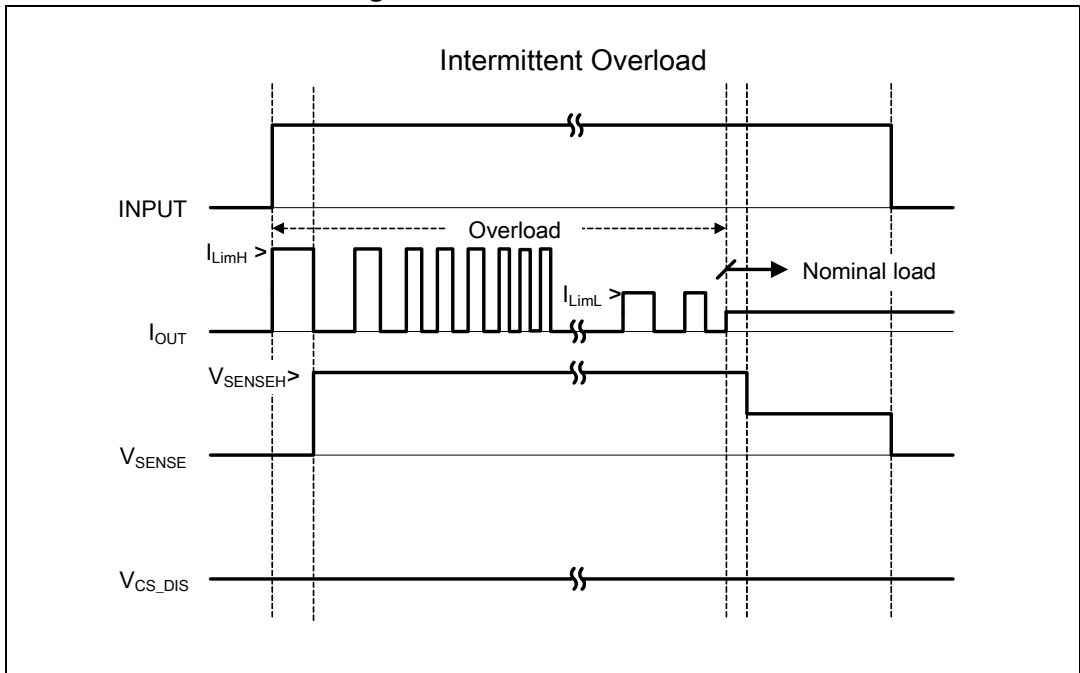
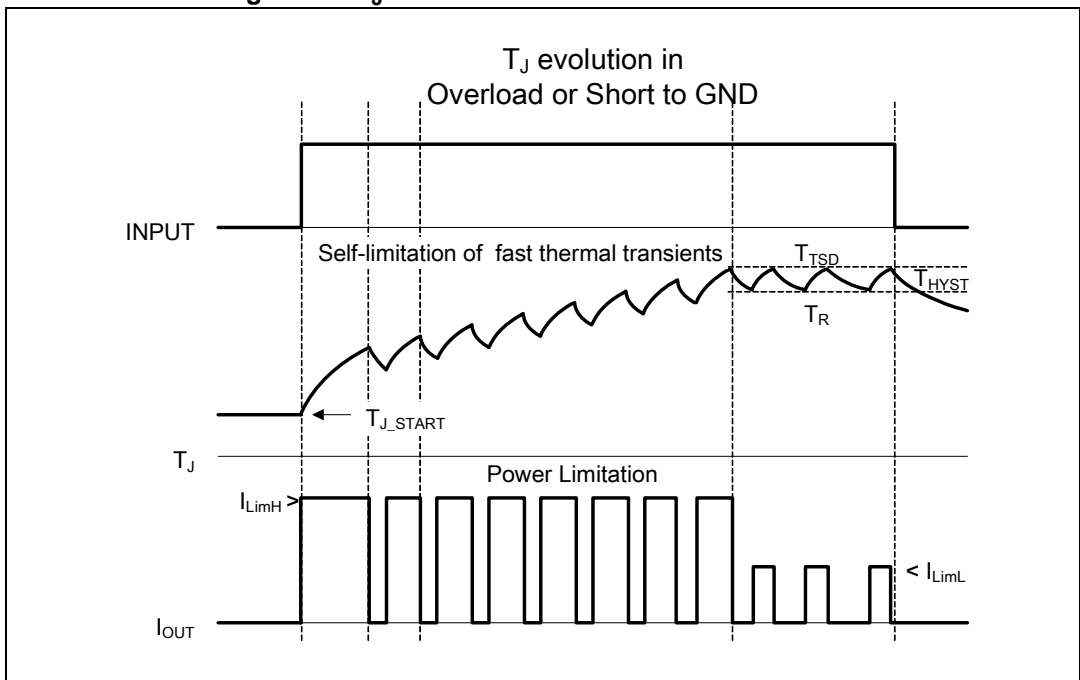


Figure 13. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 14. Off-state output current

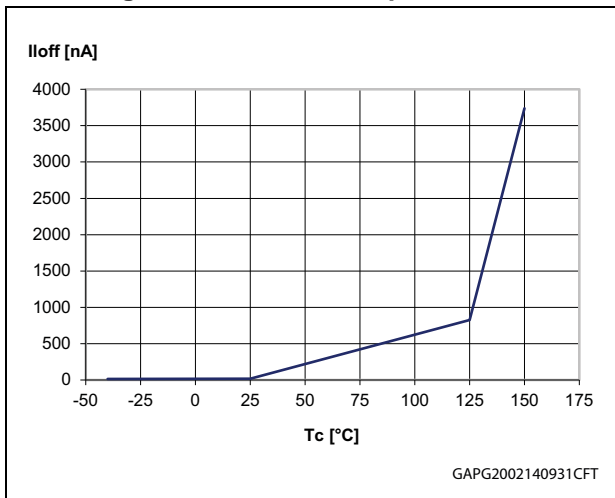


Figure 15. High level input current

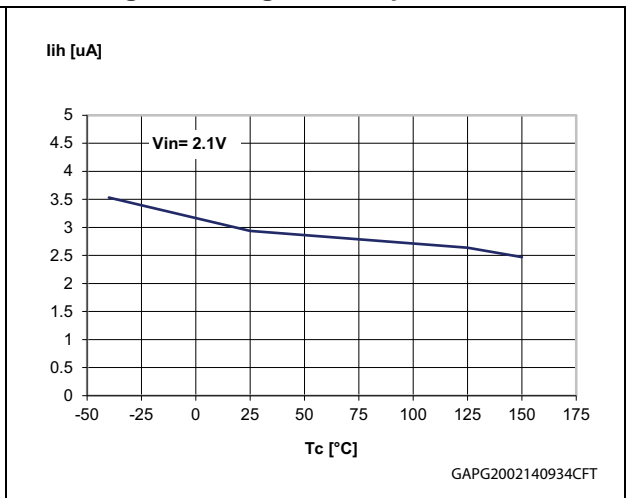


Figure 16. Input clamp level

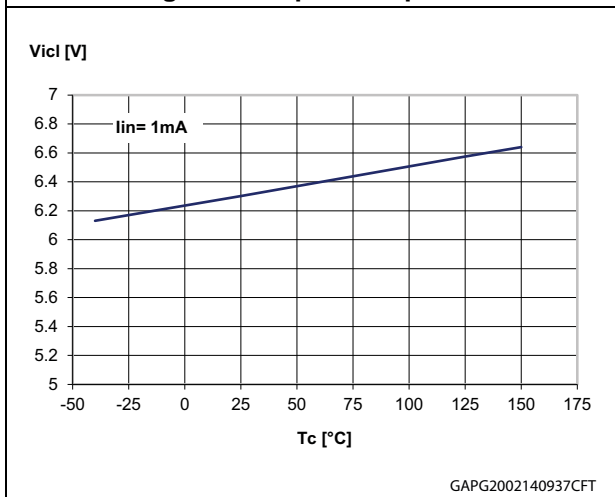


Figure 17. Input low level

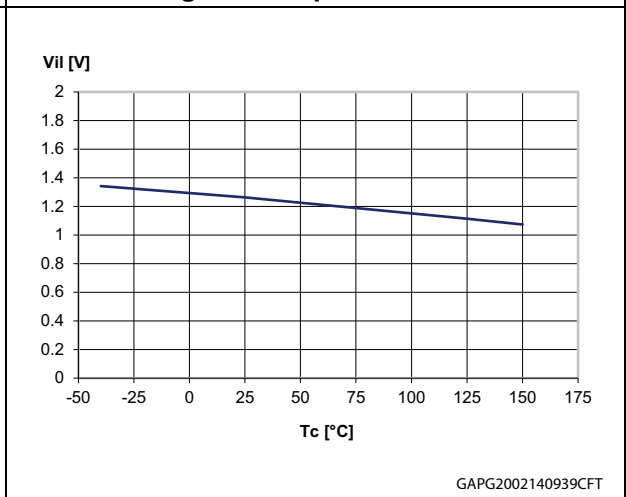


Figure 18. Input high level

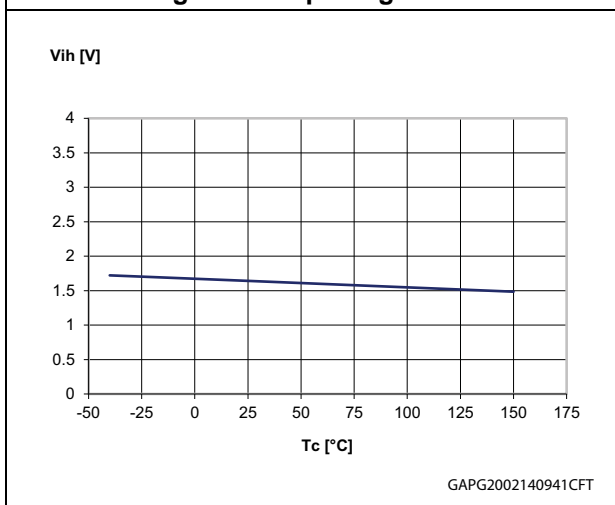
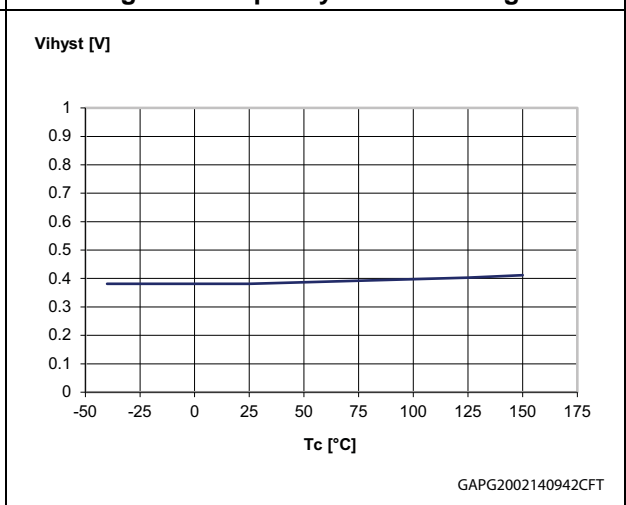


Figure 19. Input hysteresis voltage



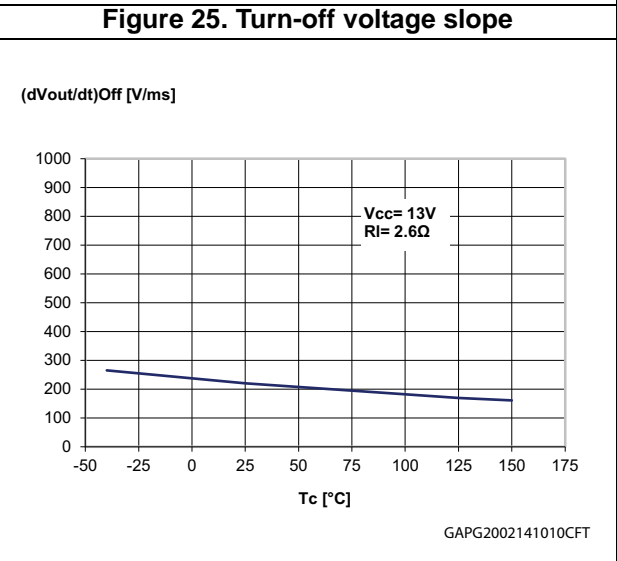
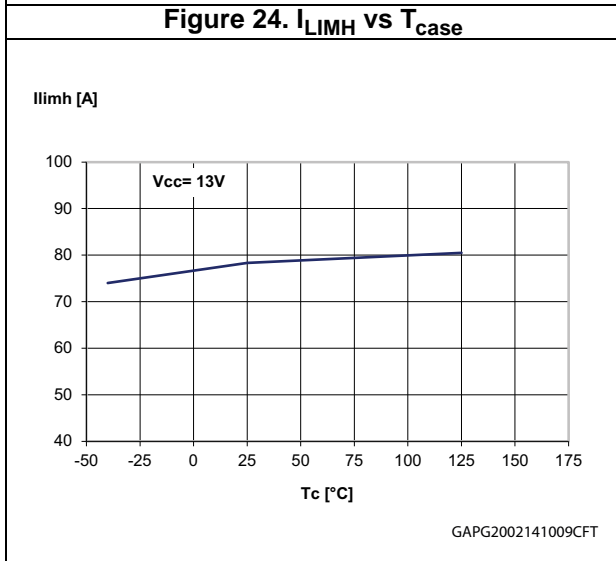
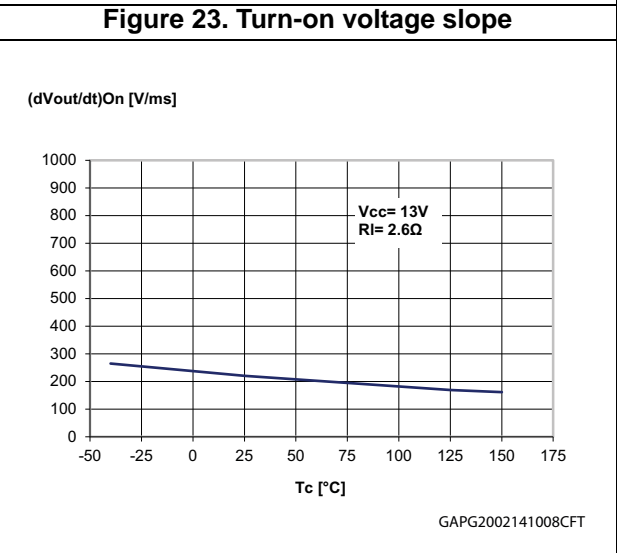
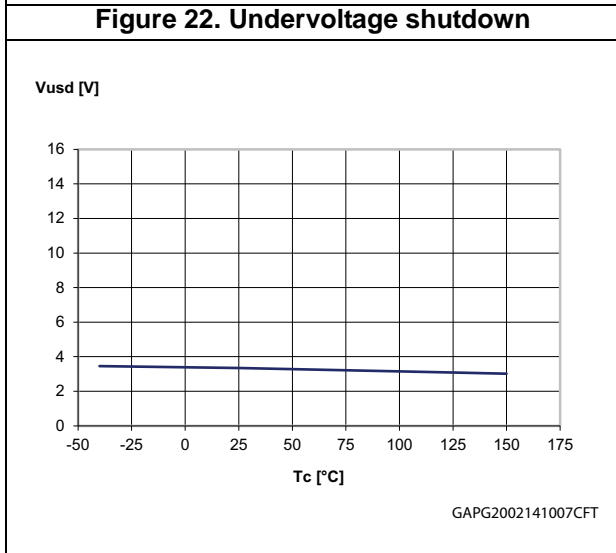
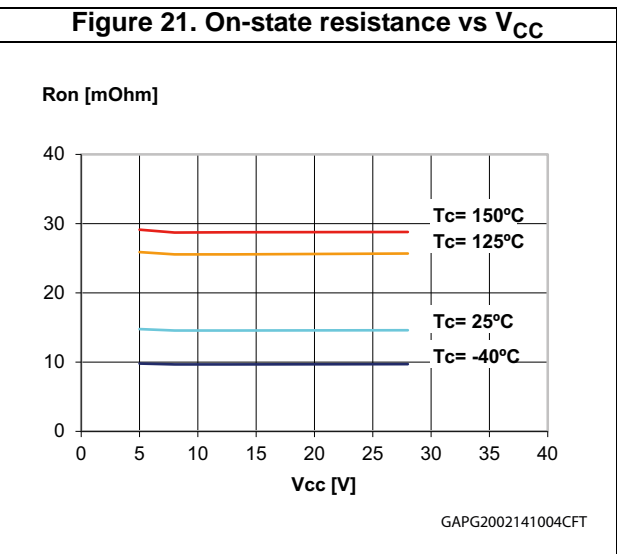
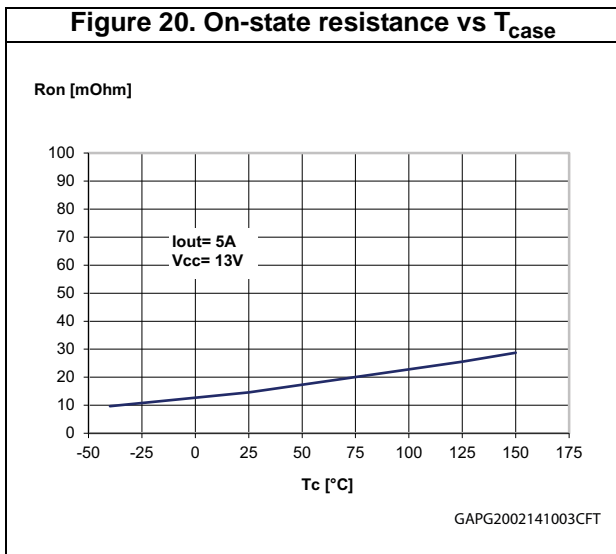


Figure 26. CS_DIS high level voltage

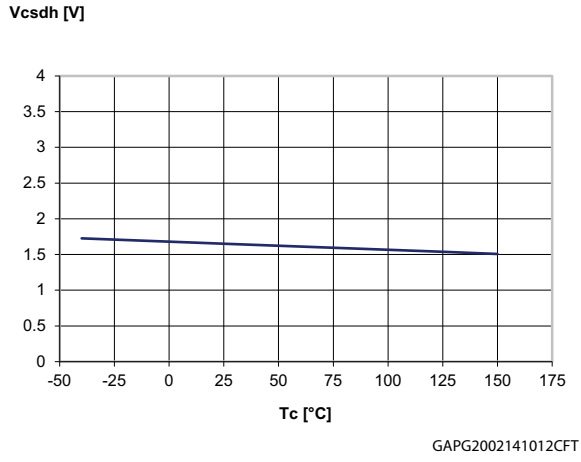


Figure 27. CS_DIS clamp voltage

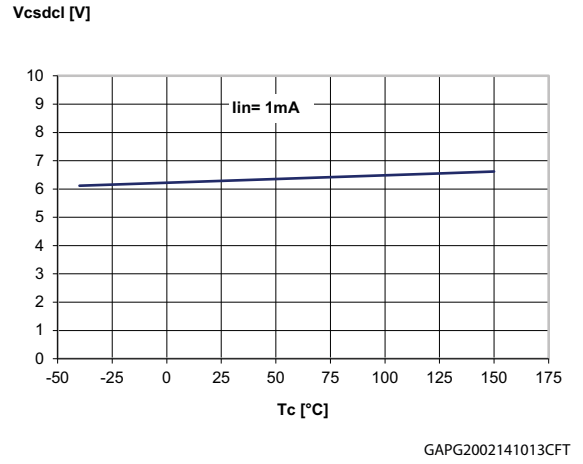
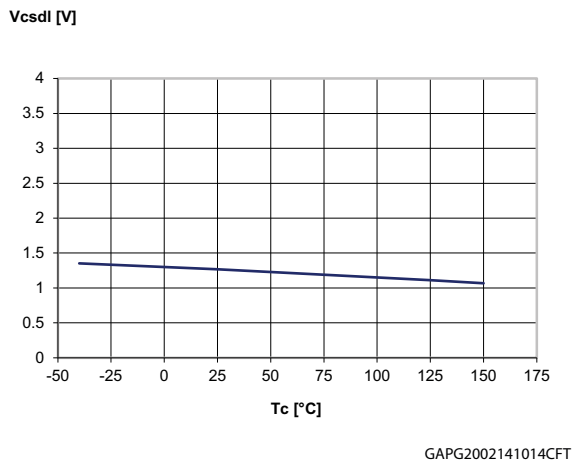
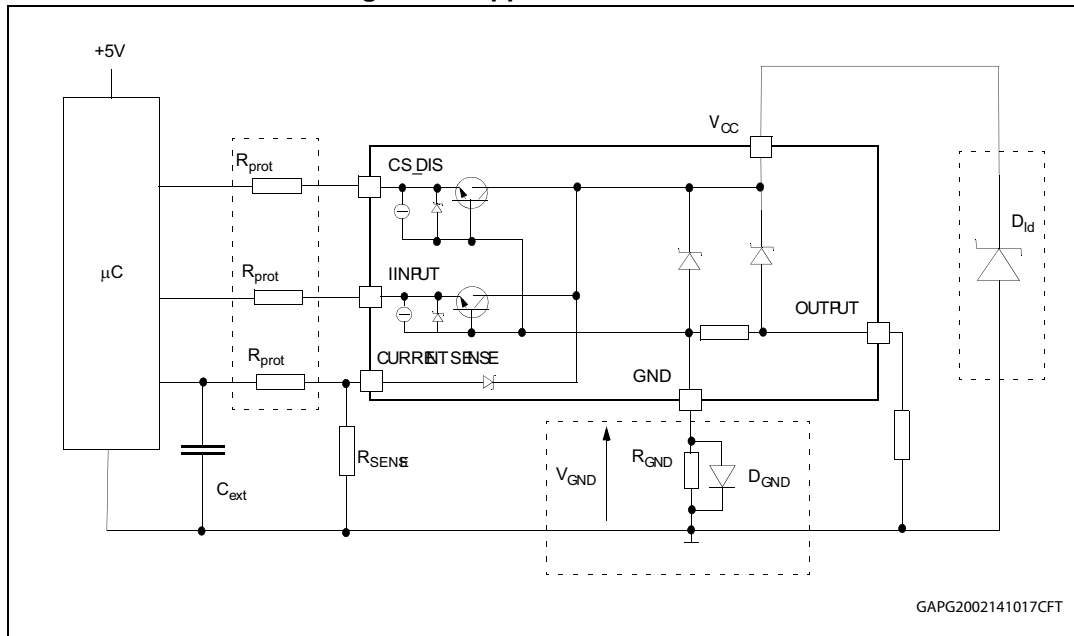


Figure 28. CS_DIS low level voltage



3 Application information

Figure 29. Application schematic



GAPG2002141017CFT

3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_GND only)

This can be used with any type of load.

The following is an indication on how to set the dimension of R_GND resistor.

$$1) R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$$

$$2) R_{GND} \geq (-V_{CC}) / (-I_{GND})$$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_GND (when $V_{CC} < 0$: during reverse battery situations) is:

Equation 1

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_GND produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same R_GND.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600 \text{ mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift not varies if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the MCU I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of MCU and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of MCU I/Os.

Equation 2

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100 \text{ V}$ and $I_{latchup} \geq 20 \text{ mA}$; $V_{OH\mu C} \geq 4.5 \text{ V}$

$$5 \text{ k}\Omega \leq R_{prot} \leq 65 \text{ k}\Omega.$$

Recommended values: $R_{prot} = 10 \text{ k}\Omega$, $C_{EXT} = 10 \text{ nF}$.

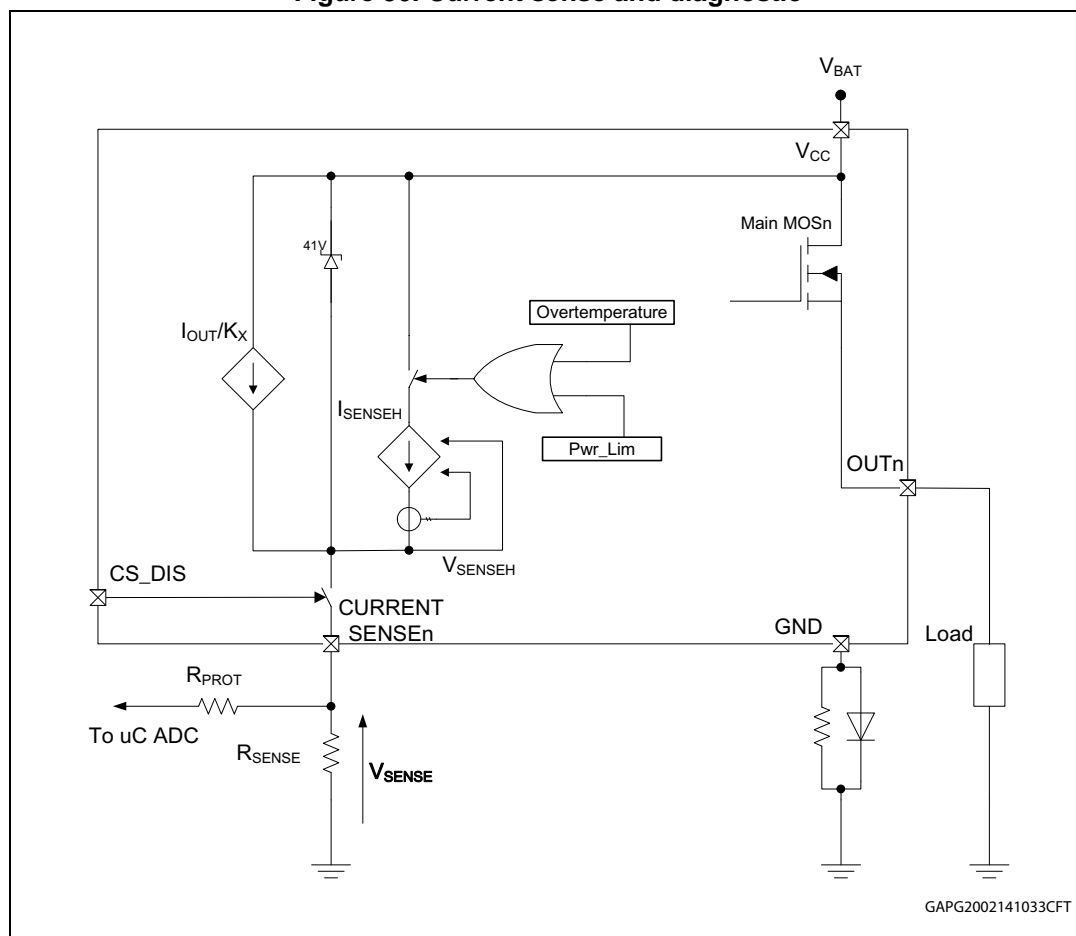
3.4 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 30: Current sense and diagnostic*):

- **Current mirror of the load current in normal operation**, delivering a current proportional to the load according to a known ratio K_x .
 The current I_{SENSE} can be easily converted into a voltage V_{SENSE} by means of an external resistor R_{SENSE} . Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < VCC < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < VCC < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 10*):
 - Power limitation activation
 - Overtemperature

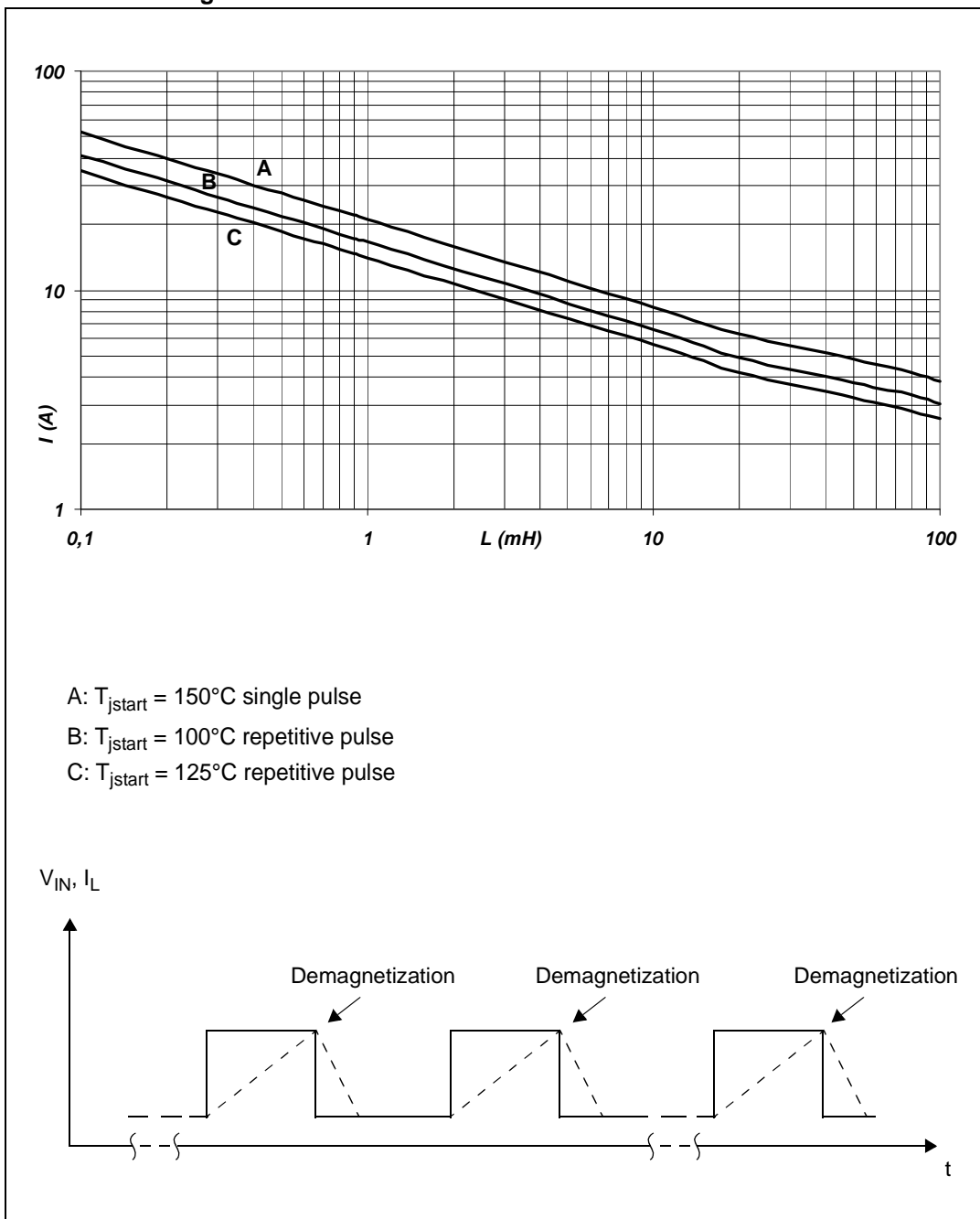
A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 30. Current sense and diagnostic



3.5 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 31. Maximum turn-off current versus inductance

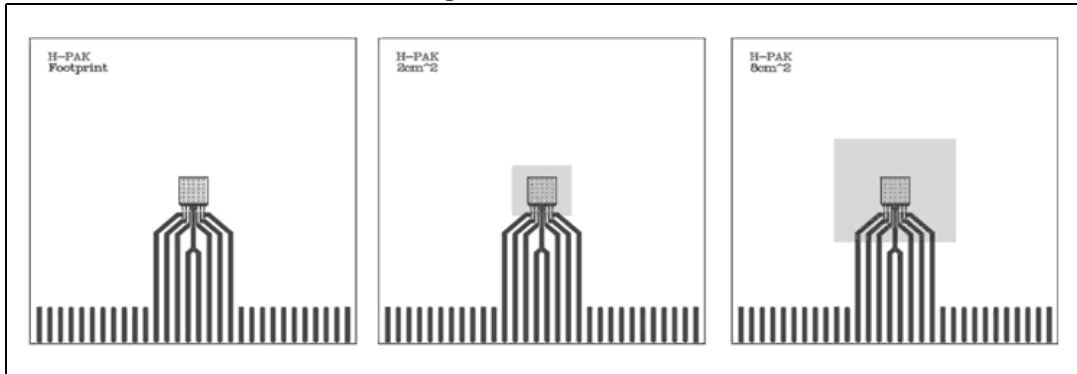


1. Values are generated with $R_L = 0\ \Omega$. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 HPak thermal data

Figure 32. PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 1.8 mm, Cu thickness = 70 μ m, Copper areas: from minimum pad lay-out to 8 cm²).

Figure 33. $R_{thj-amb}$ vs PCB copper area in open box free air condition

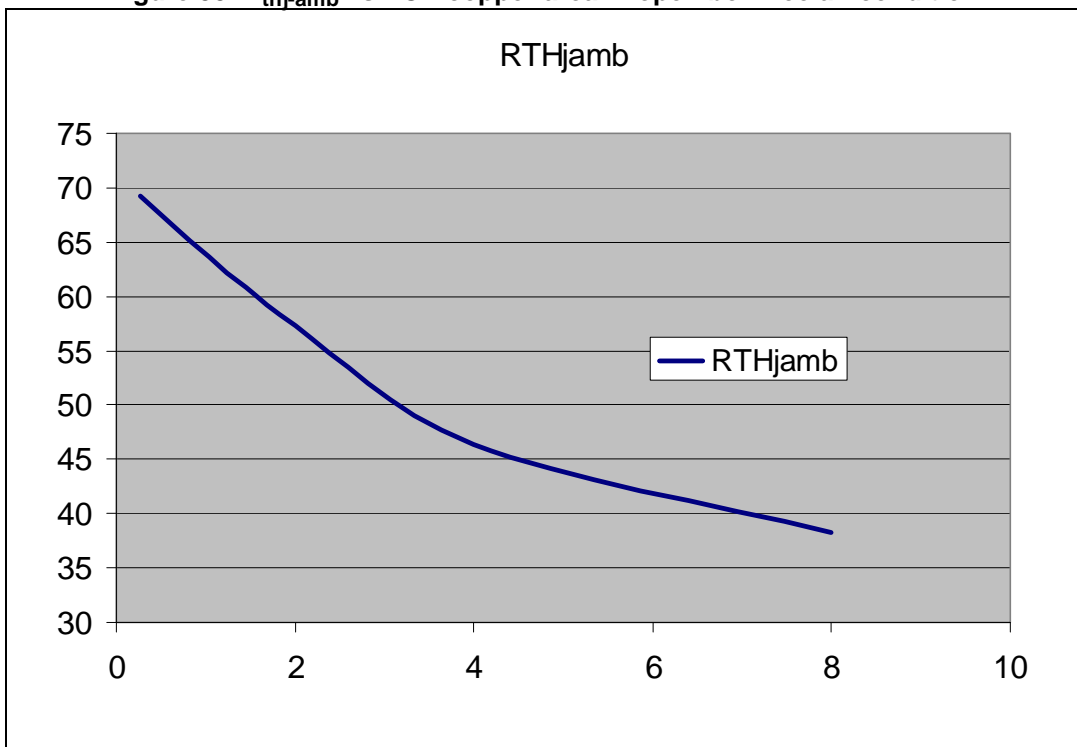
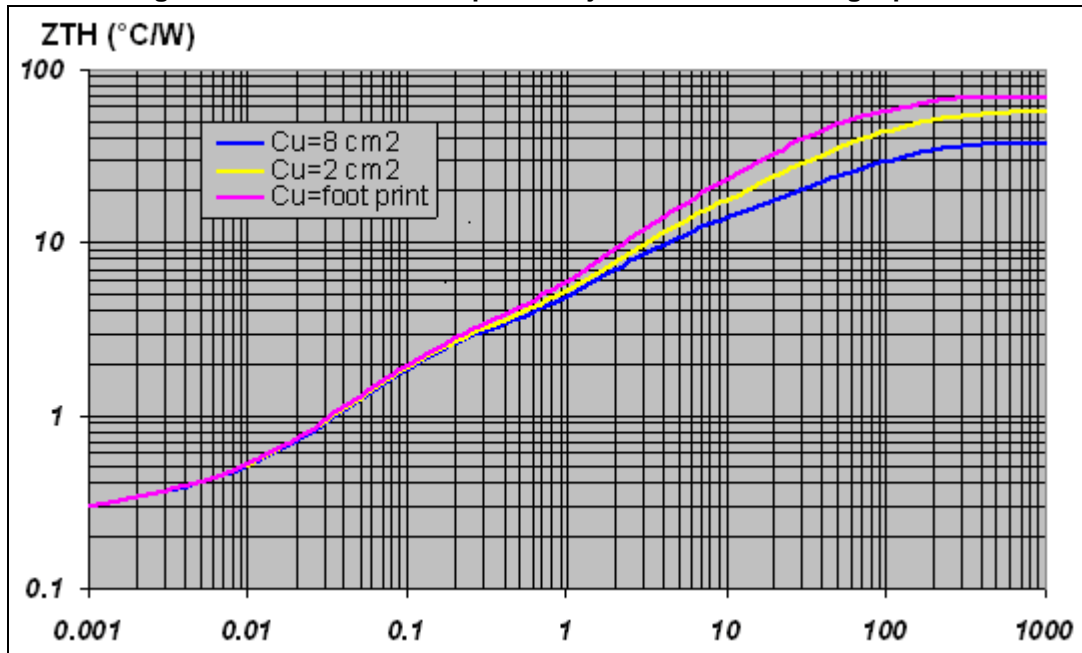


Figure 34. HPak thermal impedance junction ambient single pulse

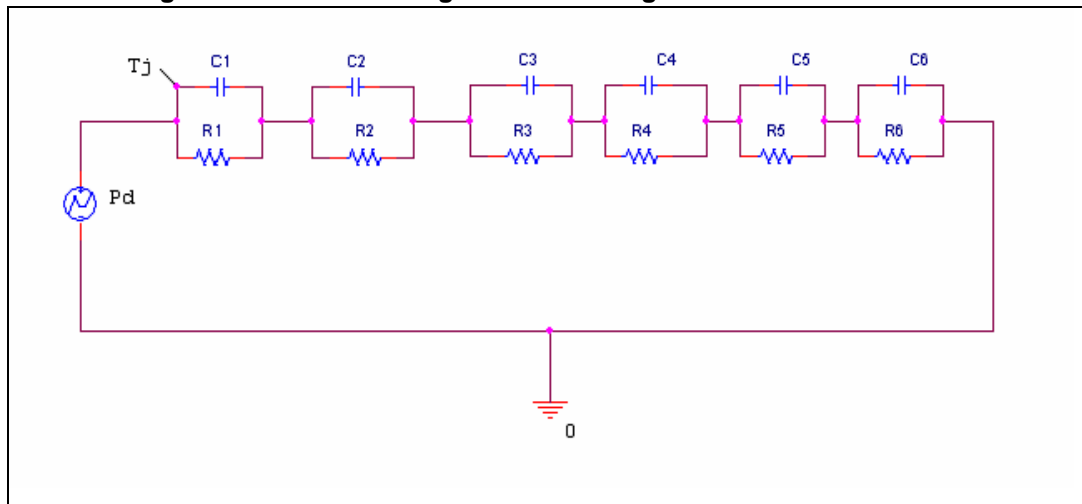


Equation 3: pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 35. Thermal fitting model of a single channel HSD in HPak



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 14. Thermal parameter

Area/island (cm ²)	Footprint	4	8
R1 (°C/W)	0.1	-	-
R2 (°C/W)	0.2	-	-
R3 (°C/W)	2	-	-
R4 (°C/W)	8	-	-
R5 (°C/W)	28	22	12
R6 (°C/W)	31	25	16
C1 (W.s/°C)	0.0001	-	-
C2 (W.s/°C)	0.002	-	-
C3 (W.s/°C)	0.05	-	-
C4 (W.s/°C)	0.4	-	-
C5 (W.s/°C)	0.8	1.4	3
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 HPak mechanical data

Figure 36. KPak package dimension

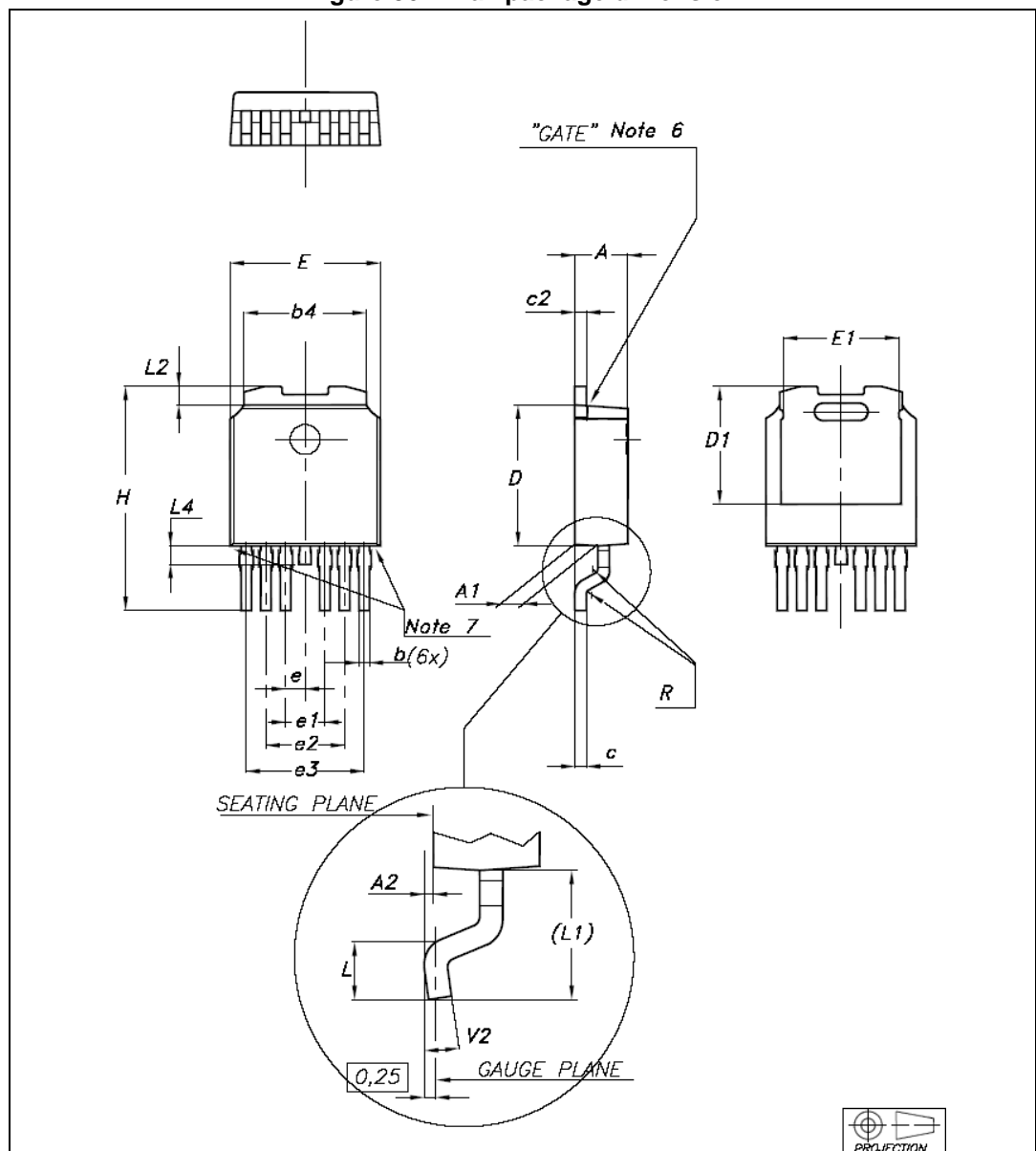


Table 15. HPak mechanical data

Ref. dim	Data book mm		
	Nom.	Min.	Max.
A		2.20	2.40
A1		0.90	1.10
A2		0.03	0.23
b		0.45	0.60
b4		5.20	5.40
c		0.45	0.60
c2		0.48	0.60
D		6.00	6.20
D1	5.10		
E		6.40	6.60
E1	5.20		
e	0.85		
e1		1.60	1.80
e2		3.30	3.50
e3		5.00	5.20
H		9.35	10.10
L		1	
(L1)	2.80		
L2	0.80		
L4		0.60	1.00
R	0.20		
V2		0°	8°

5.3 HPak packing information

The devices can be packed in tube or tape and reel shipments (see [Table 16: Device summary](#)).

Figure 37. HPak tube shipment (no suffix)

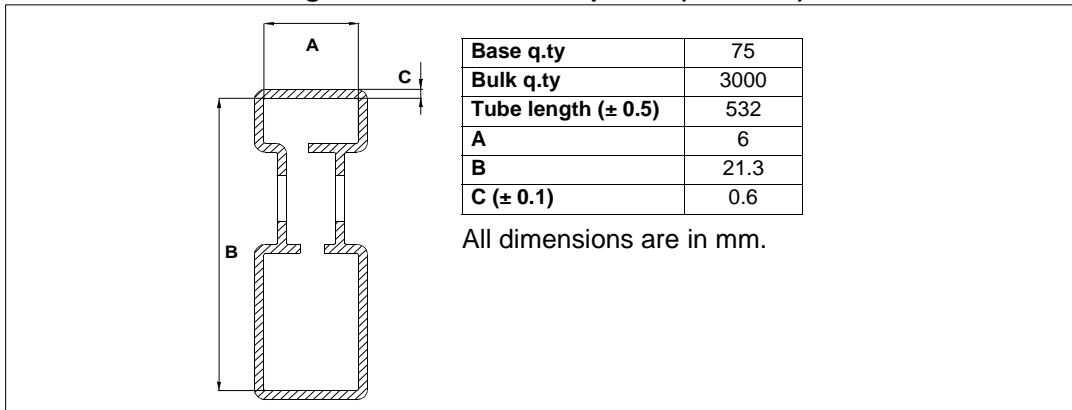
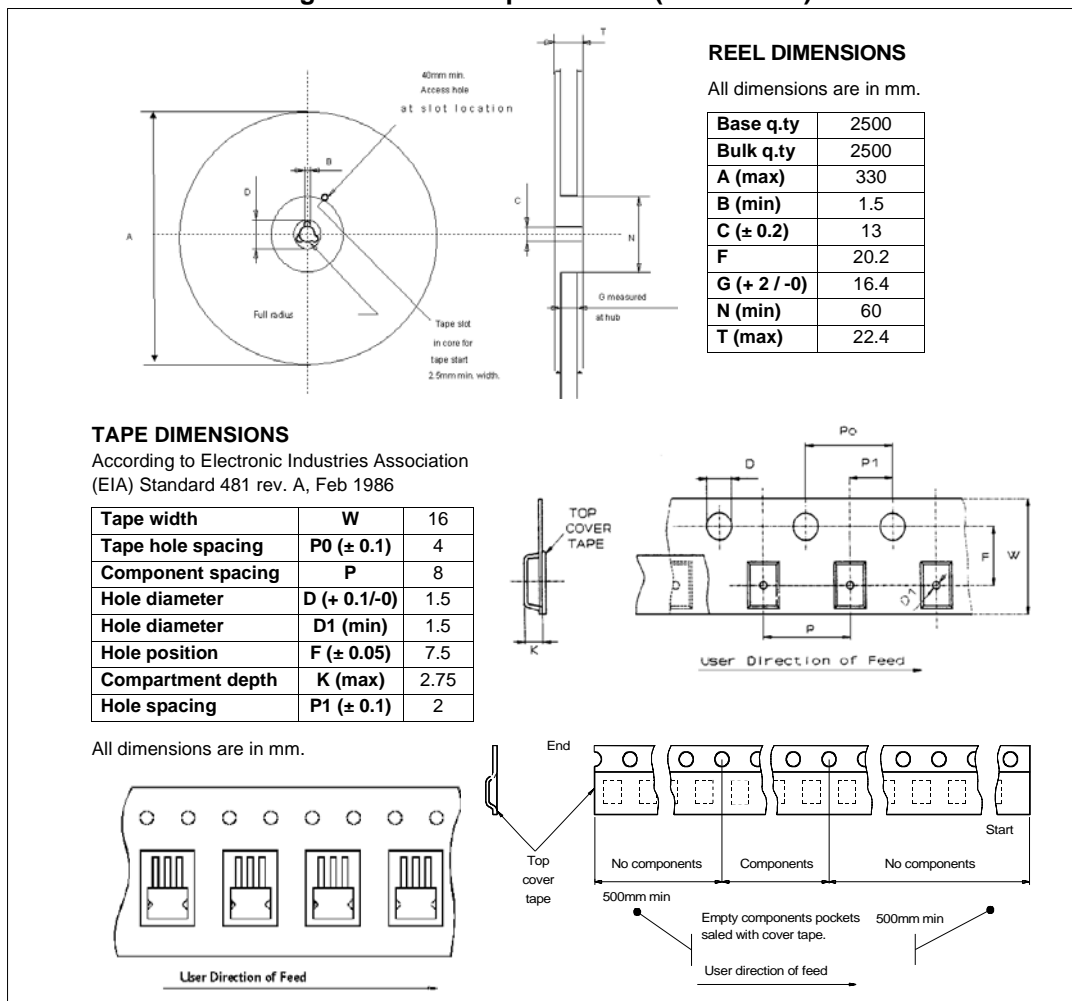


Figure 38. HPak tape and reel (suffix “TR”)



6 Order codes

Table 16. Device summary

Package	Order codes	
	Tube	Tape and reel
7 pins H-pack	Root part number 1	VN5E016MHTR-E

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
29-Jun-2010	1	Initial release.
30-Jun-2010	2	Changed status from target specification to preliminary data.
29-Jul-2010	3	<i>Table 9: Current sense (8 V < VCC < 18 V):</i> – Updated K1 maximum value for $T_j = 25\text{ °C} \dots 150\text{ °C}$
04-Aug-2010	4	<i>Table 9: Current sense (8 V < VCC < 18 V):</i> – Updated K1, K2 and K3 typical values for $T_j = -40\text{ °C} \dots 150\text{ °C}$ – Updated dK_1/K_1 test conditions Updated <i>Figure 8: IOUT/ISENSE vs IOUT</i> .
19-Feb-2014	5	Changed document status from “Preliminary data” to “Production data”
07-May-2014	6	Updated <i>Figure 2: Configuration diagram (top view) not in scale</i>

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