



## Dual Positive-Edge-Triggered D-Type Flip-Flop

Check for Samples: [SN74LVC2G80](#)

### FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.2 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Feature Supports Live Insertion, Partial-Power-Down and Back Drive Protection Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

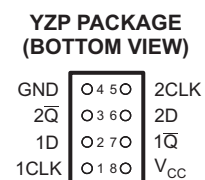
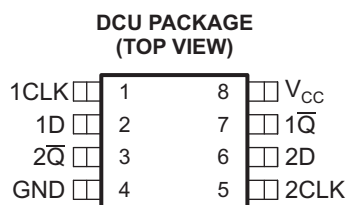
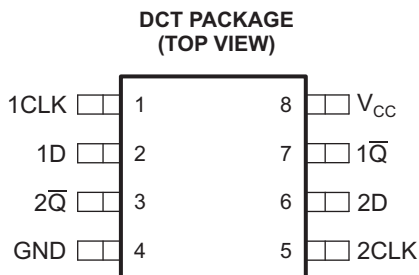
### DESCRIPTION

This dual positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the  $\bar{Q}$  output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



See mechanical drawings for dimensions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.



**Recommended Operating Conditions<sup>(1)</sup>**

			<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	0.8		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.3 × V <sub>CC</sub>		
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	–4		mA
		V <sub>CC</sub> = 2.3 V	–8		
		V <sub>CC</sub> = 3 V	–16		
		V <sub>CC</sub> = 4.5 V	–32		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4		mA
		V <sub>CC</sub> = 2.3 V	8		
		V <sub>CC</sub> = 3 V	16		
		V <sub>CC</sub> = 4.5 V	32		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V	10		
		V <sub>CC</sub> = 5 V ± 0.5 V	5		
T <sub>A</sub>	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	–40°C to 85°C			–40°C to 125°C			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 5.5 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –4 mA	1.65 V	1.2			1.2			
	I <sub>OH</sub> = –8 mA	2.3 V	1.9			1.9			
	I <sub>OH</sub> = –16 mA	3 V	2.4			2.4			
	I <sub>OH</sub> = –24 mA		2.3			2.3			
	I <sub>OH</sub> = –32 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 4 mA	1.65 V	0.45			0.45			
	I <sub>OL</sub> = 8 mA	2.3 V	0.3			0.3			
	I <sub>OL</sub> = 16 mA	3 V	0.4			0.4			
	I <sub>OL</sub> = 24 mA		0.55			0.65			
	I <sub>OL</sub> = 32 mA	4.5 V	0.55			0.65			
I <sub>I</sub>	D input	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1			μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±1			±10 μA
I <sub>CC</sub>		V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V			5			5 μA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500			500 μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	0			3.5			pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		SN74LVC2G80 –40°C to 85°C								UNIT
		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5.5 V ± 0.5 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	160		160		160		160		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	2.5		2.5		2.5		2.5		ns
t <sub>su</sub>	Setup time before CLK↑	Data high		1.4		1.1		0.9		ns
		Data low		1.4		1.1		0.9		
t <sub>h</sub>	Hold time, data after CLK↑	1.6		1		0.8		0.6		ns

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		SN74LVC2G80 –40°C to 125°C								UNIT
		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5.5 V ± 0.5 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	160		160		160		160		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	2.5		2.5		2.5		2.5		ns
t <sub>su</sub>	Setup time before CLK↑	Data high		1.4		1.1		0.9		ns
		Data low		1.4		1.1		0.9		
t <sub>h</sub>	Hold time, data after CLK↑	1.6		1		0.8		0.6		ns

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 15$  pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC2G80 –40°C to 85°C								UNIT
			$V_{CC} = 1.8$ V $\pm 0.15$ V		$V_{CC} = 2.5$ V $\pm 0.2$ V		$V_{CC} = 3.3$ V $\pm 0.3$ V		$V_{CC} = 5$ V $\pm 0.5$ V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			160		160		160		160		MHz
$t_{pd}$	CLK	$\bar{Q}$	3	9.1	1.5	6	1.3	4.2	1.1	3.8	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30$  pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC2G80 –40°C to 85°C								UNIT
			$V_{CC} = 1.8$ V $\pm 0.15$ V		$V_{CC} = 2.5$ V $\pm 0.2$ V		$V_{CC} = 3.3$ V $\pm 0.3$ V		$V_{CC} = 5$ V $\pm 0.5$ V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			160		160		160		160		MHz
$t_{pd}$	CLK	$\bar{Q}$	3.8	13.9	1.5	7	1.4	5.2	0.9	4.5	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30$  pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

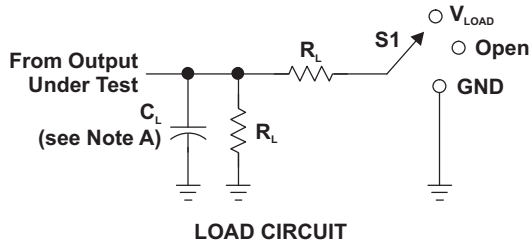
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC2G80 –40°C to 125°C								UNIT
			$V_{CC} = 1.8$ V $\pm 0.15$ V		$V_{CC} = 2.5$ V $\pm 0.2$ V		$V_{CC} = 3.3$ V $\pm 0.3$ V		$V_{CC} = 5$ V $\pm 0.5$ V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			160		160		160		160		MHz
$t_{pd}$	CLK	$\bar{Q}$	3.8	14.5	1.5	7.5	1.4	5.8	0.9	5	ns

### Operating Characteristics

$T_A = 25^\circ\text{C}$

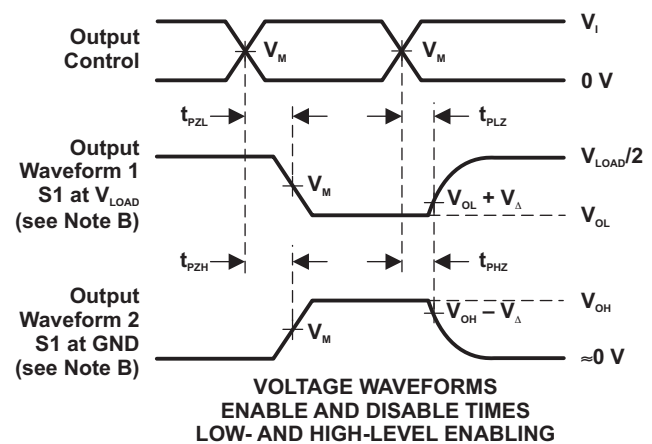
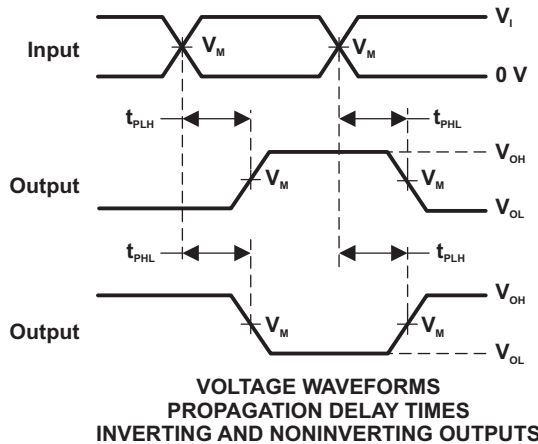
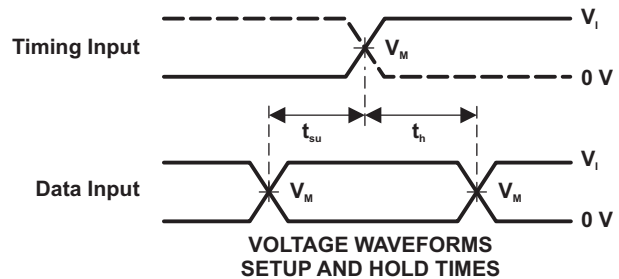
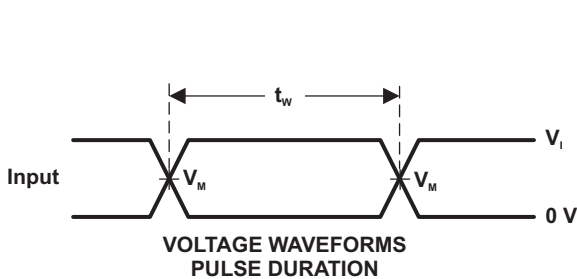
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	$V_{CC} = 5$ V	UNIT
		TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance $f = 10$ MHz	21	21	22	25	pF

Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

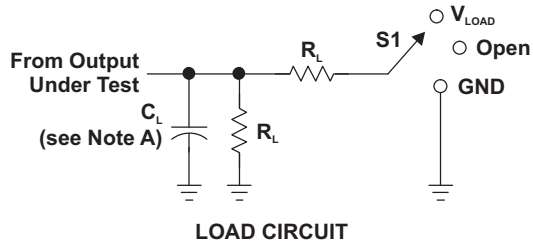
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_i/t_r$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.3 V



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

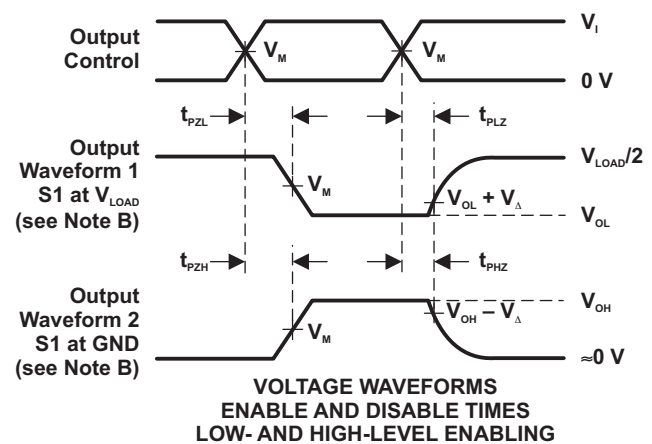
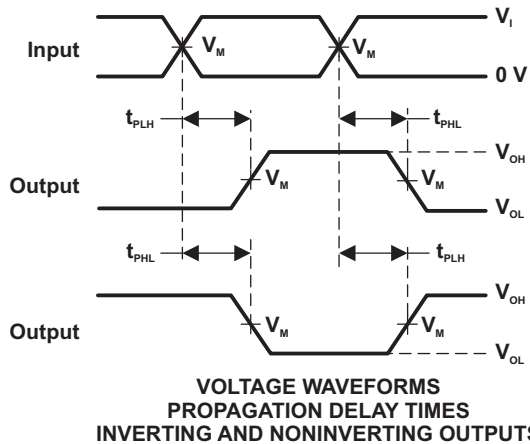
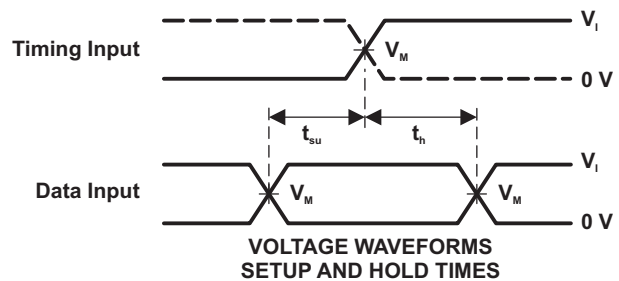
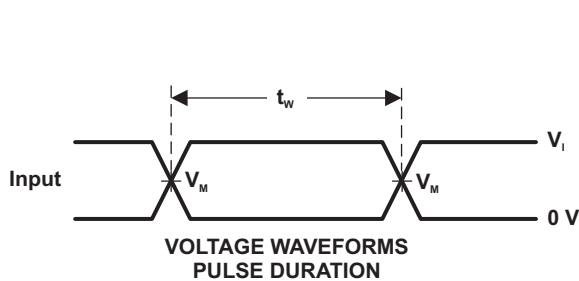
Figure 1. Load Circuit and Voltage Waveforms

Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t/t_i$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

## REVISION HISTORY

Changes from Revision E (February 2007 ) to Revision F	Page
• Updated document to new TI data sheet format. ....	1
• Removed Ordering Information table. ....	1
• Added ESD warning. ....	2
• Updated operating temperature range. ....	3

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G80DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80 Z	<a href="#">Samples</a>
SN74LVC2G80DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80 Z	<a href="#">Samples</a>
SN74LVC2G80DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	(C80Q ~ C80R)	<a href="#">Samples</a>
SN74LVC2G80DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80R	<a href="#">Samples</a>
SN74LVC2G80YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CXN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G80DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G80DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G80DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G80DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G80YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

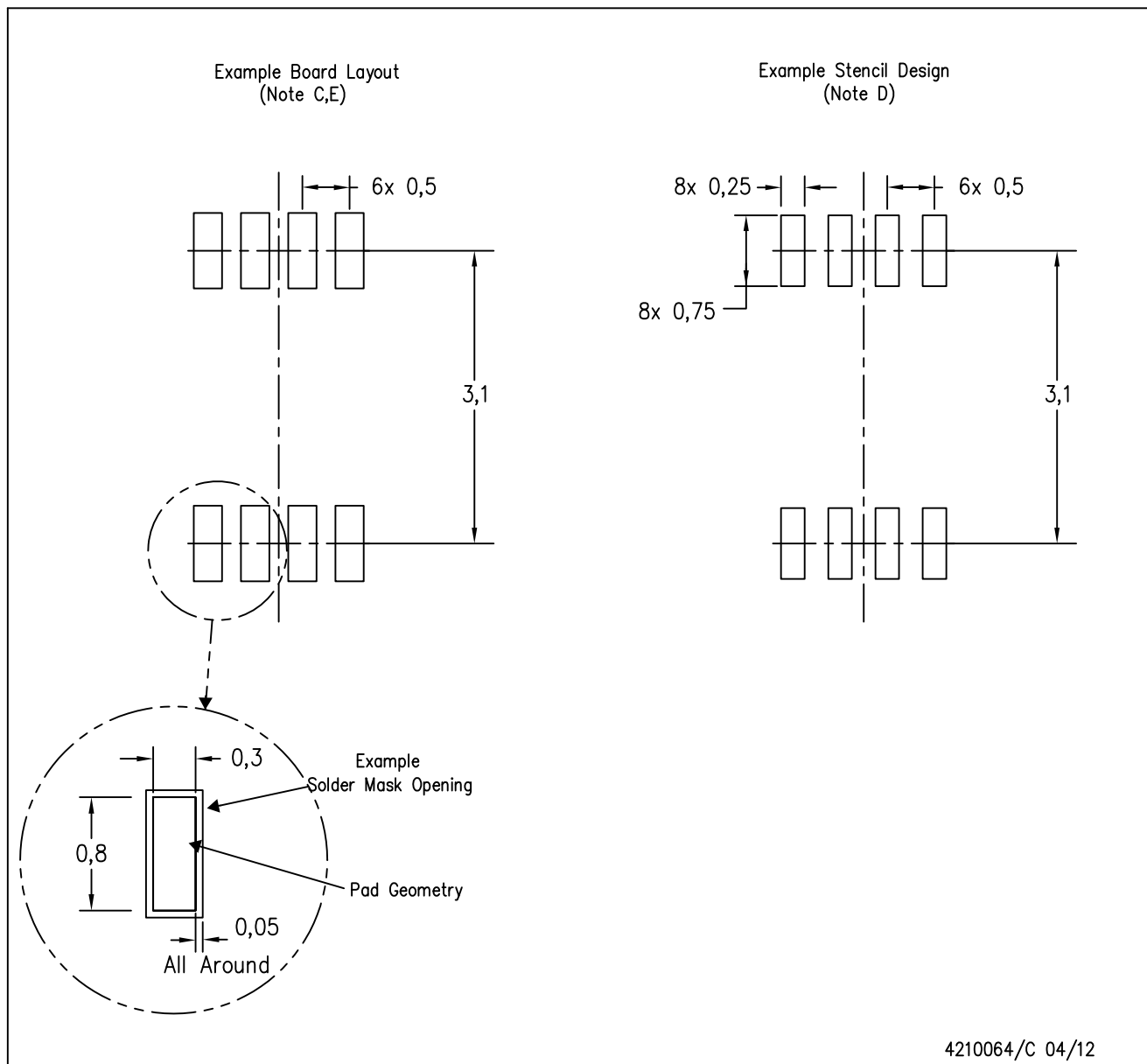

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G80DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G80DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G80DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G80DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G80YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



DCU (S-PDSO-G8)

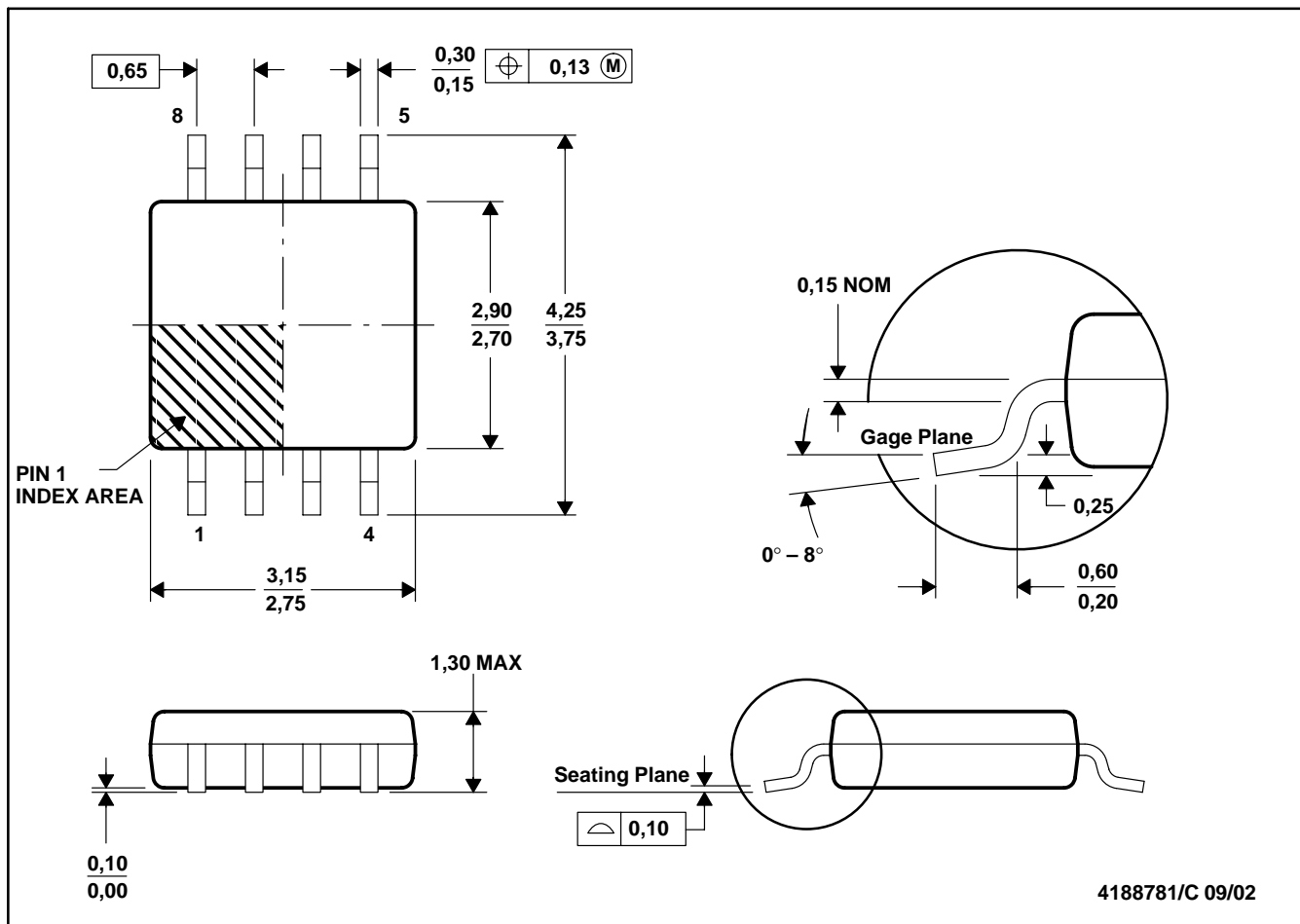
PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

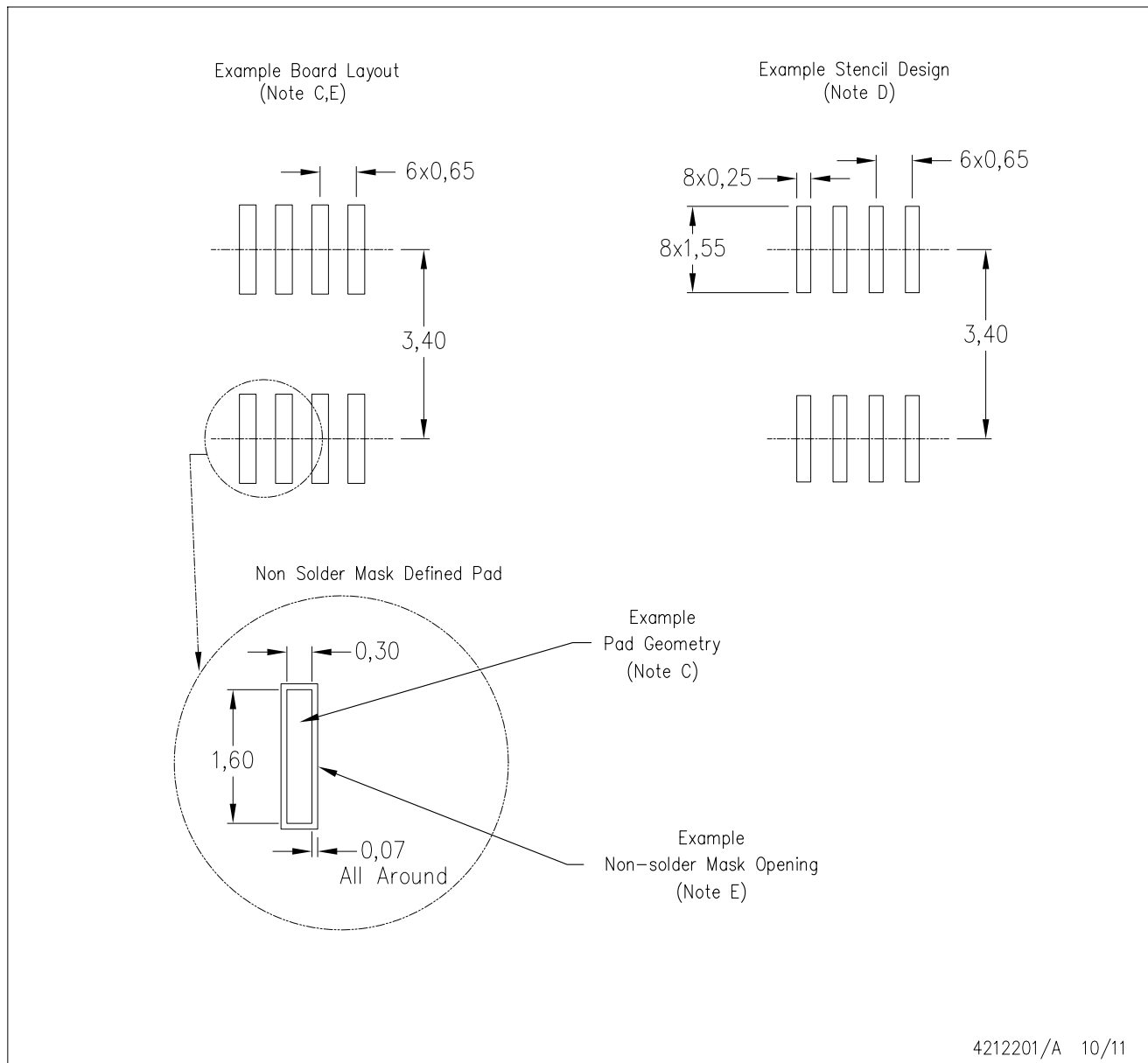


4188781/C 09/02

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion  
 D. Falls within JEDEC MO-187 variation DA.

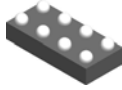
DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

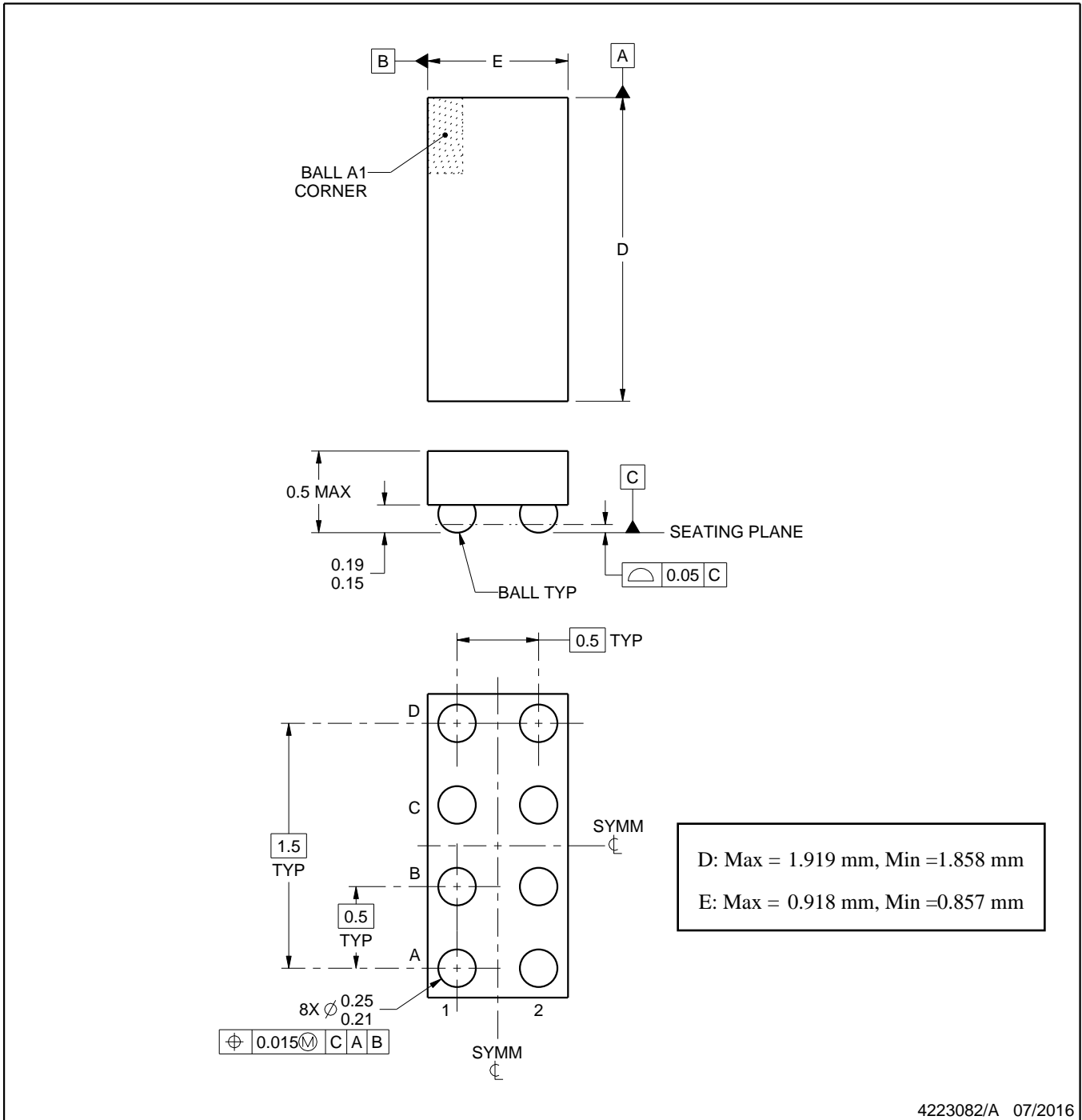
YZP0008



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

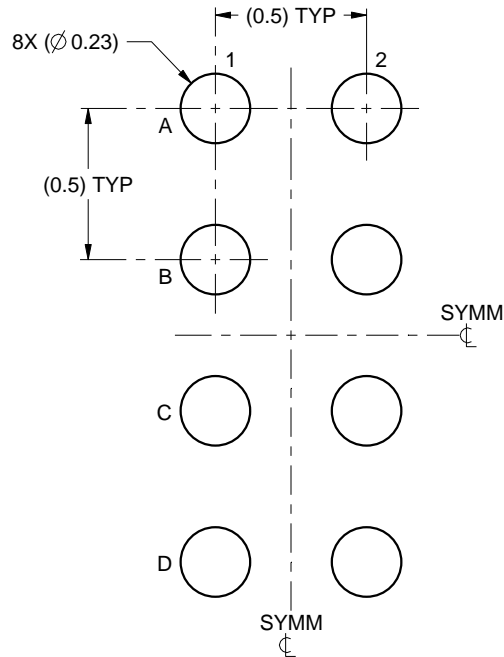
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

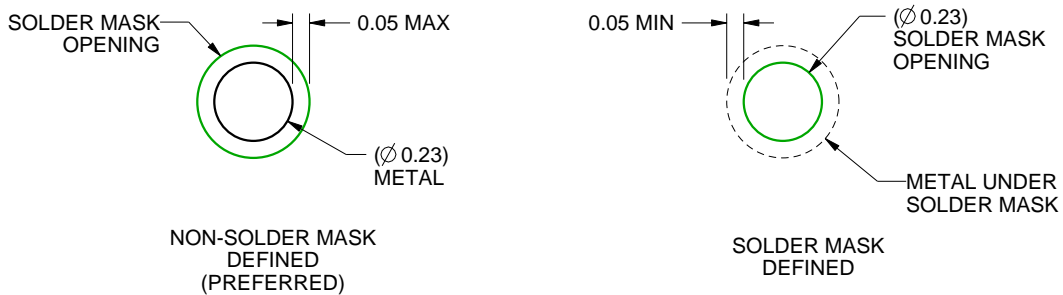
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

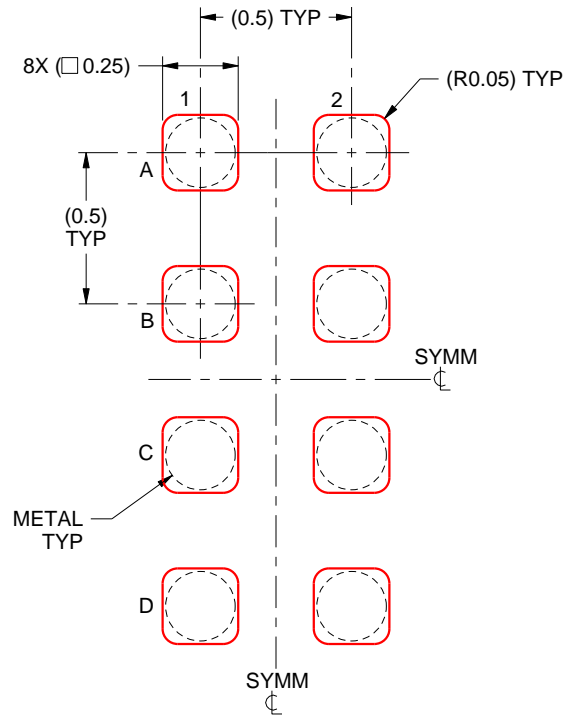
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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