THE DATASHEET OF

TISP4070J1BJR-S

TISP4070J1BJ THRU TISP4395J1BJ

BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

TISP4xxxJ1BJ Overvoltage Protector Series

Ground Return Element of Y Configuration
-2x Current Capability of Y Upper Elements
-Available in a Wide Range of Voltages
-Enables Symmetrical and Asymmetrical Y Designs
-SMB (DO-214AA) Package

Ion-Implanted Breakdown Region
-Precise and Stable Voltage
-Low Voltage Overshoot Under Surge

Device	V_{DRM} V	$V_{(BO)}$ V
TISP4070J1	58	70
TISP4080J1	65	80
TISP4095J1	75	95
TISP4115J1	90	115
TISP4125J1	100	125
TISP4145J1	120	145
TISP4165J1	135	165
TISP4180J1	145	180
TISP4200J1	155	200
TISP4219J1	180	219
TISP4250J1	190	250
TISP4290J1	220	290
TISP4350J1	275	350
TISP4395J1	320	395

..... UL Recognized Components

SMB Package (Top View)

MD4JAA

Device Symbol

SD4JAA

Rated for International Surge Wave Shapes

Wave Shape	Standard	I_{PPSM} A
2/10	GR-1089-CORE	1000
8/20	IEC 61000-4-5	800
10/160	TIA/EIA-IS-968 (FCC Part 68)	400
10/700	ITU-T K.20/21/45	350
10/560	TIA/EIA-IS-968 (FCC Part 68)	250
10/1000	GR-1089-CORE	200

Description

The TISP4xxxJ1BJ is a symmetrical voltage-triggered bidirectional thyristor device which has been designed as the tail (ground return) element of a Y circuit configured protector. As such, the TISP4xxxJ1BJ must be rated to conduct the sum of the TIP and RING currents. For example, the normal GR-1089-CORE testing can impose 200 A, 10/1000 and 1000 A, 2/10 on the ground return element of the Y configuration. Using the TISP4xxxJ1BJ together with two TISP4xxxH3BJ parts gives a 2x 100 A, 10/1000 Y protector circuit. For ITU-T applications, using the TISP4xxxJ1BJ with a TISP3xxxT3BJ gives a coordinated Y protector with a 2x 120 A, 5/310 capability. Design tables are given in the Applications Information section. These SMB package combinations are often more space efficient than single package Y protection multi-chip integrations.

These devices allow signal voltages, without clipping, up to the maximum off-state voltage value, V_{DRM}, see Figure 1. Voltages above V_{DRM} are limited and will not exceed the breakover voltage, $V_{(BO)}$, level. If sufficient current flows due to the overvoltage, the device switches into a low-voltage on-state condition, which diverts the current from the overvoltage through the device. When the diverted current falls below the holding current, I_H, level the devices switches off and restores normal system operation.

How to Order

Device	Package	Carrier	Order As
TISP4xxxJ1BJ	BJ (SMB/DO-214AA J-Bend)	R (Embossed Tape Reeled)	TISP4xxxJ1BJR-S

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
SEPTEMBER 2001 - REVISED JANUARY 2007
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage	’4070	V_{DRM}	±58	V
	’4080		±65	
	’4095		±75	
	’4115		±90	
	’4125		±100	
	’4145		±120	
	’4165		±135	
	’4180		±145	
	’4200		±155	
	’4219		±180	
	’4250		±190	
	’4290		±220	
	’4350		±275	
	‘4395		±320	
Non-repetitive peak on-state pulse current (see Notes 1 and 2)				
2/10 (Telcordia GR-1089-CORE, 2/10 voltage wave shape)		I_{PPSM}	1000	A
8/20 (IEC 61000-4-5, combination wave generator, 1.2/50 voltage wave shape)			800	
10/160 (TIA/EIA-IS-968 (Replaces FCC Part 68), 10/160 voltage wave shape)			400	
4/250 (ITU-T K.20/21, 10/700 voltage wave shape, simultaneous)			370	
5/310 (ITU-T K.20/21, 10/700 voltage wave shape, single)			350	
5/320 (TIA/EIA-IS-968 (Replaces FCC Part 68), 9/720 voltage wave shape, single)			350	
10/560 (TIA/EIA-IS-968 (Replaces FCC Part 68), 10/560 voltage wave shape)			250	
10/1000 (Telcordia GR-1089-CORE, 10/1000 voltage wave shape)			200	
Non-repetitive peak on-state current (see Notes 1 and 2)				
50 Hz, 1 cycle		I_{TSM}	80	A
60 Hz, 1 cycle			100	
Initial rate of rise of on-state current, Linear current ramp, Maximum ramp value < 50 A		di_T/dt	800	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. Initially, the device must be in thermal equilibrium with T_J = 25 °C.
2. These non-repetitive rated currents are peak values of either polarity. The surge may be repeated after the device returns to its initial conditions.

Recommended Operating Conditions

Component		Min	Typ	Max	Unit
R1, R2	Series resistor for GR-1089-CORE first-level surge survival	0			Ω
	Series resistor for ITU-T recommendation K.20/K.45/K.21 (Basic coordination with 400 V GDT)	6.5			
	Series resistor for TIA/EIA-IS-968 (Replaces FCC Part 68), 9/720 survival	0			
	Series resistor for TIA/EIA-IS-968 (Replaces FCC Part 68), 10/560 survival	0			
	Series resistor for TIA/EIA-IS-968 (Replaces FCC Part 68), 10/160 survival	0			

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Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = \pm V_{DRM}$	T_A = 25 °C			±5	μA
			T_A = 85 °C			±10	
$V_{(BO)}$	AC breakover voltage	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω	4070			±70	V
			’4080			±80	
			’4095			±95	
			’4115			±115	
			’4125			±125	
			’4145			±145	
			’4165			±165	
			’4180			±180	
			’4200			±200	
			’4219			±219	
			’4250			±250	
			’4290			±290	
			’4350			±350	
			‘4395			±395	
$V_{(BO)}$	Ramp breakover voltage	dv/dt ≤±1000 V/μs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/μs, Linear current ramp, Maximum ramp value = ±10 A	4070			±77	V
			’4080			±88	
			’4095			±104	
			’4115			±125	
			’4125			±135	
			’4145			±156	
			’4165			±177	
			’4180			±192	
			’4200			±212	
			’4219			±231	
			’4250			±263	
			’4290			±303	
			’4350			±364	
			‘4395			±409	
$V_{(BO)}$	Impulse breakover voltage	2/10 wave shape, I_{PP} = ±1000 A, R_S = 2.5 Ω, (see Note 3)	4070		±96		V
			’4080		±101		
			’4095		±112		
			’4115		±130		
			’4125		±140		
			’4145		±161		
			’4165		±183		
			’4180		±199		
			’4200		±221		
			’4219		±242		
			’4250		±276		
			’4290		±320		
			’4350		±386		
			‘4395		±434		

NOTE 3: Dynamic voltage measurements should be made with an oscilloscope with limited band width (20 MHz) to avoid high frequency noise.

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Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted) (Continued)

Parameter		Test Conditions		Min	Typ	Max	Unit
$I_{(BO)}$	Breakover current	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω				±600	mA
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±20			mA
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85 V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V	T_A = 85 °C			±10	µA
C_{off}	Off-state capacitance	f = 1 MHz, Vd = 1 V rms, V_D = 0,	'4070 thru '4115		195	235	pF
			'4125 thru '4219		120	145	
			'4250 thru '4395		105	125	
		f = 1 MHz, Vd = 1 V rms, V_D = -1 V	'4070 thru '4115		180	215	
			'4125 thru '4219		110	132	
			'4250 thru '4395		95	115	
		f = 1 MHz, Vd = 1 V rms, V_D = -2 V	'4070 thru '4115		165	200	
			'4125 thru '4219		100	120	
			'4250 thru '4395		90	105	
		f = 1 MHz, Vd = 1 V rms, V_D = -50 V	'4070 thru '4115		85	100	
			'4125 thru '4219		50	60	
			'4250 thru '4395		42	50	
		f = 1 MHz, Vd = 1 V rms, V_D = -100 V	'4125 thru '4219		40	50	
		(see Note 4)	'4250 thru '4395		35	40	

NOTE 4: To avoid possible voltage clipping, the '4125 is tested with V_D = -98 V

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 5)			90	°C/W

NOTE 5: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

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Parameter Measurement Information

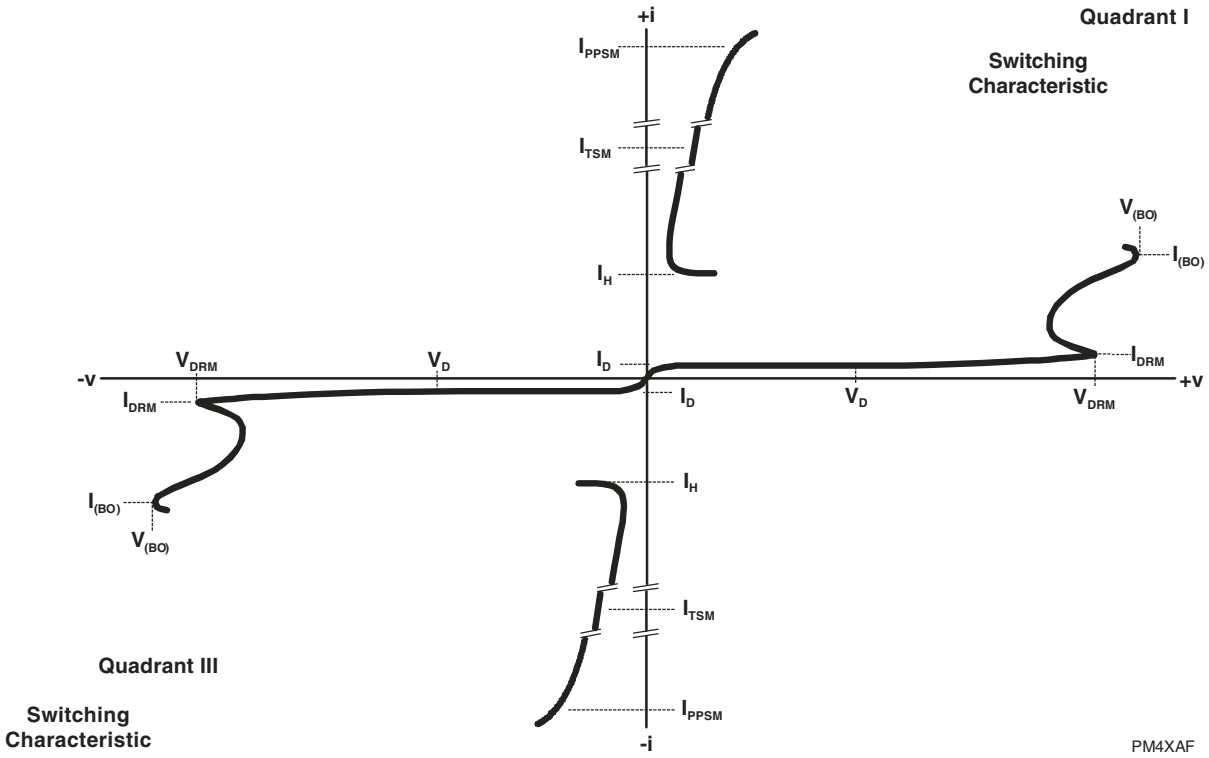

Figure 1. Voltage-Current Characteristic for Terminals 1-2
All Measurements are Referenced to Terminal 2

Specifications are subject to change without notice.
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Typical Characteristics

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

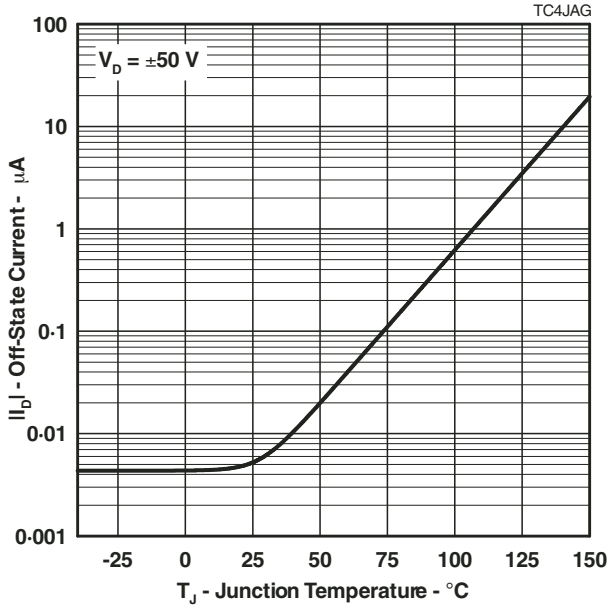

Figure 2.

NORMALIZED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

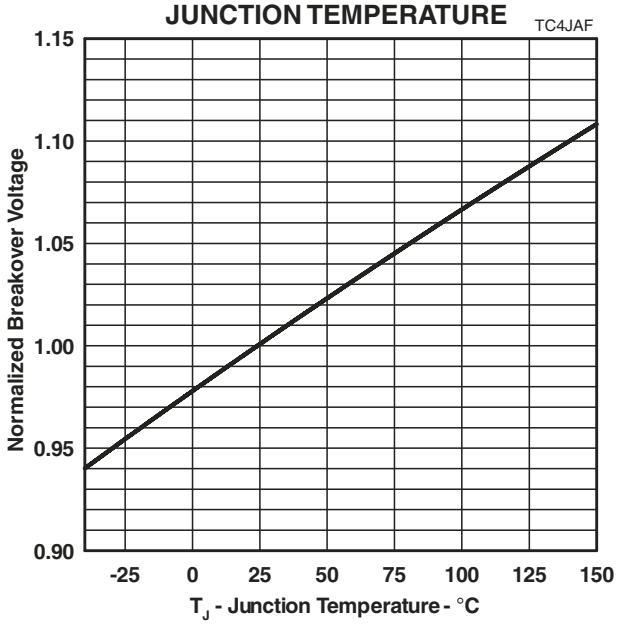

Figure 3.

ON-STATE CURRENT vs ON-STATE VOLTAGE

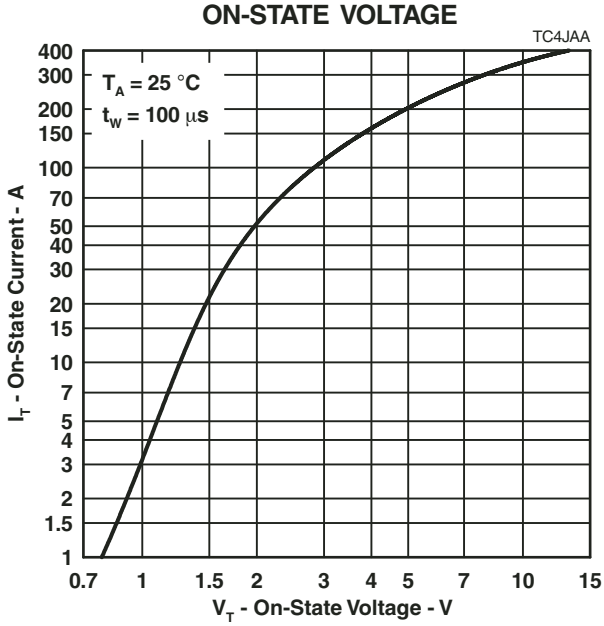

Figure 4.

NORMALIZED HOLDING CURRENT vs JUNCTION TEMPERATURE

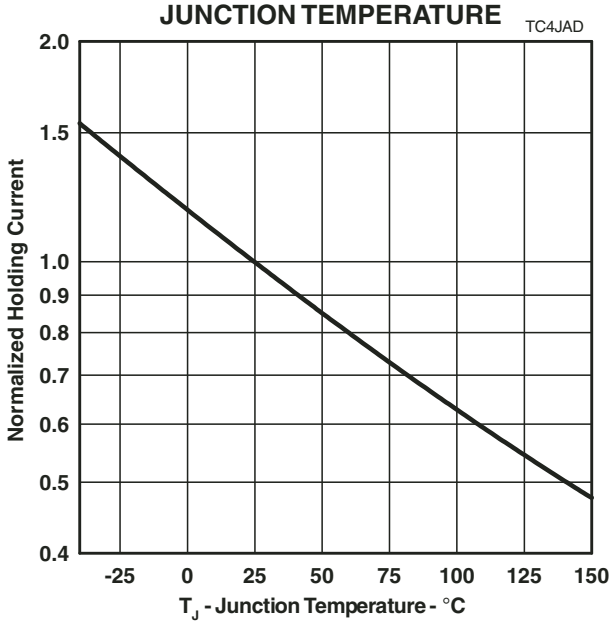

Figure 5.

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Typical Characteristics

NORMALIZED CAPACITANCE vs OFF-STATE VOLTAGE

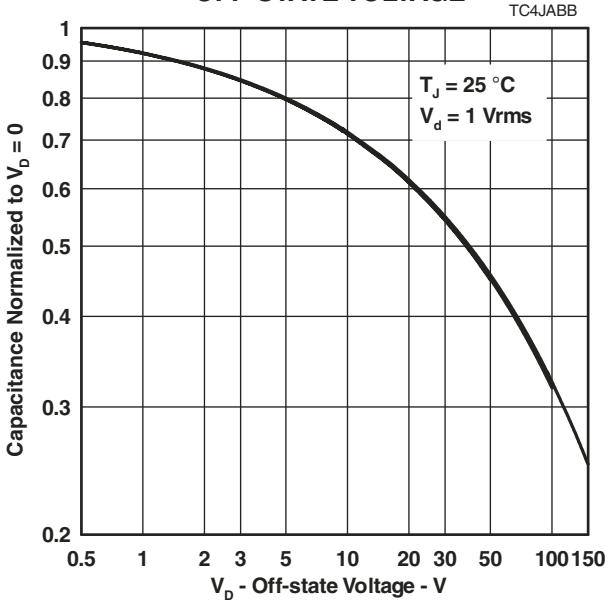

Figure 6.

DIFFERENTIAL OFF-STATE CAPACITANCE vs RATED REPETITIVE PEAK OFF-STATE VOLTAGE

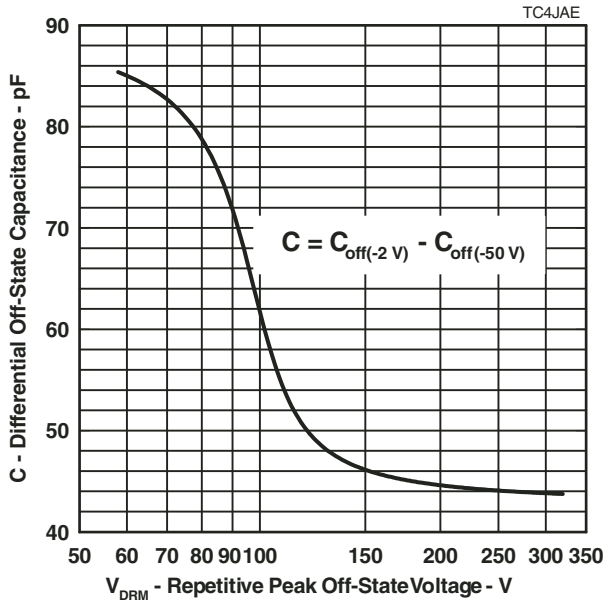

Figure 7.

NORMALIZED CAPACITANCE ASYMMETRY vs OFF-STATE VOLTAGE

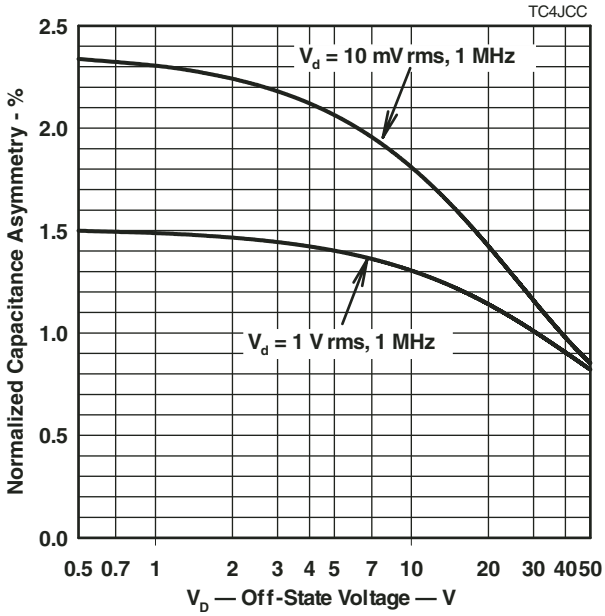

Figure 8.

Specifications are subject to change without notice.
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Rating and Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

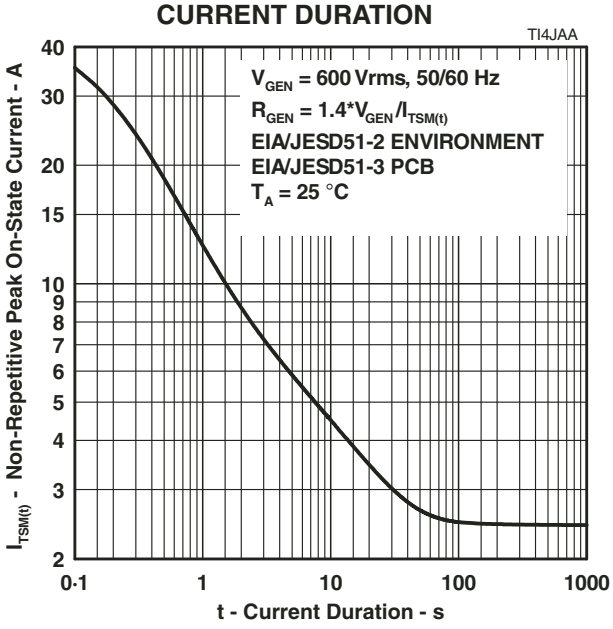

Figure 9.

V_{DRM} DERATING FACTOR vs MINIMUM AMBIENT TEMPERATURE

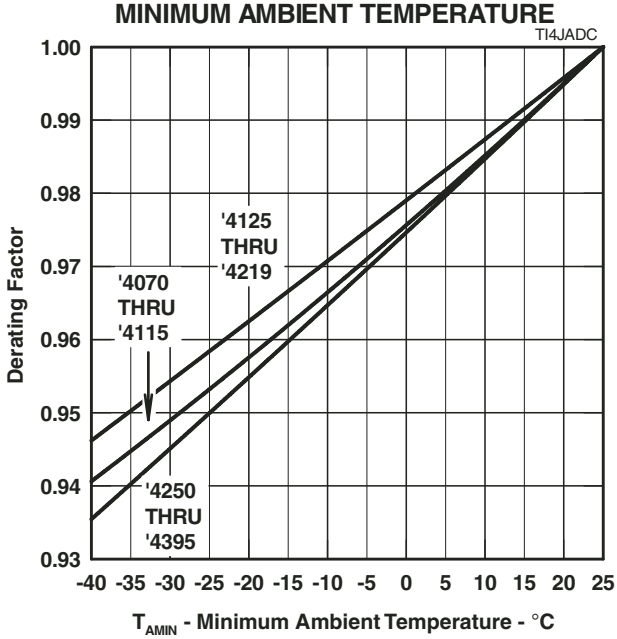

Figure 10.

Specifications are subject to change without notice.
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APPLICATIONS INFORMATION

Y Configuration Design

This protection configuration has three modes of protection. The RING to TIP terminal pair protection is given by the series combination of protectors Th1a and Th1b, see Figure 11. The terminal pair protection voltage will be the sum of the $V_{(BO)}$, breakover voltage, of Th1a and the $V_{(BO)}$ of Th1b. Protectors Th1a and Th1b are the same device type and the terminal pair protection voltage will be 2 $V_{(BO)1}$. For a terminal pair protection voltage of ±400 V, Th1a and Th1b would have $V_{(BO)1}$ = ±400/2 = ±200 V.

Similarly for the other terminal pairs, RING to GROUND protection is given by the series combination of Th1b and Th2 and the terminal pair protection voltage is $V_{(BO)1} + V_{(BO)2}$. TIP to GROUND protection voltage will also be $V_{(BO)1} + V_{(BO)2}$.

The maximum terminal pair voltage before clipping might occur is the sum of the protector V_{DRM}, off-state voltages, see Figure 12. For RING to TIP this will be 2 V_{DRM1}. The ±200 V $V_{(BO)1}$ protectors of the previous example have a V_{DRM} of ±155 V, giving a maximum non-clipping signal voltage of ±310 V. For RING to GROUND and TIP to GROUND terminal pairs, the maximum non-clipping signal voltage will be $V_{DRM1} + V_{DRM2}$.

Under longitudinal surge conditions, when the prospective currents of the line conductors, I_{RING} and I_{TIP}, are equal, Th2, the ground return protector, carries the sum of the Th1a and Th1b currents, see Figure 13. The current rating of Th2 must be twice that of Th1a and Th1b.

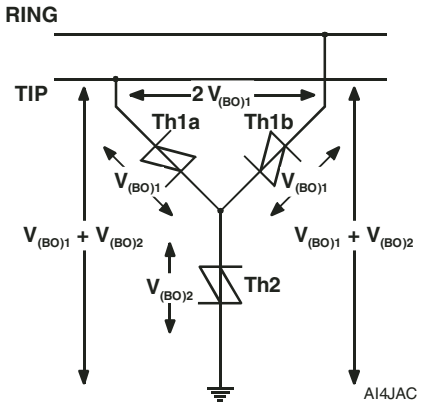

Figure 11. Protection Voltage

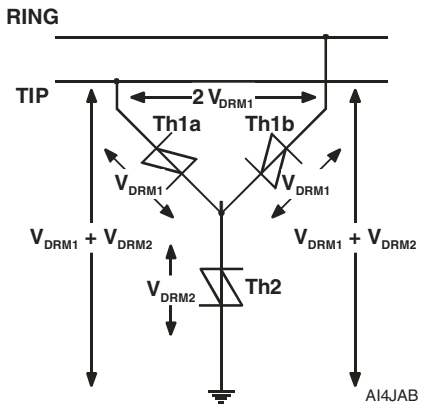

Figure 12. Off-State Voltage

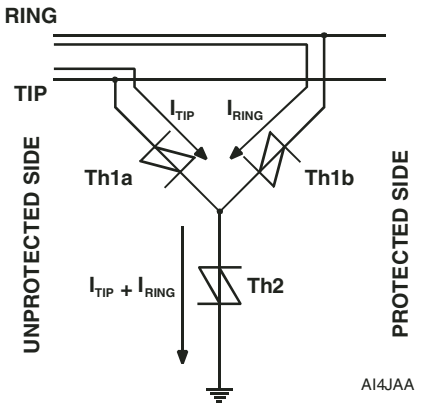

Figure 13. Current Flow

GR-1089-CORE Designs

The main impulse waveforms of the standard are 500 A, 2/10 and 100 A, 10/1000. Assuming fuse current limiters, F1a and F1b, a suitable Th1a and Th1b protector for these conductor currents is the TISP4xxxH3BJ series of devices. The ground return protector, Th2, must be rated for at least 1000 A,2/10 and 200 A, 10/1000. A suitable Th2 protector for these ground currents is the TISP4xxxJ1BJ series of devices. This arrangement is shown in Figure 14 and the following table lists all the catalogue device combinations.

RING to TIP Voltages		RING to GROUND, TIP to GROUND Voltages		GR-1089-CORE Y Configuration Parts and Part Voltages			
V_{DRM} V	$V_{(BO)}$ V	V_{DRM} V	$V_{(BO)}$ V	Th1a, Th1b Part #	Th2 Part #	V_{DRM} V	$V_{(BO)}$ V
±116	±140	±116	±140	TISP4070H3BJ	TISP4070J1BJ	±58	±70
±130	±160	±130	±160	TISP4080H3BJ	TISP4080J1BJ	±65	±80
±150	±190	±150	±190	TISP4095H3BJ	TISP4095J1BJ	±75	±95
±180	±230	±180	±230	TISP4115H3BJ	TISP4115J1BJ	±90	±115
±200	±250	±200	±250	TISP4125H3BJ	TISP4125J1BJ	±100	±125
±240	±290	±240	±290	TISP4145H3BJ	TISP4145J1BJ	±120	±145
±270	±330	±270	±330	TISP4165H3BJ	TISP4165J1BJ	±135	±165
±290	±360	±290	±360	TISP4180H3BJ	TISP4180J1BJ	±145	±180
±310	±400	±310	±400	TISP4200H3BJ	TISP4200J1BJ	±155	±200
±360	±438	±360	±438	TISP4219H3BJ	TISP4219J1BJ	±180	±219

Specifications are subject to change without notice.
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GR-1089-CORE Designs (Continued)

RING to TIP Voltages		RING to GROUND, TIP to GROUND Voltages		GR-1089-CORE Y Configuration Parts and Part Voltages			
V_{DRM} V	$V_{(BO)}$ V	V_{DRM} V	$V_{(BO)}$ V	Th1a, Th1b Part #	Th2 Part #	V_{DRM} V	$V_{(BO)}$ V
±380	±500	±380	±500	TISP4250H3BJ	TISP4250J1BJ	±190	±250
±440	±580	±440	±580	TISP4290H3BJ	TISP4290J1BJ	±220	±290
±550	±700	±550	±700	TISP4350H3BJ	TISP4350J1BJ	±275	±350
±640	±790	±640	±790	TISP4395H3BJ	TISP4395J1BJ	±320	±395

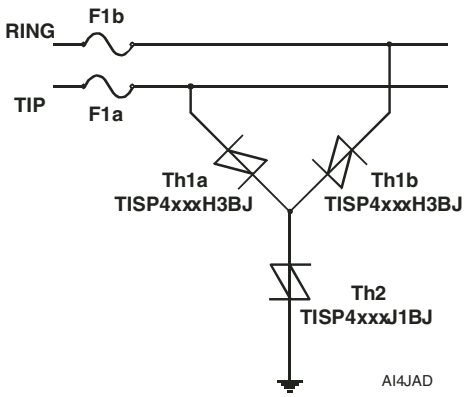

Figure 14. GR-1089-CORE Design

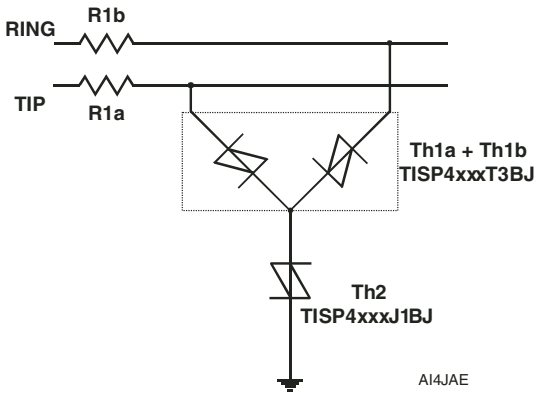

Figure 15. Coordinated ITU-T K Recommendation Design

ITU-T K.20, K.45 and K.21 Designs

The main impulse voltage wave shape of these recommendations is 10/700. The current wave shape is loading dependent, but it is 5/310 into a short circuit. To coordinate with a ±400 V primary protector a minimum series resistance of 6.5 Ω is required ("The New ITU-T Telecommunication Equipment Resistibility Recommendations", Compliance Engineering Magazine, January-February 2002). The coordination resistance limits the peak non-truncated current to ±400/6.5 = 62 A. A suitable Th1a and Th1b protector for these conductor currents is the TISP3xxxT3BJ series of devices, which combine Th1a and Th1b in a single SMB3 package. The ground return protector, Th2, must be rated for at least 124 A of a 5/310 waveshape. Suitable Th2 protectors for these ground currents are the TISP4xxxH3BJ or TISP4xxxJ1BJ series of devices. The arrangement is shown in Figure 15 and the following table lists all the catalogue device combinations. Using the SMB3 packaged TISP3xxxT3BJ saves one third of the PCB placement area compared to solution using three single protector SMB packaged devices.

RING to TIP Voltages		RING to GROUND, TIP to GROUND Voltages		ITU-T Y Configuration Parts and Part Voltages R1a = R1b = 6.5 Ω			
V_{DRM} V	$V_{(BO)}$ V	V_{DRM} V	$V_{(BO)}$ V	Th1a + Th1b Part #	Th2 Part #	V_{DRM} V	$V_{(BO)}$ V
±116	±140	±116	±140	TISP3070T3BJ	TISP4070J1BJ	±58	±70
±130	±160	±130	±160	TISP3080T3BJ	TISP4080J1BJ	±65	±80
±150	±190	±150	±190	TISP3095T3BJ	TISP4095J1BJ	±75	±95
±180	±230	±180	±230	TISP3115T3BJ	TISP4115J1BJ	±90	±115
±200	±250	±200	±250	TISP3125T3BJ	TISP4125J1BJ	±100	±125
±240	±290	±240	±290	TISP3145T3BJ	TISP4145J1BJ	±120	±145
±270	±330	±270	±330	TISP3165T3BJ	TISP4165J1BJ	±135	±165
±290	±360	±290	±360	TISP3180T3BJ	TISP4180J1BJ	±145	±180
±310	±400	±310	±400	TISP3200T3BJ	TISP4200J1BJ	±155	±200
±360	±438	±360	±438	TISP3219T3BJ	TISP4219J1BJ	±180	±219
±380	±500	±380	±500	TISP3250T3BJ	TISP4250J1BJ	±190	±250
±440	±580	±440	±580	TISP3290T3BJ	TISP4290J1BJ	±220	±290

Specifications are subject to change without notice.
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ITU-T K.20, K.45 and K.21 Designs (Continued)

RING to TIP Voltages		RING to GROUND, TIP to GROUND Voltages		ITU-T Y Configuration Parts and Part Voltages R1a = R1b = 6.5 Ω			
V_{DRM} V	$V_{(BO)}$ V	V_{DRM} V	$V_{(BO)}$ V	Th1a + Th1b Part #	Th2 Part #	V_{DRM} V	$V_{(BO)}$ V
±550	±700	±550	±700	TISP3350T3BJ	TISP4350J1BJ	±275	±350
±640	±790	±640	±790	TISP3395T3BJ	TISP4395J1BJ	±320	±395

Asymmetrical Designs

These designs are for special needs, where the RING to TIP protection voltage must be different to the RING to GROUND and TIP to GROUND voltages. ADSL modem interfaces often have a need for asymmetric voltage limiting, see Figure 16. Here, the RING to TIP voltage limitation is given by the d.c. blocking capacitor, C1, and the RING to GROUND and TIP to GROUND limitation is insulation breakdown. Often the breakdown limit is set by the spacing of the PW (Printed Wiring) tracks. Figure 17 shows a solution. Using two ±165 V $V_{(BO)}$ parts for Th1a and Th1b, the RING to TIP voltage is limited to ±330 V. Using a higher voltage ±350 V $V_{(BO)}$ part for Th2 limits the insulation stress to ±515 V. Figure 17 and its following table is for a GR-1089-CORE compliant design.

RING to TIP Voltages		RING to GROUND, TIP to GROUND Voltages		GR-1089-CORE Y Configuration Parts and Part Voltages					
				Th1a, Th1b			Th2		
V_{DRM} V	$V_{(BO)}$ V	V_{DRM} V	$V_{(BO)}$ V	Part #	V_{DRM} V	$V_{(BO)}$ V	Part #	V_{DRM} V	$V_{(BO)}$ V
±270	±330	±410	±515	TISP4165H3BJ	±135	±165	TISP4350J1BJ	±275	±350

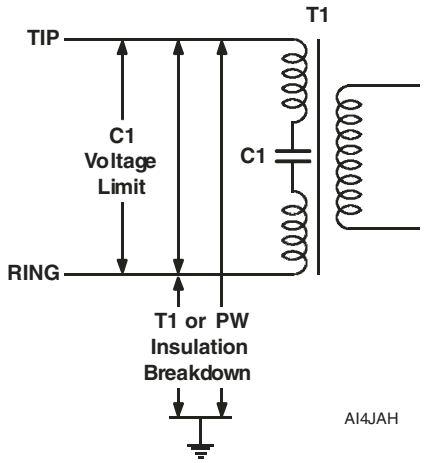


Figure 16. ADSL Modem Interface Voltage Limitations

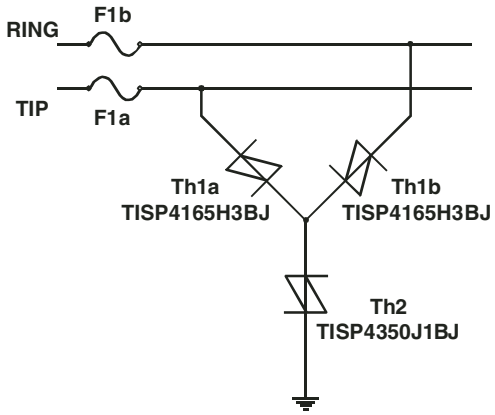


Figure 17. Asymmetrical Design for US ADSL Modems

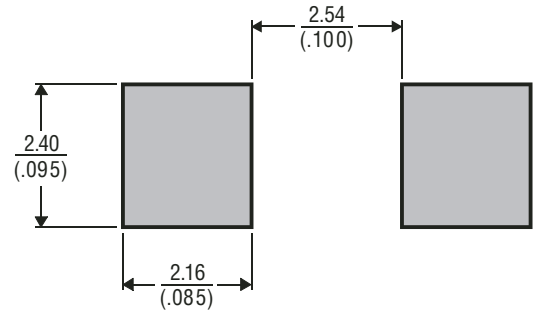
An ITU-T compliant design would probably require the replacement of the fuses by coordination resistors. With a ±410 V off-state voltage, this may seem unnecessary as modern primary protectors will switch at lower voltages and automatically coordinate. On a perfect longitudinal waveform this is true. However, the ITU-T also applies a transverse (metallic) test as well, to simulate non-simultaneous switching of the primary protection. In this case, one conductor is grounded, which places the RING to TIP protection in parallel with the unswitched primary protector. The ±270 V off-state voltage is likely to be lower than the primary switching voltage and there isn't coordination. Under GR-1089-CORE conditions with non-simultaneous switching, the 100 A 10/1000 current, which should have gone through the unswitched primary protector, is diverted through the top arms of the Y into the switched primary, causing a 200 A current flow in that primary protector.

Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

MECHANICAL DATA

Recommended Printed Wiring Land Pattern Dimensions

SMB Land Pattern



DIMENSIONS ARE: MILLIMETERS / (INCHES)

MDXX BID

Device Symbolization Code

Devices will be coded as below. As the device parameters are symmetrical, terminal 1 is not identified.

Device	Symbolization Code
TISP4070J1	4070J1
TISP4080J1	4080J1
TISP4095J1	4095J1
TISP4115J1	4115J1
TISP4125J1	4125J1
TISP4145J1	4145J1
TISP4165J1	4165J1
TISP4180J1	4180J1
TISP4200J1	4200J1
TISP4219J1	4219J1
TISP4250J1	4250J1
TISP4290J1	4290J1
TISP4350J1	4350J1
TISP4395J1	4395J1

Carrier Information

For production quantities, the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

Package	Carrier	Standard Quantity
SMB	Embossed Tape Reel Pack	3000

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