TC426/TC427/TC428

1.5A Dual High-Speed Power MOSFET Drivers

Features:

- High-Speed Switching (C_L = 1000 pF): 30 nsec
- High Peak Output Current: 1.5A
- High Output Voltage Swing:
  - V_{DD} -25 mV
  - GND +25 mV
- Low Input Current (Logic ‘0’ or ‘1’): 1 μA
- TTL/CMOS Input Compatible
- Available in Inverting and Noninverting Configurations
- Wide Operating Supply Voltage:
  - 4.5V to 18V
- Current Consumption:
  - Inputs Low – 0.4 mA
  - Inputs High – 8 mA
- Single Supply Operation
- Low Output Impedance: 6Ω
- Pinout Equivalent of DS0026 and MMH0026
- Latch-Up Resistant: Withstands > 500 mA Reverse Current
- ESD Protected: 2 kV

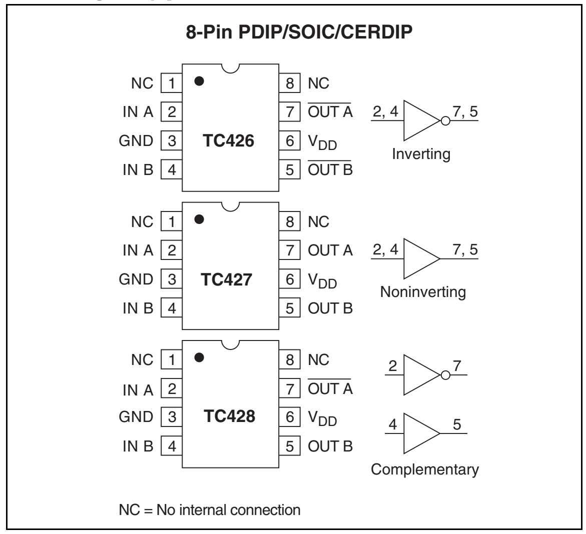
Applications:

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Clock Line Driver
- Coax Cable Driver

Device Selection Table

Part Number	Package	Configuration	Temp. Range
TC426COA	8-Pin SOIC	Inverting	0°C to +70°C
TC426CPA	8-Pin PDIP	Inverting	0°C to +70°C
TC426EOA	8-Pin SOIC	Inverting	-40°C to +85°C
TC426EPA	8-Pin PDIP	Inverting	-40°C to +85°C
TC426IJA	8-Pin CERDIP	Inverting	-25°C to +85°C
TC426MJA	8-Pin CERDIP	Inverting	-55°C to +125°C
TC427COA	8-Pin SOIC	Noninverting	0°C to +70°C
TC427CPA	8-Pin PDIP	Noninverting	0°C to +70°C
TC427EOA	8-Pin SOIC	Noninverting	-40°C to +85°C
TC427EPA	8-Pin PDIP	Noninverting	-40°C to +85°C
TC427IJA	8-Pin CERDIP	Noninverting	-25°C to +85°C
TC427MJA	8-Pin CERDIP	Noninverting	-55°C to +125°C
TC428COA	8-Pin SOIC	Complementary	0°C to +70°C
TC428CPA	8-Pin PDIP	Complementary	0°C to +70°C
TC428EOA	8-Pin SOIC	Complementary	-40°C to +85°C
TC428EPA	8-Pin PDIP	Complementary	-40°C to +85°C
TC428IJA	8-Pin CERDIP	Complementary	-25°C to +85°C
TC428MJA	8-Pin CERDIP	Complementary	-55°C to +125°C

Package Type



General Description:

The TC426/TC427/TC428 are dual CMOS high-speed drivers. A TTL/CMOS input voltage level is translated into a rail-to-rail output voltage level swing. The CMOS output is within 25 mV of ground or positive supply.

The low-impedance, high-current driver outputs swing a 1000 pF load 18V in 30 nsec. The unique current and voltage drive qualities make the TC426/TC427/TC428 ideal power MOSFET drivers, line drivers, and DC-to-DC converter building blocks.

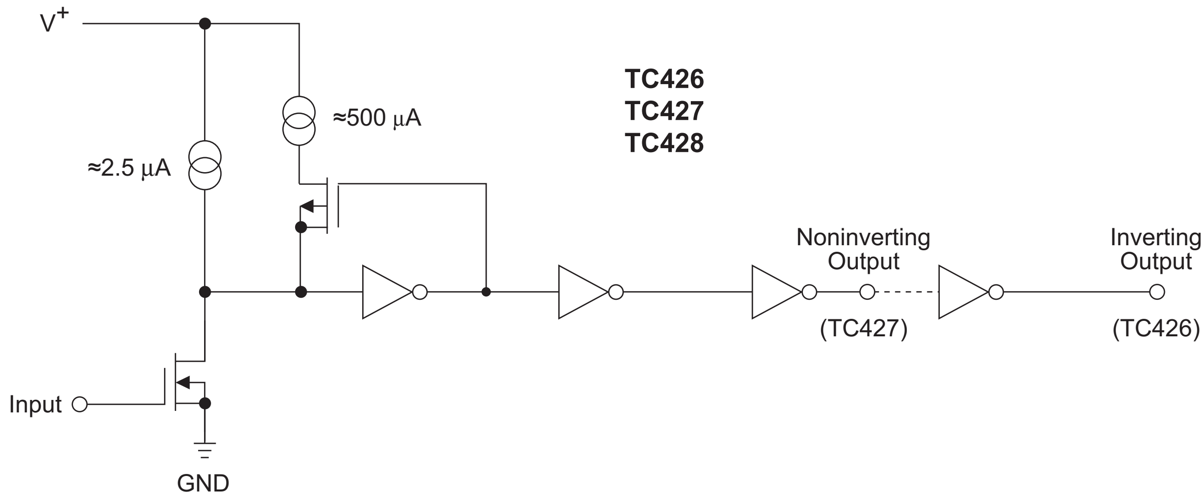
Input logic signals may equal the power supply voltage. Input current is a low 1 μA, making direct interface to CMOS/bipolar switch-mode power supply control ICs possible, as well as open-collector analog comparators.

Quiescent power supply current is 8 mA maximum. The TC426 requires 1/5 the current of the pin-compatible bipolar DS0026 device. This is important in DC-to-DC converter applications with power efficiency constraints and high-frequency switch-mode power supply applications. Quiescent current is typically 6 mA when driving a 1000 pF load 18V at 100 kHz.

The inverting TC426 driver is pin-compatible with the bipolar DS0026 and MMH0026 devices. The TC427 is noninverting; the TC428 contains an inverting and non-inverting driver.

Other pin compatible driver families are the TC1426/TC1427/TC1428, TC4426/TC4427/TC4428 and TC4426A/TC4427A/TC4428A.

Functional Block Diagram



NOTE: TC428 has one inverting and one noninverting driver.
Ground any unused driver input.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage ....+20V
Input Voltage, Any Terminal
.................................V_{DD} + 0.3V to GND – 0.3V
Power Dissipation ($T_A \leq 70°C$)
PDIP..730 mW
CERDIP ....800 mW
SOIC ....470 mW
Derating Factor
PDIP..8 mW/°C
CERDIP ....6.4 mW/°C
SOIC ....4 mW/°C
Operating Temperature Range
C Version .... 0°C to +70°C
I Version ....-25°C to +85°C
E Version.....................................-40°C to +85°C
M Version ....-55°C to +125°C
Storage Temperature Range..............-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC426/TC427/TC428 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise noted.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input						
V_{IH}	Logic 1, High Input Voltage	2.4	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-1	—	1	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
V_{OH}	High Output Voltage	V_{DD} – 0.025	—	—	V	
V_{OL}	Low Output Voltage	—	—	0.025	V	
R_{OH}	High Output Resistance	—	10	15	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
R_{OL}	Low Output Resistance	—	6	10	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
I_{PK}	Peak Output Current	—	1.5	—	A	
Switching Time (Note 1)						
t_R	Rise Time	—	—	30	nsec	Figure 3-1, Figure 3-2
t_F	Fall Time	—	—	30	nsec	Figure 3-1, Figure 3-2
t_{D1}	Delay Time	—	—	50	nsec	Figure 3-1, Figure 3-2
t_{D2}	Delay Time	—	—	75	nsec	Figure 3-1, Figure 3-2
Power Supply						
I_S	Power Supply Current	— —	— —	8 0.4	mA	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)

Note 1: Switching times ensured by design.

TC426/TC427/TC428 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Over operating temperature range with 4.5V $\le V_{DD} \le$ 18V, unless otherwise noted.						
Input						
V_{IH}	Logic 1, High Input Voltage	2.4	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-10	—	10	µA	$0V \le V_{IN} \le V_{DD}$
Output						
V_{OH}	High Output Voltage	V_{DD} – 0.025	—	—	V	
V_{OL}	Low Output Voltage	—	—	0.025	V	
R_{OH}	High Output Resistance	—	13	20	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
R_{OL}	Low Output Resistance	—	8	15	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
t_R	Rise Time	—	—	60	nsec	Figure 3-1, Figure 3-2
t_F	Fall Time	—	—	60	nsec	Figure 3-1, Figure 3-2
t_{D1}	Delay Time	—	—	75	nsec	Figure 3-1, Figure 3-2
t_{D2}	Delay Time	—	—	120	nsec	Figure 3-1, Figure 3-2
Power Supply						
I_S	Power Supply Current	— —	— —	12 0.6	mA	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)

Note 1: Switching times ensured by design.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, SOIC, CERDIP)	Symbol	Description
1	NC	No Internal Connection.
2	IN A	Control Input A, TTL/CMOS compatible logic input.
3	GND	Ground.
4	IN B	Control Input B, TTL/CMOS compatible logic input.
5	OUT B	CMOS totem-pole output.
6	V_{DD}	Supply input, 4.5V to 18V.
7	OUT A	CMOS totem-pole output.
8	NC	No internal Connection.

3.0 APPLICATIONS INFORMATION

3.1 Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 1000 pF load to 18V in 25 nsec requires an 0.72A current from the device power supply.

To ensure low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (< 0.5 in.) should be used. A 1 µF film capacitor in parallel with one or two 0.1 µF ceramic disk capacitors normally provides adequate bypassing.

3.2 Grounding

The TC426 and TC428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

3.3 Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic ‘1’ input, the maximum quiescent supply current is 8 mA. Logic ‘0’ input level signals reduce quiescent current to 0.4 mA maximum. Minimum power dissipation occurs for logic ‘0’ inputs for the TC426/TC427/TC428. **Unused driver inputs must be connected to V_{DD} or GND**.

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making the device TTL compatible over the 4.5V to 18V supply operating range. Input current is less than 1 µA over this range.

The TC426/TC427/TC428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560, and similar switch-mode power supply integrated circuits.

3.4 Power Dissipation

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations.

The TC426/TC427/TC428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA compared to the DS0026 40 mA specification. For a 15V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:

- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$$Po = P_{DC} + PAC$$
$$= Vo\,(I_{DC}) + f\,C_L\,V_S^2$$

Where:

Vo = DC output voltage
I_{DC} = DC output load current
f = Switching frequency
Vs = Supply voltage

In power MOSFET drive applications the P_{DC} term is negligible. MOSFET power transistors are high-impedance, capacitive input devices. In applications where resistive loads or relays are driven, the P_{DC} component will normally dominate.

The magnitude of P_{AC} is readily estimated for several cases:

A.	B.
1. f = 200 kHZ	1. f = 200 kHz
2. C_L =1000 pf	2. C_L =1000 pf
3. Vs = 18V	3. Vs = 15V
4. P_{AC} = 65 mW	4. P_{AC} = 45 mW

During output level state changes, a current surge will flow through the series connected N and P channel output MOSFETS as one device is turning “ON” while the other is turning “OFF”. The current spike flows only during output transitions. The input levels should not be maintained between the logic ‘0’ and logic ‘1’ levels. **Unused driver inputs must be tied to ground and not be allowed to float.** Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

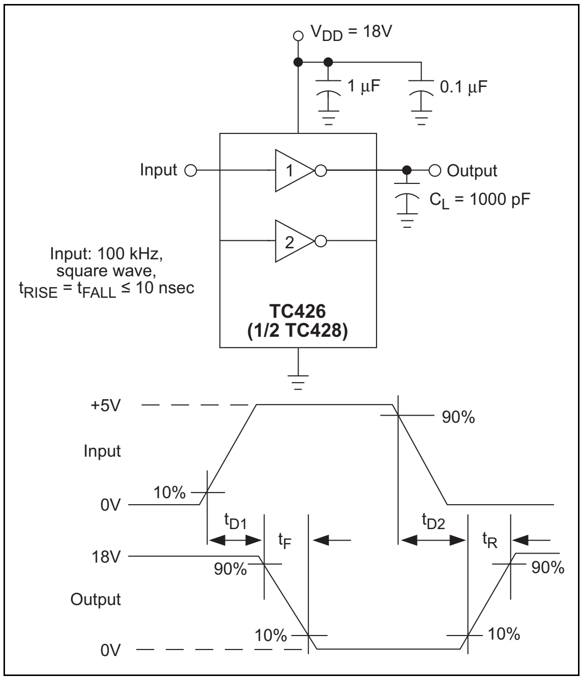


FIGURE 3-1: *Inverting Driver Switching Time Test Circuit*

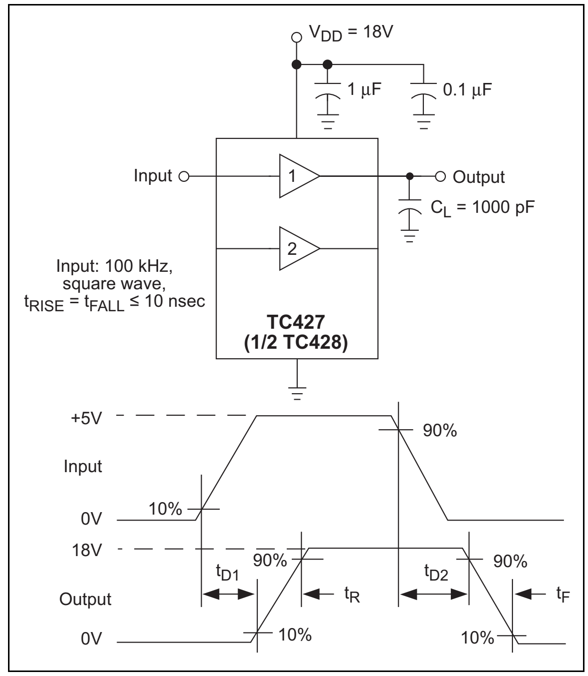


FIGURE 3-2: *Noninverting Driver Switching Time Test Circuit*

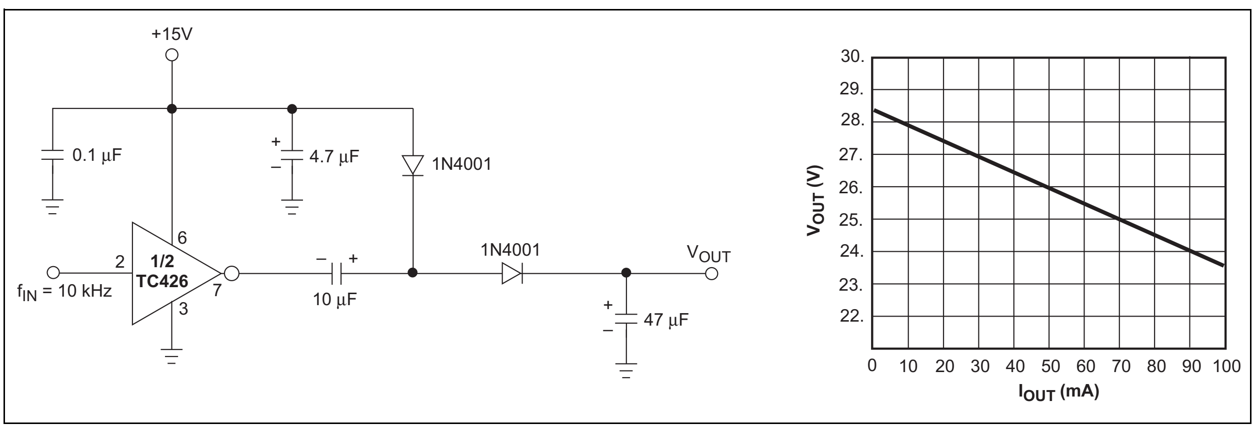


FIGURE 3-3: *Voltage Doubler*

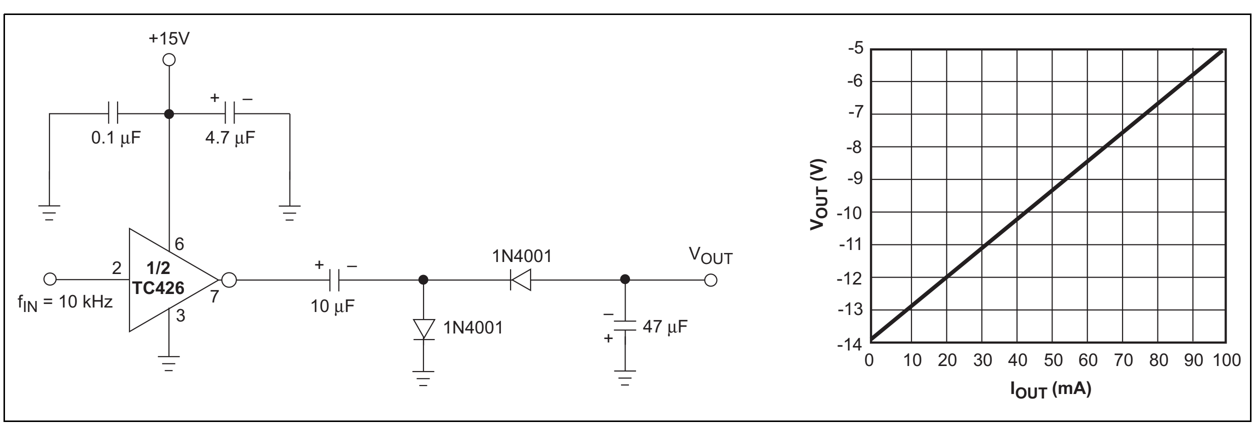
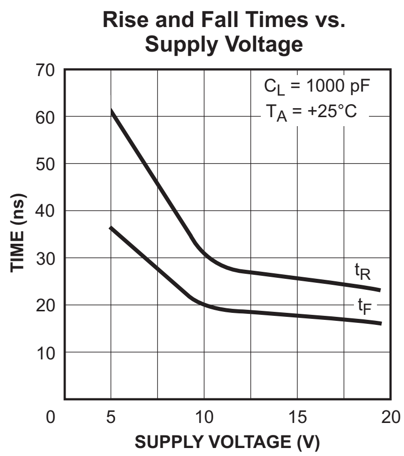
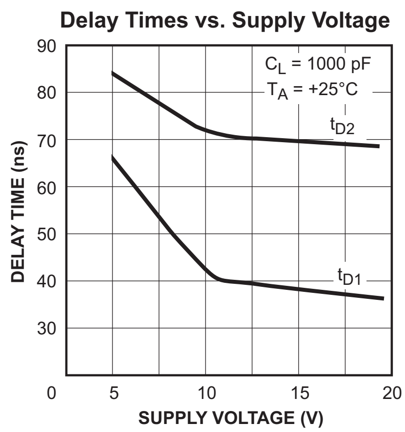


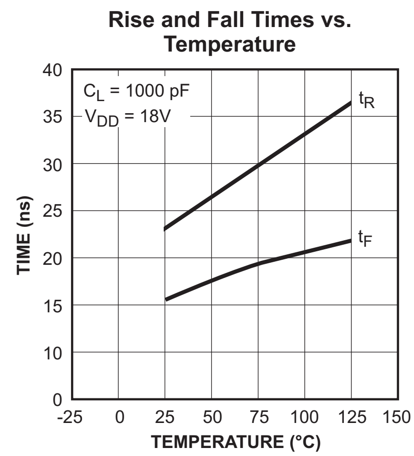
FIGURE 3-4: *Voltage Inverter*

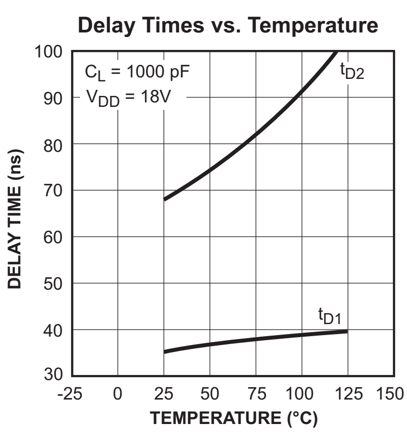
4.0 TYPICAL CHARACTERISTICS

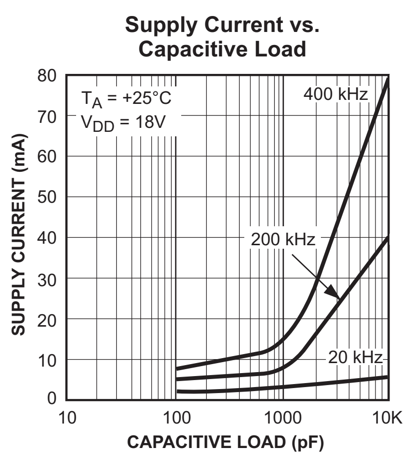
Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

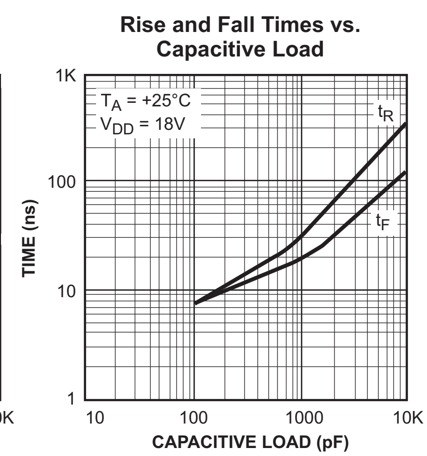


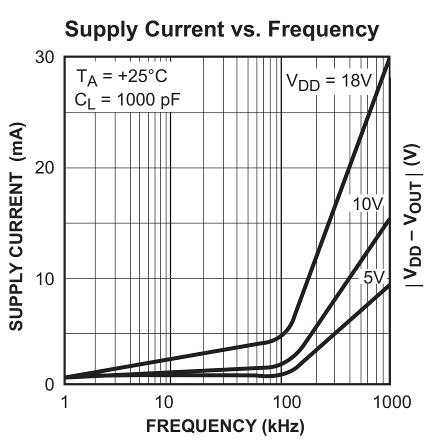


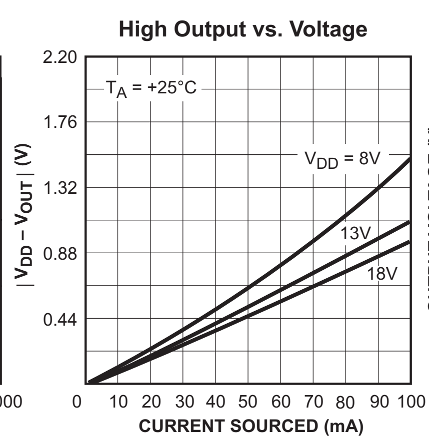


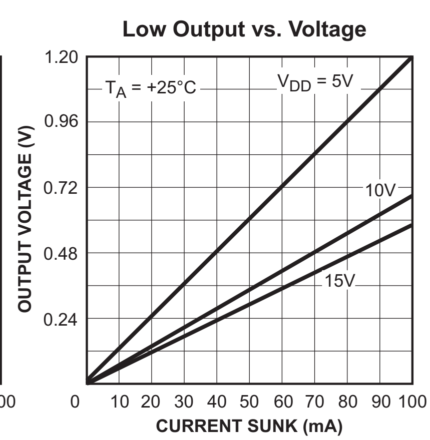




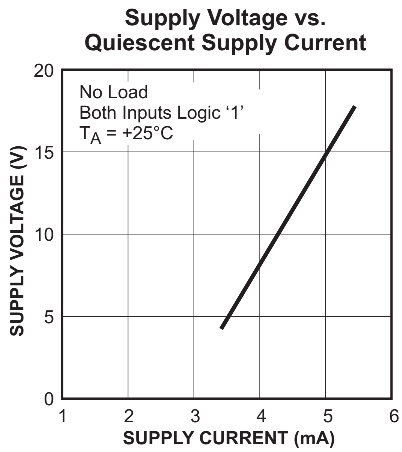


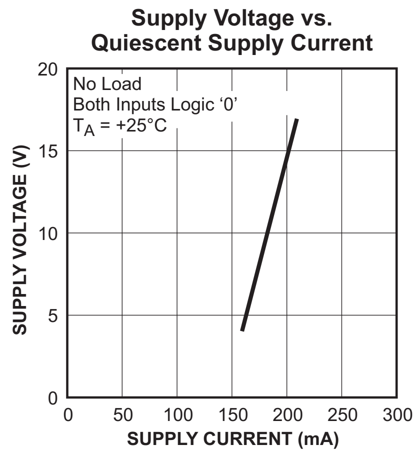


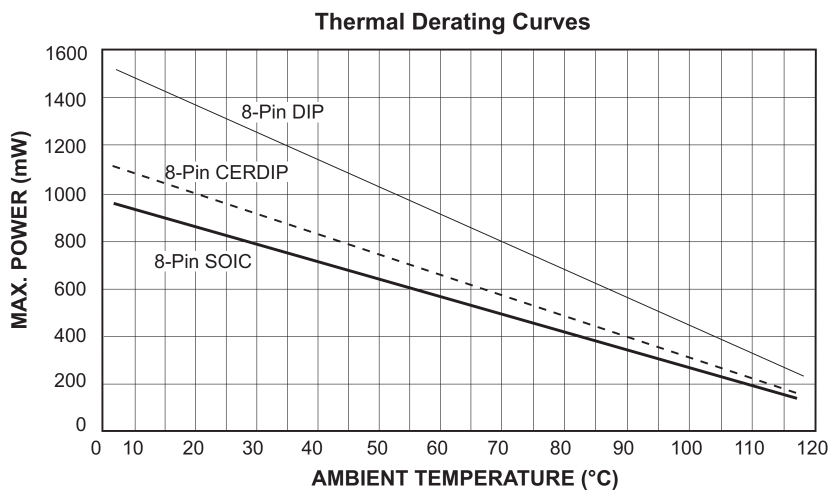




TYPICAL CHARACTERISTICS (CONTINUED)







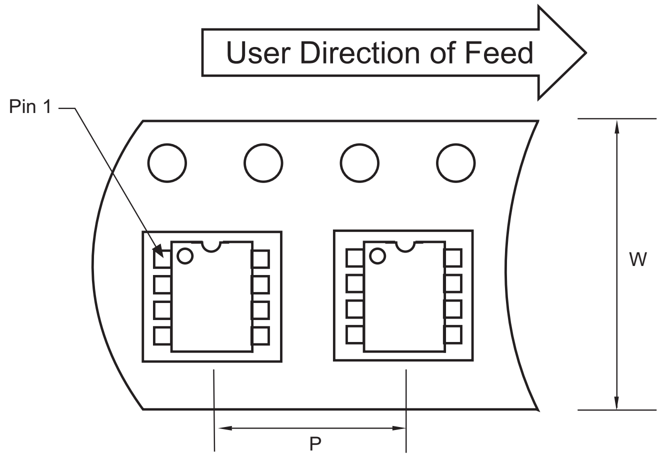
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

5.2 Taping Form

Component Taping Orientation for 8-Pin MSOP Devices

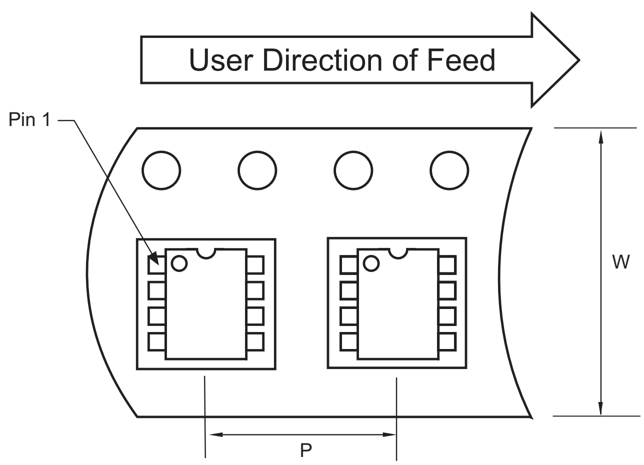


Standard Reel Component Orientation
for 713 Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



Standard Reel Component Orientation
for 713 Suffix Device

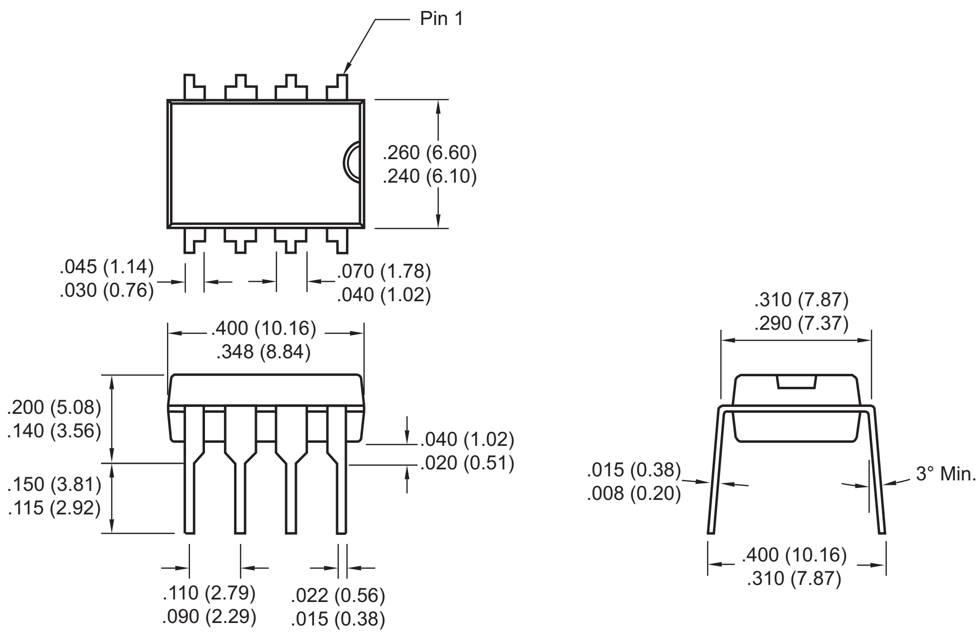
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

5.3 Package Dimensions

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

8-Pin Plastic DIP



Dimensions: inches (mm)

Package Dimensions (Continued)

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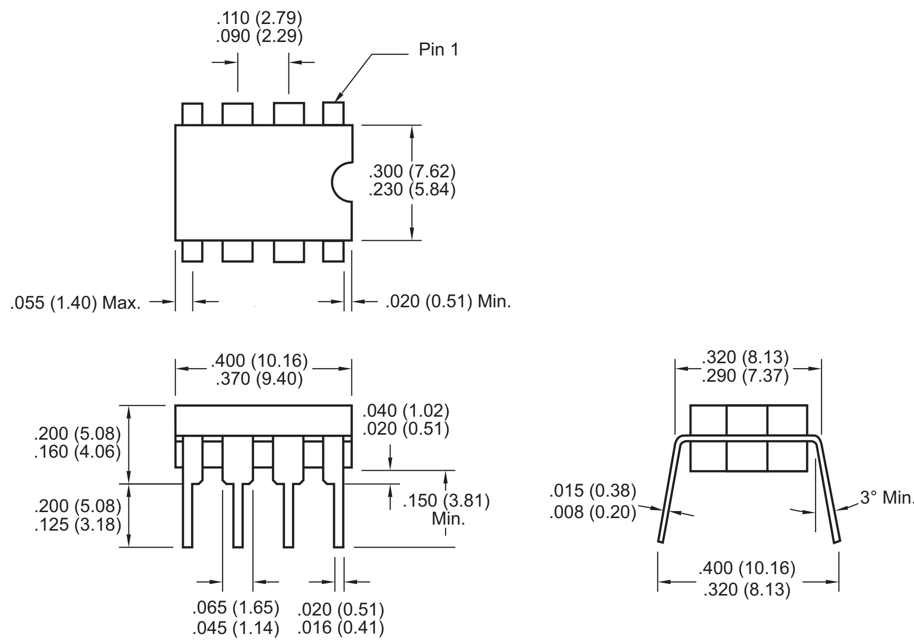
8-Pin CERDIP (Narrow)



Dimensions: inches (mm)

Package Dimensions (Continued)

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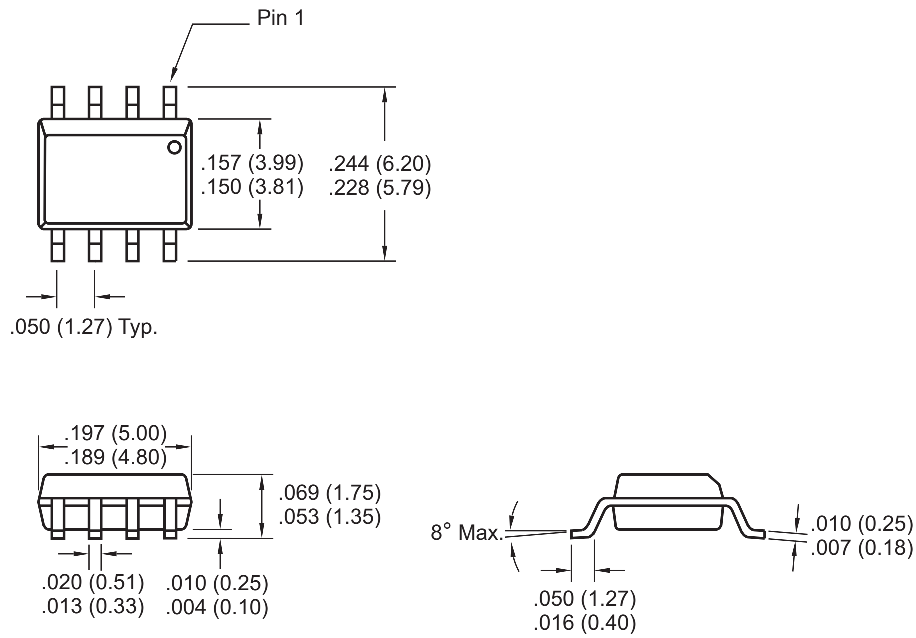
8-Pin SOIC



Dimensions: inches (mm)

6.0 REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

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ISBN: 9781620767900

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