WIN SOURCE ELECTRONICS

THE DATASHEET OF

NTS0101GW,125

NTS0101

Dual supply translating transceiver; open drain; auto direction sensing

Rev. 5 — 11 August 2014 Product data sheet

1. General description

The NTS0101 is a 1-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 1-bit input-output ports (A and B), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.65 V and 3.6 V. $V_{CC(B)}$ can be supplied at any voltage between 2.3 V and 5.5 V. This flexibility makes the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins A and OE are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.65 V to 3.6 V and $V_{CC(B)}$: 2.3 V to 5.5 V
- Maximum data rates:
  - Push-pull: 50 Mbps
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM JESD22-A114E Class 2 exceeds 2500 V for A port
  - HBM JESD22-A114E Class 3B exceeds 8000 V for B port
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1500 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Applications

- I^2C/SMBus
- UART
- GPIO

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NTS0101GW	–40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
NTS0101GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
NTS0101GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891
NTS0101GS	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202

5. Marking

Table 2. Marking

Type number	Marking code[1]
NTS0101GW	s1
NTS0101GM	s1
NTS0101GF	s1
NTS0101GS	s1

[1] The pin 1 indicator is on the lower left corner of the device, below the marking code.

6. Functional diagram

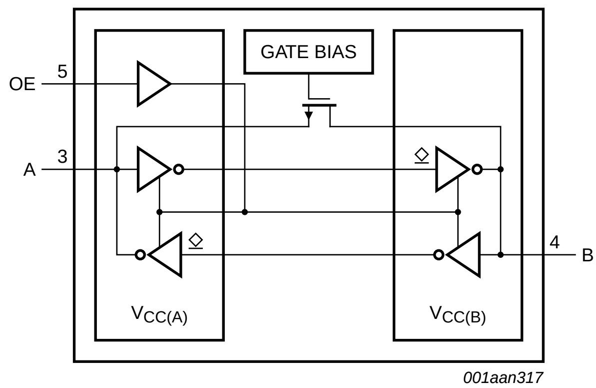


Fig 1. Logic symbol

7. Pinning information

7.1 Pinning

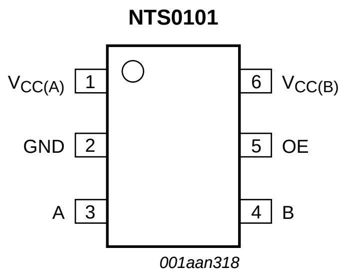


Fig 2. Pin configuration SOT363

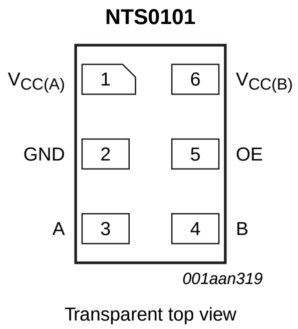


Fig 3. Pin configuration SOT886

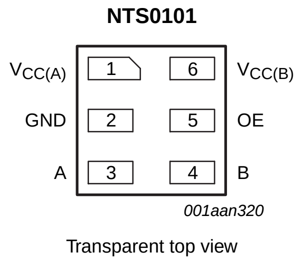


Fig 4. Pin configuration SOT891 and SOT1202

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A
GND	2	ground (0 V)
A	3	data input or output (referenced to $V_{CC(A)}$)
B	4	data input or output (referenced to $V_{CC(B)}$)
OE	5	output enable input (active HIGH; referenced to $V_{CC(A)}$)
$V_{CC(B)}$	6	supply voltage B

8. Functional description

Table 4. Function table[1]

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	A	B
1.65 V to $V_{CC(B)}$	2.3 V to 5.5 V	L	Z	Z
1.65 V to $V_{CC(B)}$	2.3 V to 5.5 V	H	input or output	output or input
GND[2]	GND[2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			–0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			–0.5	+6.5	V
V_I	input voltage	A port and OE input	[1][2]	–0.5	+6.5	V
		B port	[1][2]	–0.5	+6.5	V
V_O	output voltage	Active mode	[1][2]			
		A or B port		–0.5	V_{CCO} + 0.5	V
		Power-down or 3-state mode	[1]			
		A port		–0.5	+4.6	V
		B port		–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		–50	-	mA
I_O	output current	V_O = 0 V to V_{CCO}	[2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output.

[3] For SC-88 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For XSON6 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions[1][2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.65	3.6	V
$V_{CC(B)}$	supply voltage B		2.3	5.5	V
T_{amb}	ambient temperature		–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	10	ns/V
		OE input			
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

11. Static characteristics

Table 7. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	-	±1	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V [1]	-	-	±1	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V	-	-	±1	μA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V	-	-	±1	μA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V	-	1	-	pF
$C_{I/O}$	input/output capacitance	A port	-	4	-	pF
		B port	-	7.5	-	pF
		A or B port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V	-	11	-	pF

[1] V_{CCO} is the supply voltage associated with the output.

Table 8. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

$V_{CC(A)}$	$V_{CC(B)}$						Unit
	2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.8 V	0.1	0.5	0.1	1.5	0.1	4.6	μA
2.5 V	0.1	0.1	0.1	0.8	0.1	3.8	μA
3.3 V	-	-	0.1	0.1	0.1	2.8	μA

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port					
		$V_{CC(A)}$ = 1.65 V to 1.95 V; $V_{CC(B)}$ = 2.3 V to 5.5 V [1]	$V_{CCI} - 0.2$	-	$V_{CCI} - 0.2$	-	V
		$V_{CC(A)}$ = 2.3 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V [1]	$V_{CCI} - 0.4$	-	$V_{CCI} - 0.4$	-	V
		B port					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V [1]	$V_{CCI} - 0.4$	-	$V_{CCI} - 0.4$	-	V
		OE input					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V

Table 9. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IL}	LOW-level input voltage	A or B port						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		-	0.15	-	0.15	V
		OE input						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	I_O = –20 μA						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	[2]	$0.67V_{CCO}$	-	$0.67V_{CCO}$	-	V
V_{OL}	LOW-level output voltage	A or B port; I_O = 1 mA	[2]					
		$V_I \leq 0.15$ V; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		-	0.4	-	0.4	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		-	±2	-	±12	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	[2]	-	±2	-	±12	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V		-	±2	-	±12	μA
		B port; V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V		-	±2	-	±12	μA
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A	[1]					
		$I_{CC(A)}$						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		-	2.4	-	15	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V		-	2.2	-	15	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V		-	–1	-	–8	μA
		$I_{CC(B)}$						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		-	12	-	30	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V		-	–1	-	–5	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V		-	1	-	6	μA
		$I_{CC(A)} + I_{CC(B)}$						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		-	14.4	-	30	μA

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.

12. Dynamic characteristics

Table 10. Dynamic characteristics for temperature range –40 °C to +85 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 7; for wave forms, see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		$V_{CC(B)}$					Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	4.6	-	4.7	-	5.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	6.8	-	6.8	-	7.0	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	4.4	-	4.5	-	4.7	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	5.3	-	4.5	-	0.5	ns
t_{en}	enable time	OE to A; B	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [2]	-	25	-	25	-	25	ns
		OE to B; no external load [2]	-	25	-	25	-	25	ns
		OE to A	-	230	-	230	-	230	ns
		OE to B	-	200	-	200	-	200	ns
t_{TLH}	LOW to HIGH output transition time	A port	3.2	9.5	2.3	9.3	1.8	7.6	ns
		B port	3.3	10.8	2.7	9.1	2.7	7.6	ns
t_{THL}	HIGH to LOW output transition time	A port	2.0	5.9	1.9	6.0	1.7	13.3	ns
		B port	2.9	7.6	2.8	7.5	2.8	10.0	ns
t_W	pulse width	data inputs	20	-	20	-	20	-	ns
f_{data}	data rate		-	50	-	50	-	50	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	3.2	-	3.3	-	3.4	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	3.5	-	4.1	-	4.4	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	3.0	-	3.6	-	4.3	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	2.5	-	1.6	-	0.7	ns
t_{en}	enable time	OE to A; B	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [2]	-	20	-	20	-	20	ns
		OE to B; no external load [2]	-	20	-	20	-	20	ns
		OE to A	-	200	-	200	-	200	ns
		OE to B	-	200	-	200	-	200	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.8	7.4	2.6	6.6	1.8	6.2	ns
		B port	3.2	8.3	2.9	7.9	2.4	6.8	ns

Table 10. Dynamic characteristics for temperature range –40 °C to +85 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 7; for wave forms, see Figure 5 and Figure 6.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t_{THL}	HIGH to LOW output transition time	A port	1.9	5.7	1.9	5.5	1.8	5.3	ns
		B port	2.2	7.8	2.4	6.7	2.6	6.6	ns
t_W	pulse width	data inputs	20	-	20	-	20	-	ns
f_{data}	data rate		-	50	-	50	-	50	Mbps
$V_{CC(A)}$ = 3.3 V ± 0.3 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	-	-	2.4	-	3.1	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	-	-	4.2	-	4.4	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	-	-	2.5	-	3.3	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	-	-	2.5	-	2.6	ns
t_{en}	enable time	OE to A; B	-	-	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [2]	-	-	-	15	-	15	ns
		OE to B; no external load [2]	-	-	-	15	-	15	ns
		OE to A	-	-	-	260	-	260	ns
		OE to B	-	-	-	200	-	200	ns
t_{TLH}	LOW to HIGH output transition time	A port	-	-	2.3	5.6	1.9	5.9	ns
		B port	-	-	2.5	6.4	2.1	7.4	ns
t_{THL}	HIGH to LOW output transition time	A port	-	-	2.0	5.4	1.9	5.0	ns
		B port	-	-	2.3	7.4	2.4	7.6	ns
t_W	pulse width	data inputs	-	-	20	-	20	-	ns
f_{data}	data rate		-	-	-	50	-	50	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Delay between OE going LOW and when the outputs are disabled.

Table 11. Dynamic characteristics for temperature range –40 °C to +125 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 7; for wave forms, see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		$V_{CC(B)}$					Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	5.8	-	5.9	-	7.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	8.5	-	8.5	-	8.8	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	5.5	-	5.7	-	5.9	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	6.7	-	5.7	-	0.7	ns
t_{en}	enable time	OE to A; B	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [2]	-	30	-	30	-	30	ns
		OE to B; no external load [2]	-	30	-	30	-	30	ns
		OE to A	-	250	-	250	-	250	ns
		OE to B	-	220	-	220	-	220	ns
t_{TLH}	LOW to HIGH output transition time	A port	3.2	11.9	2.3	11.7	1.8	9.5	ns
		B port	3.3	13.5	2.7	11.4	2.7	9.5	ns
t_{THL}	HIGH to LOW output transition time	A port	2.0	7.4	1.9	7.5	1.7	16.7	ns
		B port	2.9	9.5	2.8	9.4	2.8	12.5	ns
t_W	pulse width	data inputs	20	-	20	-	20	-	ns
f_{data}	data rate		-	50	-	50	-	50	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	4.0	-	4.2	-	4.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	4.4	-	5.2	-	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	3.8	-	4.5	-	5.4	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	3.2	-	2.0	-	0.9	ns
t_{en}	enable time	OE to A; B	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [2]	-	25	-	25	-	25	ns
		OE to B; no external load [2]	-	25	-	25	-	25	ns
		OE to A	-	220	-	220	-	220	ns
		OE to B	-	220	-	220	-	220	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.8	9.3	2.6	8.3	1.8	7.8	ns
		B port	3.2	10.4	2.9	9.7	2.4	8.3	ns
t_{THL}	HIGH to LOW output transition time	A port	1.9	7.2	1.9	6.9	1.8	6.7	ns
		B port	2.2	9.8	2.4	8.4	2.6	8.3	ns

Table 11. Dynamic characteristics for temperature range –40 °C to +125 °C[1] *…continued*

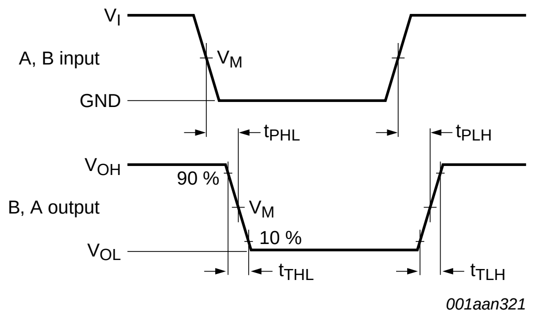
Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 7; for wave forms, see Figure 5 and Figure 6.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t_W	pulse width	data inputs	20	-	20	-	20	-	ns
f_{data}	data rate		-	50	-	50	-	50	Mbps
$V_{CC(A)}$ = 3.3 V ± 0.3 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	-	-	3.0	-	3.9	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	-	-	5.3	-	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	-	-	3.2	-	4.2	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	-	-	3.2	-	3.3	ns
t_{en}	enable time	OE to A; B	-	-	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [2]	-	-	-	20	-	20	ns
		OE to B; no external load [2]	-	-	-	20	-	20	ns
		OE to A	-	-	-	280	-	280	ns
		OE to B	-	-	-	220	-	220	ns
t_{TLH}	LOW to HIGH output transition time	A port	-	-	2.3	7.0	1.9	7.4	ns
		B port	-	-	2.5	8.0	2.1	9.3	ns
t_{THL}	HIGH to LOW output transition time	A port	-	-	2.0	6.8	1.9	6.3	ns
		B port	-	-	2.3	9.3	2.4	9.5	ns
t_W	pulse width	data inputs	-	-	20	-	20	-	ns
f_{data}	data rate		-	-	-	50	-	50	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Delay between OE going LOW and when the outputs are disabled.

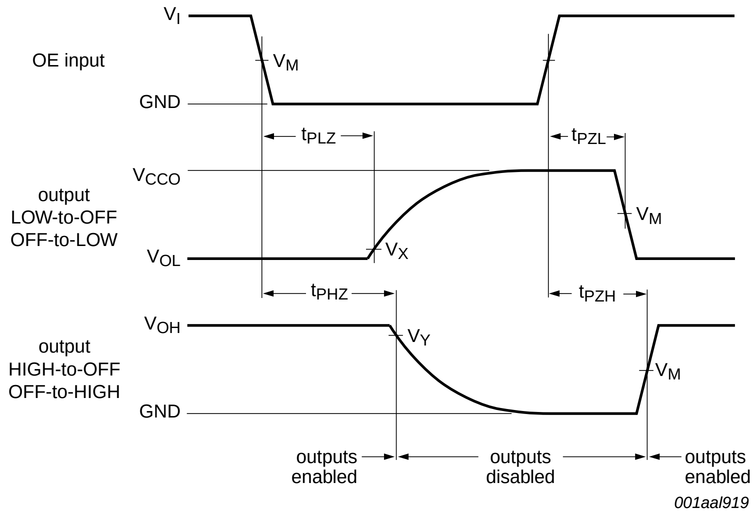
13. Waveforms



Measurement points are given in Table 12.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. The data input (A, B) to data output (B, A) propagation delay times



Measurement points are given in Table 12.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

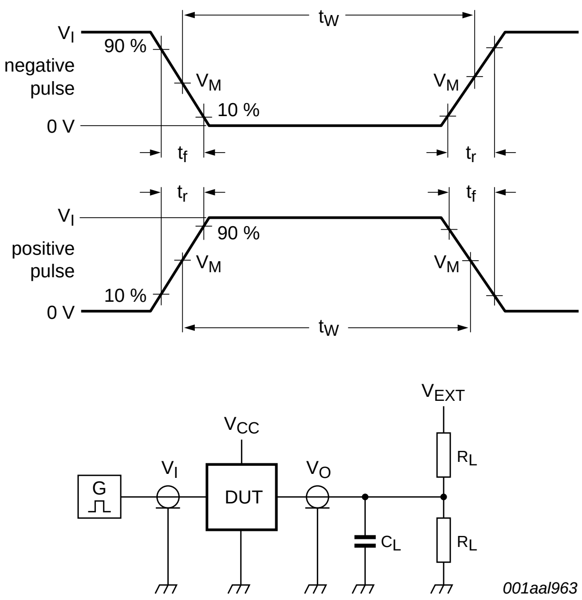
Fig 6. Enable and disable times

Table 12. Measurement points[1][2]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 13.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 13. Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	Δt/ΔV	C_L	R_L [2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
1.65 V to 3.6 V	2.3 V to 5.5 V	V_{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V_{CCO}

[1] V_{CCI} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ. For measuring enable and disable times, R_L = 50 KΩ.

[3] V_{CCO} is the supply voltage associated with the output.

14. Application information

14.1 Applications

Voltage level-translation applications. The NTS0101 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I²C or 1-wire which use open-drain drivers. It may also be used in applications where push-pull drivers are connected to the ports, however the NTB0101 may be more suitable.

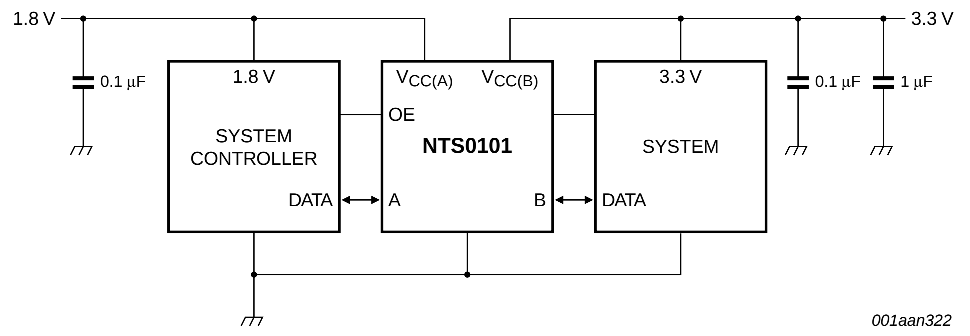


Fig 8. Typical operating circuit

14.2 Architecture

The architecture of the NTS0101 is shown in Figure 9. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

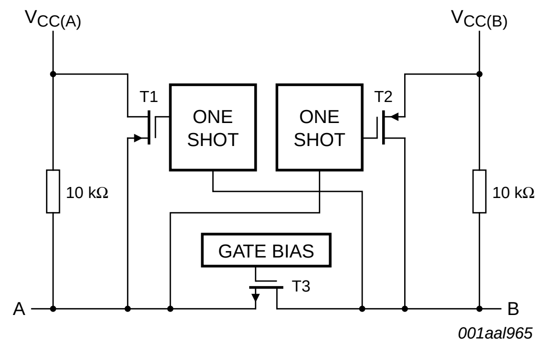


Fig 9. Architecture of NTS0101 I/O cel

The NTS0101 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2). It bypasses the 10 kΩ pull-up resistors and increases the current drive capability. The one-shot is activated once the input transition reaches approximately $V_{CCI}/2$; it is de-activated approximately 50 ns after the output reaches $V_{CCO}/2$. During the acceleration time, the driver output resistance is between approximately 50 Ω and 70 Ω. To avoid signal contention and minimize dynamic I_{CC}, the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

14.3 Input driver requirements

As the NTS0101 is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time (t_{THL}), and propagation delay (t_{PHL}), are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume a driver with output impedance below 50 Ω is used.

14.4 Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration.

To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on NTS0101 PCB layouts. The length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration (approximately 50 ns). It ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

14.5 Power-up

During operation, $V_{CC(A)}$ must never be higher than $V_{CC(B)}$. However, during power-up, $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTS0101 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

14.6 Enable and disable

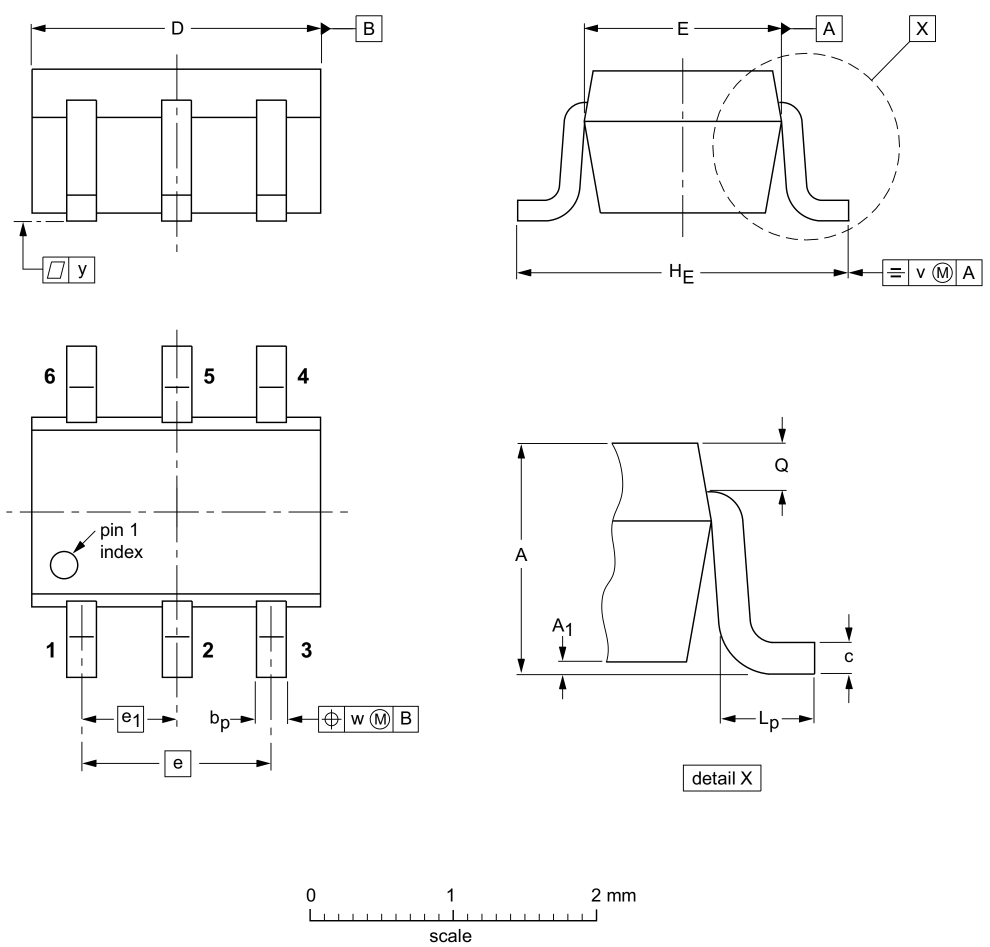
An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

14.7 Pull-up or pull-down resistors on I/Os lines

The A port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(A)}$. The B port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(B)}$. If a smaller value of pull-up resistor is required, add an external resistor in parallel to the internal 10 kΩ. This pull-up resistor effects the V_{OL} level. When OE goes LOW, the internal pull-ups of the NTS0101 are disabled.

15. Package outline

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

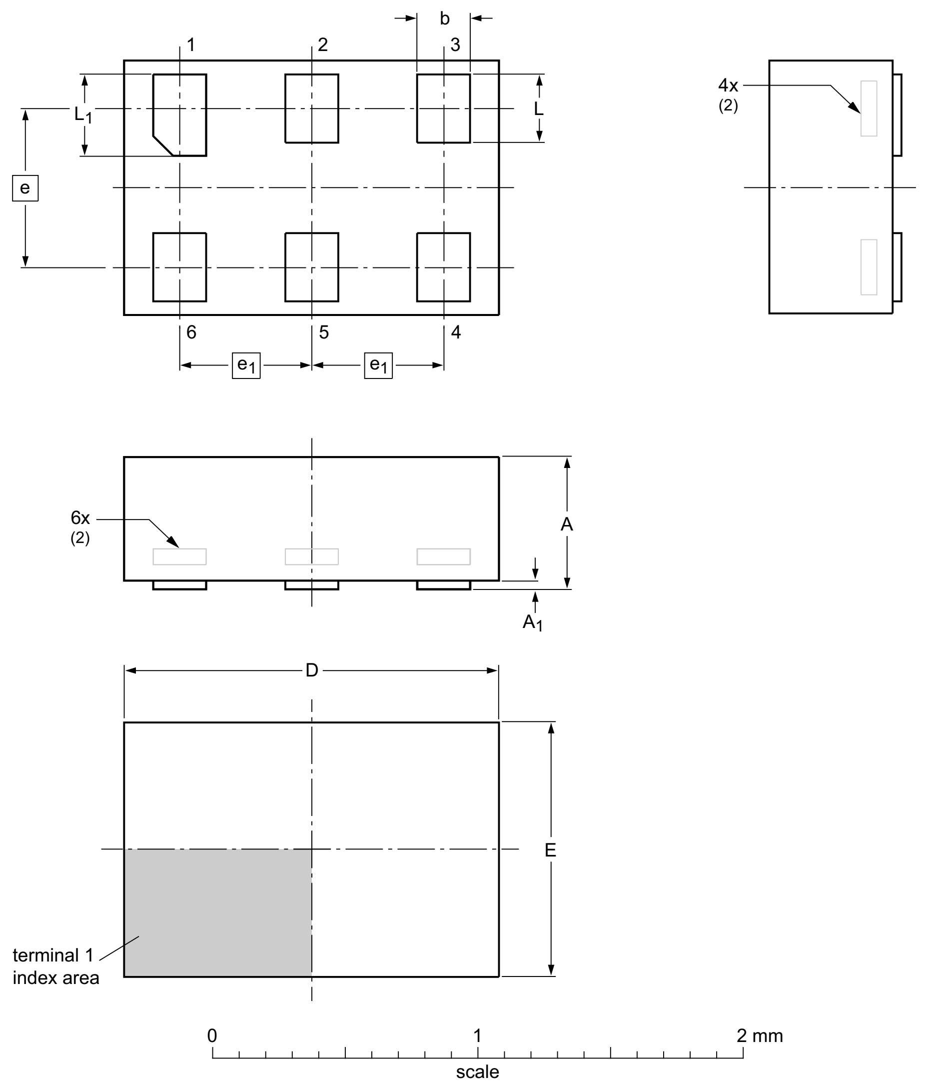
UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

Fig 10. Package outline SOT363 (SC-88)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

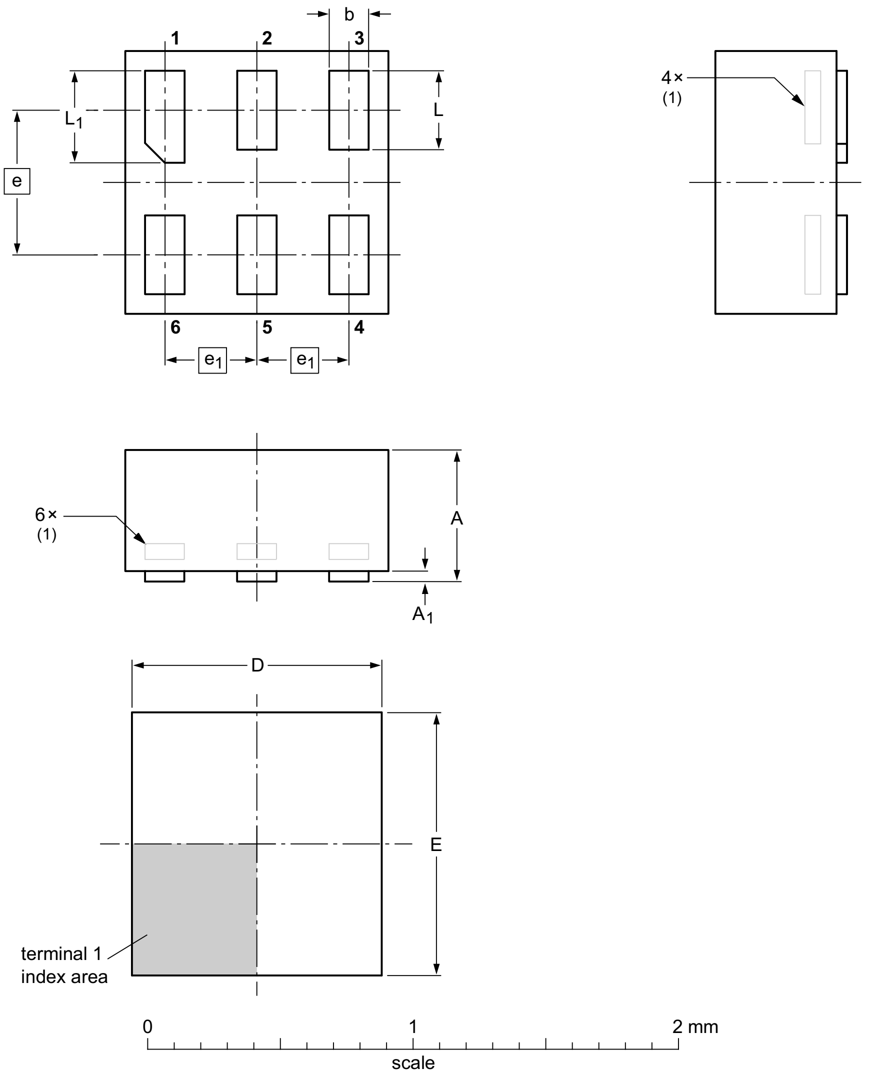
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig 11. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm **SOT891**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.20 0.12	1.05 0.95	1.05 0.95	0.55	0.35	0.35 0.27	0.40 0.32

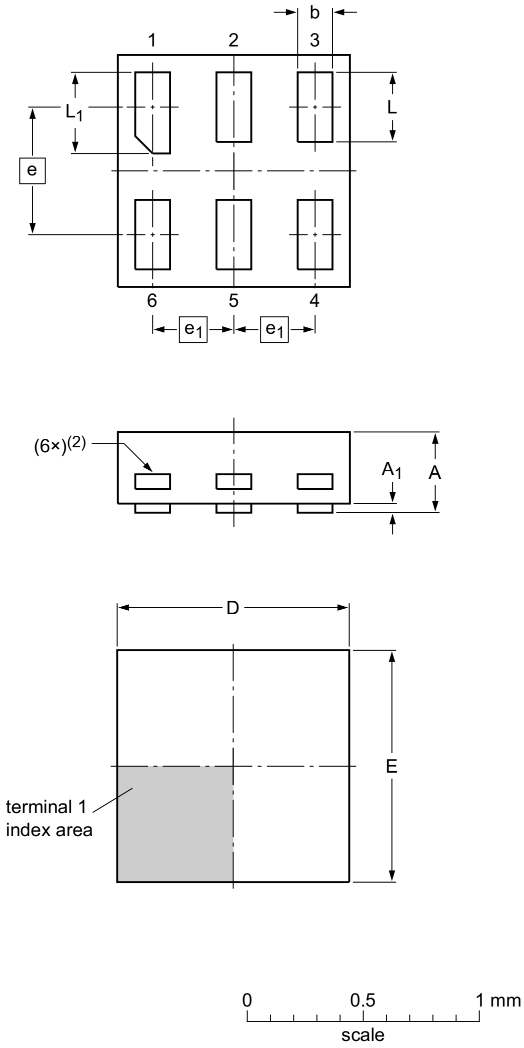
Note

1. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT891						~~05-04-06~~ 07-05-15

Fig 12. Package outline SOT891 (XSON6)

XSON6: extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		A(1)	A1	b	D	E	e	e1	L	L1
	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
mm	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

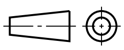
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						~~10-04-02~~ 10-04-06

Fig 13. Package outline SOT1202 (XSON6)

16. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
MM	Machine Model
PCB	Printed-Circuit Board
PMOS	Positive Metal Oxide Semiconductor
SMBus	System Management Bus
UART	Universal Asynchronous Receiver Transmitter

17. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTS0101 v.5	20140811	Product data sheet	-	NTS0101 v.4
Modifications:	• Type number NTS0101GV has been removed			
NTS0101 v.4	20120514	Product data sheet	-	NTS0101 v.3
Modifications:	• Package outline drawing of SOT886 (Figure 11) modified.			
NTS0101 v.3	20111110	Product data sheet	-	NTS0101 v.2
Modifications:	• Legal pages updated.			
NTS0101 v.2	20110427	Product data sheet	-	NTS0101 v.1
NTS0101 v.1	20101230	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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Date of release: 11 August 2014
Document identifier: NTS0101