



**THE DATASHEET OF  
SN74ALS533ANSR**

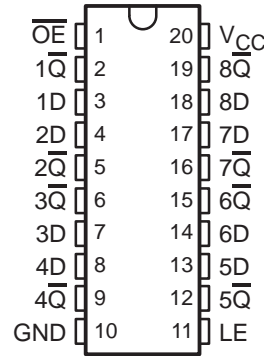


# SN74ALS533A, SN74AS533A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS270 – DECEMBER 1994

- Eight Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- pnp Inputs Reduce dc Loading on Data Lines
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

DW OR N PACKAGE  
(TOP VIEW)



## description

These 8-bit D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While latch-enable (LE) input is high, the  $\bar{Q}$  outputs follow the complements of the data (D) inputs. When LE is taken low, the  $\bar{Q}$  outputs are latched at the inverses of the levels set up at the D inputs. The SN74ALS533A and SN74AS533A are functionally equivalent to the SN74ALS373A and SN74AS373, except for having inverted outputs.

A buffered output-enable ( $\bar{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\bar{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN74ALS533A and SN74AS533A are characterized for operation from 0°C to 70°C.

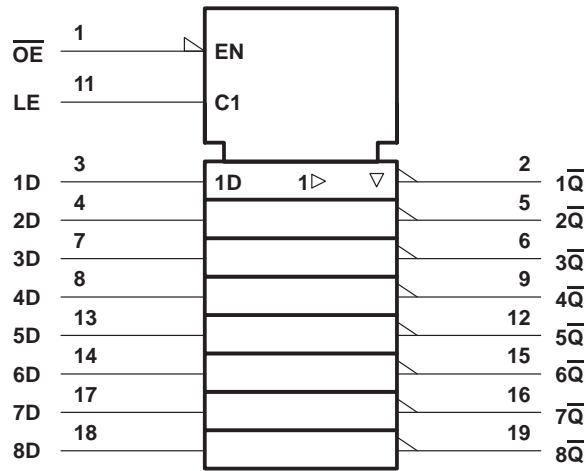
FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\bar{OE}$	LE	D	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

# SN74ALS533A, SN74AS533A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

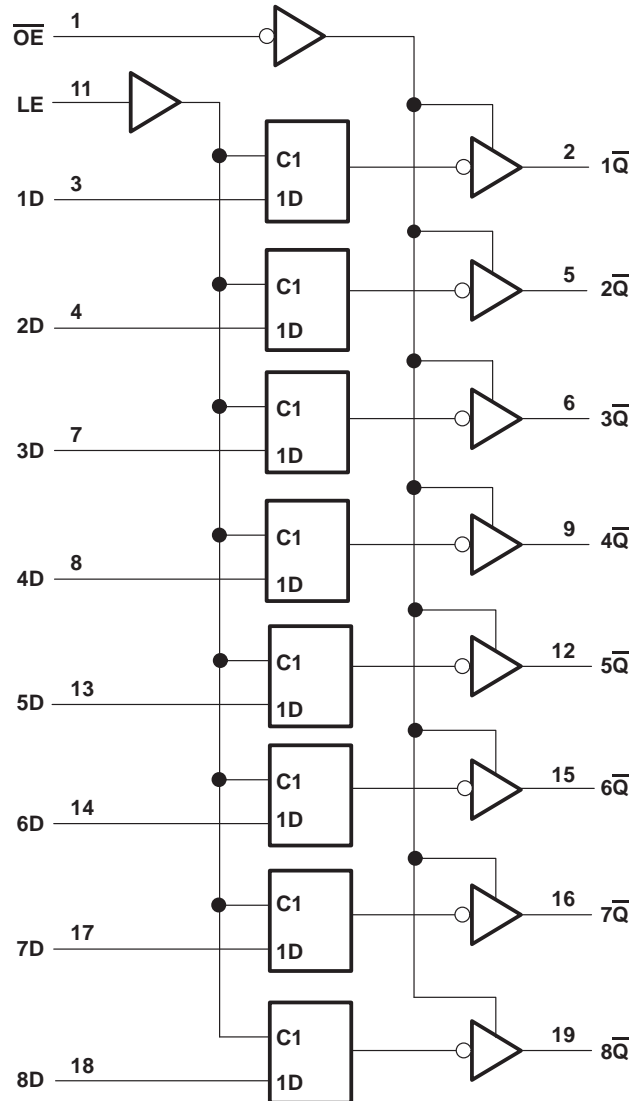
SDAS270 – DECEMBER 1994

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN74ALS533A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**SN74ALS533A, SN74AS533A**  
**OCTAL D-TYPE TRANSPARENT LATCHES**  
**WITH 3-STATE OUTPUTS**  
SDAS270 – DECEMBER 1994

**recommended operating conditions**

		SN74ALS533A			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			-2.6	mA
$I_{OL}$	Low-level output current			24	mA
$t_w$	Pulse duration, LE high	15			ns
$t_{su}$	Setup time, data before LE↓	15			ns
$t_h$	Hold time, data after LE↓	7			ns
$T_A$	Operating free-air temperature	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN74ALS533A			UNIT	
		MIN	TYP†	MAX		
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.5	V	
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			V	
	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -2.6\text{ mA}$	2.4	3.2			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	V	
		$I_{OL} = 24\text{ mA}$	0.35	0.5		
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			20	μA	
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.4\text{ V}$			-20	μA	
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1	mA	
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20	μA	
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			-0.1	mA	
$I_{O‡}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-30		-112	mA	
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high	10	17	mA	
		Outputs low		17		26
		Outputs disabled	18.5			28

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

# SN74ALS533A, SN74AS533A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS270 – DECEMBER 1994

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74ALS533A		
			MIN	MAX	
t <sub>PLH</sub>	D	$\bar{Q}$	4	19	ns
t <sub>PHL</sub>			4	13	
t <sub>PLH</sub>	LE	Any $\bar{Q}$	5	23	ns
t <sub>PHL</sub>			4	18	
t <sub>PZH</sub>	$\overline{OE}$	Any $\bar{Q}$	1	17	ns
t <sub>PZL</sub>			4	18	
t <sub>PHZ</sub>	$\overline{OE}$	Any $\bar{Q}$	2	10	ns
t <sub>PLZ</sub>			2	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T <sub>A</sub> : SN74AS533A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN74AS533A			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current			-15	mA
I <sub>OL</sub>	Low-level output current			48	mA
t <sub>w</sub>	Pulse duration, LE high	2			ns
t <sub>su</sub>	Setup time, data before LE↓	2			ns
t <sub>h</sub>	Hold time, data after LE↓	3			ns
T <sub>A</sub>	Operating free-air temperature	0		70	°C



**SN74ALS533A, SN74AS533A**  
**OCTAL D-TYPE TRANSPARENT LATCHES**  
**WITH 3-STATE OUTPUTS**

SDAS270 – DECEMBER 1994

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN74AS533A		UNIT		
		MIN	TYP†		MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.5	V	
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			V	
	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -15\text{ mA}$	2.4	3.3			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 48\text{ mA}$		0.34	0.5	V	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			50	$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.4\text{ V}$			-50	$\mu\text{A}$	
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1	mA	
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20	$\mu\text{A}$	
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			-0.02	-0.5	mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$			-30	-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high		62	100	mA
		Outputs low		64	100	
		Outputs disabled		71	110	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 1)**

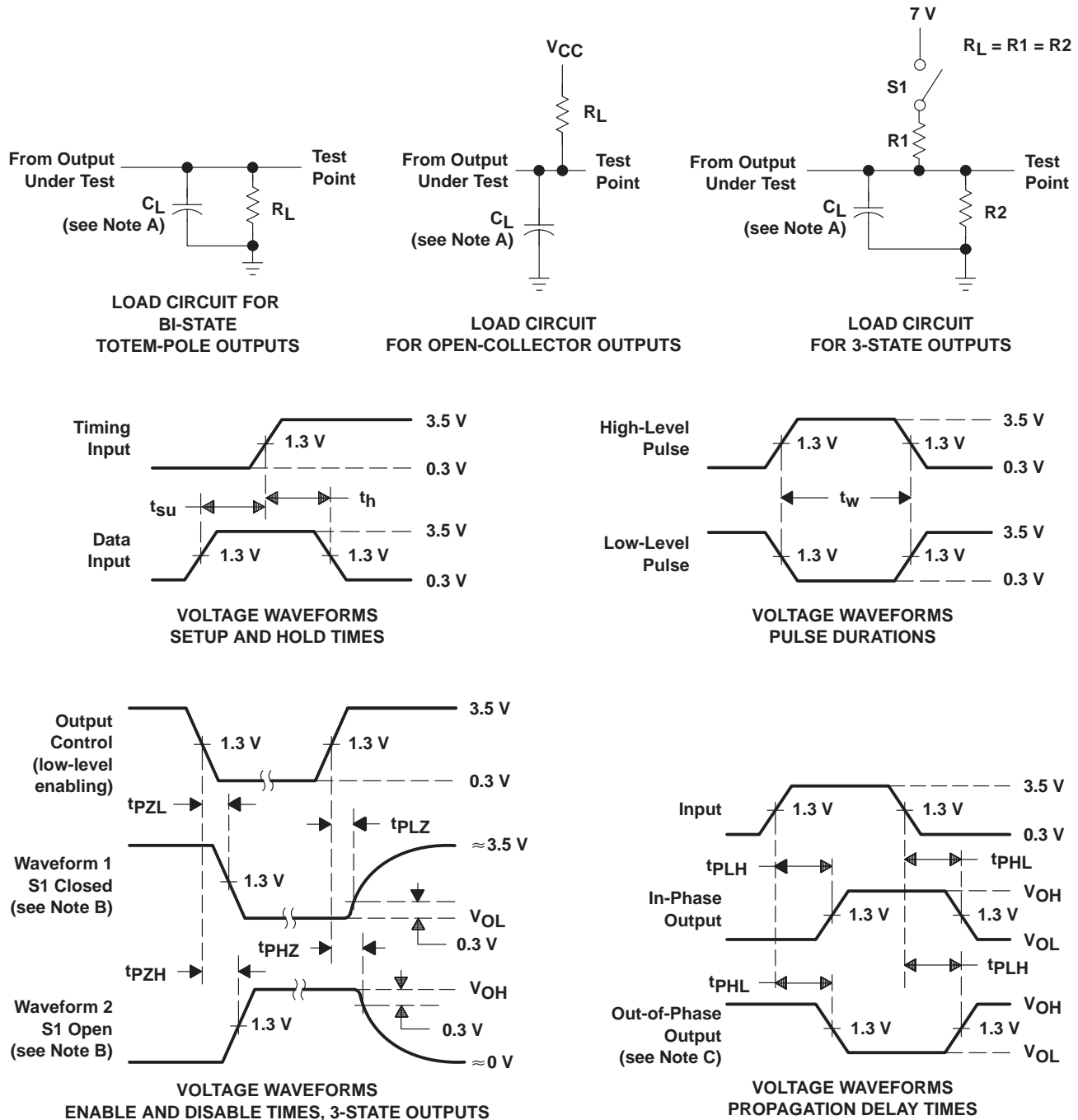
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$		UNIT
			SN74AS533A		
			MIN	MAX	
$t_{PLH}$	D	$\bar{Q}$	4	7.5	ns
$t_{PHL}$			4	7	
$t_{PLH}$	LE	Any $\bar{Q}$	5	9	ns
$t_{PHL}$			4	8	
$t_{PZH}$	$\overline{OE}$	Any $\bar{Q}$	2	6.5	ns
$t_{PZL}$			4	9.5	
$t_{PHZ}$	$\overline{OE}$	Any $\bar{Q}$	2	6.5	ns
$t_{PLZ}$			3	7	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN74ALS533A, SN74AS533A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS270 – DECEMBER 1994

## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS533ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS533A	<a href="#">Samples</a>
SN74ALS533AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS533AN	<a href="#">Samples</a>
SN74ALS533ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS533A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS533ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS533ANSR	SO	NS	20	2000	367.0	367.0	45.0

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

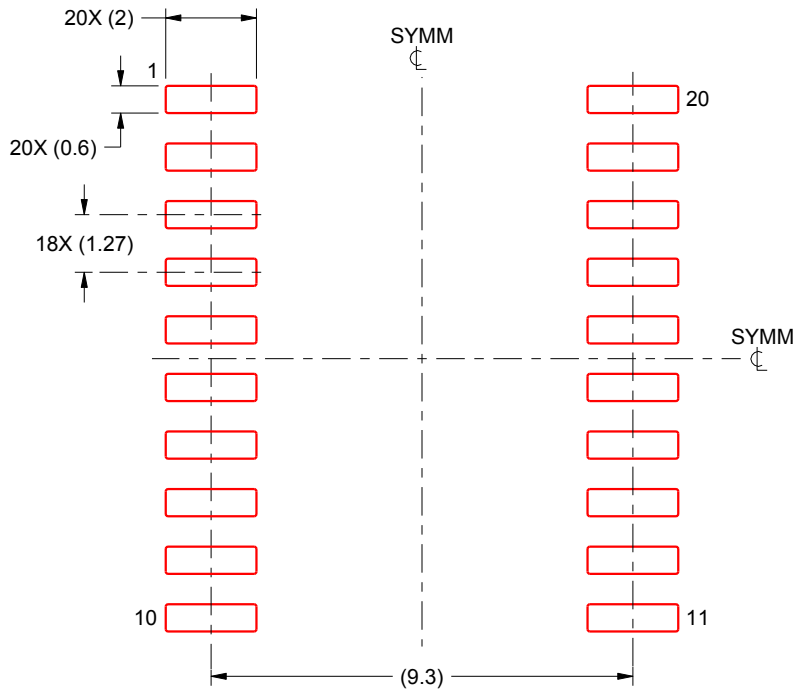
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View SN74ALS533ANSR on WIN SOURCE](#)
- ⊖ [Texas Instruments Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management