THE DATASHEET OF

TPS60255RTER

HIGH EFFICIENCY CHARGE PUMP FOR 7 WLEDs DRIVER WITH 1 WIRE INTERFACE

FEATURES

- **2.7 V to 6.0 V Input Voltage Range**
- **1× and 1.5× Charge Pump**
- **Auto Switching Between 1× and 1.5× Modes**
- **750 kHz Charge Pump Frequency**
- **Seven Individually-regulated WLED Current Sinks**
- **Single- Wire Interface for Dimming and ON/OFF Control**
- **25 mA max LED Current for Six Current Sinks**
- **One 80 mA Current Sink**
- **Open WLED Detection**
- **Built-in Soft Start and Current Limit**
- **16-pin, 3 mm × 3 mm QFN Package**

APPLICATIONS

- **Cellular Phones**
- **Portable Navigation Displays**
- **Multi-display Handheld Devices**

DESCRIPTION

The TPS60255 is a high-efficiency, constant frequency charge pump DC/DC converter that uses 1× and 1.5× conversion to maximize efficiency for the input voltage range. By using adaptive 1×/1.5× charge-pump modes and very low dropout current regulators, the TPS60255 achieves high efficiency for the entire one-cell lithium battery range. The protection features include soft start, over-current limit, thermal shut down, and over-voltage detection. The device automatically detects and removes unused current sinks from the control loop.

This device drives six 25 mA current sinks and one 80 mA current sink. These current regulators are programmed by three independent brightness registers and five ON/OFF bits using a single-wire interface (EasyScale™). This offers flexible applications for a variety of lighting control in portable devices.

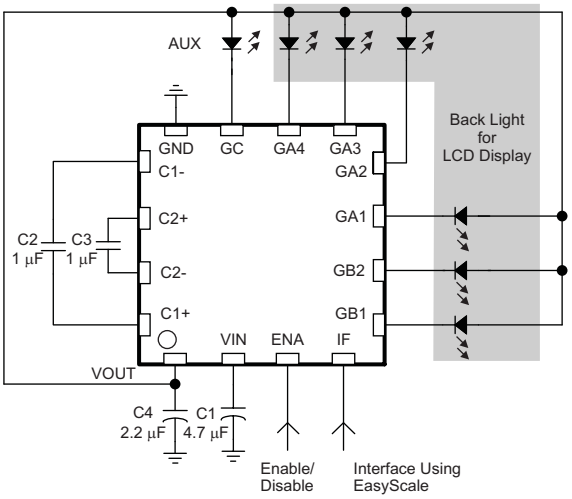

Figure 1. Typical Application

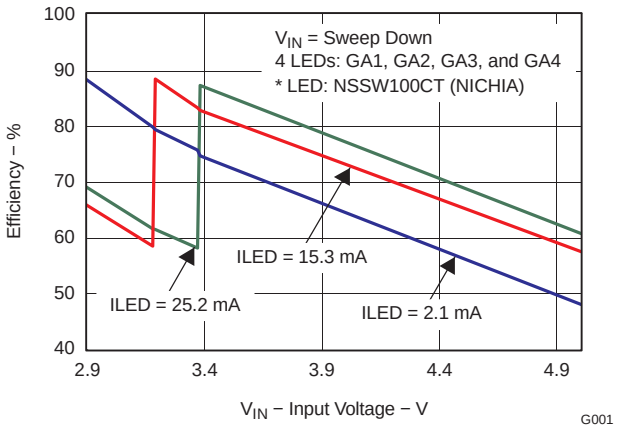

Figure 2. Characteristic Curve

ORDERING INFORMATION(1)

PART NUMBER	PACKAGE MARKING	PACKAGE	T_A
TPS60255RTE	BUP	16-Pin 3 mm × 3 mm QFN (RTE)	–40°C to +85°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

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EasyScale is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_I	Input voltage range (all pins)	–0.3 to 7	V
	HBM ESD Rating (2)	2	kV
	CDM ESD Rating(3)	500	V
	MM ESD Rating(4)	200	V
T_A	Operating temperature range	–40 to 85	°C
T_J	Maximum operating junction temperature	150	°C
T_{ST}	Storage temperature	–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The Human body model (HBM) is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The testing is done according JEDEC EIA/JESD22-A114.
(3) Charged Device Model
(4) Machine Model (MM) is a 200 pF capacitor discharged through a 500 nH inductor with no series resistor into each pin. The testing is done according JEDEC EIA/JESD22-A115.

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE, $R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
QFN 3×3 RTE	48.7°C/W	2.05 W	1.13 W	0.821 W

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	2.7		6.0	V
$I_{O(max)}$	Maximum output current		230		mA
C1	Input capacitor		1.0		µF
C4	Output capacitor	2.2	4.7		µF
C2, C3	Flying capacitor		1.0		µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_I = 3.5 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		2.7		6.0	V
I_Q	Operating quiescent current	1.5X Mode, I_O = 61 mA			8	mA
		1X mode, I_O = 61 mA			3.2	mA
		1X mode, I_O = 100 µA			68	µA
I_{SD}	Shutdown current	EN = GND			1	µA
V_{UVLO1}	UVLO threshold voltage 1(1)	V_{IN} falling	2.1	2.3	2.5	V
V_{HYS_UVLO1}	UVLO 1 hysteresis	V_{IN} rising		200		mV
V_{UVLO2}	UVLO threshold voltage 2(2)	V_{IN} falling	1.2	1.3	1.45	V

(1) Shut down charge pump and power stage, but keep register values.
(2) Shut down completely and come up with all zeros after device restart.

ELECTRICAL CHARACTERISTICS (continued)

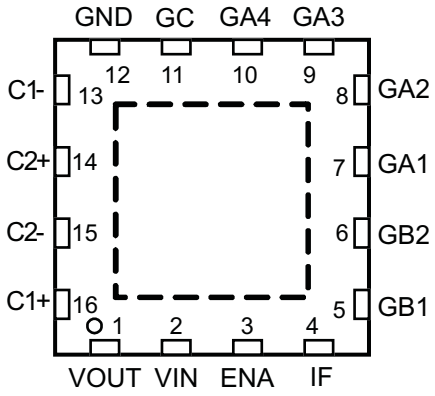
V_I = 3.5 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ENA_H}	Enable high threshold voltage		1.5		V_{IN}	V
V_{ENA_L}	Enable low threshold voltage				0.4	V
T_S	Soft start time (3)			0.5		ms
CHARGE PUMP						
V_{OUT}	Overvoltage limit			6.6		V
F_s	Switching frequency		625	750	875	kHz
R_O	Open loop output impedance	1× Mode, $(V_{IN} - V_O) \div I_O$		1.0	1.2	Ω
		1.5× Mode, $(V_{IN} \times 1.5 - V_O) \div I_O$ V_{IN} = 3.1 V, I_O = 230 mA		2.8	3.5	
CURRENT SINK						
K_{m_GB}	Current matching of Group B at light load condition (4)	T_A = 0° to 40°C, I_{GB_LED} = 100 µA × 2 3.1 V ≤ V_{IN} ≤ 4.2 V, V_{DX}= 0.4 V		±0.1	±2	%
K_m	LED to LED current matching of Group A and B (6 LEDs) (4)	I_{GAB_LED} = 15.3 mA × 6 3.1V ≤ V_{IN} ≤ 4.2 V		±0.1	±5	%
K_a	Current accuracy	I_{LED} = 15.3 mA			±10	%
		I_{LED} = 1.0 mA, T_A = 25°C			±15	
$I_{G\_AB\_M}$	Maximum LED current of GA1-4 and GB1-2	V_{GX} = 0.2 V	21.5	25.2	28.9	mA
I_{GC_M}	Maximum LED current of GC	V_{GX} = 0.2 V		80		mA
$V_{DropOut}$	LED Drop out voltage	See table note (5)		60	100	mV
V_{TH_GU}	1× Mode to 1.5× mode transition threshold voltage (6)	V_{GX} falling, measured on the lowest V_{GX} , I_O = 61 mA		105	120	mV
V_{TH_GD}	1.5× mode to 1× mode Transition threshold voltage	Measured as V_{IN}-(V_{out}-V_{GX_MIN}) I_O = 61 mA	520	550	590	mV
INTERFACE TIMING						
t_{Start}	Start time		3.5			µs
t_{H_LB}	High Time Low Bit, logic 0 detection	Signal level on IF pin is > 1.2 V	3.5		300	µs
t_{L_LB}	Low Time Low Bit, logic 0 detection	Signal level on IF pin < 0.4V	2 × t_{H_LB}		600	µs
t_{L_HB}	Low Time High Bit, logic 1 detection	Signal level on IF pin < 0.4V	3.5		300	µs
t_{H_HB}	High Time High Bit, logic 1 detection	Signal level on IF pin is > 1.2 V	2 × t_{L_HB}		600	µs
t_{EOS}	End of Stream	t_{EOS}	3.5		600	µs
t_{ACKN}	Duration of Acknowledge Condition (IF line pulled low by the device)	V_{IN} 2.7 V to 6 V	600		750	µs
t_{valACK}	Acknowledge Valid Time				3.5	µs

(3) Measurement Condition: From enabling the LED driver to 90% output voltage after V_{IN} is already up.
(4) LED current matching is defined as: $|(I - I_{AVG})|_{max} / I_{AVG}$
(5) Dropout Voltage is defined as V_{GX} (LED cathode) to GND voltage at which current into the LED drops 10% from the LED current at V_{GX} = 0.2 V.
(6) As V_{IN} drops, V_{GX} eventually falls below the switchover threshold of 100 mV, and TPS60255 switches to 1.5× mode. See the Operating Principle section for details about the mode transition thresholds.

PIN ASSIGNMENTS

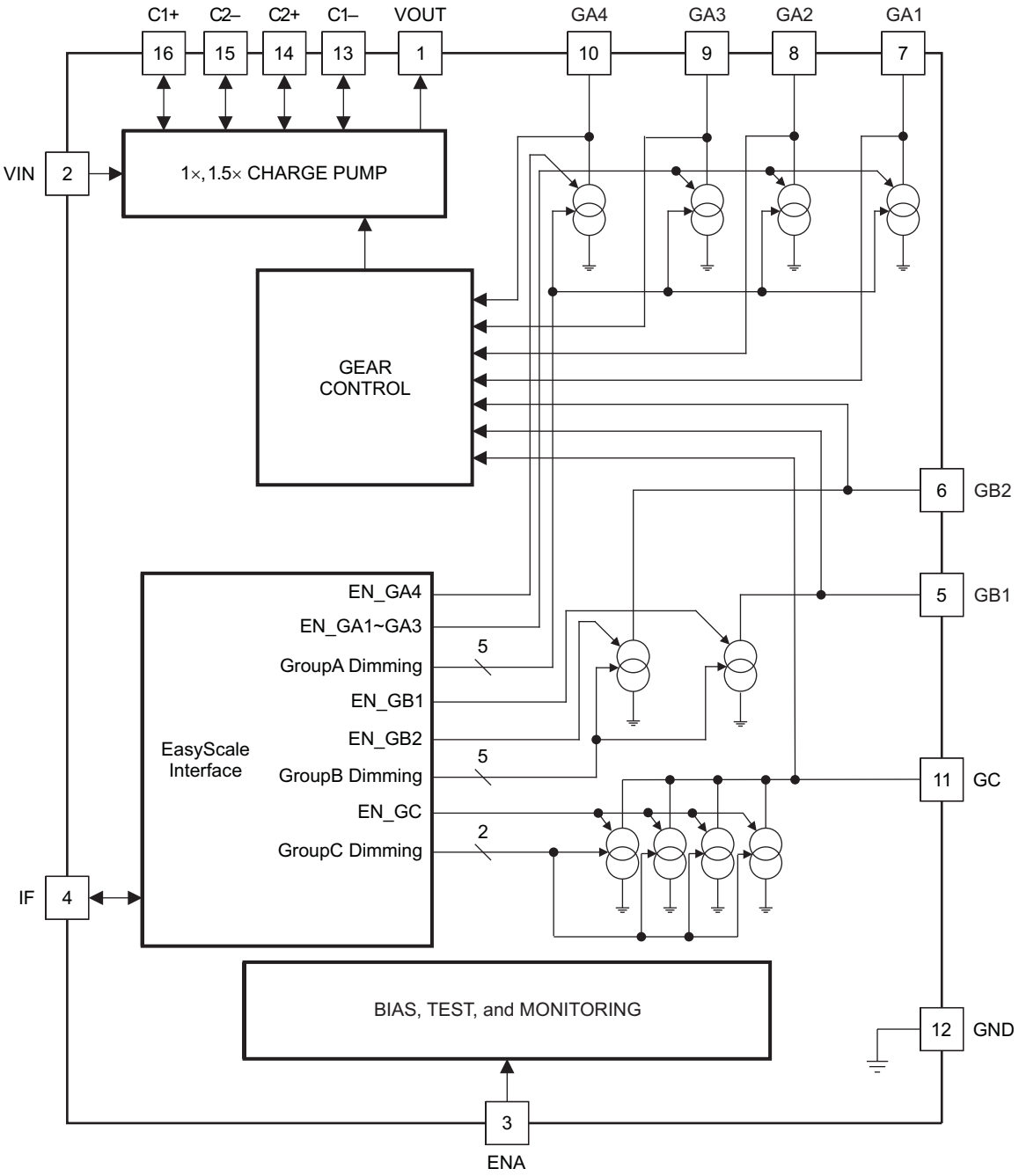
QFN 16-PIN RTE
3 mm X 3 mm
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VOUT	1	O	Connect the output capacitor and the anode of the white LEDs to this pin
VIN	2	I	Supply voltage input
ENA	3	I	Hardware Enable/Disable Pin (High = Enable)
IF	4	I	Single wire interface for on/off and brightness control.
GB1	5	I	Current sink input. Connect the cathode of the white LED to this pin.
GB2	6	I	Current sink input. Connect the cathode of the white LED to this pin.
GA1	7	I	Current sink input. Connect the cathode of the white LED to this pin.
GA2	8	I	Current sink input. Connect the cathode of the white LED to this pin.
GA3	9	I	Current sink input. Connect the cathode of the white LED to this pin.
GA4	10	I	Current sink input. Connect the cathode of the white LED to this pin.
GC	11	I	Current sink input. Connect the cathode of the white LED to this pin.
GND	12	–	Ground
C1–	13	–	Connect to the flying capacitor C1
C2+	14	–	Connect to the flying capacitor C2
C2–	15	–	Connect to the flying capacitor C2
C1+	16	–	Connect to the flying capacitor C1

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Table of Characteristic Graphs

Title	Description	Figure
Load efficiency	Efficiency vs Input Voltage, main LED current = 2.1 mA, 15.3 mA, and 25.2mA	Figure 3
Input Current	Input Current vs Input voltage, main LED current = 2.1 mA, 15.3 mA, and 25.2 mA	Figure 4
Shut down current	Shut Down Current vs Input voltage	Figure 5
Output Accuracy	Output Current Accuracy vs Temperature, main LED current = 15.3 mA	Figure 6
Output Impedance	Switch Resistance vs. Temperature, 1X mode, I_O = 230 mA	Figure 7
Output Impedance	Switch Resistance vs. Temperature, 1.5X mode, I_O = 230 mA	Figure 8
1× → 1.5× Mode Transition Up 1.5× → 1× Mode Transition down	Output Voltage vs Input Voltage, main LED current = 15.3 mA	Figure 9
Normal Operation (1× mode)	Input Voltage, Input Current, GA1 Current, V_{IN} = 4.0 V, LED current : GA1 = GA2 = GA3 = GA4 = GB1 = GB2 = 25.2 mA	Figure 11
Open Lamp Detection (1× mode)	Input Voltage, Input Current, GA1 Current, V_{IN} = 4.0 V, LED current : GA1 = GA2 = GA3 = GB1 = GB2 = 25.2 mA (GA4 is open)	Figure 12

EFFICIENCY vs INPUT VOLTAGE

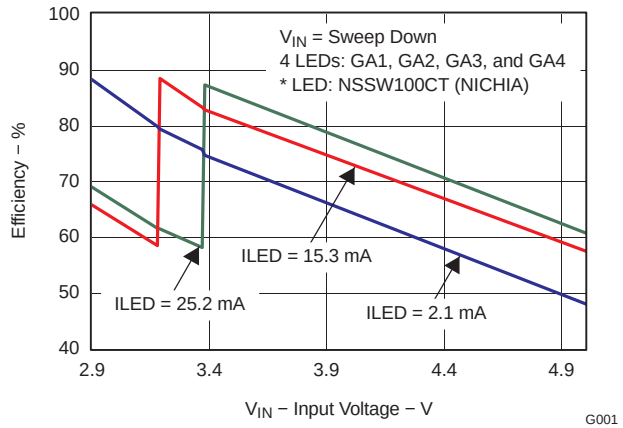


Figure 3.

INPUT CURRENT vs INPUT VOLTAGE

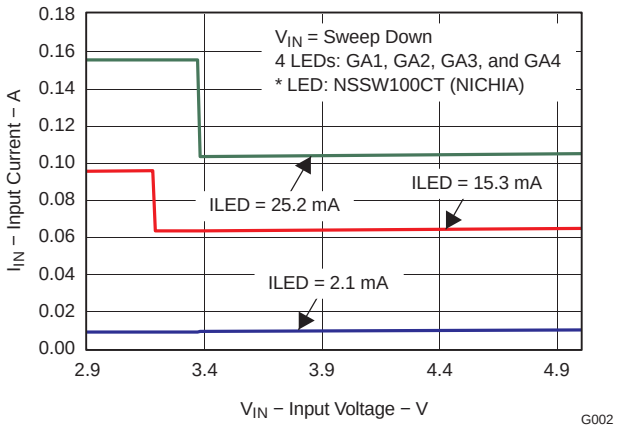


Figure 4.

SHUT DOWN CURRENT vs INPUT VOLTAGE

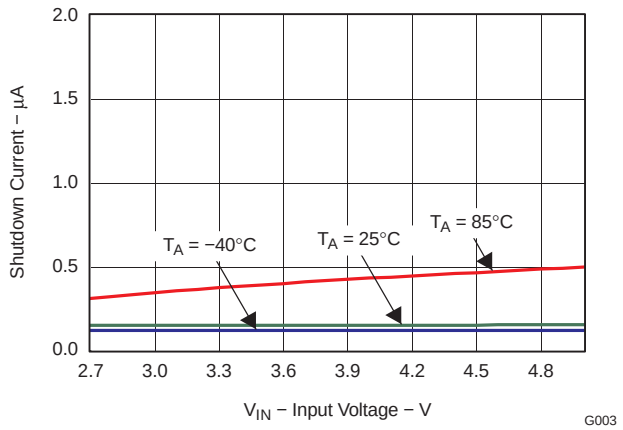


Figure 5.

OUTPUT CURRENT ACCURACY vs TEMPERATURE

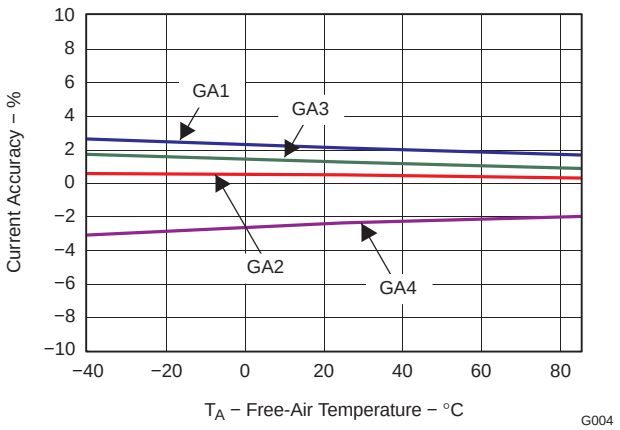


Figure 6.

SWITCH RESISTANCE vs TEMPERATURE 1x mode, I_o = 230 mA

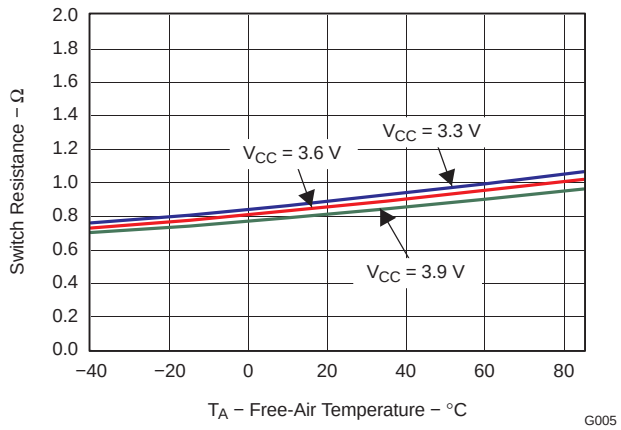


Figure 7.

SWITCH RESISTANCE vs TEMPERATURE 1.5x mode, I_o = 230 mA

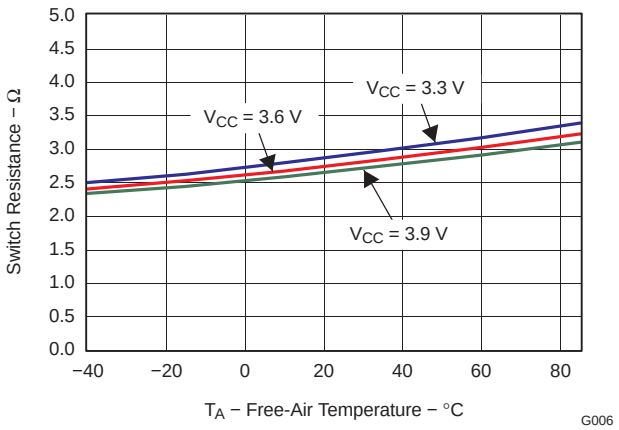


Figure 8.

INPUT VOLTAGE vs OUTPUT VOLTAGE TRANSITION

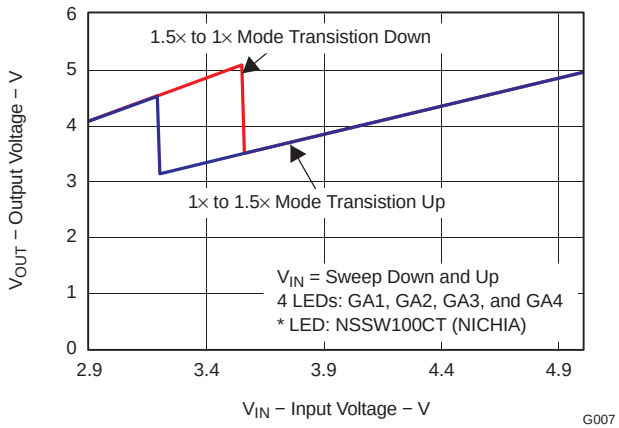


Figure 9.

APPLICATION INFORMATION

APPLICATION OVERVIEW

Most of the current mobile telephone handsets fall into one of these designs:

- **Clam Shell** (Figure 17)—a main display on the inside, a secondary display on the outside, and a keypad backlight.
- **Slide type** (Figure 18)—slide-up and slide-down design, with a main display and two keypads (inside and outside).
- **Bar** (Figure 19)—a main display and a keypad backlight.

Charge pumps are becoming increasingly attractive for driving LEDs for the display backlight and keypad backlight in handsets, where board space and maximum converter height are critical constraints. Its major advantage is use of only capacitors as storage elements. TPS60255 is well suited for use in all three major phone designs.

The device provides six 25 mA current regulators and one 80 mA current regulator. The current regulators are divided into three groups (A, B, and C), with each group having its own independent current program register and ON/OFF control. This promotes dividing and combining the groups for various LED driving configurations including LCD backlight, keypad backlight, and camera flash light. See APPLICATIONS CIRCUITS for example cell phone application circuits.

The TPS60255 adopts 1× and 1.5× charge pump configuration. The device monitors the voltage of the current feedback pins (Gx pins) and automatically switches between 1× and 1.5× mode to ensure current regulation regardless the variations of input voltage and LED forward voltage.

The TPS60255 uses only four external components, the input/output capacitors and two charge-pump-flying-capacitors. This combined with the 16-pin, 3 mm × 3 mm QFN package (0.8 mm height), provides for a small, low-profile total solution.

OPERATING PRINCIPLES

The TPS60255 charge-pump provides regulated LED current from a 2.7 V to 6.0 V input source. It operates in two modes. The 1× mode, where the input is connected to the output through a pass element, and a high efficiency 1.5× charge pump mode. The IC maximizes power efficiency by operating in 1× and 1.5× modes as input voltage and LED current conditions require. The mode of operation is automatically selected by comparing the forward voltage of the WLED plus the voltage of current sink for each LED with the input voltage.

The IC starts up in 1× mode, and automatically transitions to 1.5× mode if the voltage at any current sink input (GAx, GBx, or GC) falls below the 100-mV transition voltage. The IC returns to 1× mode as the input voltage rises. In 1.5× mode, the internal oscillator determines the charge/discharge cycles for the flying capacitors. During a charge cycle, the flying capacitors are connected in series and charged up to the input voltage. After the on-time of the internal oscillator expires, the flying capacitors are reconfigured to be in parallel and then connected in series to the input voltage. This provides an output of 1.5× of the input voltage. After the off-time of the internal oscillator expires, another charge cycle initiates and the process repeats.

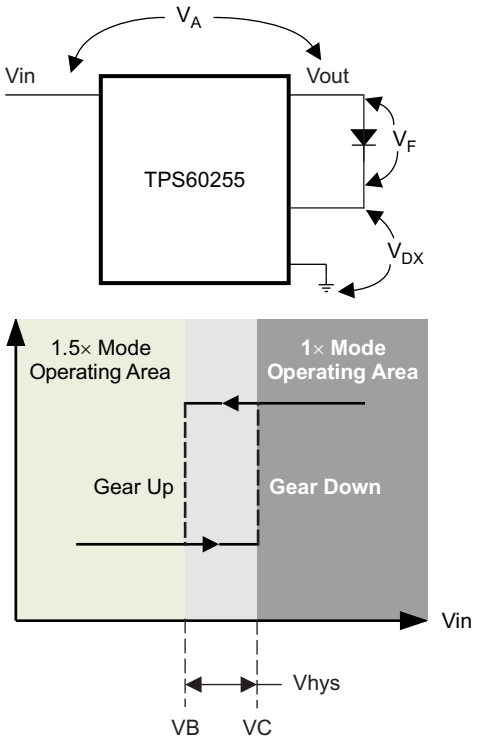


Figure 10. Input Voltage Hysteresis Between 1× and 1.5× Modes

As shown in Figure 10, there is input hysteresis voltage between 1× and 1.5× modes to ensure stable operation during mode transition. For the single-cell Li-ion battery input voltage range, the TPS60255 operates in 1× mode when a fully charged battery is installed. Once the battery voltage drops below the V_B level, the WLED driver operates in the 1.5× mode. Once in 1.5× mode with the same LED current condition, the battery voltage must rise to the V_C level in order to transition from 1.5× to 1× mode. This hysteresis ensures stable operation when there is some input voltage fluctuation at the 1×/1.5× mode transition.

The input transition voltage (V_B) depends on the drop out voltage of the charge pump stage (V_A), WLED forward voltage (V_F), and the mode transition threshold voltage (V_{TH_GU}). The input transition voltage is calculated as:

$V_B = V_A + V_F + V_{TH\_GU}$

$V_A = R_{O\_1X} \times I_O$

where R_{O_1X} is the 1× mode output impedance and I_O is the total output current. See the ELECTRICAL CHARACTERISTICS table for output impedance specifications.

The TPS60255 switches to 1.5× mode when the input voltage is below V_B and remains in the 1.5× mode as long as the input is lower than V_C. When the input voltage rises above V_C, 1.5× Mode is exited. V_C is calculated as:

$V_C = V_F + 550mV$

The input voltage mode transition hysteresis voltage (V_{HYS}) between the 1× and 1.5× modes is calculated as:

$V_{HYS} = V_C – V_B = 550$ mV $– V_{TH\_GU} – V_A$, where $V_{TH\_GU} = 100$ mV

Note that V_A is the key factor in determining V_{HYS} and is dependant on the 1× mode charge pump output impedance and WLED current.

Example: If we choose LWE67C (Osram) and set I_{led} = 15.3 mA, then VF = 3.55 V according to the LED characteristics curve.

Total load current, $I_O = 15.3$ mA × 6 = 91.8 mA

$V_B = R_{O1X} * I_O + V_{TH\_GU} + V_F = 1*0.0918 + 0.1 + 3.55 = 3.748$ (Gear up voltage)

V_C = VF + 550 mV = 3.55 + 0.55 = 4.1 (Gear down voltage)

LED CURRENT SINKS (Group A, B, and C)

The TPS60255 has constant current sinks which drive seven individual LED current paths. Each current sink regulates the LED current to a constant value determined by the single-wire EasyScale interface. The internal register addressing controls the LED channels GA1 to GA4 independent of the GB1 to GB2 or the auxiliary current path GC.

All the LED channels sink up to 25 mA of current, except GC which has an 80 mA maximum current. Using the EasyScale interface, a user can assign GC to a torch, keypad light, or low/weak camera flash with 80 mA current using four dimming steps (full scale, 70%, 40%, and 20%).

These optimized current sinks minimize the voltage headroom required to drive each LED and maximize power efficiency by increasing the amount of time the controller stays in 1× mode before transitioning to the 1.5× mode.

OPEN LAMP DETECTION

In system production, it is often necessary to leave LED-current-paths open depending on the phone model. For example, one phone can use two LEDs to backlight the main display, while another uses four LEDs. Rather than use two different integrated circuits for these different phone applications, the TPS60255 can be used in both applications. In traditional LED driver applications when an LED current path is open, the current sink voltage falls to ground and the current regulation circuitry drives the output to a maximum voltage in an attempt to regulate the current for the missing LED path. This can severely reduce the system efficiency. The TPS60255 uses seven internal comparators to detect when one or more open LED condition occurs and prevent activation of 1.5X mode transition due to missing LEDs.

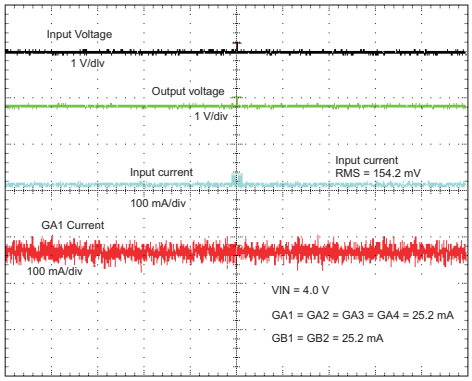


Figure 11. Normal Operation (1× Mode)

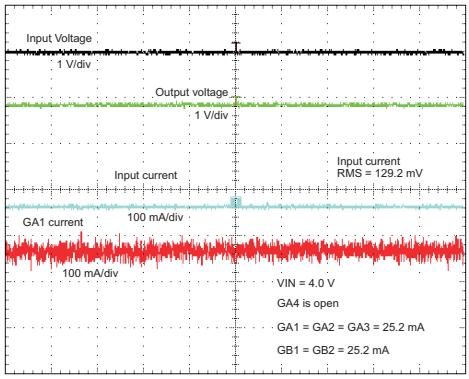


Figure 12. Open Lamp Detection (1× Mode)

CAPACITOR SELECTION

The TPS60255 is optimized to work with ceramic capacitors having a dielectric of X5R or better. The two flying capacitors must be the same value for proper operation. The 750-kHz switching frequency requires the flying capacitor to be less than 4.7uF. Using 1uF ceramic capacitors for both charge-pump-flying-capacitors is recommended. For good input voltage filtering, low ESR ceramic capacitors are recommended. A 1uF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased to 4.7uF. The output capacitor determines the amount of ripple on the output. A 4.7uF output capacitor is recommended for the output capacitor. If better output filtering and lower ripple are desired, a larger output capacitor may be used.

EasyScale: Single-pin serial interface for ON/OFF and brightness control

General

EasyScale is a simple, but very flexible single-pin interface. The interface is based on a master/slave structure, where the master is typically a microcontroller or application processor. The advantage of EasyScale compared to other single-pin interfaces is that its bit detection is largely independent of the bit transmission rate. It can automatically detect bit rates from 1.2 Kbps up to 95 Kbps.

Protocol

All bits are transmitted MSB first and LSB last. Figure 14 (Timing & Bit coding) shows the protocol without acknowledge (Bit RFA = 0) and Figure 15 shows the protocol with acknowledge (Bit RFA = 1) request.

Prior to both bytes (Table 1—device address byte and Table 2—data byte), a start condition must be applied. For this, the IF pin must be pulled high for at least t_{start} (3.5µs) before the bit transmission starts with the falling edge. If the IF pin is already at high level, no start condition is needed prior to the device address byte.

The transmission of each byte is closed with an End of Stream condition for at least t_{EOS} (3.5us).

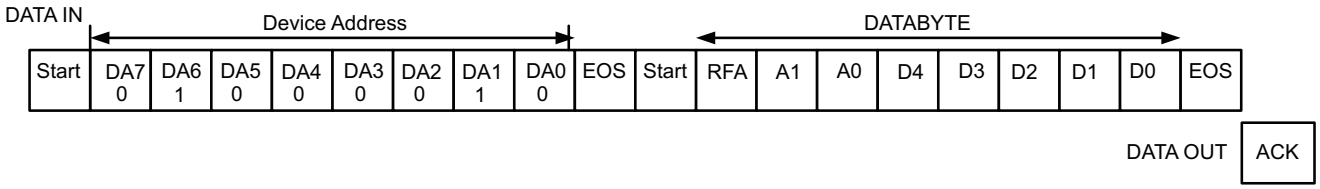


Figure 13. EasyScale Protocol Overview

Table 1. EasyScale Bit Description for Address Byte

BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
7 (MSB)	DA7	IN	DA7 MSB Device Address
6	DA6		DA6
5	DA5		DA5
4	DA4		DA4
3	DA3		DA3
2	DA2		DA2
1	DA1		DA1
0 (LSB)	DA0		DA0 LSB device address

Table 2. EasyScale Bit Description for Data Byte

BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
7(MSB)	RFA	IN	Request For Acknowledge, if high, Acknowledge condition applied by the device
6	A1		Address Bit 1
5	A0		Address Bit 0
4	D4		Data Bit 4
3	D3		Data Bit 3
2	D2		Data Bit 2
1	D1		Data Bit 1
0 (LSB)	D0		Data Bit 0
	ACK	OUT	Acknowledge condition active 0, this condition is only applied when the RFA bit is set. Open drain output, that is, line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open drain output stage. In case of a push pull output stage, Acknowledge condition can not be requested.

Bit Detection

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH}.

It can be simplified to:

- **High Bit:** $t_{High} > t_{Low}$, but with t_{High} at least twice the duration of t_{Low}, see Figure 16.
- **Low Bit :** $t_{High} < t_{Low}$, but with t_{Low} at least twice the duration of t_{High}, see Figure 16.

The bit detection starts with a falling edge on the IF pin and ends with the next falling edge. Depending on the relation between t_{High} and t_{Low}, the logic 0 or 1 is detected.

Acknowledge

The acknowledge condition is applied only if:

- Acknowledge is requested by a set RFA bit.
- The transmitted device address matches with the device's address.
- All 16 bits are received correctly.

If the device turns on the internal ACKN-MOSFET and pulls the IF pin low for the time t_{ACKN}, which is 512 µs maximum, then the Acknowledge condition is valid after an internal delay time t_{valACK}. This means that the internal ACKN-MOSFET is turned on after t_{valACK}, when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the IF pin after t_{valACK} and read back a logic 0. The IF pin can be used again after the acknowledge condition ends.

Note that the acknowledge condition can only be requested in case the master device has an open drain output.

For a push-pull output stage, using a series resistor in the IF line to limit the current to 500 µA is recommended to:

- Prevent an accidental request of acknowledge.
- Protect the internal ACKN-MOSFET.

MODE Selection

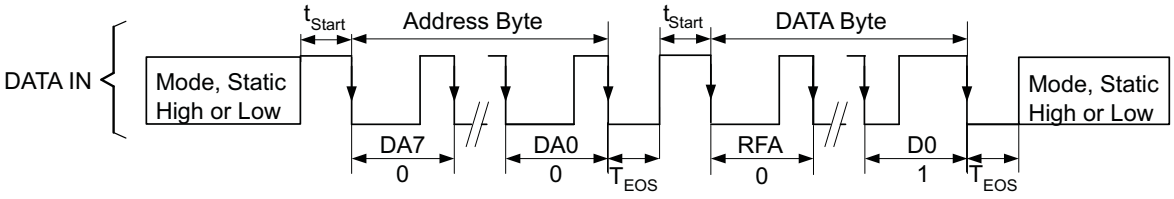


Figure 14. EasyScale Protocol Without Acknowledge (RFA=0)

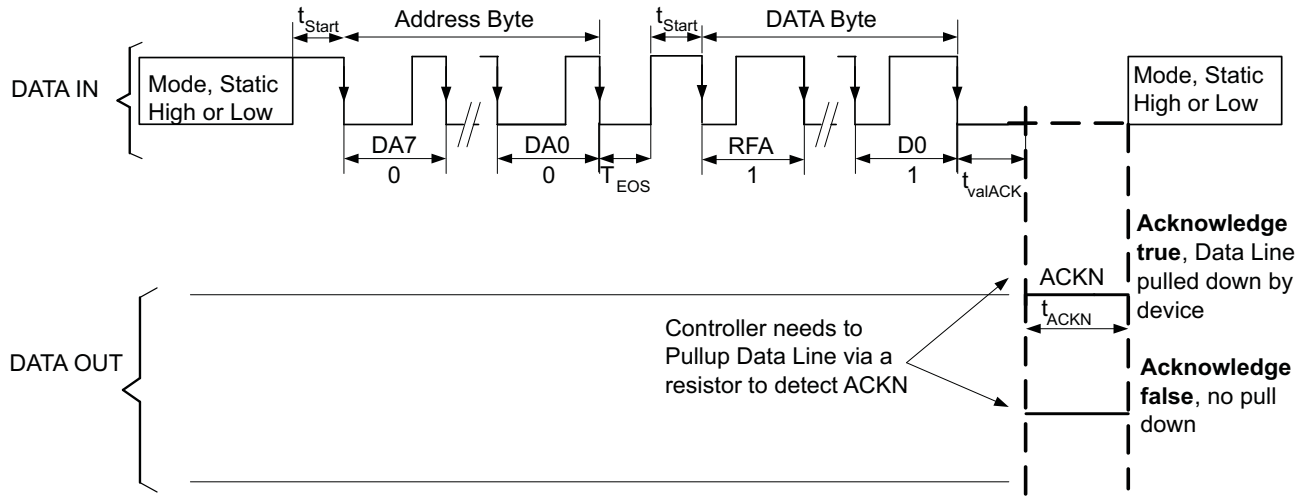


Figure 15. EasyScale Protocol With Acknowledge (RFA=1)

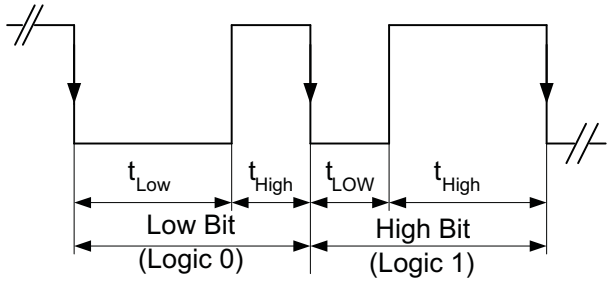


Figure 16. EasyScale Bit Coding

Control Registers of TPS60255 Using EasyScale

Group B Display Current Control Register

Group B DISP CURRENT	A1	A0	D4	D3	D2	D1	D0
BIT data	0	0	IB4	IB3	IB2	IB1	IB0

Bit 4 to Bit 0 (IB4 to IB0)

5-bit command (32 steps) to set the current for Group B
For LED currents between 100 µA and 1.0 mA, one step = 100 µA.
For LED currents between 1.0 mA and 25.2 mA, one step = 1.1 mA.

Group A Display Current Control Register

Group A DISP CURRENT	A1	A0	D4	D3	D2	D1	D0
BIT data	0	1	IA4	IA3	IA2	IA1	IA0

Bit 4 to Bit 0 (IA4 to IA0)	5-bit command (32 steps) to set the current for Group A For LED currents between 100 µA and 1.0 mA, one step = 100 µA. For LED currents between 1.0 mA and 25.2 mA, one step = 1.1 mA.

Current Control Register Values

Table 3. Current Control Register Value for Group A and B

Number	Current (mA)	D4 IA4 (IB4)	D3 IA3 (IB3)	D2 IA2 (IB2)	D1 IA1 (IB1)	D0 IA0 (IB0)
0	0.1	0	0	0	0	0
1	0.2	0	0	0	0	1
2	0.3	0	0	0	1	0
3	0.4	0	0	0	1	1
4	0.5	0	0	1	0	0
5	0.6	0	0	1	0	1
6	0.7	0	0	1	1	0
7	0.8	0	0	1	1	1
8	0.9	0	1	0	0	0
9	1.0	0	1	0	0	1
10	2.1	0	1	0	1	0
11	3.2	0	1	0	1	1
12	4.3	0	1	1	0	0
13	5.4	0	1	1	0	1
14	6.5	0	1	1	1	0
15	7.6	0	1	1	1	1
16	8.7	1	0	0	0	0
17	9.8	1	0	0	0	1
18	10.9	1	0	0	1	0
19	12.0	1	0	0	1	1
20	13.1	1	0	1	0	0
21	14.2	1	0	1	0	1
22	15.3	1	0	1	1	0
23	16.4	1	0	1	1	1
24	17.5	1	1	0	0	0
25	18.6	1	1	0	0	1
26	19.7	1	1	0	1	0
27	20.8	1	1	0	1	1
28	21.9	1	1	1	0	0
29	23.0	1	1	1	0	1
30	24.1	1	1	1	1	0
31	25.2	1	1	1	1	1

Enable Control Register

ENABLE	A1	A0	D4	D3	D2	D1	D0
BIT data	1	0	EN_OLD	EN_GB1	EN_GB2	EN_GA	EN_GA4

Bit 4 (EN_OLD)

1: Open Lamp Detection Enabled
0: Open Lamp Detection Disabled

Bit 3 (EN_GB1)

1: Enable GB1
0: Disable GB1

Bit 2 (EN_GB2)

1: Enable GB2
0: Disable GB2

Bit 1 (EN_GA)

1: Enable GA1 to GA3
0: Disable GA1 to GA3

Bit 0 (EN_GA4)

1: Enable GA4
0: Disable GA4

GC Brightness and Operation Mode Control Register

Aux DISP CURRENT	A1	A0	D4	D3	D2	D1	D0
BIT data	1	1	Mode1	Mode0	GC0	GC1	EN_GC

Bit 4 to Bit 3

Mode1	Mode0	TPS6055 Mode
0	0	Auto-switchover Mode. The TPS60255 selects 1× or 1.5× mode automatically as described in the OPERATING PRINCIPLES section.
1	1	Shut down, All LED current shuts down.
1	0	1× Mode. TPS60255 remains in 1× mode regardless of the input voltage. LED current can not regulate at lower input voltages when in this mode.
0	1	1.5× Mode. TPS60255 remains in 1.5× mode regardless of the input voltage

Bit 2 to Bit 1

2-bit command (four steps) to set the current for GC

GC0	GC1	Dimming Step
0	0	20 %
1	0	40 %
0	1	70 %
1	1	100 %

Bit 0

EN_GC
1: Enable GC
0: Disable GC

ADDITIONAL APPLICATION CIRCUITS

These application circuits apply to the common designs for mobile telephones:

- **Clam Shell** (Figure 17)—application circuit for driving four LEDs for main display and two LEDs for the subdisplay.
- **Slide** (Figure 18)—application circuit for driving four LEDs for LCD display backlight and LEDs for both sub- and main keypad backlight.
- **Bar** (Figure 19)—application circuit for driving four LEDs for LCD display backlight and LEDs for key pad backlight.

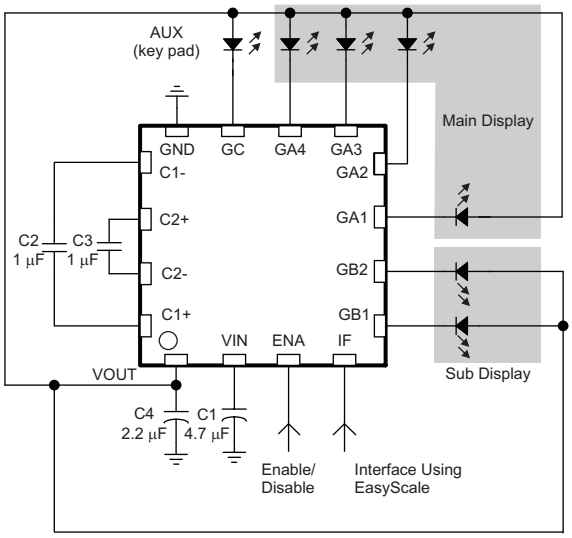


Figure 17. Application Circuit—Clam Shell Mobile Phone Design

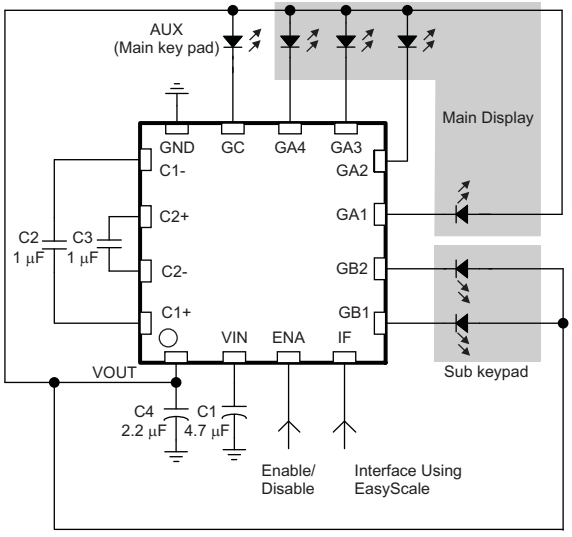


Figure 18. Application Circuit—Slide Mobile Phone Design

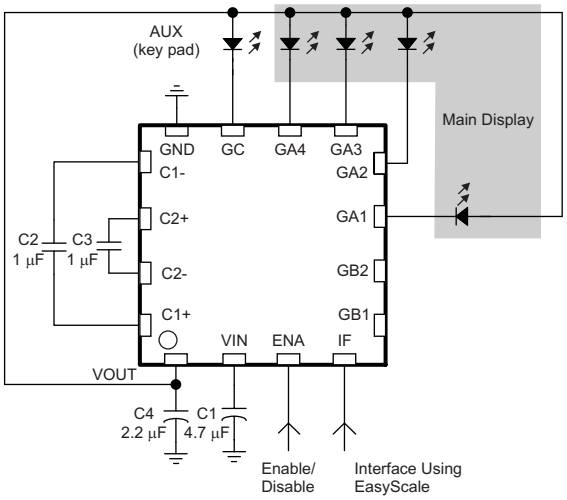


Figure 19. Application Circuit—Bar Mobile Phone Design

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60255RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BUP	Samples
TPS60255RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BUP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

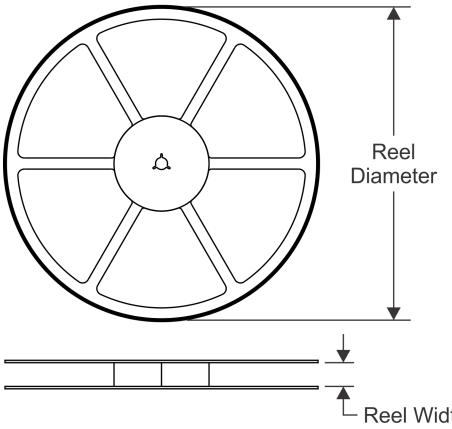
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

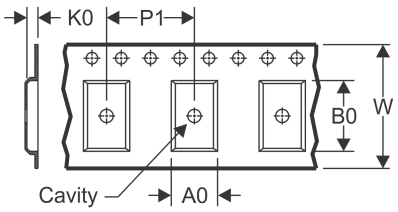
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

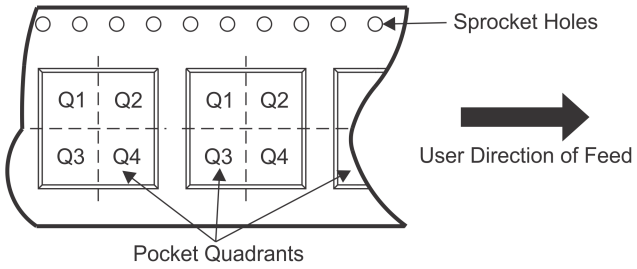


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

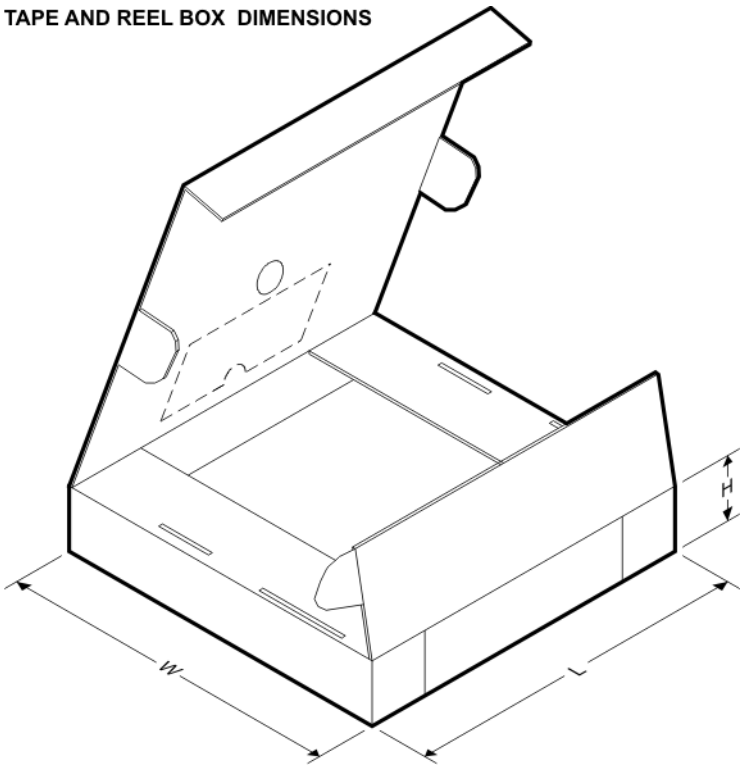
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60255RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS60255RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

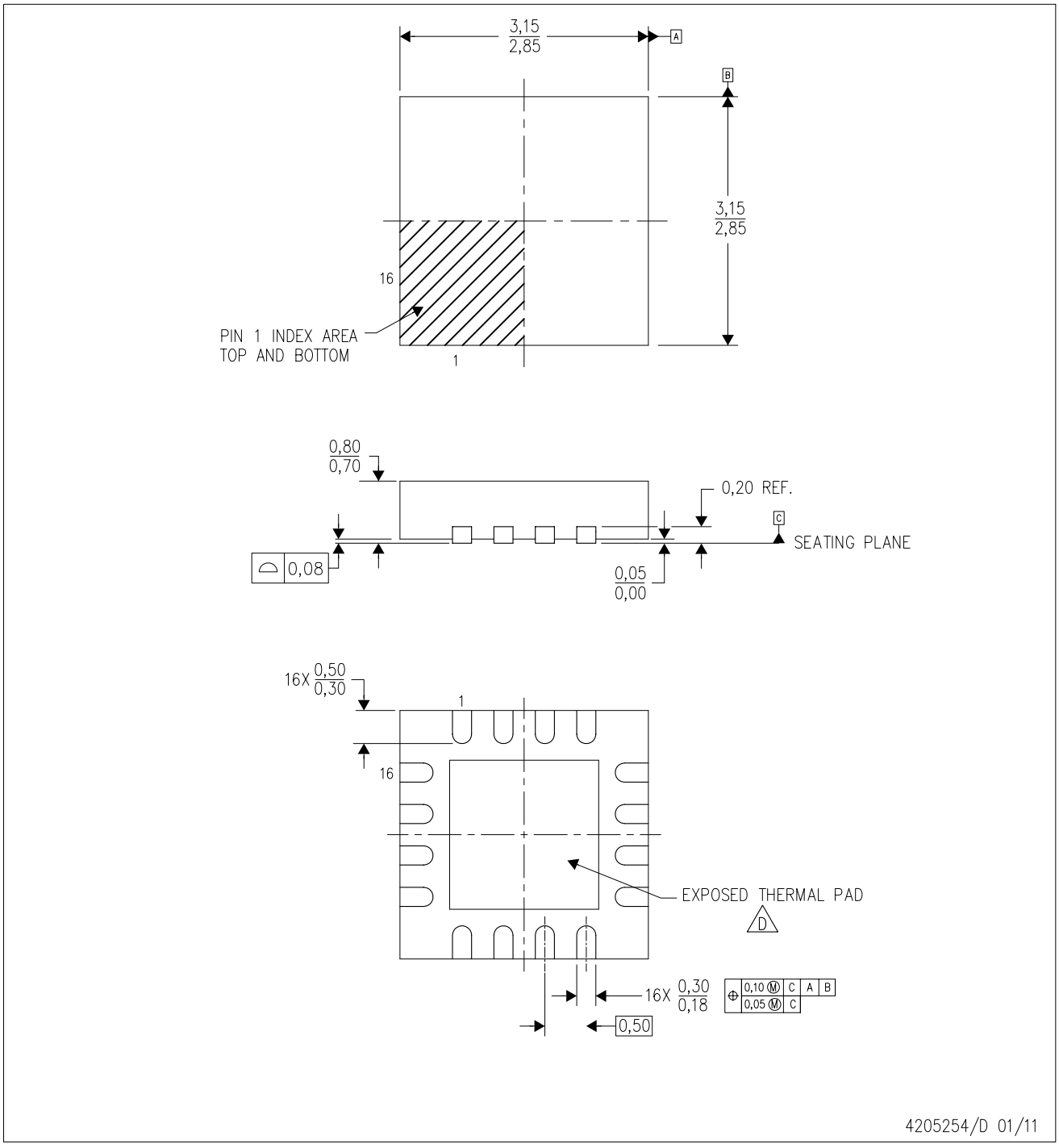
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60255RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS60255RTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

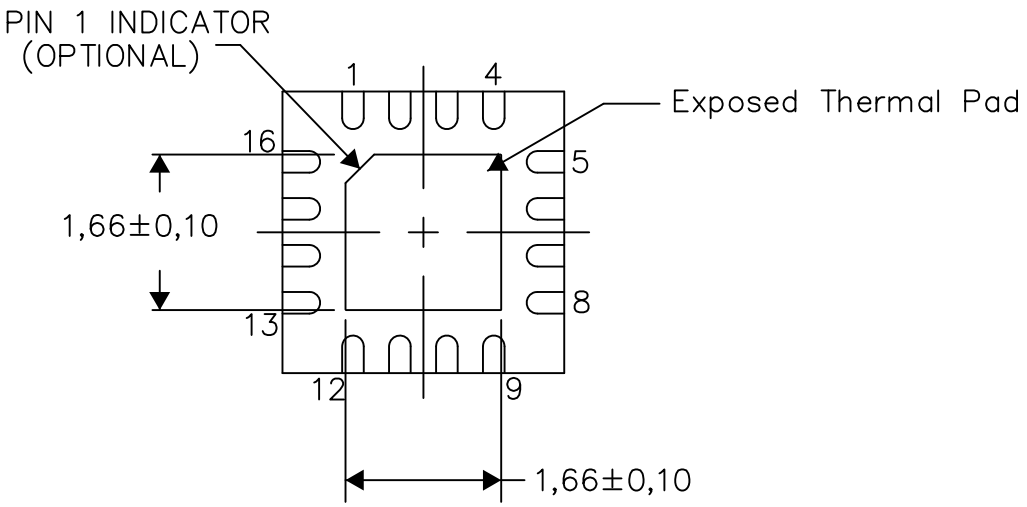
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



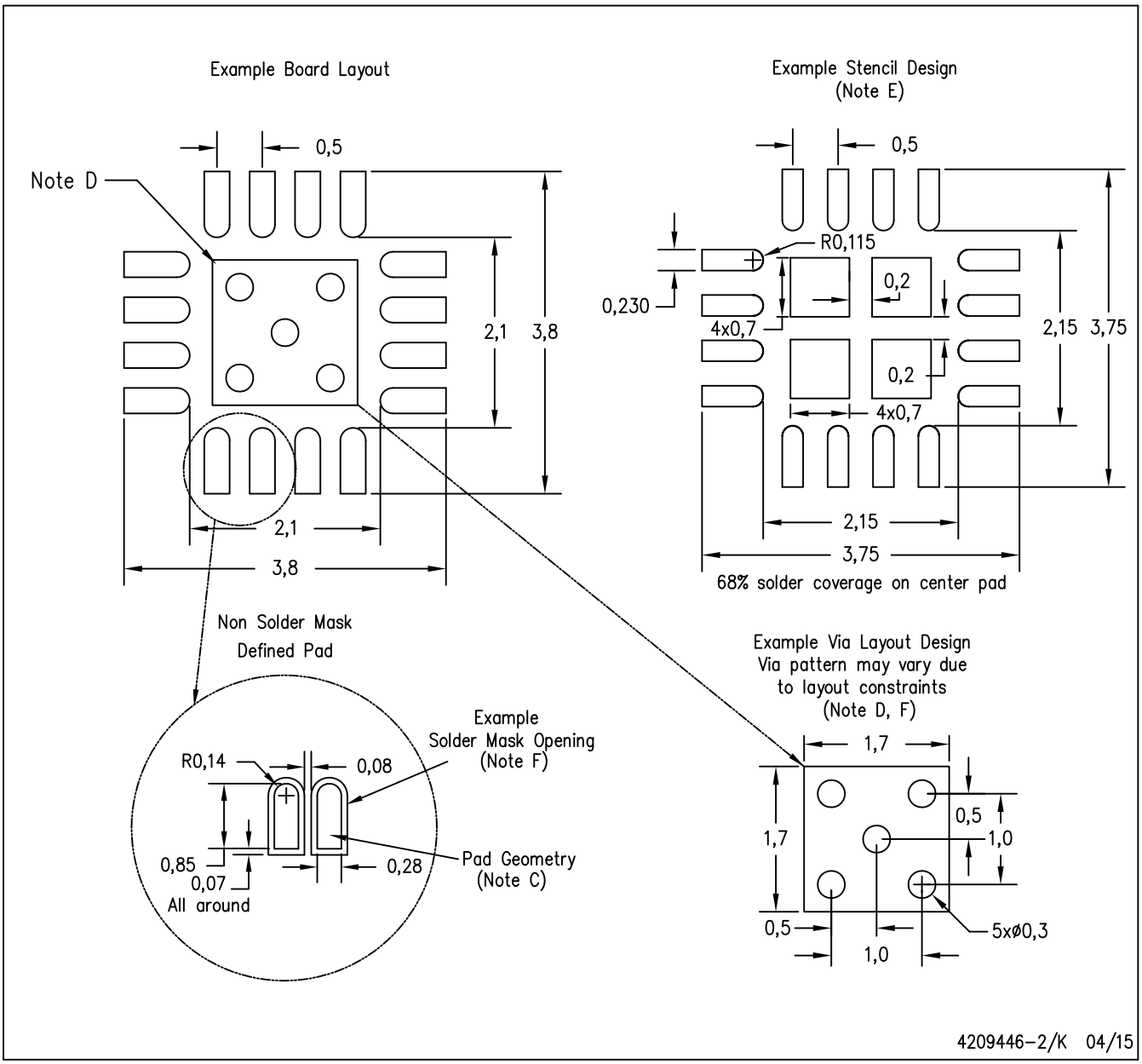
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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