THE DATASHEET OF

ADA4000-4ARUZ

www.win-source.net 0086-755-83957316

Low Cost, Precision JFET Input Operational Amplifiers

Data Sheet

ADA4000-1/ADA4000-2/ADA4000-4

FEATURES

High slew rate: 20 V/µs
Fast settling time
Low offset voltage: 1.70 mV maximum
Bias current: 40 pA maximum
±4 V to ±18 V operation
Low voltage noise: 16 nV/√Hz
Unity gain stable
Common-mode voltage includes +V_S
Wide bandwidth: 5 MHz

APPLICATIONS

Reference gain/buffers
Level shift/driving
Active filters
Power line monitoring/control
Current/voltage sense or monitoring
Data acquisition
Sample-and-hold circuits
Integrators

GENERAL DESCRIPTION

The ADA4000-1/ADA4000-2/ADA4000-4 are junction field effect transistor (JFET) input operational amplifiers featuring precision, very low bias current, and low power. Combining high input impedance, low input bias current, wide bandwidth, fast slew rate, and fast settling time, the ADA4000-1/ADA4000-2/ADA4000-4 are ideal amplifiers for driving analog-to-digital inputs and buffering digital-to-analog converter outputs. The input common-mode voltage includes the positive power supply, which makes the device an excellent choice for high-side signal conditioning.

Additional applications for the ADA4000-1/ADA4000-2/ADA4000-4 include electronic instruments, automated test equipment (ATE) amplification, buffering, integrator circuits, instrumentation-quality photodiode amplification, and fast precision filters (including phase-locked loop filters). The devices also include utility functions, such as reference buffering, level shifting, control input/output interface, power supply control, and monitoring functions.

PIN CONFIGURATIONS

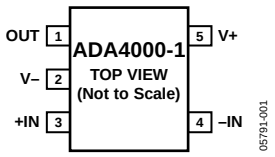

Figure 1. 5-Lead TSOT (UJ-5)

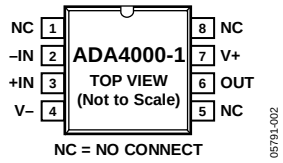

Figure 2. 8-Lead SOIC (R-8)

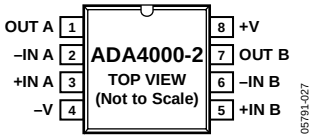

Figure 3. 8-Lead SOIC (R-8)

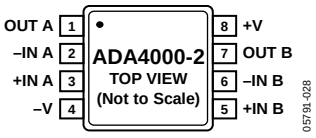

Figure 4. 8-Lead MSOP (RM-8)

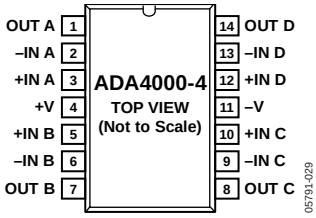

Figure 5. 14-Lead SOIC (R-14)

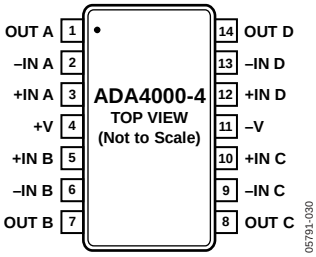

Figure 6. 14-Lead TSSOP (RU-14)

Rev. B **Document Feedback**
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REVISION HISTORY

3/16—Rev. A to Rev. B

Change to Figure 12 Caption ... 6
Changes to Output Phase Reversal and Input Noise Section and Capacitive Load Drive Section ... 10
Updated Outline Dimensions ... 13

3/09—Rev. 0 to Rev. A

Changes to Input Voltage Range Parameter ... 4
Changes to Common-Mode Rejection Ration Parameter ... 4
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5/07—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = ±15.0 V, V_{CM} = V_S/2 V, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	1.70	mV
		−40°C ≤ T_A ≤ +125°C			3.0	mV
Input Bias Current	I_B			5	40	pA
		−40°C ≤ T_A ≤ +85°C			170	pA
		−40°C ≤ T_A ≤ +125°C			4.5	nA
Input Offset Current	I_{OS}			2	40	pA
		−40°C ≤ T_A ≤ +85°C			80	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range	IVR		−11		+15	V
Common-Mode Rejection Ratio	CMRR	−11 V ≤ V_{CM} ≤ +15 V	80	100		dB
		−40°C ≤ T_A ≤ +125°C		100		dB
Open-Loop Gain	A_{VO}	R_L = 2 kΩ, V_O = ±10 V	100	110		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to ground	13.60	13.90		V
		−40°C ≤ T_A ≤ +125°C	13.40			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to ground		−13.4	−13.0	V
		−40°C ≤ T_A ≤ +125°C			−12.80	V
Short-Circuit Current	I_{SC}			±28		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.0 V to ±18.0 V	82	92		dB
Supply Current/Amplifier	I_{SY}			1.35	1.65	mA
		−40°C ≤ T_A ≤ +125°C			1.80	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_I = 10 V, R_L = 2 kΩ		20		V/µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	Φ_M			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		1		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.01		pA/√Hz
INPUT IMPEDANCE						
Differential Mode	$(R\|\|C)_{IN\text{-}DIFF}$			10||4		GΩ||pF
Common Mode	$(R\|\|C)_{INCM}$			10^3||5.5		GΩ||pF

V_S = ±5 V, V_{CM} = V_S/2 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.20	1.70	mV
		−40°C ≤ T_A ≤ +125°C			3.0	mV
Input Bias Current	I_B			5	40	pA
		−40°C ≤ T_A ≤ +85°C			170	pA
		−40°C ≤ T_A ≤ +125°C			3	nA
Input Offset Current	I_{OS}			2	40	pA
		−40°C ≤ T_A ≤ +85°C			80	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range	IVR		−1.0		+5.0	V
Common-Mode Rejection Ratio	CMRR	−1.0 V ≤ V_{CM} ≤ +5.0 V	72	80		dB
		−40°C ≤ T_A ≤ +125°C		80		dB
Open-Loop Gain	A_{VO}	R_L = 2 kΩ, V_O = ±2.5 V	106	114		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to ground	4.0	4.20		V
		−40°C ≤ T_A ≤ +125°C	3.80			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to ground		−3.45	−3.20	V
		−40°C ≤ T_A ≤ +125°C			−3.00	V
Short-Circuit Current	I_{SC}			±28		mA
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}			1.25	1.65	mA
		−40°C ≤ T_A ≤ +125°C			1.80	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_I = 10 V, R_L = 2 kΩ		20		V/µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	Φ_M			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		1		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.01		pA/√Hz
INPUT IMPEDANCE						
Differential Mode	$(R\|\|C)_{IN\text{-}DIFF}$			10||4		GΩ||pF
Common Mode	$(R\|\|C)_{INCM}$			10^3||5.5		GΩ||pF

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	±V supply
Differential Input Voltage	±V supply
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead TSOT (UJ-5)	172.92	61.76	°C/W
8-Lead SOIC (R-8)	112.38	61.6	°C/W
8-Lead MSOP (RM-8)	141.9	43.7	°C/W
14-Lead SOIC (R-14)	88.2	56.3	°C/W
14-Lead TSSOP (RU-14)	114	23.3	°C/W

POWER SEQUENCING

The operational amplifier supply voltages must be established simultaneously with, or before, any input signals are applied. If this is not possible, the input current must be limited to 10 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

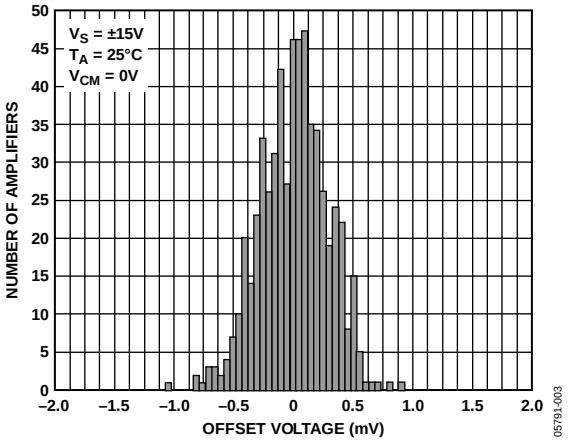


Figure 7. Input Offset Voltage Distribution, V_S = ±15 V

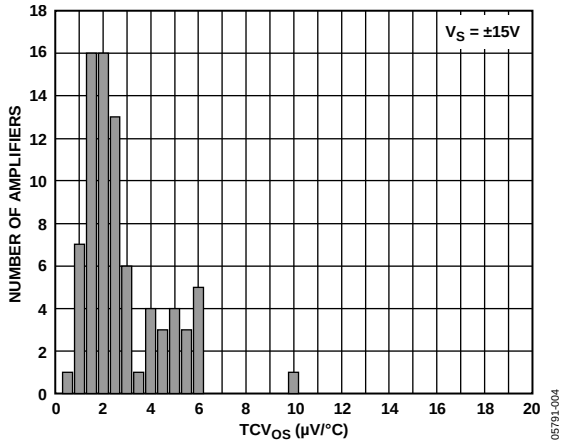


Figure 8. Offset Voltage Drift Distribution, V_S = ±15 V

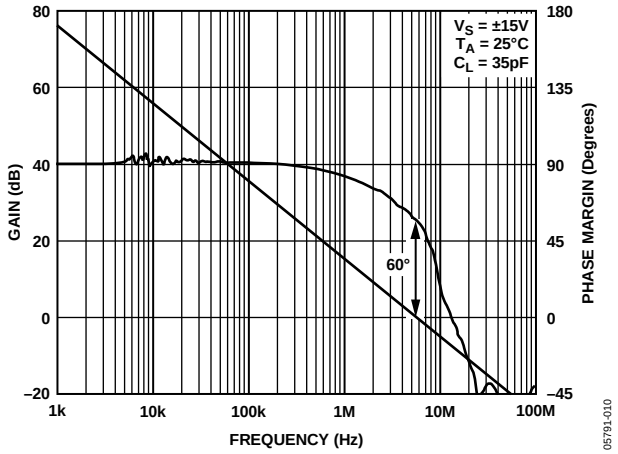


Figure 9. Open-Loop Gain and Phase Margin vs. Frequency, V_S = ±15 V

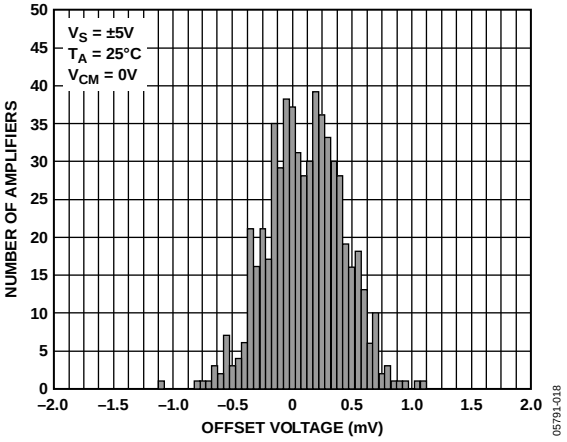


Figure 10. Input Offset Voltage Distribution, V_S = ±5 V

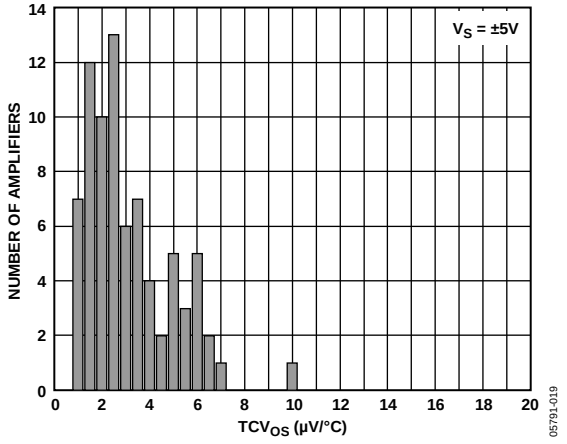


Figure 11. Offset Voltage Drift Distribution, V_S = ±5 V

Figure 12. Open-Loop Gain and Phase Margin vs. Frequency, V_S = ±5 V

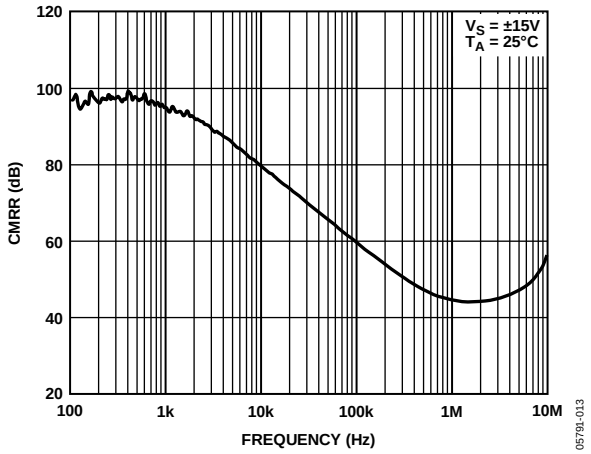


Figure 13. Common-Mode Rejection Ratio vs. Frequency, V_S = ±15 V

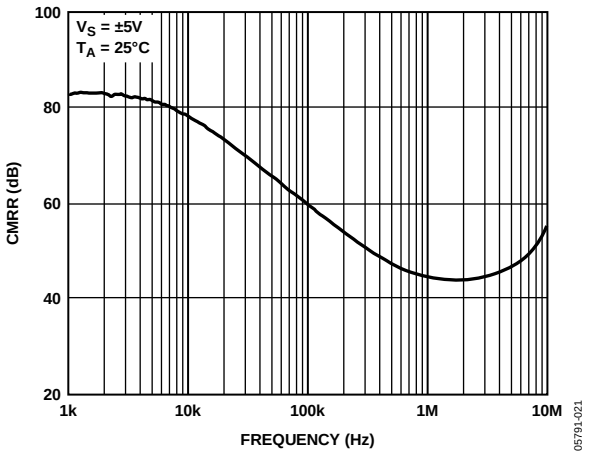


Figure 16. Common-Mode Rejection Ratio vs. Frequency, V_S = ±5 V

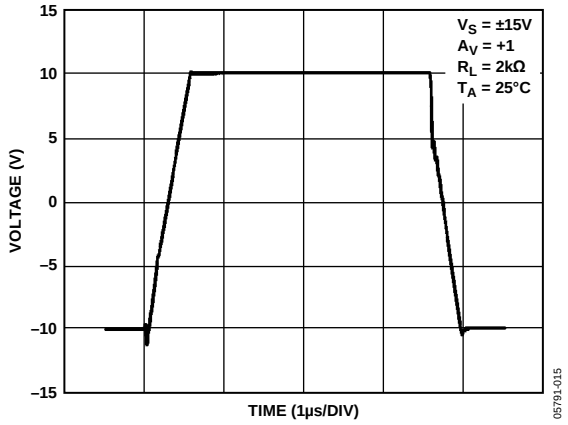


Figure 14. Large Signal Transient Response, V_S = ±15 V

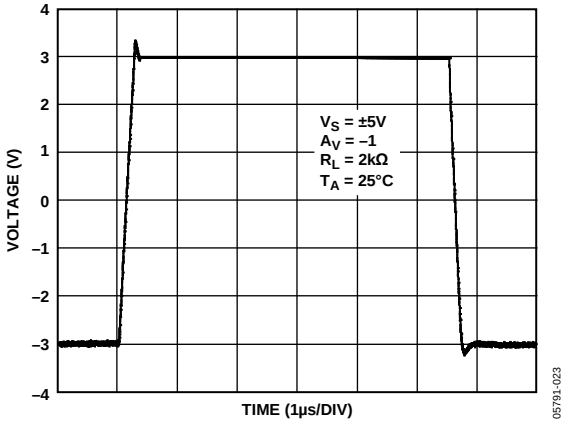


Figure 17. Large Signal Transient Response, V_S = ±5 V

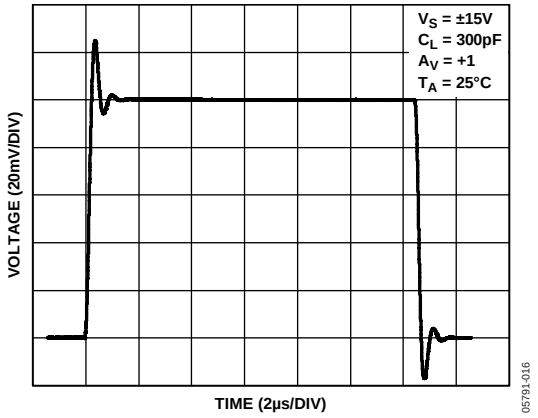


Figure 15. Small Signal Transient Response, V_S = ±15 V

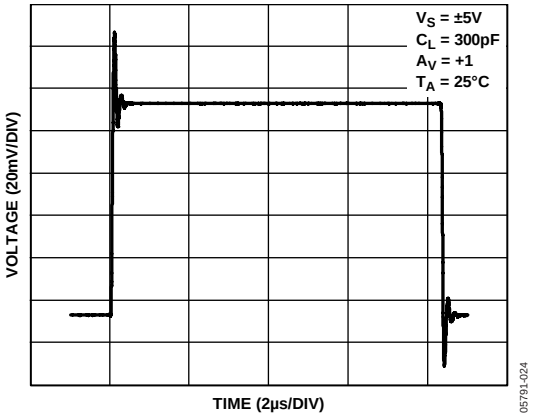


Figure 18. Small Signal Transient Response, V_S = ±5 V

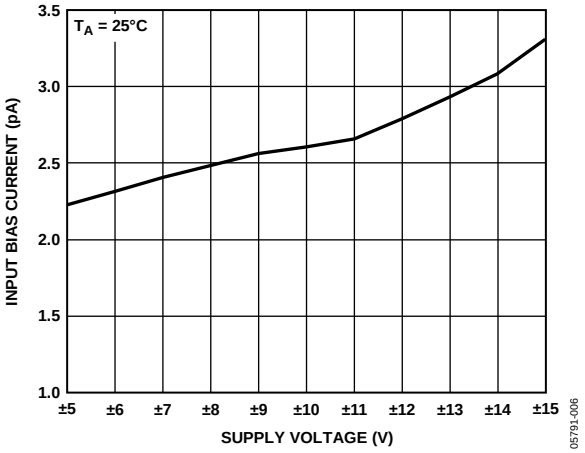


Figure 19. Input Bias Current vs. Supply Voltage

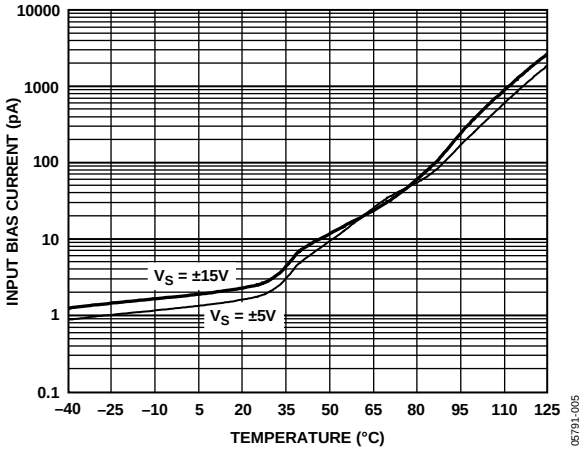


Figure 20. Input Bias Current vs. Temperature

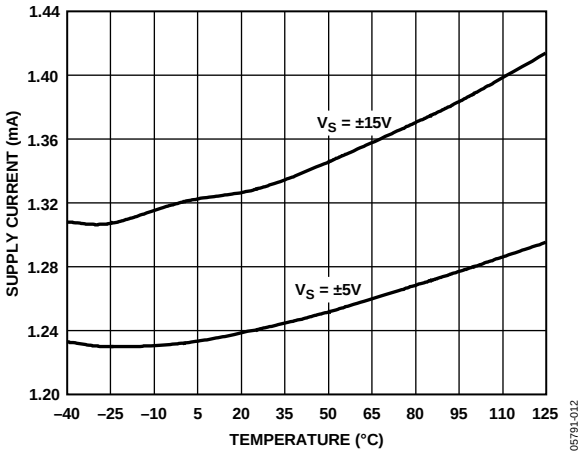


Figure 21. Supply Current vs. Temperature

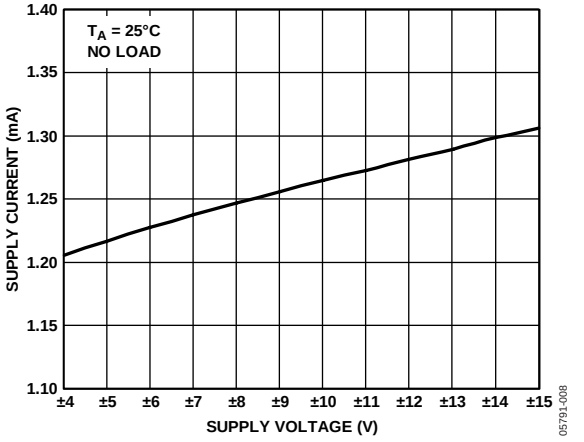


Figure 22. Supply Current vs. Supply Voltage

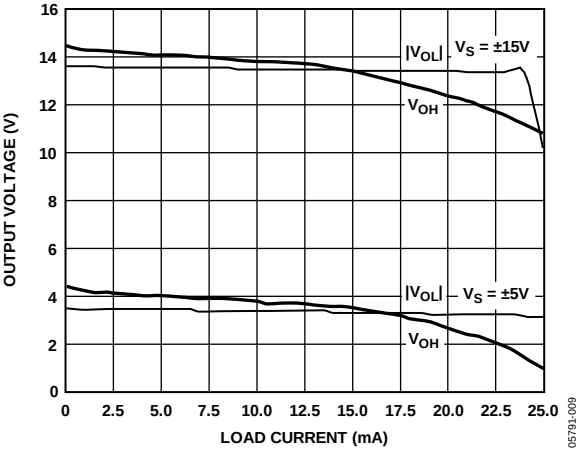


Figure 23. Output Voltage vs. Load Current

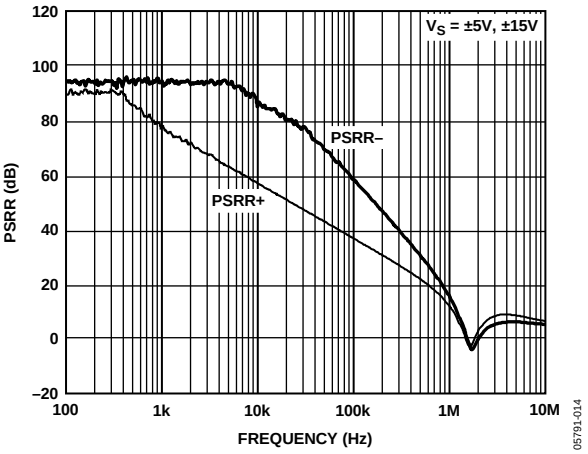


Figure 24. PSRR vs. Frequency

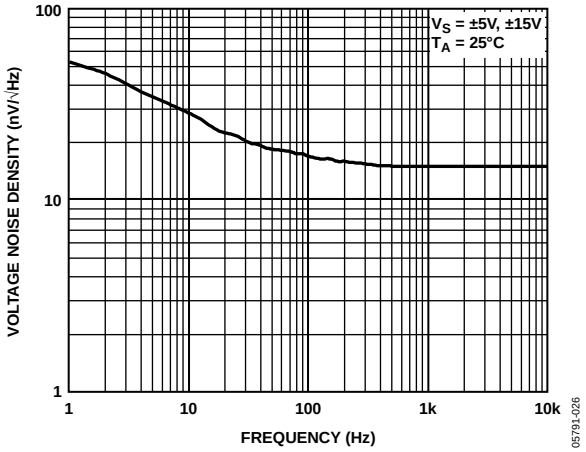


Figure 25. Voltage Noise Density vs. Frequency

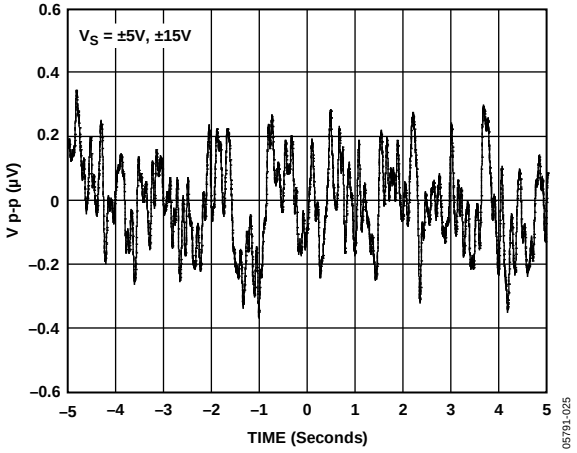


Figure 28. 0.1 Hz to 10 Hz Input Voltage Noise

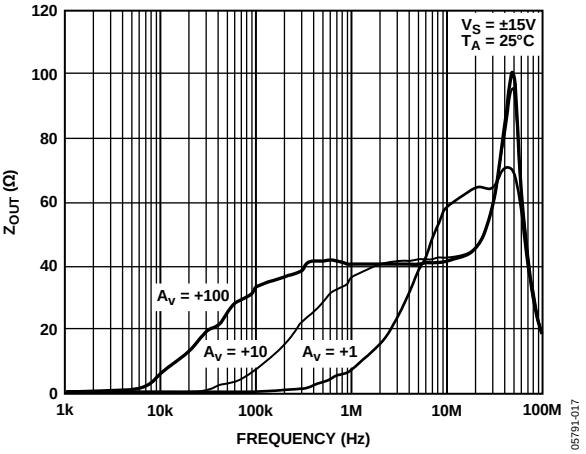


Figure 26. Output Impedance vs. Frequency

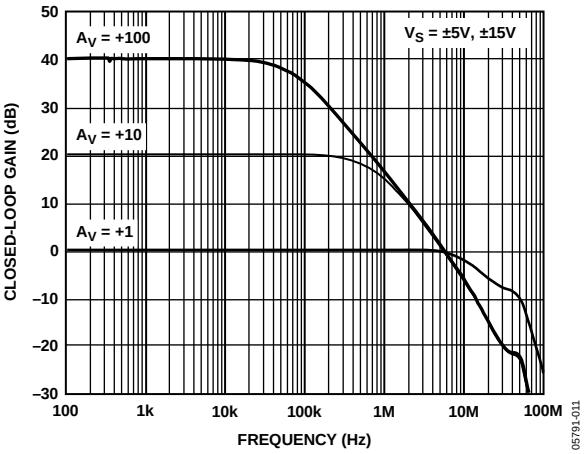


Figure 29. Closed-Loop Gain vs. Frequency

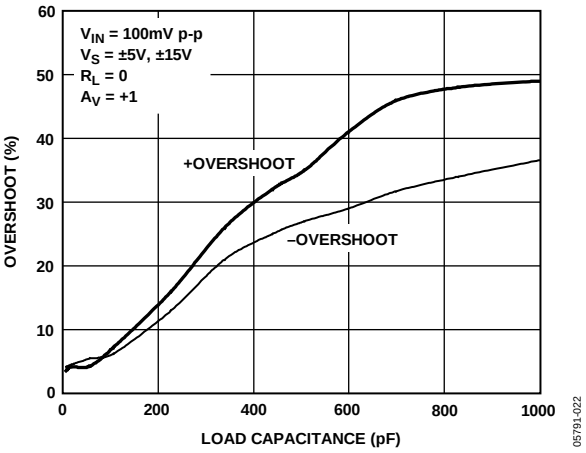


Figure 27. Overshoot vs. Load Capacitance

APPLICATIONS INFORMATION

OUTPUT PHASE REVERSAL AND INPUT NOISE

Phase reversal is a change of polarity in the transfer function of the amplifier. This can occur when the voltage applied at the input of the amplifier exceeds the maximum common-mode voltage. Phase reversal happens when the device is configured in the gain of 1.

Most JFET amplifiers invert the phase of the input signal if the input exceeds the common-mode input. Phase reversal is a temporary behavior of the ADA4000-1/ADA4000-2/ADA4000-4 family. Each device returns to normal operation by bringing back the common-mode voltage. The cause of this effect is saturation of the input stage, which leads to the forward-biasing of a drain-gate diode. In noninverting applications, a simple fix for this is to insert a series resistor between the input signal and the noninverting terminal of the amplifier. The value of the resistor depends on the application, because adding a resistor adds to the total input noise of the amplifier. The total noise density of the circuit is

$$e_{nTOTAL} = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S}$$

where:

e_n is the input voltage noise density of the device.
i_n is the input current noise density of the device.
R_S is the source resistance at the noninverting terminal.
k is Boltzmann's constant (1.38×10^{-23} J/K).
T is the ambient temperature in Kelvin (T = 273 + °C).

In general, it is good practice to limit the input current to less than 5 mA to avoid driving a great deal of current into the amplifier inputs.

CAPACITIVE LOAD DRIVE

The ADA4000-1/ADA4000-2/ADA4000-4 are stable at all gains in both inverting and noninverting configurations. The devices are capable of driving up to 1000 pF of capacitive loads without oscillations in unity gain configurations.

However, as with most amplifiers, driving larger capacitive loads in a unity gain configuration can cause excessive overshoot and ringing. A simple solution to this problem is to use a snubber network (see Figure 30).

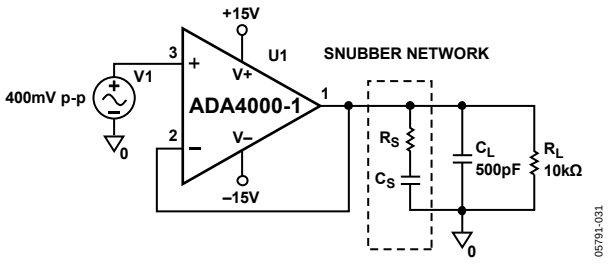


Figure 30. Snubber Network Configuration

The advantage of this compensation method is that the swing at the output is not reduced because R_S is out of the feedback network, and the gain accuracy does not change. Depending on the capacitive loading of the circuit, the values of R_S and C_S change, and the optimum value can be determined empirically. In Figure 31, the oscilloscope image shows the output of the ADA4000-1/ADA4000-2/ADA4000-4 family in response to a 400 mV pulse. The circuit is configured in the unity gain configuration with 500 pF in parallel with 10 kΩ of load capacitive.

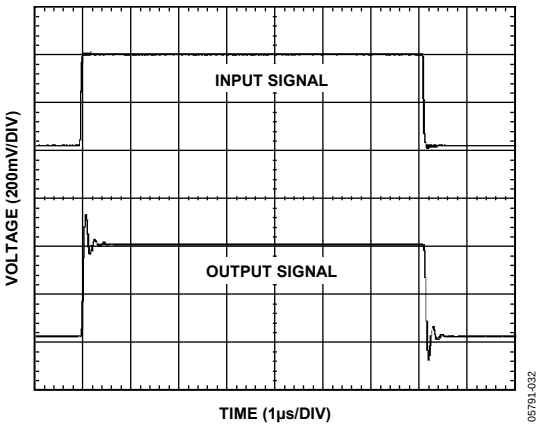


Figure 31. Capacitive Load Drive Without Snubber Network

When the snubber circuit is used, the overshoot is reduced from 30% to 6% with the same load capacitance. Ringing is virtually eliminated, as shown in Figure 32. In this circuit, R_S is 41 Ω and C_S is 10 nF.

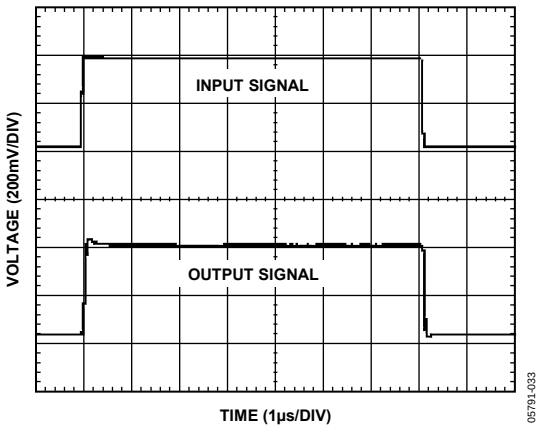


Figure 32. Capacitive Load with Snubber Network

SETTLING TIME

Settling time is the amount of time it takes the amplifier output to reach and remain within a percentage of the final value. This is an important parameter in data acquisition systems. Because most bipolar DAC converters have current output, an external operational amplifier is required to convert the current to voltage. Therefore, the amplifier settling time plays a role in the total settling time of the output signal. A good approximation for the total settling time is

$$t_S\ Total = \sqrt{(t_S\ DAC)^2 + (t_S\ AMP)^2}$$

The ADA4000-1/ADA4000-2/ADA4000-4 settle to within 0.1% of their final value in less than 1.2 µs. The settling time has been tested by using the configuration circuit in Figure 34.

The input signal is a 10 V pulse and the output is the error signal for the settling time shown in Figure 33.

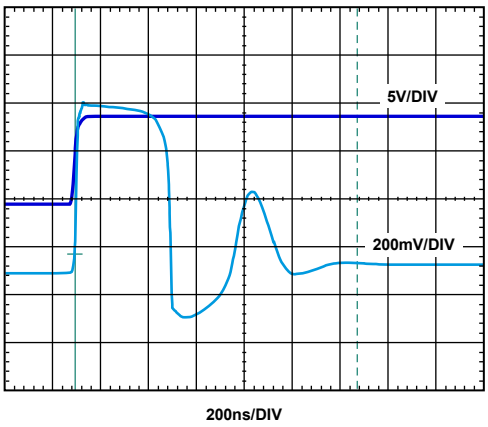


Figure 33. Settling Time Measurement Using the False Summing Node Method

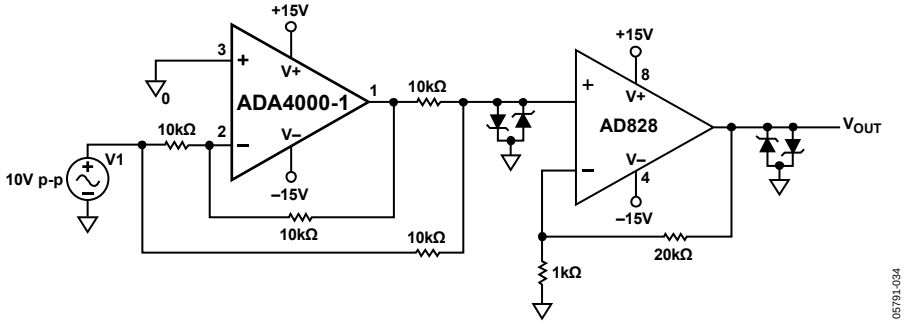
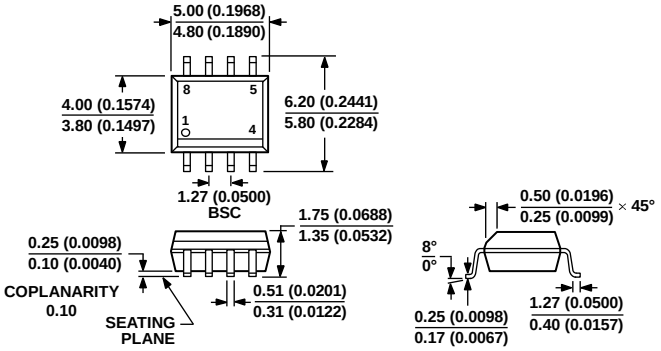


Figure 34. Settling Time Test Circuit

OUTLINE DIMENSIONS



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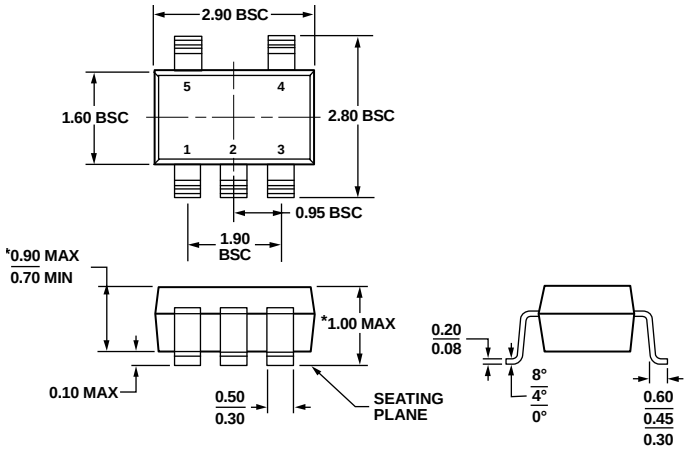
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

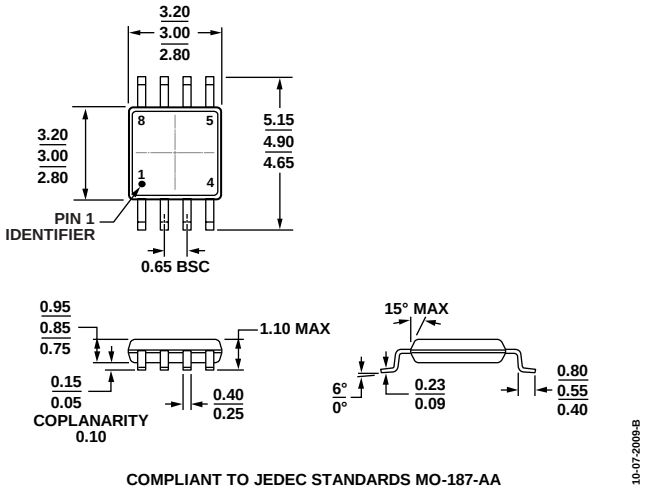
Figure 35. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH
THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

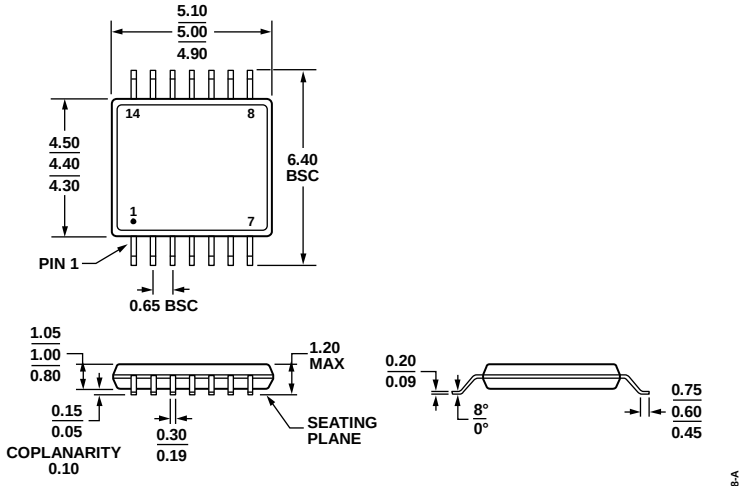
100708-A

Figure 36. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 37. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 38. 14-Lead Standard Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

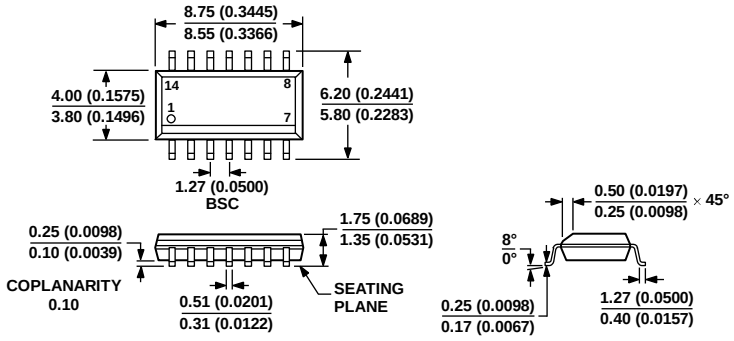


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Figure 39. 14-Lead Standard Small Outline Package [SOIC_N]
(R-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4000-1ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-1ARZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-1ARZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-1AUJZ-R2	−40°C to +125°C	5-Lead TSOT	UJ-5	A14
ADA4000-1AUJZ-R7	−40°C to +125°C	5-Lead TSOT	UJ-5	A14
ADA4000-1AUJZ-RL	−40°C to +125°C	5-Lead TSOT	UJ-5	A14
ADA4000-2ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-2ARZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-2ARZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-2ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	A1H
ADA4000-2ARMZ-RL	−40°C to +125°C	8-Lead MSOP	RM-8	A1H
ADA4000-4ARZ	−40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4000-4ARZ-R7	−40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4000-4ARZ-RL	−40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4000-4ARUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	
ADA4000-4ARUZ-RL	−40°C to +125°C	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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