

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT4015**

**Dual 4-bit serial-in/parallel-out shift register**

Product specification  
File under Integrated Circuits, IC06

December 1990

## Dual 4-bit serial-in/parallel-out shift register

## 74HC/HCT4015

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4015 are high-speed Si-gate CMOS devices and are pin compatible with the "4015" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4015 are dual edge-triggered 4-bit static shift registers (serial-to-parallel converters). Each shift register has a serial data input (1D and 2D), a clock input (1CP and 2CP), four fully buffered parallel outputs (1Q<sub>0</sub> to 1Q<sub>3</sub> and 2Q<sub>0</sub> to 2Q<sub>3</sub>) and an overriding asynchronous master reset (1MR and 2MR). Information present on nD is shifted to the first register position, and all data in the register is shifted one position to the right on the LOW-to-HIGH transition of nCP.

A HIGH on nMR clears the register and forces nQ<sub>0</sub> to nQ<sub>3</sub> to LOW, independent of nCP and nD.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

| SYMBOL                              | PARAMETER                                  | CONDITIONS                                    | TYPICAL |     | UNIT |
|-------------------------------------|--|---|---------|-----|------|
|                                     |  |   | HC      | HCT |      |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay nCP to nQ <sub>n</sub>   | C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V | 16      | 18  | ns   |
| f <sub>max</sub>                    | maximum clock frequency                    |   | 110     | 74  | MHz  |
| C <sub>I</sub>                      | input capacitance                          |   | 3.5     | 3.5 | pF   |
| C <sub>PD</sub>                     | power dissipation capacitance per register | notes 1 and 2                                 | 35      | 40  | pF   |

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

### ORDERING INFORMATION

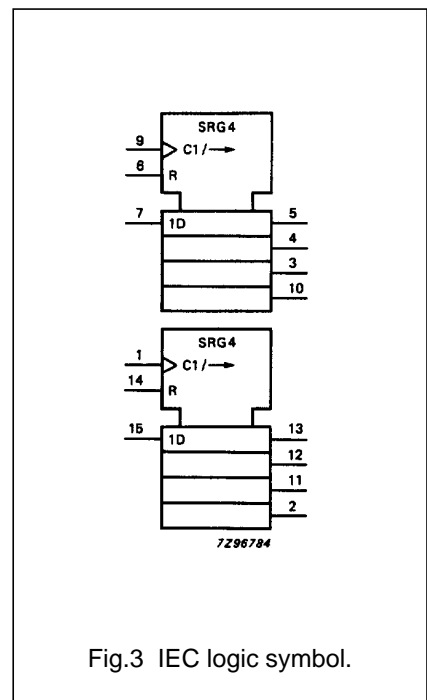
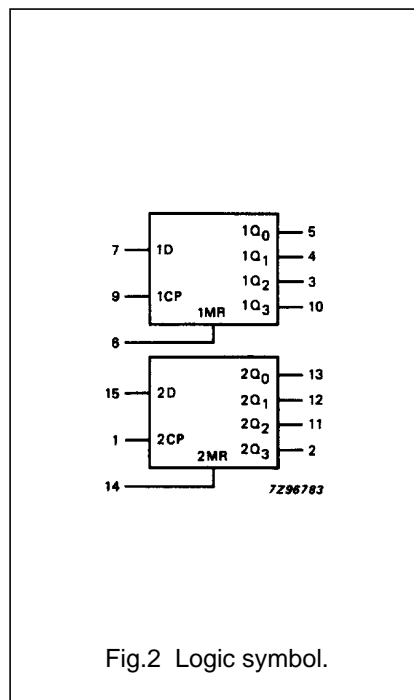
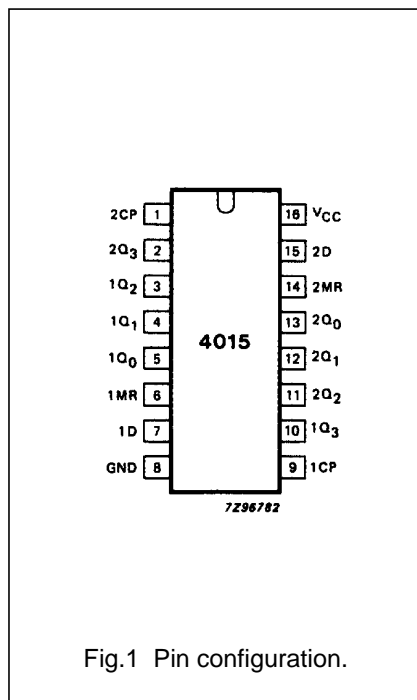
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# Dual 4-bit serial-in/parallel-out shift register

# 74HC/HCT4015

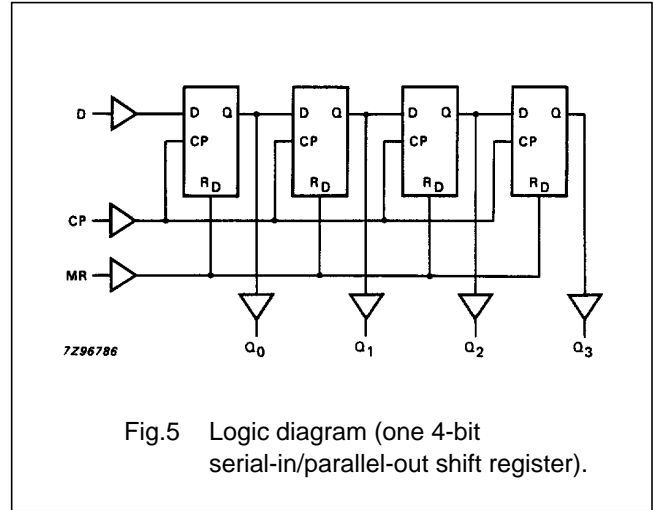
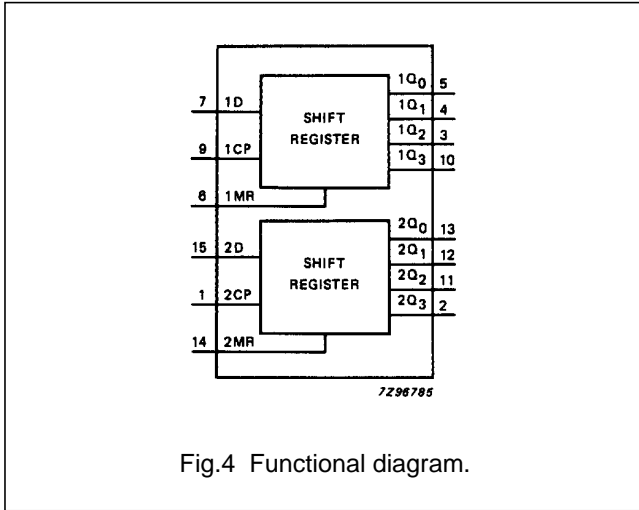
## PIN DESCRIPTION

| PIN NO.       | SYMBOL                             | NAME AND FUNCTION                              |
|---------------|------------------------------------|--|
| 5, 4, 3, 10   | 1Q <sub>0</sub> to 1Q <sub>3</sub> | flip-flop outputs                              |
| 6, 14         | 1MR, 2MR                           | asynchronous master reset inputs (active HIGH) |
| 7, 15         | 1D, 2D                             | serial data inputs                             |
| 8             | GND                                | ground (0 V)                                   |
| 9, 1          | 1CP, 2CP                           | clock inputs (LOW-to-HIGH, edge-triggered)     |
| 13, 12, 11, 2 | 2Q <sub>0</sub> to 2Q <sub>3</sub> | flip-flop outputs                              |
| 16            | V <sub>CC</sub>                    | positive supply voltage                        |



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FUNCTION TABLE

| INPUTS |     |                |     | OUTPUTS         |                 |                 |                 |
|--------|-----|----------------|-----|-----------------|-----------------|-----------------|-----------------|
| n      | nCP | nD             | nMR | nQ <sub>0</sub> | nQ <sub>1</sub> | nQ <sub>2</sub> | nQ <sub>3</sub> |
| 1      | ↑   | D <sub>1</sub> | L   | D <sub>1</sub>  | X               | X               | X               |
| 2      | ↑   | D <sub>2</sub> | L   | D <sub>2</sub>  | D <sub>1</sub>  | X               | X               |
| 3      | ↑   | D <sub>3</sub> | L   | D <sub>3</sub>  | D <sub>2</sub>  | D <sub>1</sub>  | X               |
| 4      | ↑   | D <sub>4</sub> | L   | D <sub>4</sub>  | D <sub>3</sub>  | D <sub>2</sub>  | D <sub>1</sub>  |
|        | ↓   | X              | L   | no change       |                 |                 |                 |
|        | X   | X              | H   | L               | L               | L               | L               |

Notes

- H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH clock transition  
 ↓ = HIGH-to-LOW clock transition  
 n = number of clock pulse transitions  
 D<sub>n</sub> = either HIGH or LOW

APPLICATIONS

- Serial-to-parallel converter
- Buffer stores
- General purpose register

## Dual 4-bit serial-in/parallel-out shift register

## 74HC/HCT4015

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                   | T <sub>amb</sub> (°C) |                  |                 |                 |                 |                 | UNIT            | TEST CONDITIONS        |                   |       |
|-------------------------------------|---|-----------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------|-------------------|-------|
|                                     |   | 74HC                  |                  |                 |                 |                 |                 |                 | V <sub>CC</sub><br>(V) | WAVEFORMS         |       |
|                                     |   | +25                   |                  |                 | -40 to +85      |                 | -40 to +125     |                 |                        |                   |       |
|                                     |   | min.                  | typ.             | max.            | min.            | max.            | min.            |                 |                        |                   | max.  |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nCP to nQ <sub>n</sub> |                       | 52<br>19<br>15   | 175<br>35<br>30 |                 | 220<br>44<br>37 |                 | 265<br>53<br>45 | ns                     | 2.0<br>4.5<br>6.0 | Fig.6 |
| t <sub>PHL</sub>                    | propagation delay<br>nMR to nQ <sub>n</sub> |                       | 44<br>16<br>13   | 175<br>35<br>30 |                 | 220<br>44<br>37 |                 | 265<br>53<br>45 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7 |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                      |                       | 19<br>7<br>6     | 75<br>15<br>13  |                 | 95<br>19<br>16  |                 | 110<br>22<br>19 | ns                     | 2.0<br>4.5<br>6.0 | Fig.6 |
| t <sub>w</sub>                      | clock pulse width<br>HIGH or LOW            | 80<br>16<br>14        | 17<br>6<br>5     |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns                     | 2.0<br>4.5<br>6.0 | Fig.6 |
| t <sub>w</sub>                      | master reset pulse<br>width HIGH            | 80<br>16<br>14        | 17<br>6<br>5     |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7 |
| t <sub>rem</sub>                    | removal time<br>nMR to nCP                  | 60<br>12<br>10        | 17<br>6<br>5     |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  |                 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7 |
| t <sub>su</sub>                     | set-up time<br>nD to nCP                    | 60<br>12<br>10        | 8<br>3<br>2      |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  |                 | ns                     | 2.0<br>4.5<br>6.0 | Fig.8 |
| t <sub>h</sub>                      | hold time<br>nD to nCP                      | 5<br>5<br>5           | 0<br>0<br>0      |                 | 5<br>5<br>5     |                 | 5<br>5<br>5     |                 | ns                     | 2.0<br>4.5<br>6.0 | Fig.8 |
| f <sub>max</sub>                    | maximum clock pulse<br>frequency            | 6.0<br>30<br>35       | 33<br>100<br>119 |                 | 4.8<br>24<br>28 |                 | 4.0<br>20<br>24 |                 | MHz                    | 2.0<br>4.5<br>6.0 | Fig.6 |

## Dual 4-bit serial-in/parallel-out shift register

## 74HC/HCT4015

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-------|-----------------------|
| nD    | 0.30                  |
| nMR   | 1.50                  |
| nCP   | 1.50                  |

**AC CHARACTERISTICS FOR 74HCT**

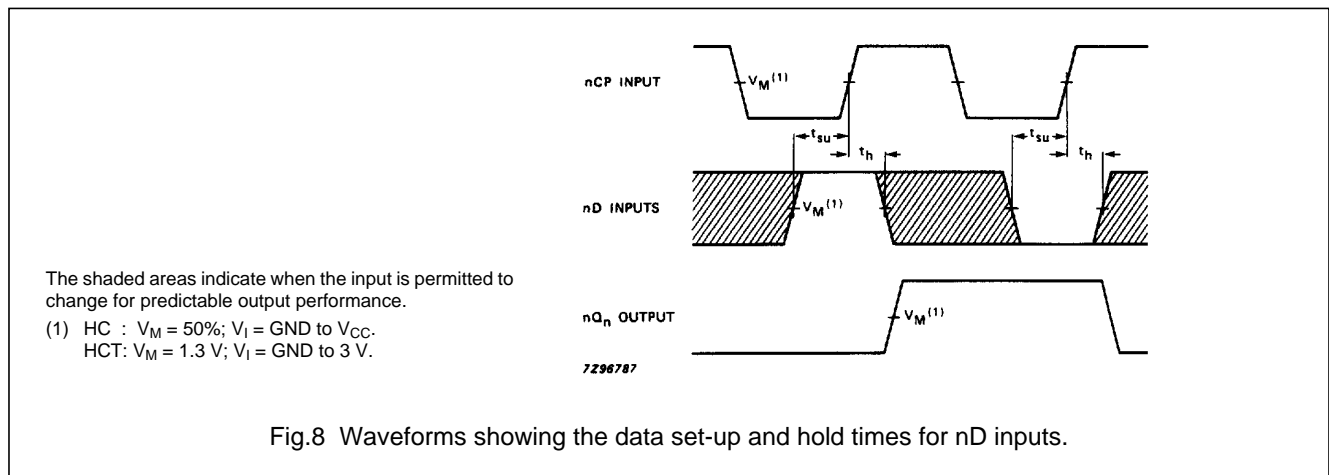
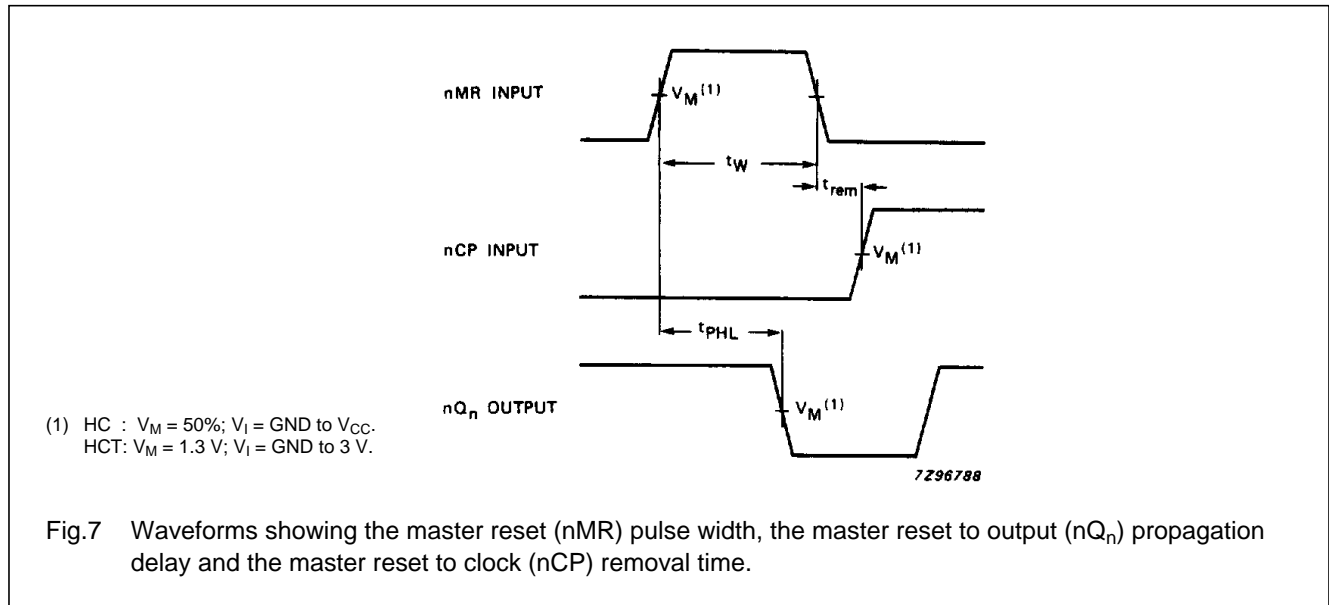
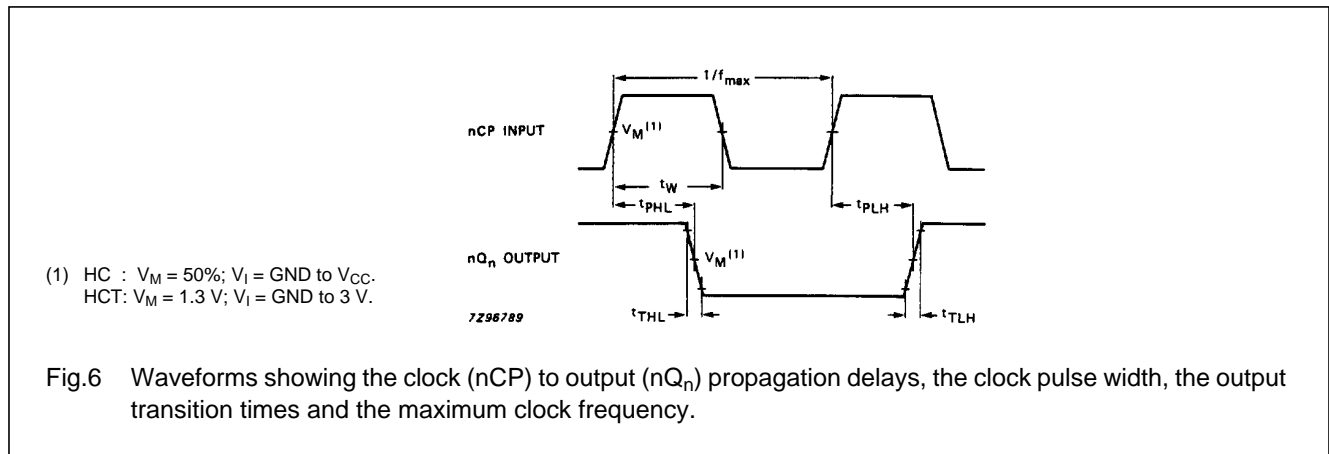
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                              | PARAMETER                                   | T <sub>amb</sub> (°C) |      |      |            |      |                |      |     | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|---|-----------------------|------|------|------------|------|----------------|------|-----|------|------------------------|-----------|
|                                     |   | 74HCT                 |      |      |            |      |                |      |     |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |   | +25                   |      |      | -40 to +85 |      | -40<br>to +125 |      |     |      |                        |           |
|                                     |   | min.                  | typ. | max. | min.       | max. | min.           | max. |     |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nCP to nQ <sub>n</sub> |                       | 21   | 35   |            | 44   |                | 53   | ns  | 4.5  | Fig.6                  |           |
| t <sub>PHL</sub>                    | propagation delay<br>nMR to nQ <sub>n</sub> |                       | 18   | 35   |            | 44   |                | 53   | ns  | 4.5  | Fig.7                  |           |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                      |                       | 7    | 15   |            | 19   |                | 22   | ns  | 4.5  | Fig.6                  |           |
| t <sub>w</sub>                      | clock pulse width<br>HIGH or LOW            | 16                    | 7    |      | 20         |      | 24             |      | ns  | 4.5  | Fig.6                  |           |
| t <sub>w</sub>                      | master reset pulse width<br>HIGH            | 16                    | 5    |      | 20         |      | 24             |      | ns  | 4.5  | Fig.7                  |           |
| t <sub>rem</sub>                    | removal time<br>nMR to nCP                  | 20                    | 10   |      | 25         |      | 30             |      | ns  | 4.5  | Fig.7                  |           |
| t <sub>su</sub>                     | set-up time<br>nD to nCP                    | 12                    | 4    |      | 15         |      | 18             |      | ns  | 4.5  | Fig.8                  |           |
| t <sub>h</sub>                      | hold time<br>nD to nCP                      | 5                     | -2   |      | 5          |      | 5              |      | ns  | 4.5  | Fig.8                  |           |
| f <sub>max</sub>                    | maximum clock pulse<br>frequency            | 30                    | 67   |      | 24         |      | 20             |      | MHz | 4.5  | Fig.6                  |           |

Dual 4-bit serial-in/parallel-out shift register

74HC/HCT4015

AC WAVEFORMS



Dual 4-bit serial-in/parallel-out shift register

74HC/HCT4015

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**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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