



**THE DATASHEET OF
ONET4291PARGVR**



1-Gbps to 4.25-Gbps Rate-Selectable Limiting Amplifier

FEATURES

- Multirate Operation from 1 Gbps up to 4.25 Gbps
- Loss-of-Signal Detection (LOS)
- Two-Wire Digital Interface
- Digitally Selectable LOS Threshold
- Digitally Selectable Bandwidth
- Digitally Selectable Output Voltage
- Low Power Consumption
- Input Offset Cancellation

- CML Data Outputs With On-Chip, 50- Ω Back-Termination to V_{CC}
- Single 3.3-V Supply
- Surface-Mount, Small-Footprint, 4-mm \times 4-mm, 16-Terminal QFN Package

APPLICATIONS

- Multirate SONET/SDH Transmission Systems
- 4.25-Gbps, 2.125-Gbps, and 1.0625-Gbps Fibre-Channel Receivers
- Gigabit Ethernet Receivers

DESCRIPTION

The ONET4291PA is a versatile, high-speed, rate-selectable limiting amplifier for multiple fiber-optic applications with data rates up to 4.25 Gbps.

The device provides a two-wire interface, which allows digital bandwidth selection, digital output amplitude selection, and digital loss of signal threshold adjust.

This device provides a gain of about 43 dB, which ensures a fully differential output swing for input signals as low as 5 mV_{p-p}.

The ONET4291PA provides loss-of-signal detection with either digital or analog threshold adjust.

The part is available in a small-footprint, 4-mm \times 4-mm, 16-terminal QFN package. It requires a single 3.3-V supply.

This power-efficient, rate-selectable limiting amplifier is characterized for operation from -40°C to 85°C ambient temperature.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

BLOCK DIAGRAM

A simplified block diagram of the ONET4291PA is shown in Figure 1.

This compact, 3.3-V, low-power, 1-Gbps to 4.25-Gbps rate-selectable limiting amplifier consists of a high-speed data path with offset cancellation block (dc feedback), a loss-of-signal detection block using two peak detectors, a programmable resistor, a two-wire interface and control-logic block, and a band-gap voltage reference and bias-current generation block.

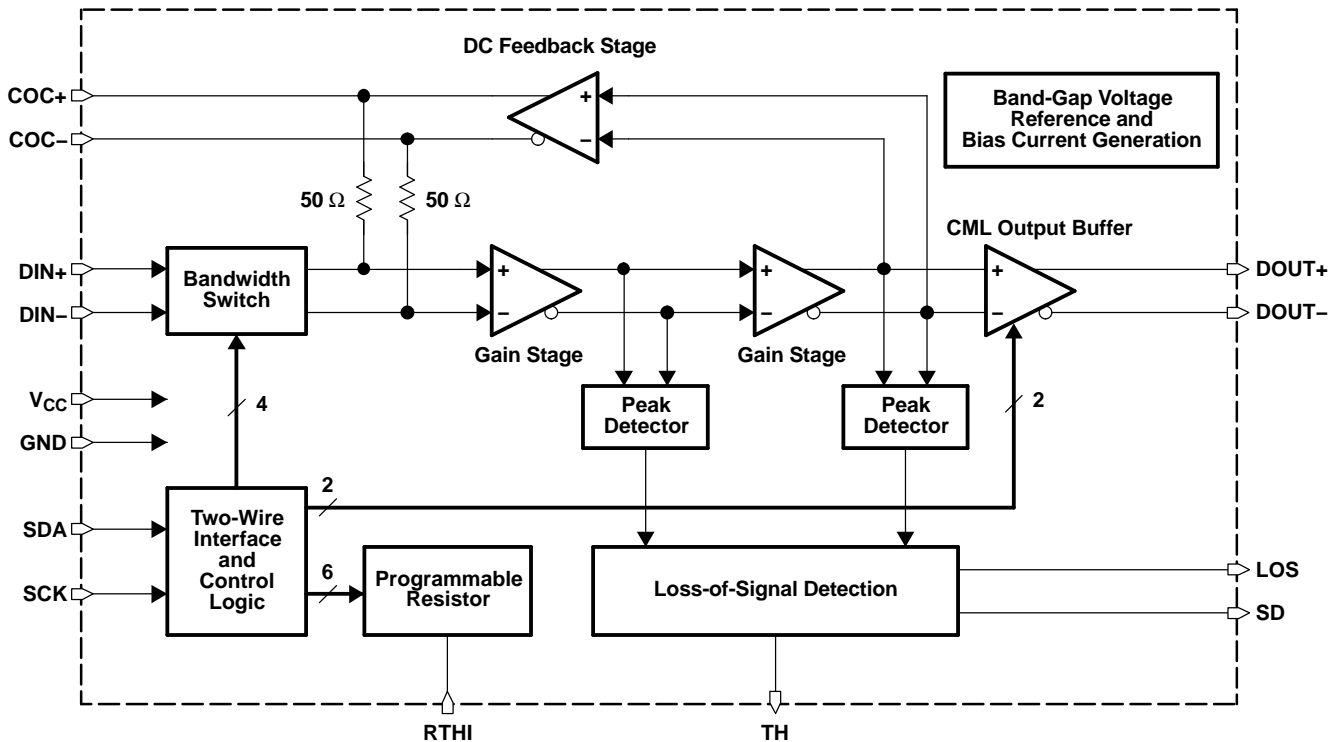


Figure 1. Simplified Block Diagram of the ONET4291PA

B0067-01

HIGH-SPEED DATA PATH

The high-speed data signal is applied to the data path by means of the input signal terminals DIN+ and DIN-. The data path consists of a digitally controllable bandwidth switch followed by two 50- Ω on-chip line termination resistors; two gain stages, which provide a typical gain of about 37 dB; and a CML output stage, which provides another 6-dB gain. The amplified data-output signal is available at the output terminals DOUT+ and DOUT-, which feature on-chip $2 \times 50\text{-}\Omega$ back-termination to V_{CC} .

A dc feedback stage compensates for internal offset voltages and thus ensures proper operation even for small input data signals. This stage is driven by the output signal of the second gain stage. The signal is low-pass filtered, amplified, and fed back to the input of the first gain stage via the on-chip 50- Ω termination resistors. The required low-frequency cutoff is determined by an external 0.1- μF capacitor, which must be differentially connected to the COC+ and COC- terminals.

LOSS-OF-SIGNAL DETECTION AND PROGRAMMABLE RESISTOR

The peak values of the output signals of the first and second gain stages are monitored by two peak detectors. The peak values are compared to a predefined loss-of-signal threshold voltage inside the loss-of-signal detection block. As a result of the comparison, the loss-of-signal detection block generates the SD signal, which indicates a sufficient input-signal amplitude, or the LOS signal, which indicates that the input signal amplitude is below the defined threshold level.

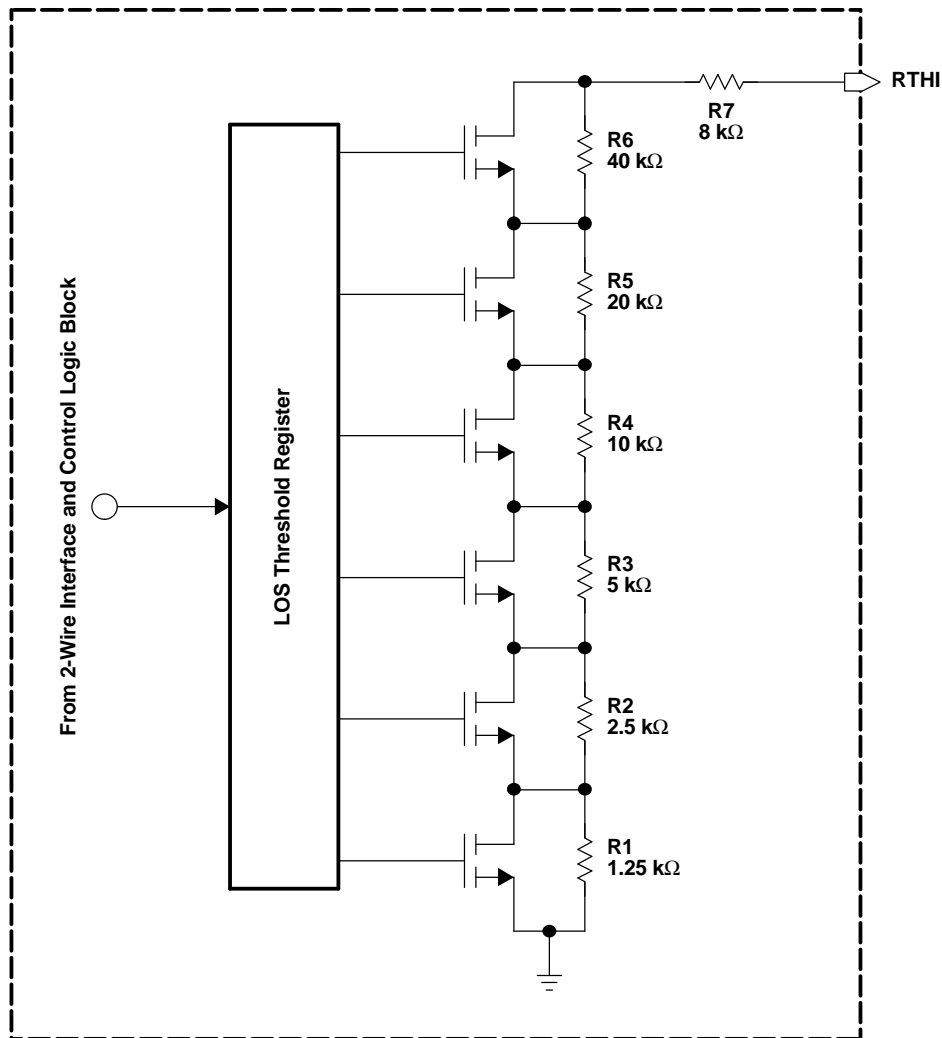
The threshold voltage can be set within a certain range by means of an external resistor connected between the TH terminal and ground (GND). Alternatively, shorting the TH and RTHI terminals causes an internal, digitally selectable resistor to be used for threshold adjustment. The resistor value is selectable using the two-wire interface.

The principle of the digitally selectable resistor is shown in Figure 2. The complete resistor between the RTHI terminal and GND consists of seven series-connected resistors.

Six of the resistors have binary-weighted resistance values, and each can be shunted individually by means of a parallel-connected MOS transistor.

The seventh resistor defines the minimum remaining resistance in case all six MOS devices are conductive.

With the resistor values shown in Figure 2, the minimum selectable resistance is 8 k Ω , the maximum resistance is 86.75 k Ω , and the resolution is 1.25 k Ω /step.



S0098-01

Figure 2. Digitally Controllable On-Chip Resistor

TWO-WIRE INTERFACE AND CONTROL LOGIC

The ONET4291PA uses a two-wire serial interface for digital control of the amplifier bandwidth, output amplitude, and LOS threshold. A simplified block diagram of this interface is given in [Figure 3](#).

SDA and SCK are inputs for the serial data and the serial clock, respectively, and can be driven by a microprocessor. Both inputs have 100-k Ω pullup resistors to V_{CC} . For driving these inputs, an open-drain output is recommended.

A write cycle consists of a START command, 3 address bits with MSB first, 8 data bits with MSB first, and a STOP command. In idle mode, both the SDA and SCK lines are at a high level.

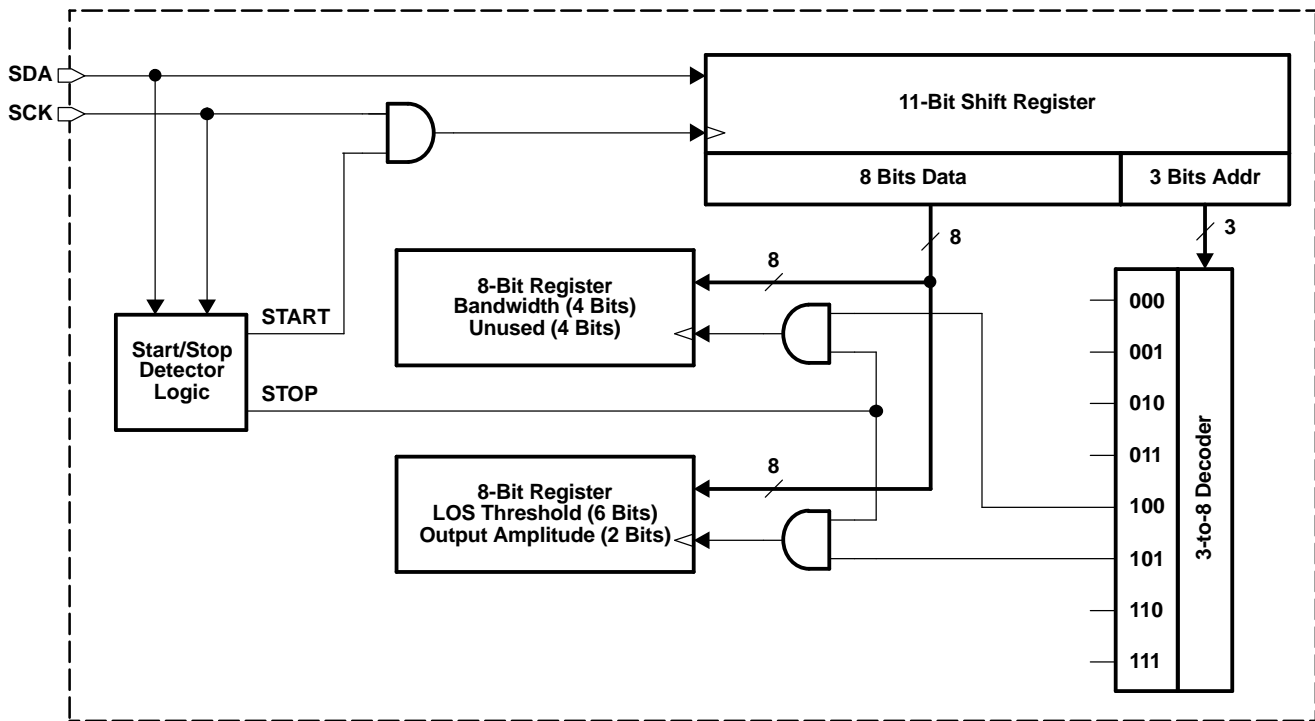
A START command is initiated by a falling edge on SDA with SCK at a high level.

Bits are clocked into an 11-bit-wide shift register while the SCK level is high.

A STOP command is detected on the rising edge of SDA after SCK has changed from a low level to a high level.

At the time of detection of a STOP command, the 8 data bits from the shift register are copied to a selected 8-bit register. Register selection occurs according to the 3 address bits in the shift register, which are decoded to 8 independent select signals using a 3-to-8 decoder block.

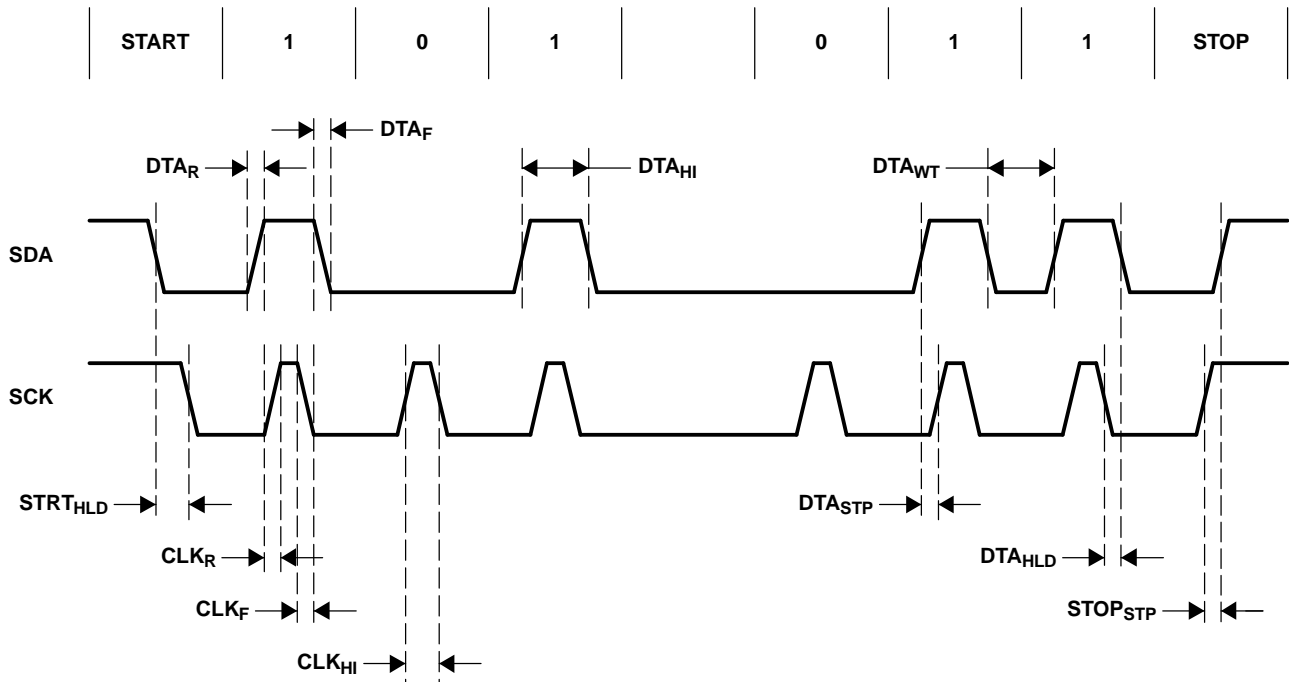
In the ONET4291PA, only addresses 4 (100b) and 5 (101b) are used.



B0068-01

Figure 3. Simplified Two-Wire Interface Block Diagram

The timing definition for the serial data signal SDA and the serial clock signal SCK is shown in Figure 4.



T0077-01

PARAMETER		DESCRIPTION	MIN	MAX	UNIT
STRT _{HLD}	START hold time	Time required from data falling edge to clock falling edge at START	10		ns
CLK _R , DTA _R	Clock and data rise time	Clock and data rise time		10	ns
CLK _F , DTA _F	Clock and data fall time	Clock and data fall time		10	ns
CLK _{HI}	Clock high time	Minimum clock high period	50		ns
DTA _{HI}	Data high time	Minimum data high period	100		ns
DTA _{STP}	Data setup time	Minimum time from data rising edge to clock rising edge	10		ns
DTA _{WT}	Data wait time	Minimum time from data falling edge to data rising edge	50		ns
DTA _{HLD}	Data hold time	Minimum time from clock falling edge to data falling edge	10		ns
STOP _{STP}	STOP setup time	Minimum time from clock rising edge to data rising edge at STOP	10		ns

Figure 4. Two-Wire Interface Timing Diagram

The register mapping for register addresses 4 (100b) and 5 (101b) is shown in Table 1 and Table 2, respectively.

Table 1. Register 4 (100b) Mapping

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BW3	BW2	BW1	BW0	–	–	–	–

Table 2. Register 5 (101b) Mapping

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
A1	A0	R5	R4	R3	R2	R1	R0

Table 3 through Table 5 describe circuit functionality based on the register settings.

Table 3. Bandwidth Selection

BW3	BW2	BW1	BW0	TYP	UNIT
0	0	0	0	4.39	GHz
0	0	0	1	3.91	GHz
0	0	1	0	3.47	GHz
0	0	1	1	3.03	GHz
0	1	0	0	2.81	GHz
0	1	0	1	2.31	GHz
0	1	1	0	1.82	GHz
0	1	1	1	1.60	GHz
1	0	0	0	1.55	GHz
1	0	0	1	1.33	GHz
1	0	1	0	1.11	GHz
1	0	1	1	1.03	GHz
1	1	0	0	0.86	GHz
1	1	0	1	0.82	GHz
1	1	1	0	0.76	GHz
1	1	1	1	0.73	GHz

Table 4. Output Amplitude Selection

A1	A0	TYP	UNIT
0	0	400	mV _{p-p}
0	1	600	mV _{p-p}
1	0	800	mV _{p-p}
1	1	1000	mV _{p-p}

Table 5. LOS-Threshold Digitally Controlled Resistor Selection

R5	R4	R3	R2	R1	R0	TYP	UNIT
0	0	0	0	0	0	86.75	kΩ
0	0	0	0	0	1	85.5	kΩ
0	0	0	0	1	0	84.25	kΩ
0	0	0	0	1	1	83	kΩ
0	0	0	1	0	0	81.75	kΩ
0	0	0	1	0	1	80.5	kΩ
0	0	0	1	1	0	79.25	kΩ
0	0	0	1	1	1	78	kΩ
0	0	1	0	0	0	76.75	kΩ
0	0	1	0	0	1	75.5	kΩ
0	0	1	0	1	0	74.25	kΩ
0	0	1	0	1	1	73	kΩ
0	0	1	1	0	0	71.75	kΩ
0	0	1	1	0	1	70.5	kΩ
0	0	1	1	1	0	69.25	kΩ
0	0	1	1	1	1	68	kΩ
0	1	0	0	0	0	66.75	kΩ
0	1	0	0	0	1	65.5	kΩ
0	1	0	0	1	0	64.25	kΩ
0	1	0	0	1	1	63	kΩ
0	1	0	1	0	0	61.75	kΩ

Table 5. LOS-Threshold Digitally Controlled Resistor Selection (continued)

R5	R4	R3	R2	R1	R0	TYP	UNIT
0	1	0	1	0	1	60.5	kΩ
0	1	0	1	1	0	59.25	kΩ
0	1	0	1	1	1	58	kΩ
0	1	1	0	0	0	56.75	kΩ
0	1	1	0	0	1	55.5	kΩ
0	1	1	0	1	0	54.25	kΩ
0	1	1	0	1	1	53	kΩ
0	1	1	1	0	0	51.75	kΩ
0	1	1	1	0	1	50.5	kΩ
0	1	1	1	1	0	49.25	kΩ
0	1	1	1	1	1	48	kΩ
1	0	0	0	0	0	46.75	kΩ
1	0	0	0	0	1	45.5	kΩ
1	0	0	0	1	0	44.25	kΩ
1	0	0	0	1	1	43	kΩ
1	0	0	1	0	0	41.75	kΩ
1	0	0	1	0	1	40.5	kΩ
1	0	0	1	1	0	39.25	kΩ
1	0	0	1	1	1	38	kΩ
1	0	1	0	0	0	36.75	kΩ
1	0	1	0	0	1	35.5	kΩ
1	0	1	0	1	0	34.25	kΩ
1	0	1	0	1	1	33	kΩ
1	0	1	1	0	0	31.75	kΩ
1	0	1	1	0	1	30.5	kΩ
1	0	1	1	1	0	29.25	kΩ
1	0	1	1	1	1	28	kΩ
1	1	0	0	0	0	26.75	kΩ
1	1	0	0	0	1	25.5	kΩ
1	1	0	0	1	0	24.25	kΩ
1	1	0	0	1	1	23	kΩ
1	1	0	1	0	0	21.75	kΩ
1	1	0	1	0	1	20.5	kΩ
1	1	0	1	1	0	19.25	kΩ
1	1	0	1	1	1	18	kΩ
1	1	1	0	0	0	16.75	kΩ
1	1	1	0	0	1	15.5	kΩ
1	1	1	0	1	0	14.25	kΩ
1	1	1	0	1	1	13	kΩ
1	1	1	1	0	0	11.75	kΩ
1	1	1	1	0	1	10.5	kΩ
1	1	1	1	1	0	9.25	kΩ
1	1	1	1	1	1	8	kΩ

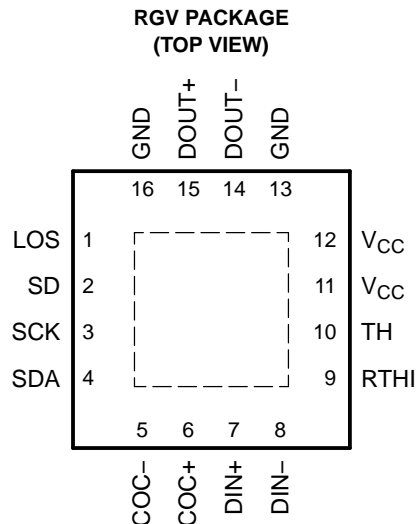
BAND-GAP VOLTAGE AND BIAS GENERATION

The ONET4291PA limiting amplifier is supplied by a single, 3.3-V supply voltage connected to the V_{CC} terminals. This voltage is referred to GND.

On-chip band-gap voltage circuitry generates a reference voltage, independent of supply voltage, from which all other internally required voltages and bias currents are derived.

TERMINAL ASSIGNMENTS

For the ONET4291PA, a small-footprint 4-mm × 4-mm, 16-terminal QFN package is used, with a terminal pitch of 0,65 mm.



P0030-01

TERMINAL DESCRIPTION

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
COC+	6	Analog	Offset cancellation filter capacitor plus terminal. An external 0.1- μ F filter capacitor must be connected between this terminal and COC– (terminal 5).
COC–	5	Analog	Offset cancellation filter capacitor minus terminal. An external 0.1- μ F filter capacitor must be connected between this terminal and COC+ (terminal 6).
DIN+	7	Analog input	Non-inverted data input. On-chip 50- Ω terminated to COC+. Differentially 100- Ω terminated to DIN–.
DIN–	8	Analog input	Inverted data input. On-chip 50- Ω terminated to COC–. Differentially 100- Ω terminated to DIN+.
DOUT+	15	CML output	Non-inverted data output. On-chip 50- Ω back-terminated to V_{CC} .
DOUT–	14	CML output	Inverted data output. On-chip 50- Ω back-terminated to V_{CC} .
GND	13, 16, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
LOS	1	Open-drain MOS	High level indicates that the input signal amplitude is below the programmed threshold level. Open-drain output. Requires an external 10-k Ω pullup resistor to V_{CC} for proper operation.
RTHI	9	Analog	Digitally controlled internal resistor to ground, which can be used for LOS threshold adjustment. A 6-bit-wide control register can be set via the two-wire interface.
SCK	3	CMOS input	Two-wire interface serial clock. Includes a 100-k Ω pullup resistor to V_{CC} .
SD	2	CMOS output	High level indicates that sufficient input signal amplitude is applied to the device. Low level indicates that the input signal amplitude is below the programmed threshold level.
SDA	4	CMOS input	Two-wire interface serial data input. Includes a 100-k Ω pullup resistor to V_{CC} .
TH	10	Analog input	LOS threshold adjustment with resistor to GND. For use of the internal digitally controlled resistor, connect TH with RTHI (terminal 9).
V_{CC}	11, 12	Supply	3.3-V, +10%/–12% supply voltage

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

V_{CC}	Supply voltage ⁽²⁾	–0.3 V to 4 V
V_{DIN+} , V_{DIN-}	Voltage at DIN+, DIN– ⁽²⁾	0.5 V to 4 V
V_{LOS} , V_{SD} , V_{SCK} , V_{SDA} , V_{COC+} , V_{COC-} , V_{RTHI} , V_{TH} , V_{DOUT+} , V_{DOUT-}	Voltage at LOS, SD, SCK, SDA, COC+, COC–, RTHI, TH, DOUT+, DOUT– ⁽²⁾	–0.3 V to 4 V
$V_{DIN,DIFF}$	Differential voltage between DIN+ and DIN–	±1.25 V
I_{LOS}	Current into LOS	10 mA
I_{DIN+} , I_{DIN-} , I_{DOUT+} , I_{DOUT-}	Continuous current at inputs and outputs	20 mA
ESD	ESD rating at all terminals (HBM)	4 kV
$T_{J,max}$	Maximum junction temperature	125°C
T_{stg}	Storage temperature range	–65°C to 85°C
T_A	Characterized free-air operating temperature range	–40°C to 85°C
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC} , V_{CCO}	Supply voltage	2.9	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C
	CMOS input high voltage	2			V
	CMOS input low voltage			0.8	V

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} , V_{CCO}	Supply voltage		2.9	3.3	3.6	V
I_{VCC}	Supply current ⁽¹⁾	$V_{OD} = 1000$ mV _{p-p} , maximum bandwidth selected	35	50	64	mA
		$V_{OD} = 800$ mV _{p-p} , maximum bandwidth selected	32	46	59	
		$V_{OD} = 600$ mV _{p-p} , maximum bandwidth selected	28	41	53	
		$V_{OD} = 400$ mV _{p-p} , maximum bandwidth selected	24	36	48	
R_{IN} , R_{OUT}	Data input/output resistance	Single-ended		50		Ω
	CMOS output high voltage	$I_{SINK} = 1$ mA	2.3			V
	CMOS output low voltage	$I_{SOURCE} = 1$ mA			0.5	V
	LOS low voltage	$I_{SOURCE} = 1.5$ mA			0.5	V
	Optimum LOS threshold resistor		12		62	kΩ

- (1) Use of the bandwidth select switch increases current consumption. The MSB bandwidth-select bit, BW3, typically consumes 5 mA, BW2 2.6 mA, BW1 1.3 mA, and BW0 0.7 mA.

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{3dB-H}	High-frequency –3-dB bandwidth	Maximum bandwidth selected (BW3 = BW2 = BW1 = BW0 = 0)	3.5	4.5	6	GHz
		Minimum bandwidth selected (BW3 = BW2 = BW1 = BW0 = 1)	0.7			
f_{3dB-L}	Low-frequency –3-dB bandwidth	$C_{OC} = 0.1\ \mu\text{F}$		23	50	kHz
	Data rate	Maximum bandwidth selected (BW3 = BW2 = BW1 = BW0 = 0)	4.25			Gbps
$V_{IN,MIN}$	Data input sensitivity	K28.5 at 4.25 Gbps, BER < 10^{-12} (noise limited)		1.9	2.7	mV _{p-p}
		$V_{OD-min} \geq 0.95 * V_{OD}$ (at $V_{IN} = 25\text{ mV}_{p-p}$) (gain limited)		8	14	
A	Small-signal gain		38	43	46	dB
	Small-signal gain vs temperature				2.5	dB
	Small-signal gain vs supply voltage V_{CC}				1	dB
$V_{IN,MAX}$	Data input overload		2000			mV _{p-p}
DJ	Deterministic jitter	$V_{IN} = 5\text{ mV}_{p-p}$, K28.5 at 4.25 Gbps, maximum bandwidth		10	18	ps _{p-p}
		$V_{IN} = 10\text{ mV}_{p-p}$, K28.5 at 4.25 Gbps, maximum bandwidth		9	17	
		$V_{IN} = 25\text{ mV}_{p-p}$, K28.5 at 4.25 Gbps, maximum bandwidth		8	15	
RJ	Random jitter	Input = 5 mV_{p-p} , maximum bandwidth		3		ps _{RMS}
		Input = 10 mV_{p-p} , maximum bandwidth		1.5		
V_{OD}	Differential-data output voltage	800-mV output amplitude selected (default), $V_{IN} > 25\text{ mV}_{p-p}$	700	850	1000	mV _{p-p}
t_R	Output rise time	20% to 80%, $V_{IN} > 25\text{ mV}_{p-p}$, maximum bandwidth		45	90	ps
t_F	Output fall time	20% to 80%, $V_{IN} > 25\text{ mV}_{p-p}$, maximum bandwidth		45	90	ps
V_{TH}	LOS assert threshold range	K28.5 pattern at 4.25 Gbps, $R_{TH} = 62\text{ k}\Omega$		5.5		mV _{p-p}
		K28.5 pattern at 4.25 Gbps, $R_{TH} = 12\text{ k}\Omega$		30		
	LOS threshold variation vs temperature			1		dB
	LOS threshold variation vs supply voltage V_{CC}				1.5	dB
	LOS hysteresis	K28.5 pattern at 4.25 Gbps	2		7.4	dB
T_{LOS_AST}	LOS assert time		400		1500	ns
T_{LOS_DEA}	LOS deassert time		15		80	ns

TYPICAL CHARACTERISTICS

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$.

FREQUENCY RESPONSE FOR DIFFERENT BANDWIDTH SETTINGS

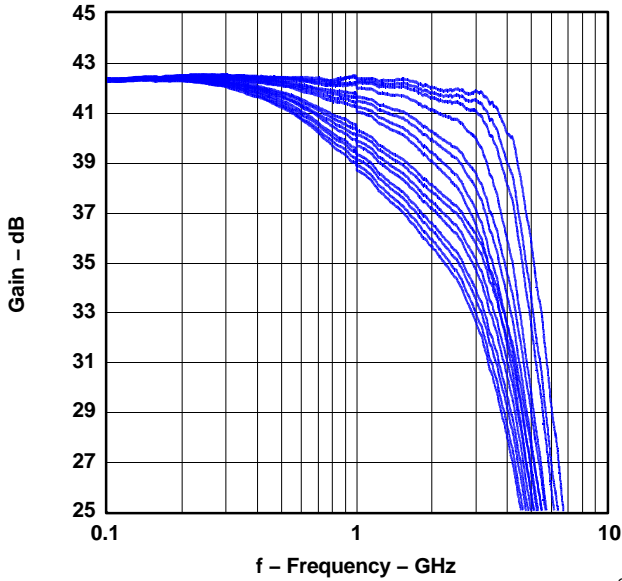


Figure 5.

G001

BANDWIDTH VS REGISTER-4 SETTING

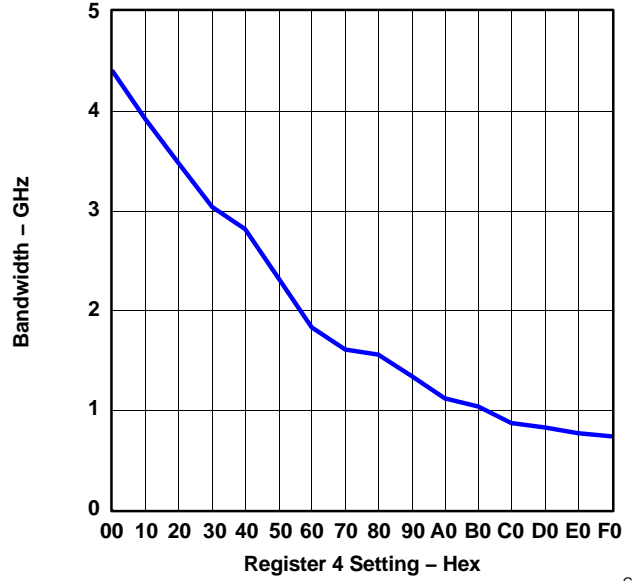


Figure 6.

G002

DIFFERENTIAL INPUT RETURN GAIN VS FREQUENCY (MAXIMUM BANDWIDTH)

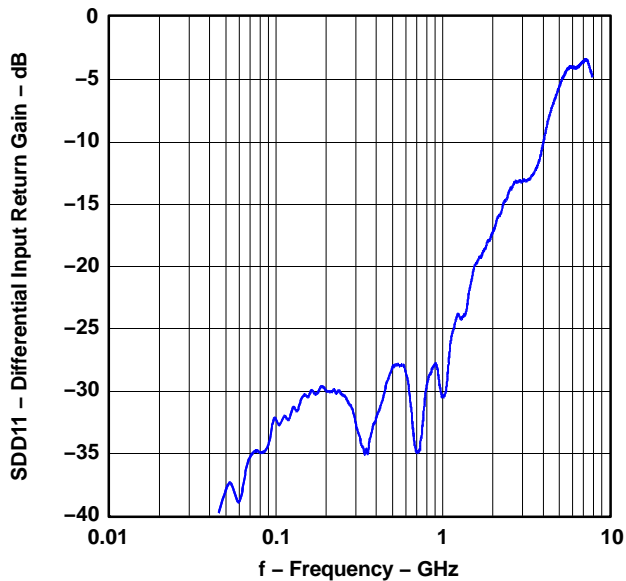


Figure 7.

G003

RANDOM JITTER VS INPUT AMPLITUDE (4.25 Gbps, MAXIMUM BANDWIDTH)

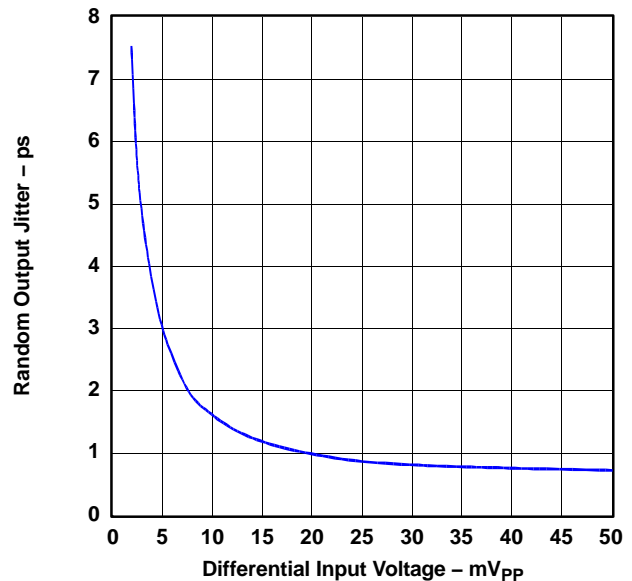


Figure 8.

G004

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$.

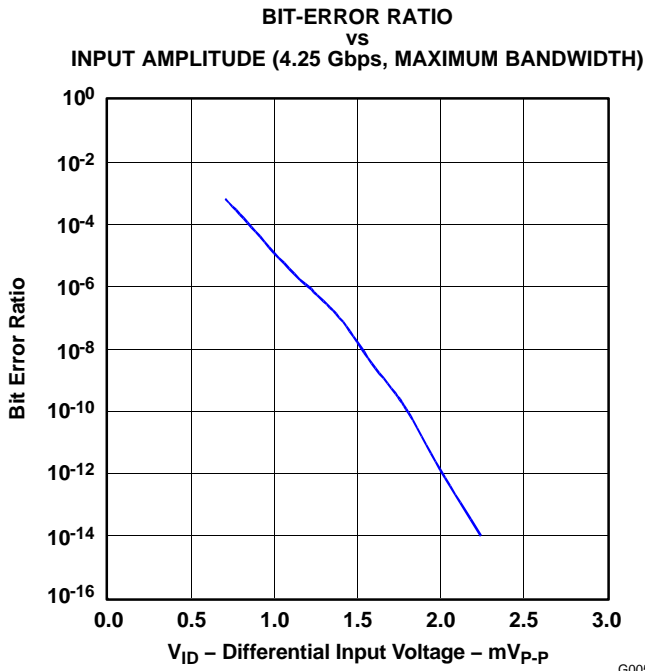


Figure 9.

G005

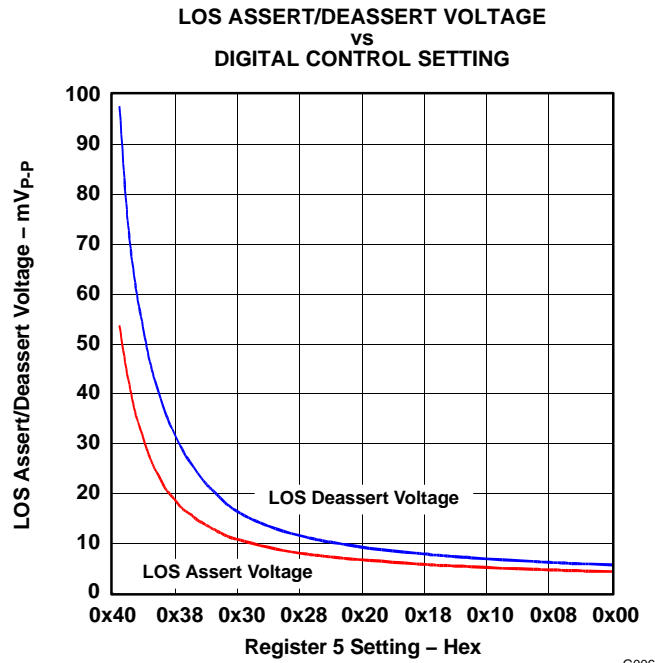


Figure 10.

G006

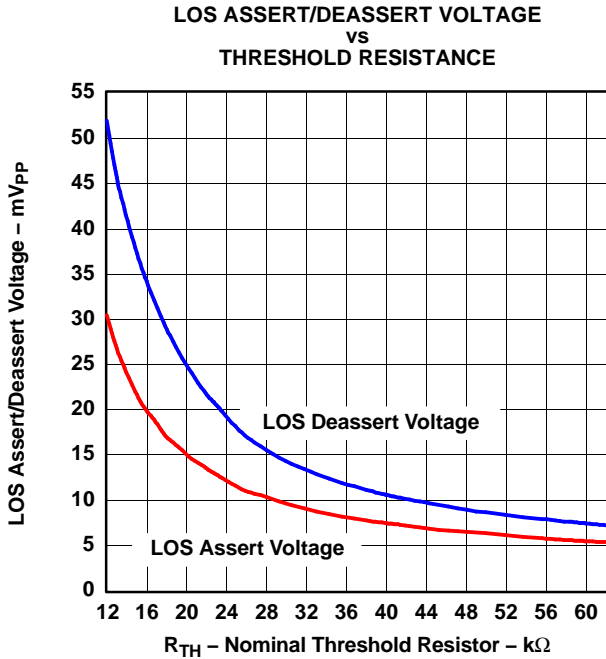


Figure 11.

G013

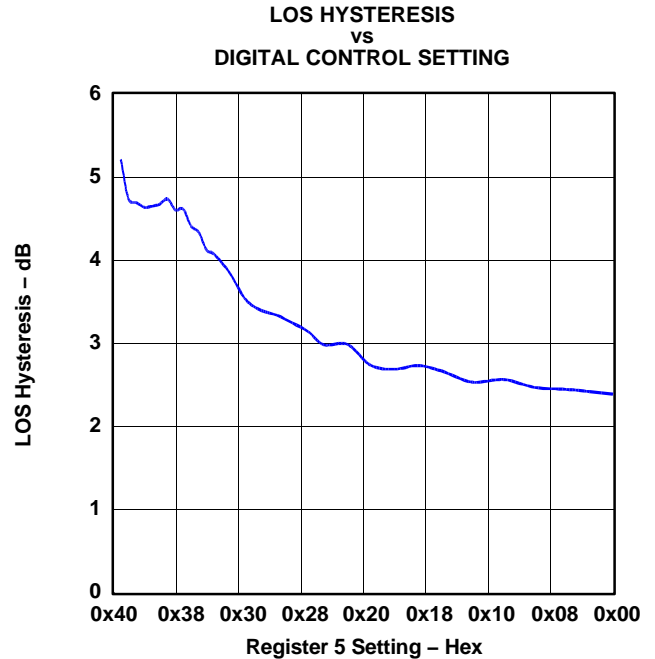


Figure 12.

G007

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$.

**LOS HYSTERESIS
vs
THRESHOLD RESISTANCE**

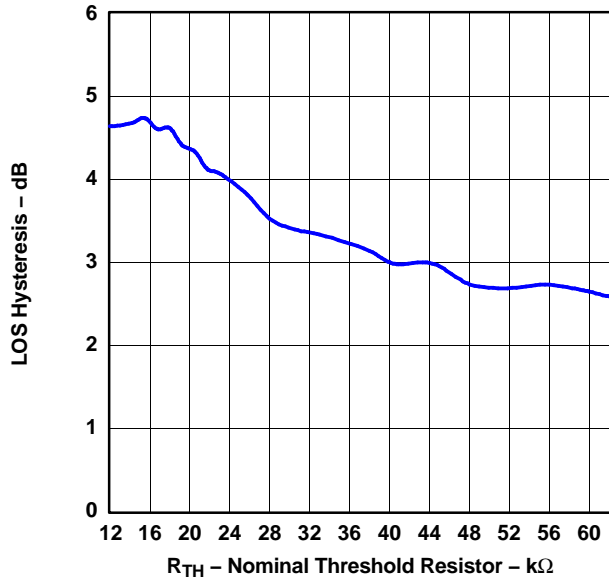


Figure 13.

G014

**LOS THRESHOLD VARIATION OVER TEMPERATURE
vs
DIGITAL CONTROL SETTING**

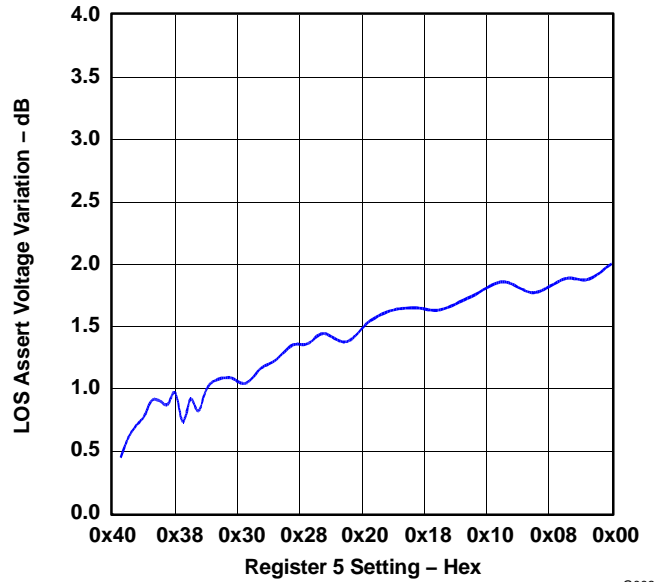


Figure 14.

G008

**OUTPUT EYE DIAGRAM AT 4.25 Gbps
AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})
(K28.5 PATTERN, MAXIMUM BANDWIDTH)**

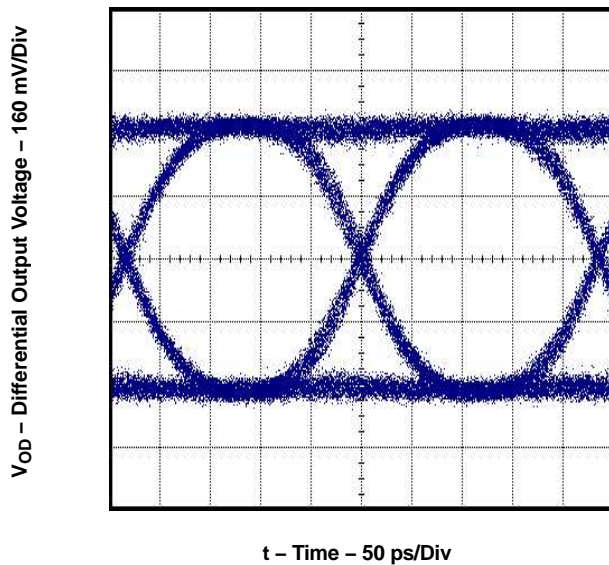


Figure 15.

G009

**OUTPUT EYE DIAGRAM AT 4.25 Gbps
AND MAXIMUM INPUT VOLTAGE (2000 mV_{p-p})
(K28.5 PATTERN, MAXIMUM BANDWIDTH)**

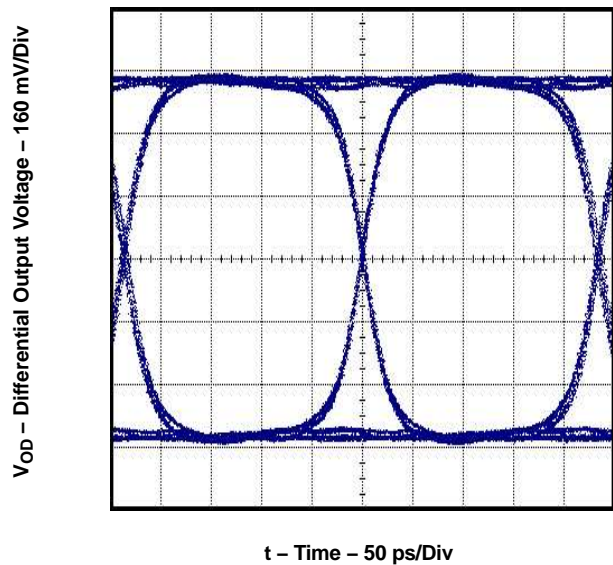


Figure 16.

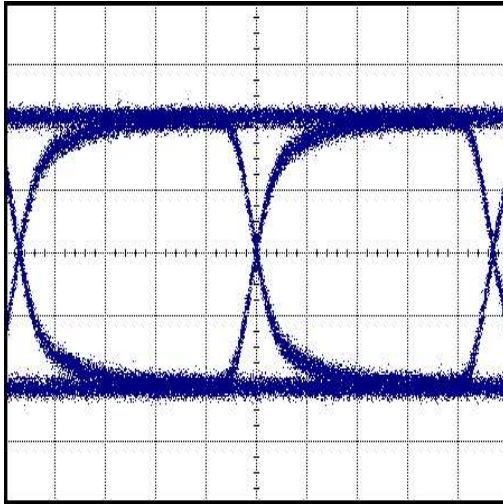
G010

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$.

**OUTPUT EYE DIAGRAM AT 1.0625 Gbps
AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})
(K28.5 PATTERN, REGISTER 4 SET TO 0x70)**

V_{OD} – Differential Output Voltage – 160 mV/Div



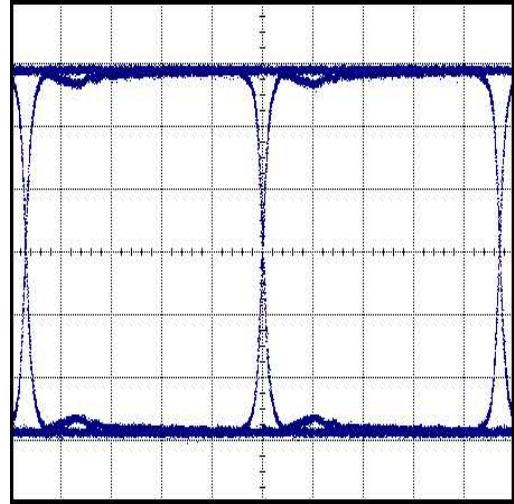
t – Time – 200 ps/Div

G011

Figure 17.

**OUTPUT EYE DIAGRAM AT 1.0625 Gbps
AND MAXIMUM INPUT VOLTAGE (2000 mV_{p-p})
(K28.5 PATTERN, REGISTER 4 SET TO 0x70)**

V_{OD} – Differential Output Voltage – 160 mV/Div



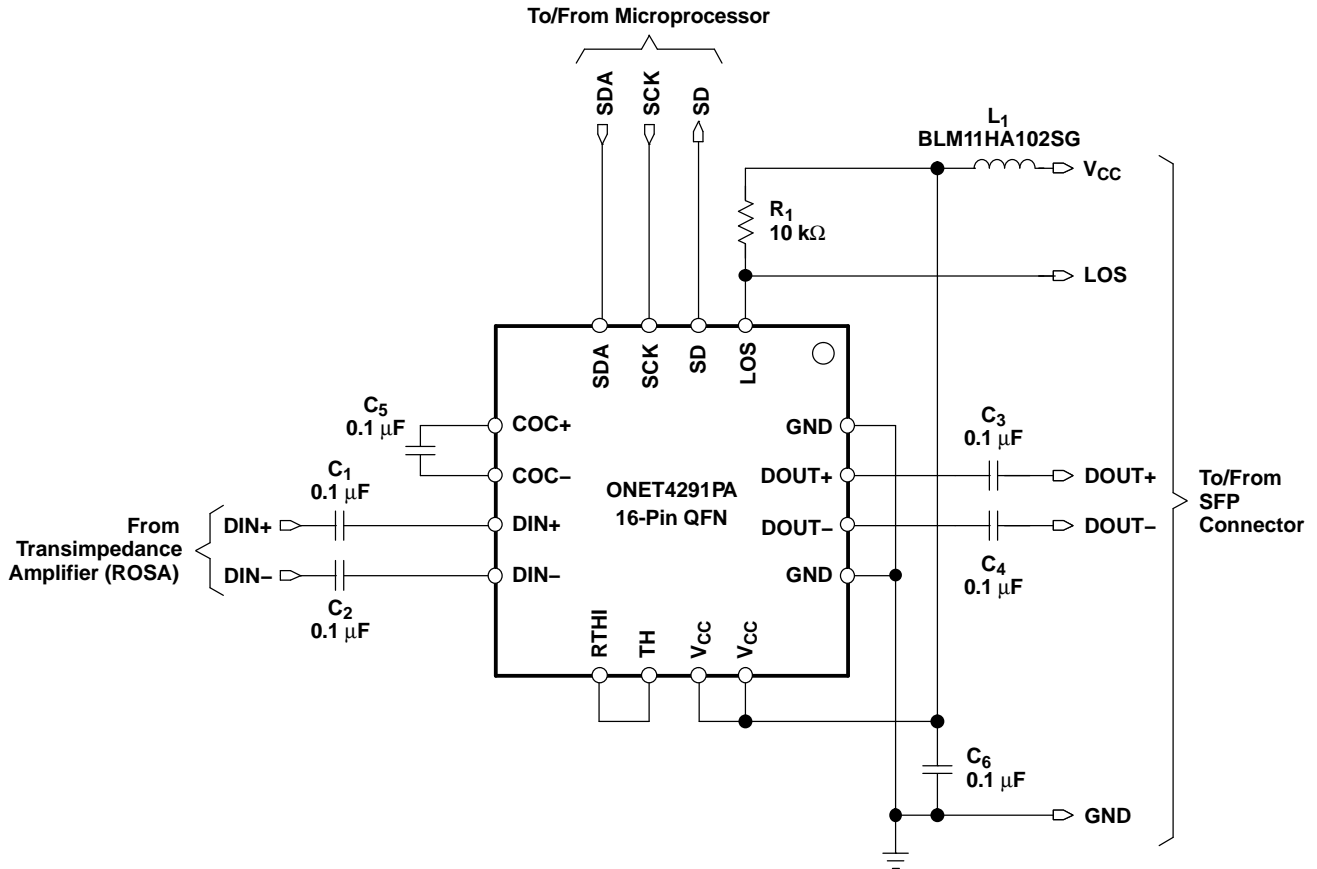
t – Time – 200 ps/Div

G012

Figure 18.

APPLICATION INFORMATION

Figure 19 shows a typical application circuit using the ONET4291PA with a microprocessor for digital control of the LOS threshold, output amplitude, and bandwidth.

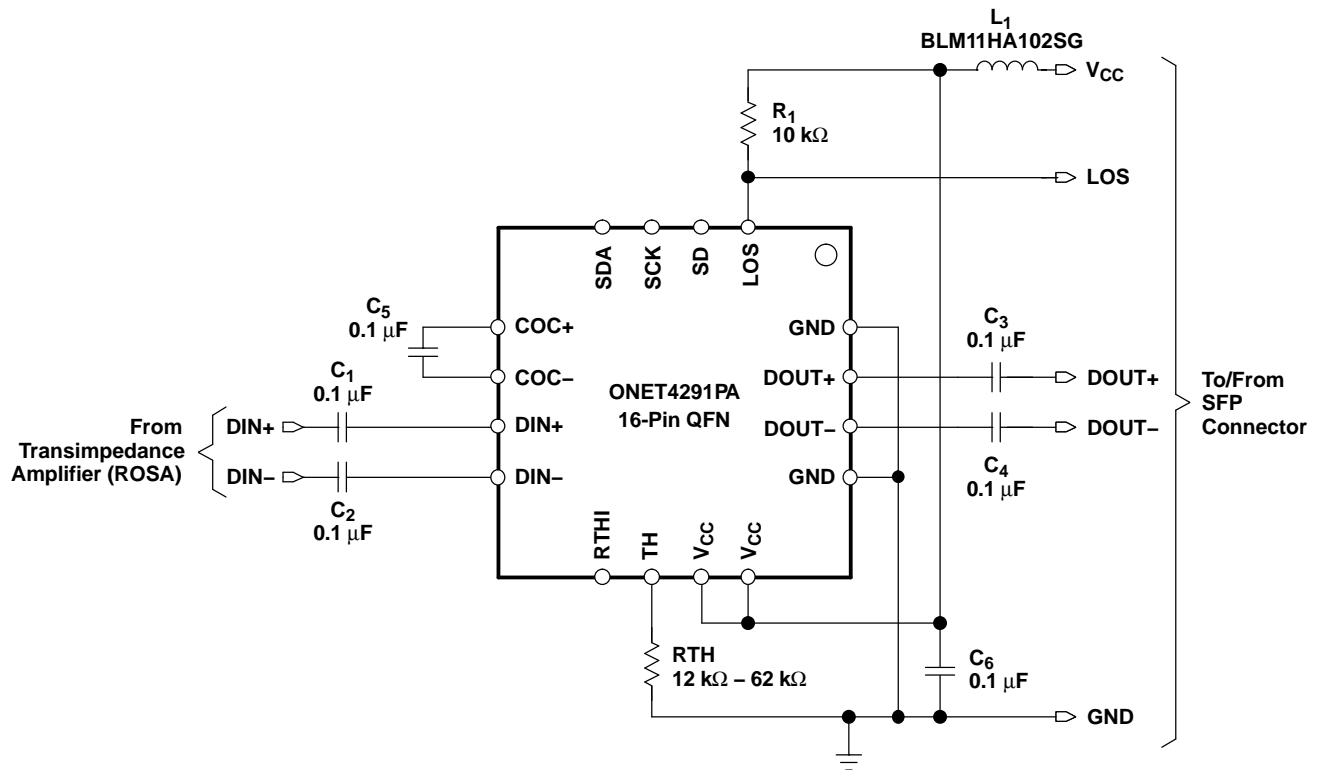


S0099-01

Figure 19. Basic Application Circuit With Digital Control

APPLICATION INFORMATION (continued)

Figure 20 shows a typical application without digital control. In this case, the output amplitude and bandwidth are fixed. The LOS threshold is adjusted by means of a resistor connected to the TH terminal.



S0099-02

Figure 20. Basic Application Circuit With External LOS Threshold Resistor

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET4291PARGVR	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4291PA	Samples
ONET4291PARGVT	ACTIVE	VQFN	RGV	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4291PA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

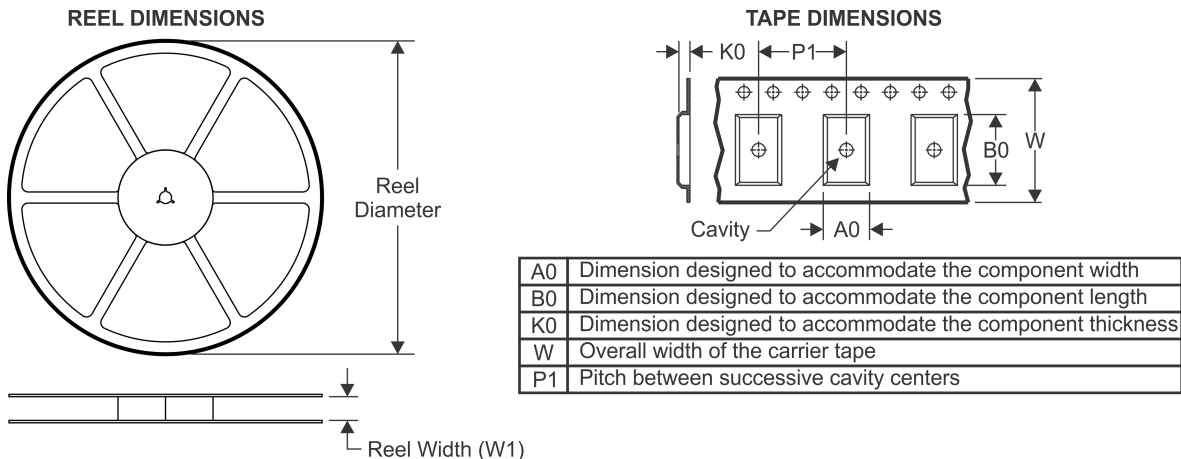
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET4291PARGVR	VQFN	RGV	16	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ONET4291PARGVT	VQFN	RGV	16	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

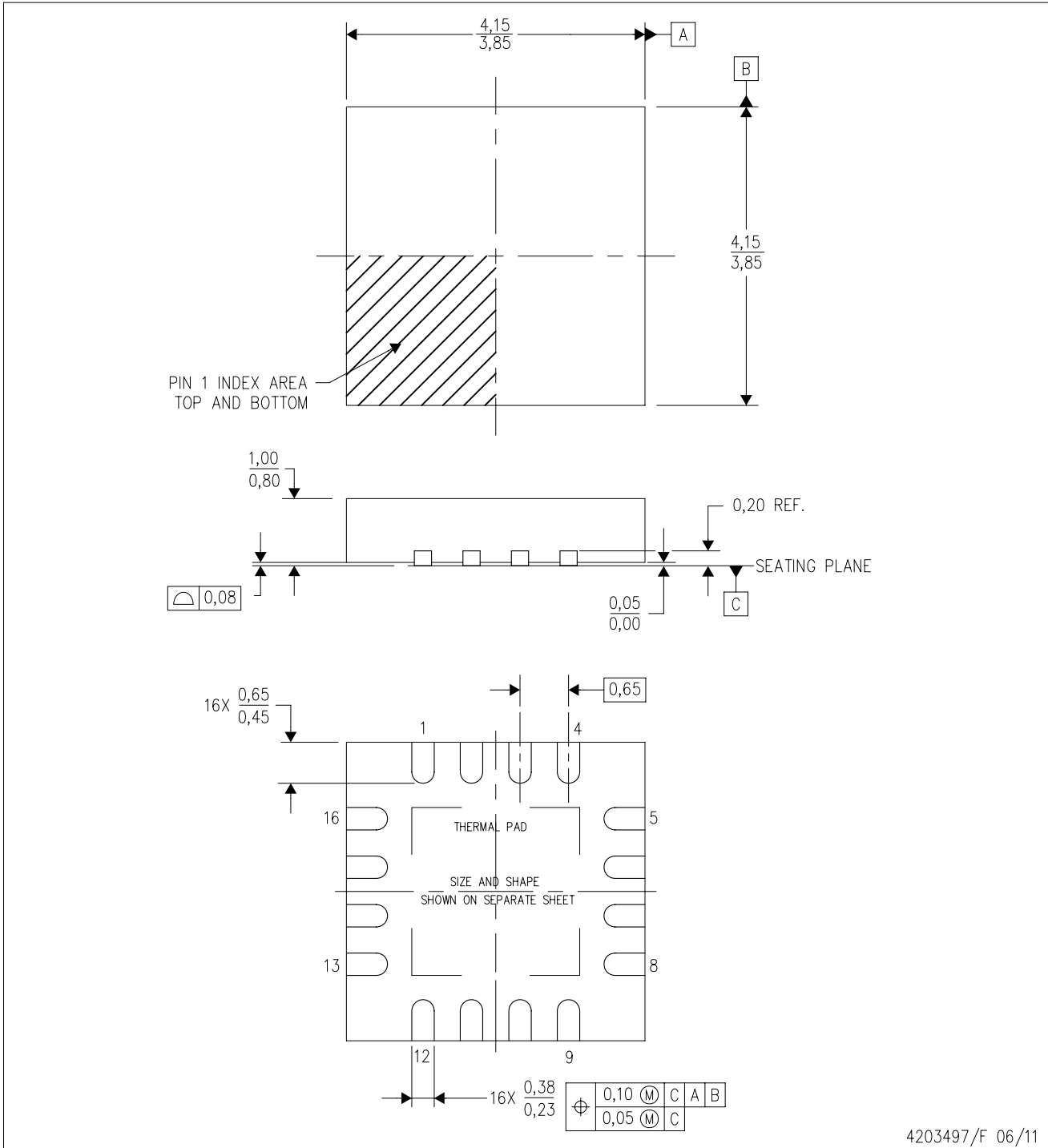
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET4291PARGVR	VQFN	RGV	16	2500	350.0	350.0	43.0
ONET4291PARGVT	VQFN	RGV	16	250	210.0	185.0	35.0

RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203497/F 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGV (S-PVQFN-N16)

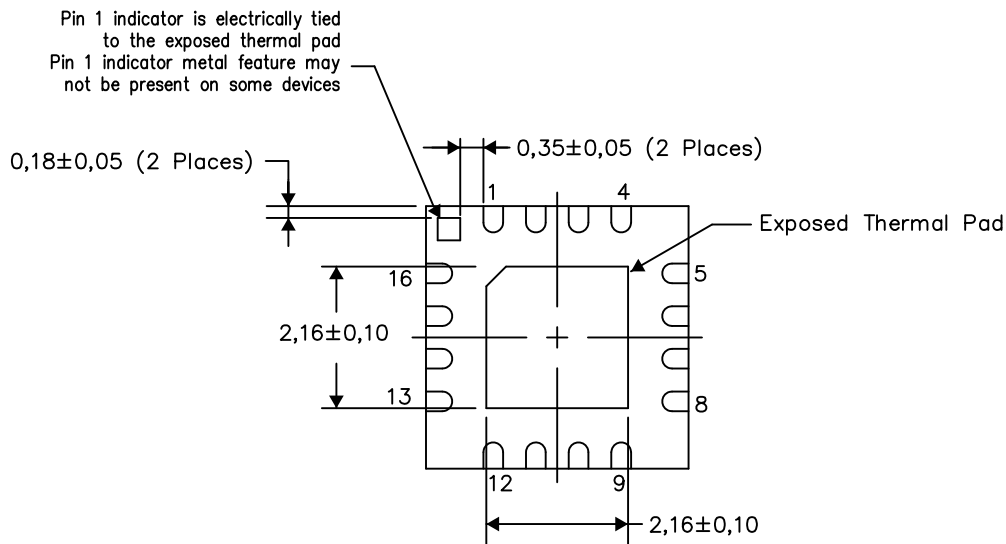
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



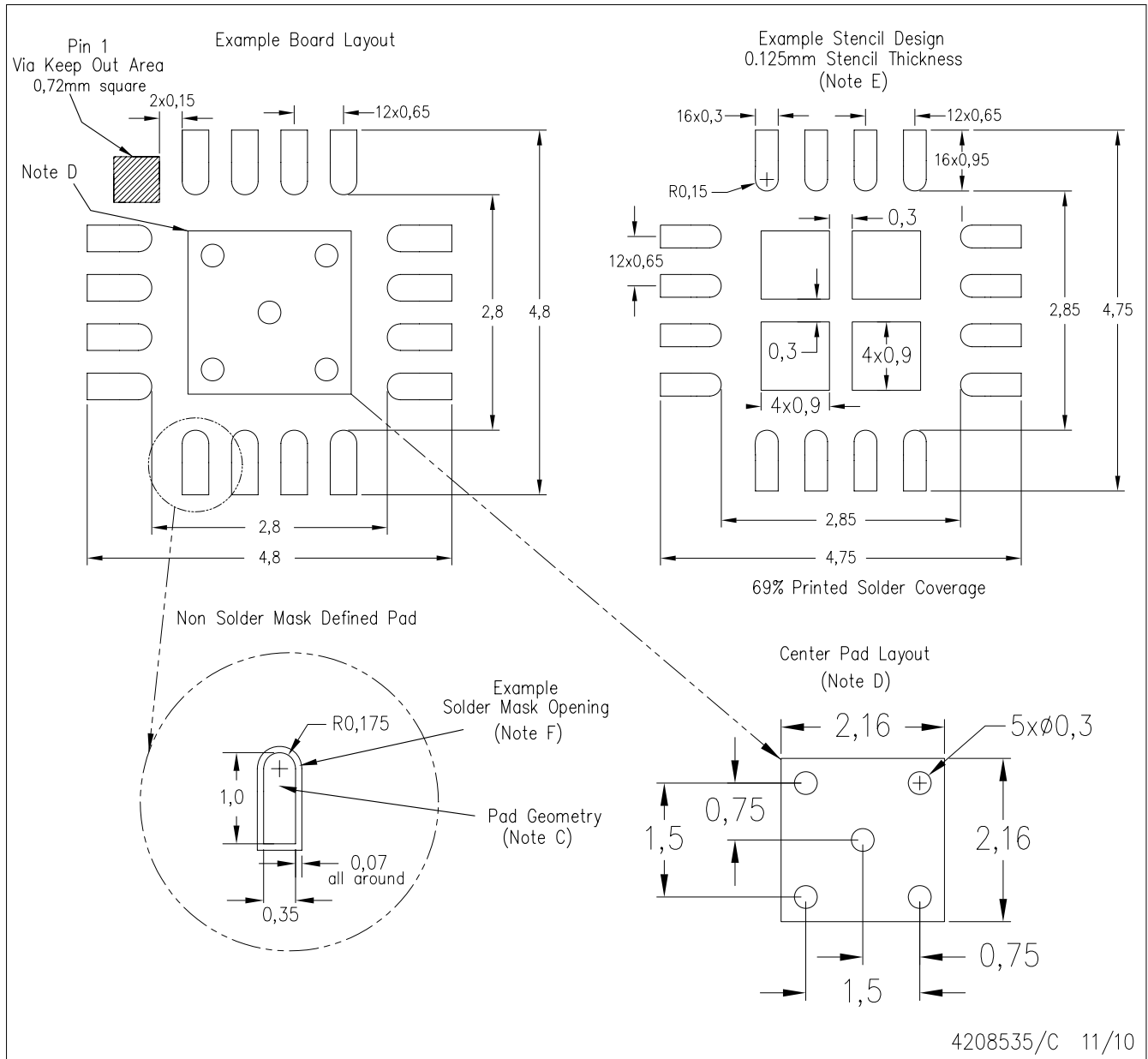
Exposed Thermal Pad Dimensions

4206351-2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208535/C 11/10

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View ONET4291PARGVR on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management