



## QUAD-CHANNEL DIGITAL ISOLATOR

### Features

- High-speed operation:  
DC – 150 Mbps
- Low propagation delay:  
<10 ns
- Wide Operating Supply Voltage:  
2.375–5.5 V
- Low power: I1 + I2 <  
12 mA/channel at 100 Mbps
- Precise timing:  
2 ns pulse width distortion  
1 ns channel-channel matching  
2 ns pulse width skew
- 2500 V<sub>RMS</sub> isolation
- Transient Immunity: >25 kV/μs
- Tri-state outputs with ENABLE control
- DC correct
- No start-up initialization required
- <10 μs Startup Time
- High temperature operation:  
125 °C at 100 Mbps  
100 °C at 150 Mbps
- Wide body SOIC-16 package

### Applications

- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power factor correction systems

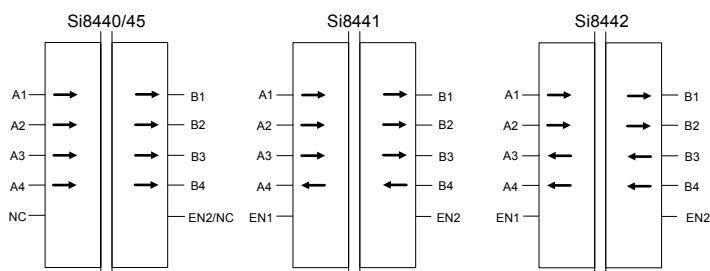
### Safety Regulatory Approvals

- UL recognition: 2500 V<sub>RMS</sub> for 1 Minute per UL1577
- CSA component acceptance notice
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

### Description

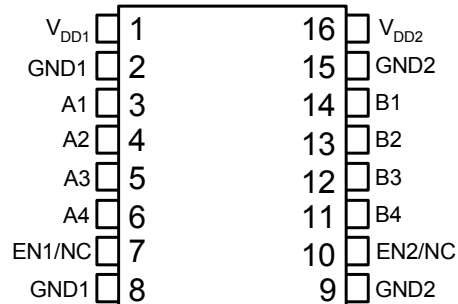
Silicon Lab's family of digital isolators are CMOS devices that employ an RF coupler to transmit digital information across an isolation barrier. Very high speed operation at low power levels is achieved. These parts are available in a 16-pin wide body SOIC package. Three speed grade options (1, 10, 150 Mbps) are available and achieve typical propagation delay of less than 10 ns.

### Block Diagram



### Pin Assignments

#### Wide Body SOIC



Top View

U.S. Patent #6,262,600  
 U.S. Patent #6,525,566  
 U.S. Patent #6,873,065  
 U.S. Patent #7,075,329  
 U.S. Patent #7,302,247  
 U.S. Patent #7,376,212  
 Other Patents Pending



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# Si8440/41/42/45

## 1. Electrical Specifications

**Table 1. Electrical Characteristics**

( $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 5\text{ V}$ ,  $T_A = -40\text{ to }125\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	$V_{IH}$		2.0	—	—	V
Low Level Input Voltage	$V_{IL}$		—	—	0.8	V
High Level Output Voltage	$V_{OH}$	$I_{OH} = -4\text{ mA}$	$V_{DD1}, V_{DD2} - 0.4$	4.8	—	V
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 4\text{ mA}$	—	0.2	0.4	V
Input Leakage Current	$I_L$		—	—	$\pm 10$	$\mu\text{A}$
Enable Input High Current	$I_{ENH}$	$V_{ENx} = V_{IH}$	—	4	—	$\mu\text{A}$
Enable Input Low Current	$I_{ENL}$	$V_{ENx} = V_{IL}$	—	20	—	$\mu\text{A}$
<b>DC Supply Current (All inputs 0 V or at Supply)</b>						
Si8440/45-A,-B,-C, $V_{DD1}$		All inputs 0 DC	—	8	12	$\text{mA}$
Si8440/45-A,-B,-C, $V_{DD2}$		All inputs 0 DC	—	7	12	$\text{mA}$
Si8440/45-A,-B,-C, $V_{DD1}$		All inputs 1 DC	—	15	22	$\text{mA}$
Si8440/45-A,-B,-C, $V_{DD2}$		All inputs 1 DC	—	7	12	$\text{mA}$
Si8441-A,-B,-C, $V_{DD1}$		All inputs 0 DC	—	9	14	$\text{mA}$
Si8441-A,-B,-C, $V_{DD2}$		All inputs 0 DC	—	11	17	$\text{mA}$
Si8441-A,-B,-C, $V_{DD1}$		All inputs 1 DC	—	14	21	$\text{mA}$
Si8441-A,-B,-C, $V_{DD2}$		All inputs 1 DC	—	13	19	$\text{mA}$
Si8442-A,-B,-C, $V_{DD1}$		All inputs 0 DC	—	10	15	$\text{mA}$
Si8442-A,-B,-C, $V_{DD2}$		All inputs 0 DC	—	10	15	$\text{mA}$
Si8442-A,-B,-C, $V_{DD1}$		All inputs 1 DC	—	13	20	$\text{mA}$
Si8442-A,-B,-C, $V_{DD2}$		All inputs 1 DC	—	13	20	$\text{mA}$
<b>10 Mbps Supply Current (All inputs = 5 MHz square wave, <math>C_I = 15\text{ pF}</math> on all outputs)</b>						
Si8440/45-B,-C, $V_{DD1}$			—	11	17	$\text{mA}$
Si8440/45-B,-C, $V_{DD2}$			—	16	22	$\text{mA}$
Si8441-B,-C, $V_{DD1}$			—	12	18	$\text{mA}$
Si8441-B,-C, $V_{DD2}$			—	14	20	$\text{mA}$
Si8442-B,-C, $V_{DD1}$			—	13	18	$\text{mA}$
Si8442-B,-C, $V_{DD2}$			—	13	18	$\text{mA}$
<b>100 Mbps Supply Current (All inputs = 50 MHz square wave, <math>C_I = 15\text{ pF}</math> on all outputs)</b>						
Si8440-C, $V_{DD1}$			—	12	17	$\text{mA}$
Si8440-C, $V_{DD2}$			—	27	32	$\text{mA}$
Si8441-C, $V_{DD1}$			—	16	23	$\text{mA}$
Si8441-C, $V_{DD2}$			—	27	34	$\text{mA}$
Si8442-C, $V_{DD1}$			—	22	29	$\text{mA}$
Si8442-C, $V_{DD2}$			—	22	29	$\text{mA}$

**Table 1. Electrical Characteristics (Continued)** $(V_{DD1} = 5\text{ V}, V_{DD2} = 5\text{ V}, T_A = -40\text{ to }125\text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Timing Characteristics</b>						
<b>Si844x-A</b>						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	1000	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	—	—	75	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 2	—	—	30	ns
Propagation Delay Skew <sup>1</sup>	$t_{PSK(P-P)}$		—	—	50	ns
Channel-Channel Skew	$t_{PSK}$		—	—	40	ns
<b>Si844x-B</b>						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	100	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	—	—	35	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 2	—	—	7.5	ns
Propagation Delay Skew <sup>1</sup>	$t_{PSK(P-P)}$		—	—	25	ns
Channel-Channel Skew	$t_{PSK}$		—	—	5	ns
<b>Si844x-C</b>						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.6	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	4	6.5	9.5	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 2	—	—	3	ns
Propagation Delay Skew <sup>1</sup>	$t_{PSK(P-P)}$		—	—	5.5	ns
Channel-Channel Skew	$t_{PSK}$		—	—	3	ns

# Si8440/41/42/45

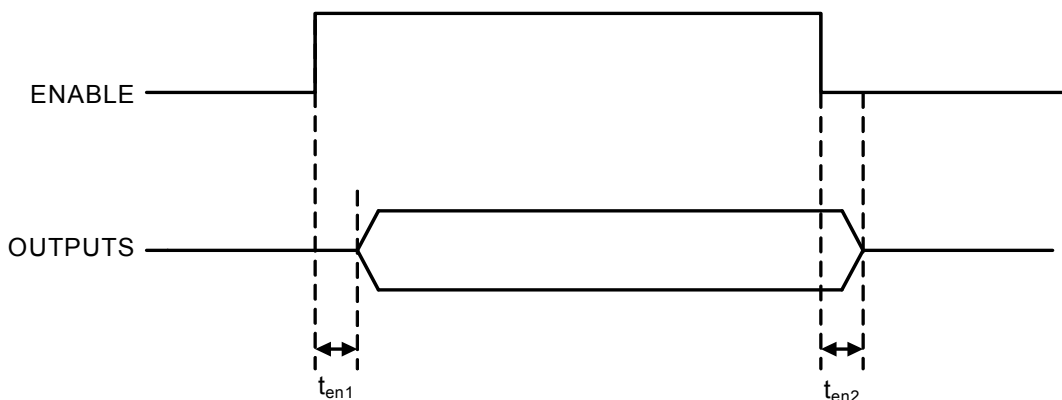
**Table 1. Electrical Characteristics (Continued)**

( $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 5\text{ V}$ ,  $T_A = -40\text{ to }125\text{ }^\circ\text{C}$ )

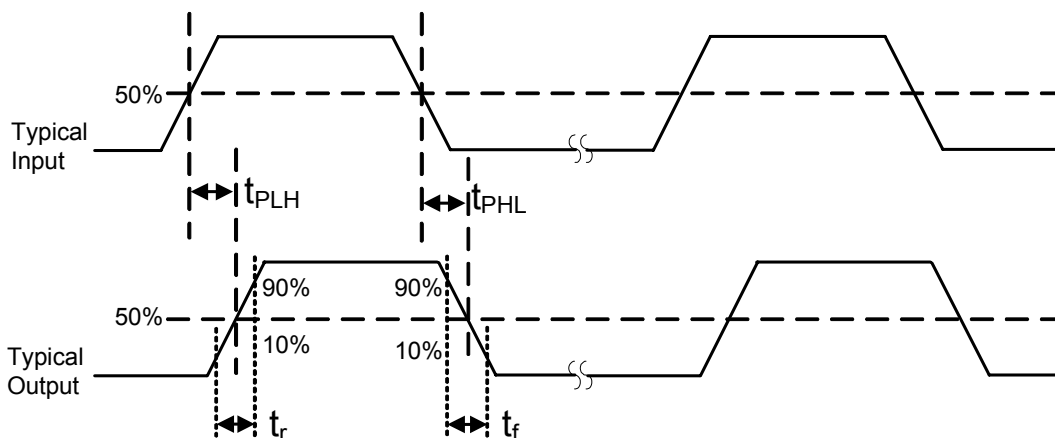
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>For All Models</b>						
Output Rise Time	$t_r$	$C_L = 15\text{ pF}$ See Figure 2	—	2	—	ns
Output Fall Time	$t_f$	$C_L = 15\text{ pF}$ See Figure 2	—	2	—	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or $0\text{ V}$	25	30	—	kV/ $\mu\text{s}$
Enable to Data Valid	$t_{en1}$	See Figure 1	—	5	—	ns
Enable to Data Tri-State	$t_{en2}$	See Figure 1	—	5	—	ns
Start-up Time <sup>2</sup>	$t_{SU}$		—	3	—	$\mu\text{s}$

**Notes:**

- $t_{PSK(P-P)}$  is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
- Start-up time is the time period from the application of power to valid data at the output.



**Figure 1. ENABLE Timing Diagram**



**Figure 2. Propagation Delay Timing**

**Table 2. Electrical Characteristics** $(V_{DD1} = 3.3\text{ V}, V_{DD2} = 3.3\text{ V}, T_A = -40\text{ to }125\text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	$V_{IH}$		2.0	—	—	V
Low Level Input Voltage	$V_{IL}$		—	—	0.8	V
High Level Output Voltage	$V_{OH}$	$I_{OH} = -4\text{ mA}$	$V_{DD1}, V_{DD2} - 0.4$	3.1	—	V
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 4\text{ mA}$	—	0.2	0.4	V
Input Leakage Current	$I_L$		—	—	$\pm 10$	$\mu\text{A}$
Enable Input High Current	$I_{ENH}$	$V_{ENx} = V_{IH}$	—	4	—	$\mu\text{A}$
Enable Input Low Current	$I_{ENL}$	$V_{ENx} = V_{IL}$	—	20	—	$\mu\text{A}$
<b>DC Supply Current (All inputs 0 V or at supply)</b>						
Si8440/45-A,-B,-C, $V_{DD1}$		All inputs 0 DC	—	7	12	mA
Si8440/45-A,-B,-C, $V_{DD2}$		All inputs 0 DC	—	7	12	mA
Si8440/45-A,-B,-C, $V_{DD1}$		All inputs 1 DC	—	14	21	mA
Si8440/45-A,-B,-C, $V_{DD2}$		All inputs 1 DC	—	6	11	mA
Si8441-A,-B,-C, $V_{DD1}$		All inputs 0 DC	—	8	13	mA
Si8441-A,-B,-C, $V_{DD2}$		All inputs 0 DC	—	11	17	mA
Si8441-A,-B,-C, $V_{DD1}$		All inputs 1 DC	—	13	20	mA
Si8441-A,-B,-C, $V_{DD2}$		All inputs 1 DC	—	12	18	mA
Si8442-A,-B,-C, $V_{DD1}$		All inputs 0 DC	—	9	14	mA
Si8442-A,-B,-C, $V_{DD2}$		All inputs 0 DC	—	9	14	mA
Si8442-A,-B,-C, $V_{DD1}$		All inputs 1 DC	—	12	18	mA
Si8442-A,-B,-C, $V_{DD2}$		All inputs 1 DC	—	12	18	mA
<b>10 Mbps Supply Current (All inputs = 5 MHz square wave, <math>C_I = 15\text{ pF}</math> on all outputs)</b>						
Si8440/45-B,-C, $V_{DD1}$			—	11	16	mA
Si8440/45-B,-C, $V_{DD2}$			—	13	19	mA
Si8441-B,-C, $V_{DD1}$			—	11	17	mA
Si8441-B,-C, $V_{DD2}$			—	13	19	mA
Si8442-B,-C, $V_{DD1}$			—	12	17	mA
Si8442-B,-C, $V_{DD2}$			—	12	17	mA
<b>100 Mbps Supply Current (All inputs = 50 MHz square wave, <math>C_I = 15\text{ pF}</math> on all outputs)</b>						
Si8440-C, $V_{DD1}$			—	11	17	mA
Si8440-C, $V_{DD2}$			—	19	25	mA
Si8441-C, $V_{DD1}$			—	13	20	mA
Si8441-C, $V_{DD2}$			—	21	27	mA
Si8442-C, $V_{DD1}$			—	18	23	mA
Si8442-C, $V_{DD2}$			—	18	23	mA

# Si8440/41/42/45

**Table 2. Electrical Characteristics (Continued)**

( $V_{DD1} = 3.3\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ ,  $T_A = -40\text{ to }125\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Timing Characteristics</b>						
<b>Si844x-A</b>						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	1000	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	—	—	75	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 2	—	—	30	ns
Propagation Delay Skew <sup>1</sup>	$t_{PSK(P-P)}$		—	—	50	ns
Channel-Channel Skew	$t_{PSK}$		—	—	40	ns
<b>Si844x-B</b>						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	100	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	—	—	35	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 2	—	—	7.5	ns
Propagation Delay Skew <sup>1</sup>	$t_{PSK(P-P)}$		—	—	25	ns
Channel-Channel Skew	$t_{PSK}$		—	—	5	ns
<b>Si844x-C</b>						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.6	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	4	6.5	9.5	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 2	—	—	3	ns
Propagation Delay Skew <sup>1</sup>	$t_{PSK(P-P)}$		—	—	5.5	ns
Channel-Channel Skew	$t_{PSK}$		—	—	3	ns

**Table 2. Electrical Characteristics (Continued)** $(V_{DD1} = 3.3\text{ V}, V_{DD2} = 3.3\text{ V}, T_A = -40\text{ to }125\text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>For All Models</b>						
Output Rise Time	$t_r$	$C_L = 15\text{ pF}$ See Figure 2	—	2	—	ns
Output Fall Time	$t_f$	$C_L = 15\text{ pF}$ See Figure 2	—	2	—	ns
Common Mode Transient Immunity at Logic Low Output	CMTI	$V_I = V_{DD}$ or 0 V	25	30	—	kV/ $\mu\text{s}$
Enable to Data Valid	$t_{en1}$	See Figure 1	—	5	—	ns
Enable to Data Tri-State	$t_{en2}$	See Figure 1	—	5	—	ns
Start-up Time <sup>2</sup>	$t_{SU}$		—	3	—	$\mu\text{s}$
<b>Notes:</b>						
1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
2. Start-up time is the time period from the application of power to valid data at the output.						

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**Table 3. Electrical Characteristics**

( $V_{DD1} = 2.5\text{ V}$ ,  $V_{DD2} = 2.5\text{ V}$ ,  $T_A = -40\text{ to }100\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	$V_{IH}$		2.0	—	—	V
Low Level Input Voltage	$V_{IL}$		—	—	0.8	V
High Level Output Voltage	$V_{OH}$	$I_{oh} = -4\text{ mA}$	$V_{DD1}, V_{DD2} - 0.4$	2.3	—	V
Low Level Output Voltage	$V_{OL}$	$I_{ol} = 4\text{ mA}$	—	0.2	0.4	V
Input Leakage Current	$I_L$		—	—	$\pm 10$	$\mu\text{A}$
Enable Input High Current	$I_{ENH}$	$V_{ENx} = V_{IH}$	—	4	—	$\mu\text{A}$
Enable Input Low Current	$I_{ENL}$	$V_{ENx} = V_{IL}$	—	20	—	$\mu\text{A}$
<b>DC Supply Current (All inputs 0 V or at supply)</b>						
Si8440/45-A,-B,-C, $V_{DD1}$		All inputs 0 DC	—	7	10	mA
Si8440/45-A,-B,-C, $V_{DD2}$		All inputs 0 DC	—	6	10	mA
Si8440/45-A,-B,-C, $V_{DD1}$		All inputs 1 DC	—	13	17	mA
Si8440/45-A,-B,-C, $V_{DD2}$		All inputs 1 DC	—	6	10	mA
Si8441-A,-B,-C, $V_{DD1}$		All inputs 0 DC	—	8	11	mA
Si8441-A,-B,-C, $V_{DD2}$		All inputs 0 DC	—	10	12	mA
Si8441-A,-B,-C, $V_{DD1}$		All inputs 1 DC	—	12	15	mA
Si8441-A,-B,-C, $V_{DD2}$		All inputs 1 DC	—	11	14	mA
Si8442-A,-B,-C, $V_{DD1}$		All inputs 0 DC	—	9	12	mA
Si8442-A,-B,-C, $V_{DD2}$		All inputs 0 DC	—	9	12	mA
Si8442-A,-B,-C, $V_{DD1}$		All inputs 1 DC	—	12	15	mA
Si8442-A,-B,-C, $V_{DD2}$		All inputs 1 DC	—	12	15	mA
<b>10 Mbps Supply Current (All inputs = 5 MHz square wave, <math>C_I = 15\text{ pF}</math> on all outputs)</b>						
Si8440/45-B,-C, $V_{DD1}$			—	10	12	mA
Si8440/45-B,-C, $V_{DD2}$			—	11	14	mA
Si8441-B,-C, $V_{DD1}$			—	11	13	mA
Si8441-B,-C, $V_{DD2}$			—	12	15	mA
Si8442-B,-C, $V_{DD1}$			—	11	14	mA
Si8442-B,-C, $V_{DD2}$			—	11	14	mA
<b>100 Mbps Supply Current (All inputs = 50 MHz square wave, <math>C_I = 15\text{ pF}</math> on all outputs)</b>						
Si8440-C, $V_{DD1}$			—	11	13	mA
Si8440-C, $V_{DD2}$			—	16	20	mA
Si8441-C, $V_{DD1}$			—	13	16	mA
Si8441-C, $V_{DD2}$			—	17	21	mA
Si8442-C, $V_{DD1}$			—	15	18	mA
Si8442-C, $V_{DD2}$			—	15	18	mA

**Table 3. Electrical Characteristics (Continued)** $(V_{DD1} = 2.5\text{ V}, V_{DD2} = 2.5\text{ V}, T_A = -40\text{ to }100\text{ }^{\circ}\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Timing Characteristics</b>						
<b>Si844x-A</b>						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	1000	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	—	—	75	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 2	—	—	30	ns
Propagation Delay Skew <sup>1</sup>	$t_{PSK(P-P)}$		—	—	50	ns
Channel-Channel Skew	$t_{PSK}$		—	—	40	ns
<b>Si844x-B</b>						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	100	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	—	—	35	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 2	—	—	7.5	ns
Propagation Delay Skew <sup>1</sup>	$t_{PSK(P-P)}$		—	—	25	ns
Channel-Channel Skew	$t_{PSK}$		—	—	5	ns
<b>Si844x-C</b>						
Maximum Data Rate			0	—	100	Mbps
Minimum Pulse Width			—	—	10	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	5	10	17	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 2	—	—	7	ns
Propagation Delay Skew <sup>1</sup>	$t_{PSK(P-P)}$		—	—	12	ns
Channel-Channel Skew	$t_{PSK}$		—	—	4	ns

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**Table 3. Electrical Characteristics (Continued)**

( $V_{DD1} = 2.5\text{ V}$ ,  $V_{DD2} = 2.5\text{ V}$ ,  $T_A = -40\text{ to }100\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>For All Models</b>						
Output Rise Time	$t_r$	$C_L = 15\text{ pF}$ See Figure 2	—	2	—	ns
Output Fall Time	$t_f$	$C_L = 15\text{ pF}$ See Figure 2	—	2	—	ns
Common Mode Transient Immunity at Logic Low Output	CMTI	$V_I = V_{DD}$ or $0\text{ V}$	25	30	—	kV/ $\mu\text{s}$
Enable to Data Valid	$t_{en1}$	See Figure 1	—	5	—	ns
Enable to Data Tri-State	$t_{en2}$	See Figure 1	—	5	—	ns
Start-up Time <sup>2</sup>	$t_{SU}$		—	3	—	$\mu\text{s}$

**Notes:**

- $t_{PSK(P-P)}$  is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
- Start-up time is the time period from the application of power to valid data at the output.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature	$T_{STG}$	-65	—	150	°C
Ambient Temperature Under Bias	$T_A$	-40	—	125	°C
Supply Voltage	$V_{DD1}, V_{DD2}$	-0.5	—	6	V
Input Voltage	$V_I$	-0.5	—	$V_{DD} + 0.5$	V
Output Voltage	$V_O$	-0.5	—	$V_{DD} + 0.5$	V
Output Current Drive Channel	$L_O$	—	—	10	mA
Lead Solder Temperature (10s)		—	—	260	°C
Maximum Isolation Voltage		—	—	4000	$V_{DC}$

**Note:** Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.

Table 5. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	$T_A$	100 Mbps, 15 pF, 5 V	-40	25	125	°C
		150 Mbps, 15 pF, 5 V	0	25	100	°C
Supply Voltage	$V_{DD1}$		2.375	—	5.5	V
	$V_{DD2}$		2.375	—	5.5	V

**\*Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

**Table 6. Regulatory Information**

<b>CSA</b>
The Si84xx is certified under CSA Component Acceptance Notice. For more details, see File 232873.
<b>VDE</b>
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
<b>UL</b>
The Si84xx is certified under UL1577 component recognition program to provide basic insulation to 2500 V <sub>RMS</sub> (1 minute). It is production tested $\geq 3000$ V <sub>RMS</sub> for 1 second. For more details, see File E257455.

**Table 7. Insulation and Safety-related Specifications**

Parameter	Symbol	Test Condition	Value	Unit
Minimum Air Gap (Clearance)	L(IO1)		7.7 min	mm
Minimum External Tracking (Creepage)	L(IO2)		8.1	mm
Minimum Internal Gap (Internal Clearance)			0.008 min	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 60112/VDE 0303 Part 1	>175	V
Resistance (Input-Output) <sup>1</sup>	R <sub>IO</sub>		10 <sup>12</sup>	$\Omega$
Capacitance (Input-Output) <sup>1</sup>	C <sub>IO</sub>	f = 1 MHz	1.4	pF
Input Capacitance <sup>2</sup>	C <sub>I</sub>		4.0	pF
<b>Notes:</b>				
1. To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.				
2. Measured from input pin to ground.				

Table 8. IEC 60664-1 (VDE 0884 Part 2) Ratings

Parameter	Test Conditions	Specification
Basic isolation group	Material Group	IIIa
Installation Classification	Rated Mains Voltages $\leq 150 V_{RMS}$	I-IV
	Rated Mains Voltages $\leq 300 V_{RMS}$	I-III
	Rated Mains Voltages $\leq 400 V_{RMS}$	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics\*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	$V_{IORM}$		560	V peak
Input to Output Test Voltage	$V_{PR}$	Method a After Environmental Tests Subgroup 1 ( $V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge $< 5$ pC)	896	V peak
		Method b1 ( $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test, $t_m = 1$ sec, Partial Discharge $< 5$ pC)	1050	
		After Input and/or Safety Test Subgroup 2/3 ( $V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge $< 5$ pC)	672	
Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR} = 10$ sec)	$V_{TR}$		4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$		$>10^9$	$\Omega$

**\*Note:** This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.

Table 10. IEC Safety Limiting Values

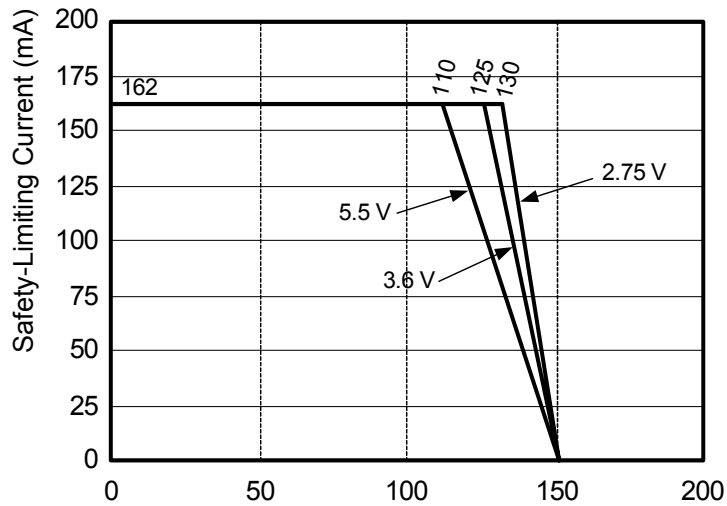
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Case Temperature	$T_S$		—	—	150	$^{\circ}C$
Safety input, output, or supply current	$I_S$	$\theta_{JA} = 107$ $^{\circ}C/W$ , $V_I = 5.5$ V, $T_J = 150$ $^{\circ}C$ , $T_A = 25$ $^{\circ}C$	—	—	210	mA

**\*Note:** Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 3.

**Table 11. Thermal Characteristics**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IC Junction-to-Case Thermal Resistance	$\theta_{JC}$	Thermocouple located at center of package	—	45	—	°C/W
IC Junction-to-Air Thermal Resistance	$\theta_{JA}$		—	107	—	°C/W
Device Power Dissipation*	$P_D$		—	—	250	mW

**\*Note:** The Si8440-C-IS is tested with  $V_{DD1} = V_{DD2} = 5.5\text{ V}$ ,  $T_J = 150\text{ °C}$ ,  $C_L = 15\text{ pF}$ , input a 150 Mbps 50% duty cycle square wave.



**Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2**

## 2. Typical Performance Characteristics

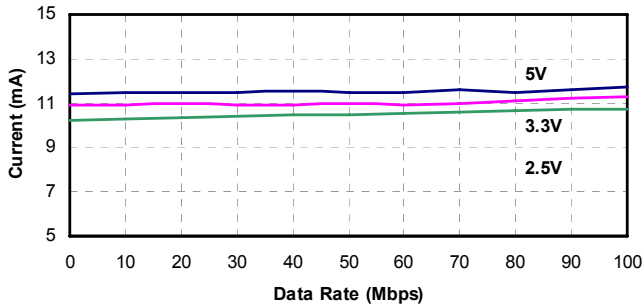


Figure 4. Si8440/45 Typical  $V_{DD1}$  Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

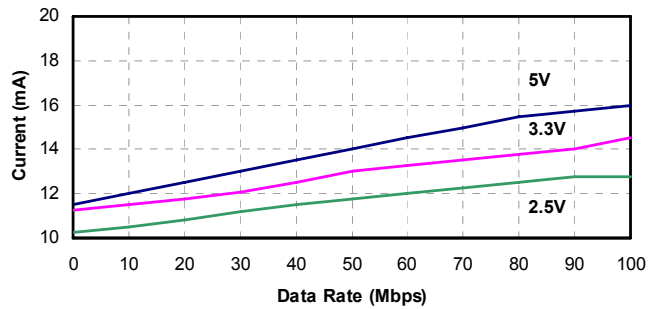


Figure 6. Si8441 Typical  $V_{DD1}$  Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

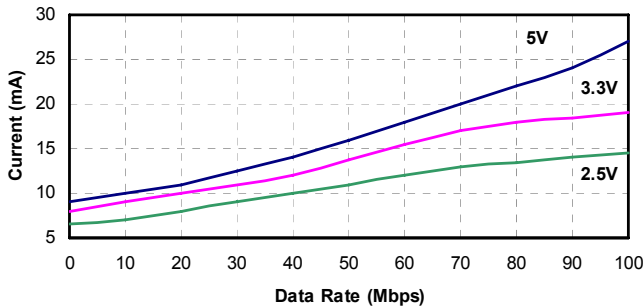


Figure 5. Si8440/45 Typical  $V_{DD2}$  Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

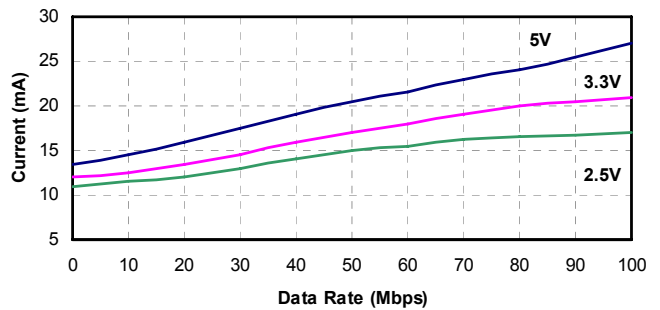


Figure 7. Si8441 Typical  $V_{DD2}$  Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

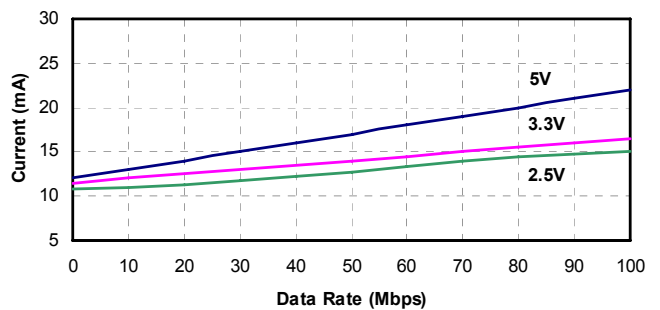
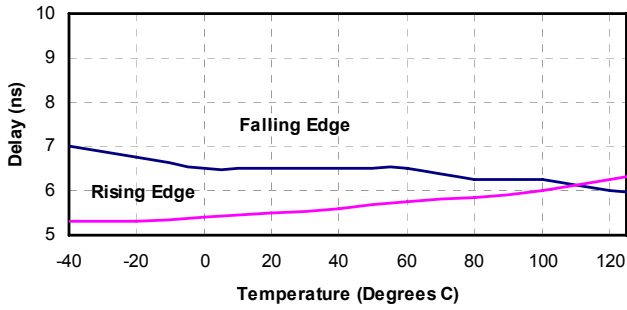
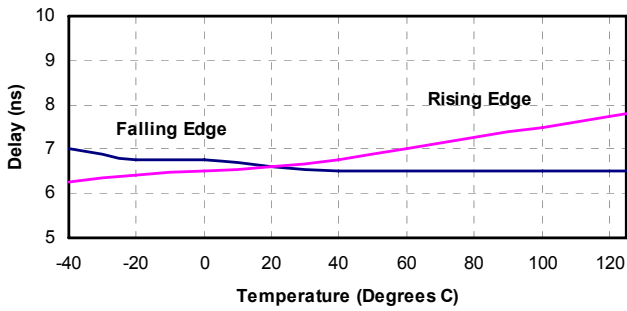


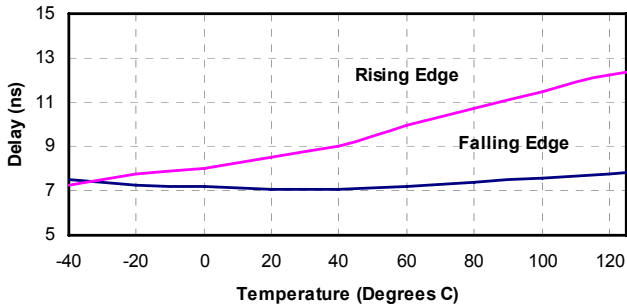
Figure 8. Si8442 Typical  $V_{DD1}$  or  $V_{DD2}$  Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)



**Figure 9. Propagation Delay vs. Temperature 5 V Operation**



**Figure 10. Propagation Delay vs. Temperature 3.3 V Operation**



**Figure 11. Propagation Delay vs. Temperature 2.5 V Operation**

### 3. Application Information

#### 3.1. Theory of Operation

The operation of an Si8440 channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si8440 channel is shown in Figure 12. A channel consists of an RF transmitter and receiver separated by a transformer.

Referring to the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying and applies the resulting waveform to the primary of the transformer. The receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver.

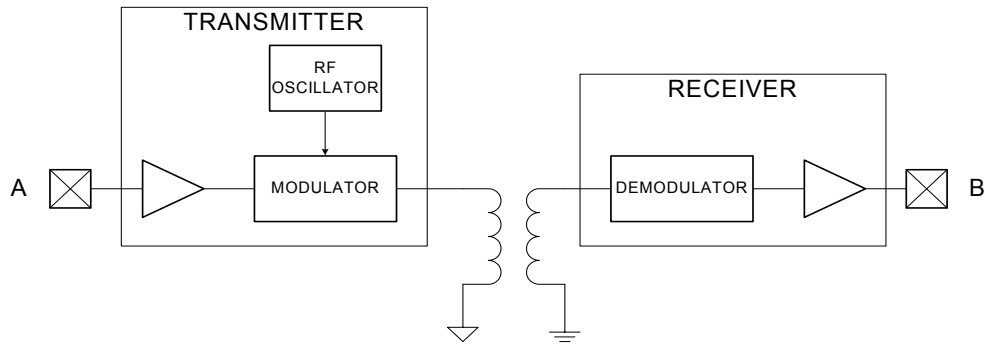


Figure 12. Simplified Channel Diagram

#### 3.2. Eye Diagram

Figure 13 illustrates an eye-diagram taken on an Si8440. The test used an Anritsu (MP1763C) Pulse Pattern Generator for the data source. The output of the generator's clock and data from an Si8440 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that very low pulse width distortion and very little jitter were exhibited.

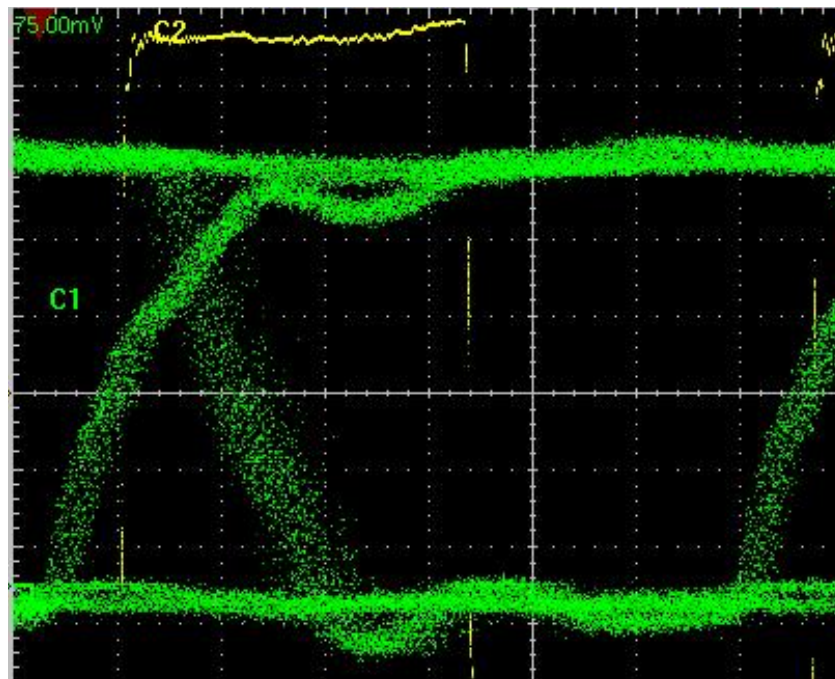


Figure 13. Eye Diagram

## 4. Layout Recommendations

Dielectric isolation is a set of specifications produced by the safety regulatory agencies from around the world that describes the physical construction of electrical equipment that derives power from a high-voltage power system such as 100–240 V<sub>AC</sub> systems or industrial power systems. The dielectric test (or HIPOT test) given in the safety specifications places a very high voltage between the input power pins of a product and the user circuits and the user touchable surfaces of the product. For the IEC relating to products deriving their power from the 220–240 V power grids, the test voltage is 2500 V<sub>AC</sub> (or 3750 V<sub>DC</sub>—the peak equivalent voltage).

There are two terms described in the safety specifications:

- Creepage—the distance along the insulating surface an arc may travel.
- Clearance—the distance through the shortest path through air that an arc may travel.

Figure 14 illustrates the accepted method of providing the proper creepage distance along the surface. For a 220–240 V application, this distance is 8 mm and the wide body SOIC package must be used. There must be no copper traces within this 8 mm exclusion area, and the surface should have a conformal coating such as solder resist. The digital isolator chip must straddle this exclusion area.

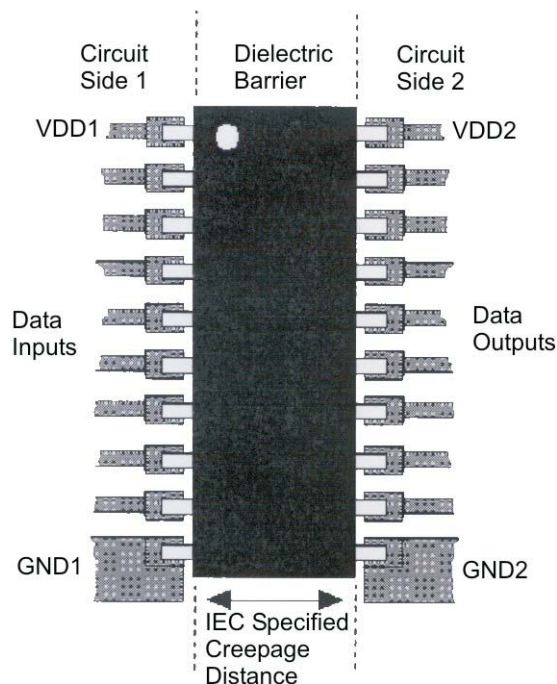


Figure 14. Creepage Distance

### 4.1. Supply Bypass

The Si844x requires a 0.1  $\mu$ F bypass capacitor between V<sub>DD1</sub> and GND1 and V<sub>DD2</sub> and GND2. The capacitor should be placed as close as possible to the package.

## 4.2. Input and Output Characteristics

The Si844x inputs and outputs are standard CMOS drivers/receivers. Table 12 details powered and unpowered operation of the Si84xx.

**Table 12. Si84xx Operation Table**

$V_I$ Input <sup>1,2</sup>	EN Input <sup>1,2,3,4</sup>	VDDI State <sup>1,5,6</sup>	VDDO State <sup>1,5,6</sup>	$V_O$ Output <sup>1,2</sup>	Comments
H	H or NC	P	P	H	Enabled, normal operation.
L	H or NC	P	P	L	
X	L	P	P	Hi-Z	Disabled
X	H or NC	UP	P	L	Upon the transition of VDDI from unpowered to powered, $V_O$ returns to the same state as $V_I$ in less than 1 $\mu$ s.
X	L	UP	P	Hi-Z	Disabled
X	X	P	UP	L	Upon the transition of VDDI from unpowered to powered, $V_O$ returns to the same state as $V_I$ in less than 1 $\mu$ s, if EN is in either the H or NC state.

**Notes:**

- VDDI and VDDO are the input and output power supplies.  $V_I$  and  $V_O$  are the respective input and output terminals. EN is the enable control input located on the same output side.
- X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
- It is recommended that the enable inputs be connected to an external logic high or low level when the Si84xx is operating in noisy environments.
- No Connect (NC) replaces EN1 on Si8440/45. No Connect replaces EN2 on the Si8445. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
- "Powered" state (P) is defined as  $2.375\text{ V} < VDD < 5.5\text{ V}$ .
- "Unpowered" state (UP) is defined as  $VDD = 0\text{ V}$ .

## 4.3. Enable Inputs

Enable inputs EN1 and EN2 can be used for multiplexing, for clock sync, or other output control. EN1, EN2 logic operation is summarized for each isolator product in Table 13. These inputs are internally pulled-up to local VDD by a 9  $\mu$ A current source allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do **not** connect circuit traces to EN1 or EN2 if they are left floating. If EN1, EN2 are unused, it is recommended they be connected to an external logic level, especially if the Si84xx is operating in a noisy environment.

**Table 13. Enable Input Truth Table**

P/N	EN1*	EN2*	Operation
Si8440	—	H	Outputs B1, B2, B3, B4 are enabled.
	—	L	Outputs B1, B2, B3, B4 are disabled and in high impedance state.
Si8441	H	X	Output A4 enabled.
	L	X	Output A4 disabled and in high impedance state.
	X	H	Outputs B1, B2, B3 are enabled.
	X	L	Outputs B1, B2, B3 are disabled and in high impedance state.
Si8442	H	X	Outputs A3 and A4 are enabled.
	L	X	Outputs A3 and A4 are disabled and in high impedance state.
	X	H	Outputs B1 and B2 are enabled.
	X	L	Outputs B1 and B2 are disabled and in high impedance state.
Si8445	—	—	Outputs B1, B2, B3, B4 are enabled.

**\*Note:** X = not applicable; H = Logic High; L = Logic Low.

## 4.4. RF Radiated Emissions

The Si8440 family uses a RF carrier frequency of approximately 2.1 GHz. This will result in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC chip but due to a small amount of RF energy driving the isolated ground planes which can act as a dipole antenna.

The unshielded Si8440 evaluation board passes FCC requirements. Table 14 shows measured emissions compared to FCC requirements.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

**Table 14. Radiated Emissions**

Frequency (GHz)	Measured (dB $\mu$ V/m)	FCC Spec (dB $\mu$ V/m)	Compared to Spec (dB)
2.094	70.0	74.0	-4.0
2.168	68.3	74.0	-5.7
4.210	61.9	74.0	-12.1
4.337	60.7	74.0	-13.3
6.315	58.3	74.0	-15.7
6.505	60.7	74.0	-13.3
8.672	45.6	74.0	-28.4

## 4.5. RF Immunity and Common Mode Transient Immunity

The Si8440 family has very high common mode transient immunity while transmitting data. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures up to 30 kV/ $\mu$ s. During a high surge event the output may glitch low for up to 20–30 ns, but the output corrects immediately after the surge event.

The Si844x family passes the industrial requirements of CISPR24 for RF immunity of 3 V/m using an unshielded evaluation board. As shown in Figure 15, the isolated ground planes form a parasitic dipole antenna, while Figure 16 shows the RMS common mode voltage versus frequency above which the Si844x becomes susceptible to data corruption. To avoid compromising data, care must be taken to keep RF common-mode voltage below the envelope specified in Figure 16. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

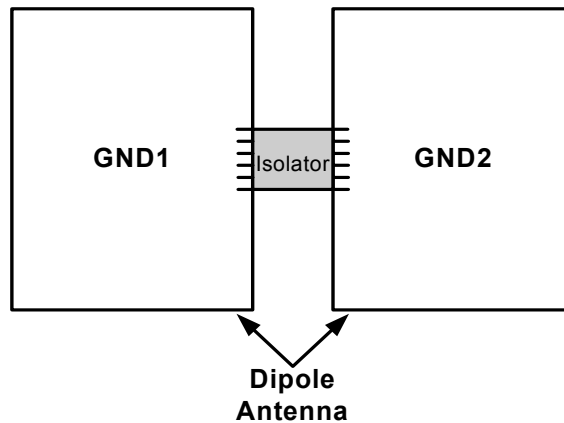


Figure 15. Dipole Antenna

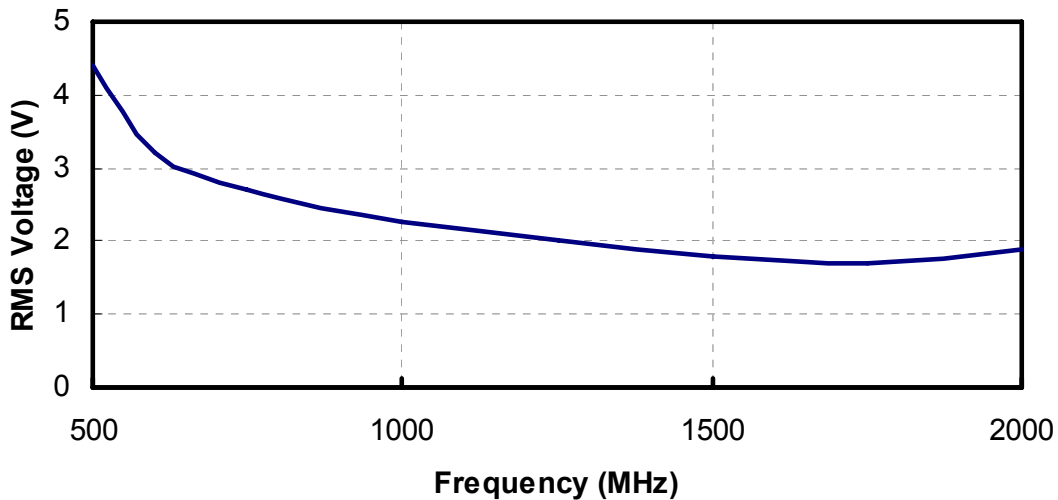
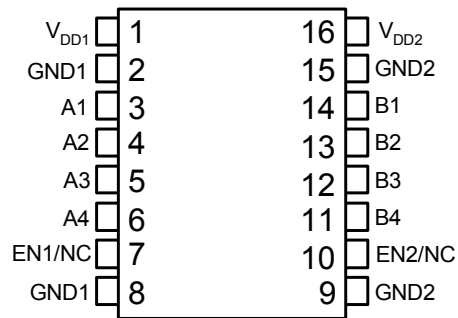


Figure 16. RMS Common Mode Voltage vs. Frequency

## 5. Pin Descriptions



Top View

### Wide Body SOIC

Name	SOIC-16 Pin#	Type	Description
$V_{DD1}$	1	Supply	Side 1 power supply.
GND1	2	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital I/O	Side 1 digital input or output.
A4	6	Digital I/O	Side 1 digital input or output.
EN1/NC*	7	Digital Input	Side 1 active high enable. NC on Si8440/45.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2/NC*	10	Digital Input	Side 2 active high enable. NC on Si8445.
B4	11	Digital I/O	Side 2 digital input or output.
B3	12	Digital I/O	Side 2 digital input or output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15	Ground	Side 2 ground.
$V_{DD2}$	16	Supply	Side 2 power supply.

**\*Note:** No Connect. These pins are not internally connected. They can be left floating, tied to  $V_{DD}$  or tied to GND.

## 6. Ordering Guide

Ordering Part Number	Number of Inputs V <sub>DD1</sub> Side	Number of Inputs V <sub>DD2</sub> Side	Maximum Data Rate	Temperature	Package Type
Si8440-A-IS	4	0	1	–40 to 125 °C	SOIC-16
Si8440-B-IS	4	0	10	–40 to 125 °C	SOIC-16
Si8440-C-IS	4	0	150	–40 to 125 °C	SOIC-16
Si8441-A-IS	3	1	1	–40 to 125 °C	SOIC-16
Si8441-B-IS	3	1	10	–40 to 125 °C	SOIC-16
Si8441-C-IS	3	1	150	–40 to 125 °C	SOIC-16
Si8442-A-IS	2	2	1	–40 to 125 °C	SOIC-16
Si8442-B-IS	2	2	10	–40 to 125 °C	SOIC-16
Si8442-C-IS	2	2	150	–40 to 125 °C	SOIC-16
Si8445-B-IS	4	0	10	–40 to 125 °C	SOIC-16

**Note:** All packages are Pb-free and RoHS compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications, and peak solder temperature.

### 7. Package Outline: Wide Body SOIC

Figure 17 illustrates the package details for the Quad-Channel Digital Isolator. Table 14 lists the values for the dimensions shown in the illustration.

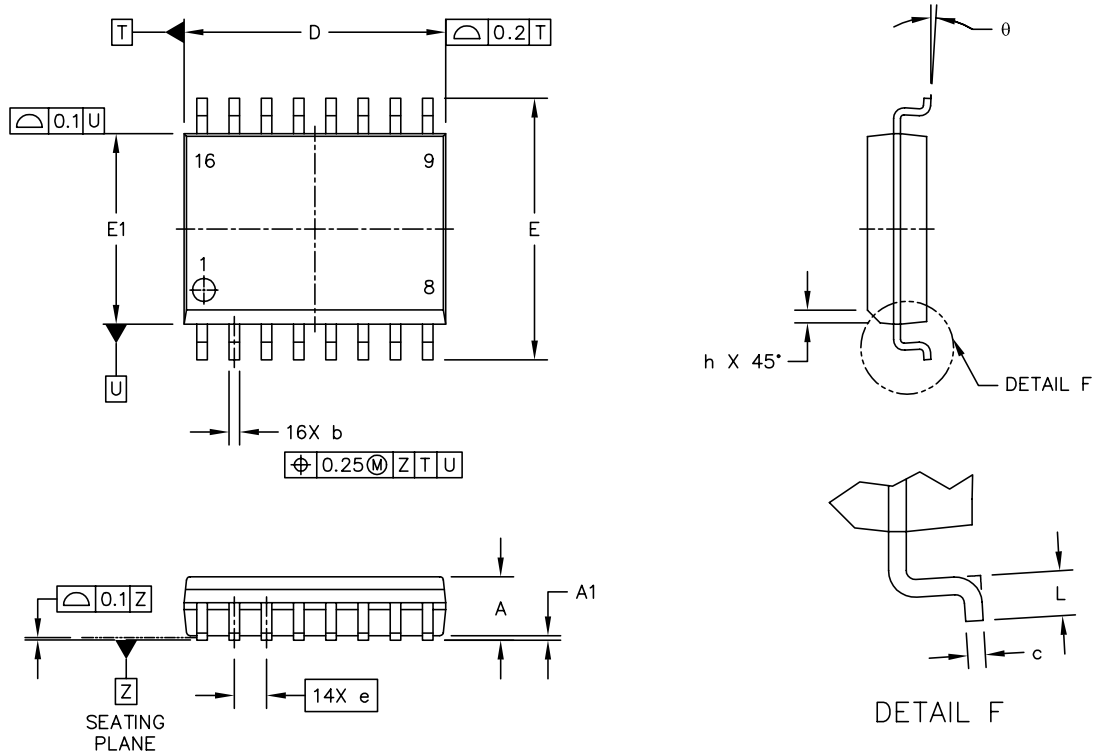


Figure 17. 16-Pin Wide Body SOIC

Table 14. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

## DOCUMENT CHANGE LIST

### Revision 0.2 to Revision 0.3

- Added enable high and low typical current specifications to Tables 1, 2, and 3.
- Added startup time specifications (with note 5) to Tables 1, 2, and 3.
- Rewrote paragraph 1 in section "4.5. RF Immunity and Common Mode Transient Immunity" on page 24 to reflect 30kV/ $\mu$ s transient immunity capability.

### Revision 0.3 to Revision 0.4

- Added minimum and maximum values to the 5.0 V, 3.3 V, and 2.5 V electrical specifications in Table 1, Table 2, and Table 3, respectively.

### Revision 0.4 to Revision 0.5

- Updated Block Diagram on page 1.
- Added Si8445 to various tables.
- Updated Table 6, "Package Characteristics," on page 13.
- Updated Table 7, "Regulatory Information," on page 14.
- Updated Table 9, "DIN EN 60747-5-2 (VDE 0884 Part 2) Insulation Characteristics," on page 15.
- Updated Figure 3, "Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2," on page 16.
- Added Table 12, "Si84xx Operation Table," on page 21.
- Added Table 13, "Enable Input Truth Table," on page 22.

### Revision 0.5 to Revision 0.51

- Added NC note (Note 3) to Table 12, "Si84xx Operation Table," on page 21.
- Added NC note (\*) to "5. Pin Descriptions" on page 25.

### Revision 0.51 to Revision 0.6

- Updated Notes to Tables 1, 2, & 3.
- Updated Figure 2.
- Updated Tables 6–11 to clarify specifications, test limits, & device characteristics.

### Revision 0.6 to Revision 0.61

- Changed MSL2 to MSL3 in the "6. Ordering Guide" on page 26.

### Revision 0.61 to Revision 0.62

- Added pertinent patent numbers.

**NOTES:**

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