

DATA SHEET

TDA7057AQ

**2 × 8 W stereo BTL audio output
amplifier with DC volume control**

Product specification
Supersedes data of 1997 July 15
File under Integrated Circuits, IC01

1998 Apr 07

2 × 8 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057AQ is a stereo BTL output amplifier with DC volume control. The device is designed for use in TVs and monitors, but is also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for single-ended headphone applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_{out}	output power	$V_P = 12\text{ V}; R_L = 16\ \Omega$	3.0	3.5	–	W
		$V_P = 12\text{ V}; R_L = 8\ \Omega$	–	5.3	–	W
		$V_P = 15\text{ V}; R_L = 8\ \Omega$	–	8	–	W
G_v	voltage gain		39.5	40.5	41.5	dB
ΔG_v	voltage gain control		68	73.5	–	dB
$I_{q(tot)}$	total quiescent current	$V_P = 12\text{ V}; R_L = \infty$	–	22	25	mA
THD	total harmonic distortion	$P_o = 0.5\text{ W}$	–	0.3	1	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7057AQ	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

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with DC volume control**

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BLOCK DIAGRAM

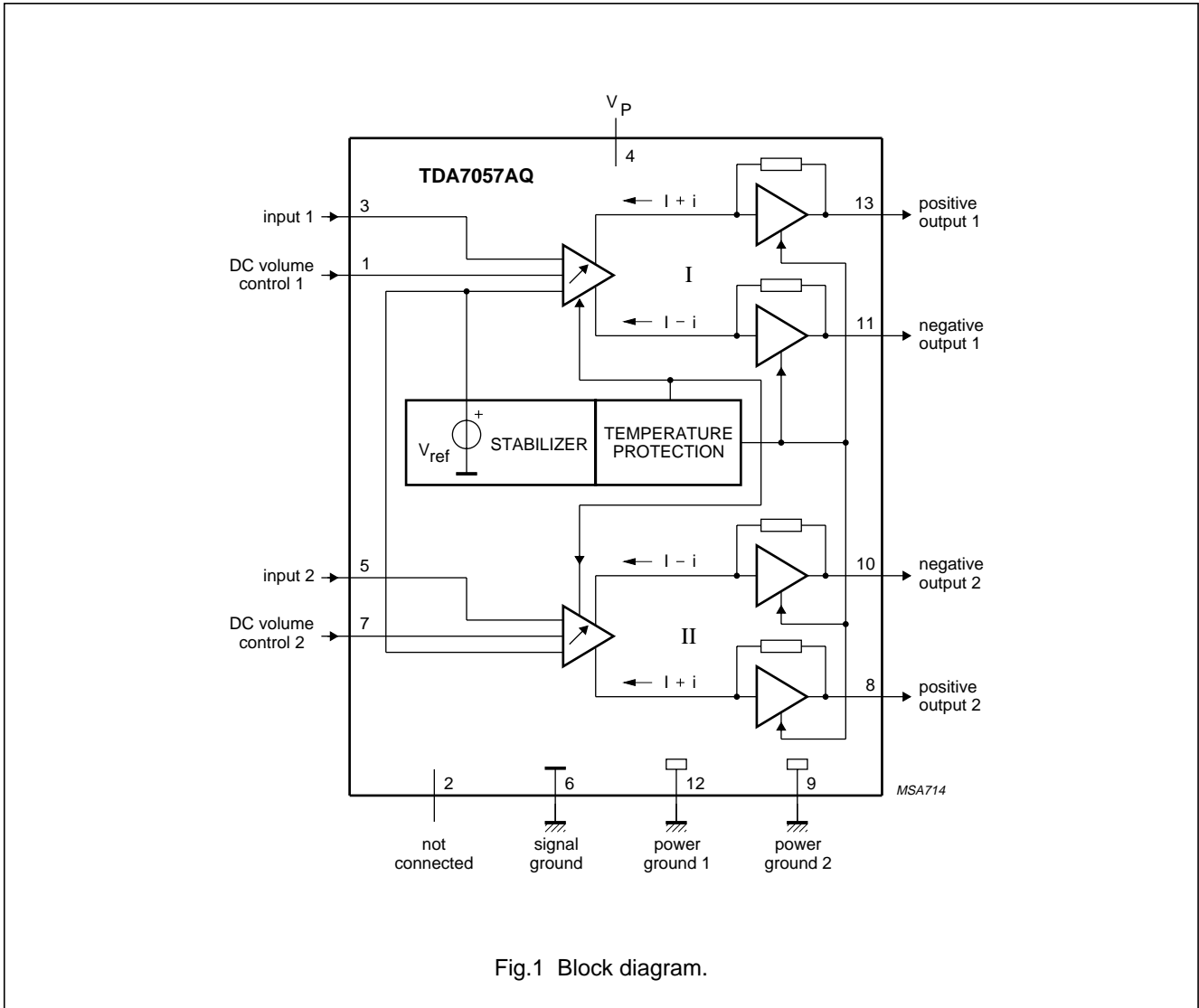


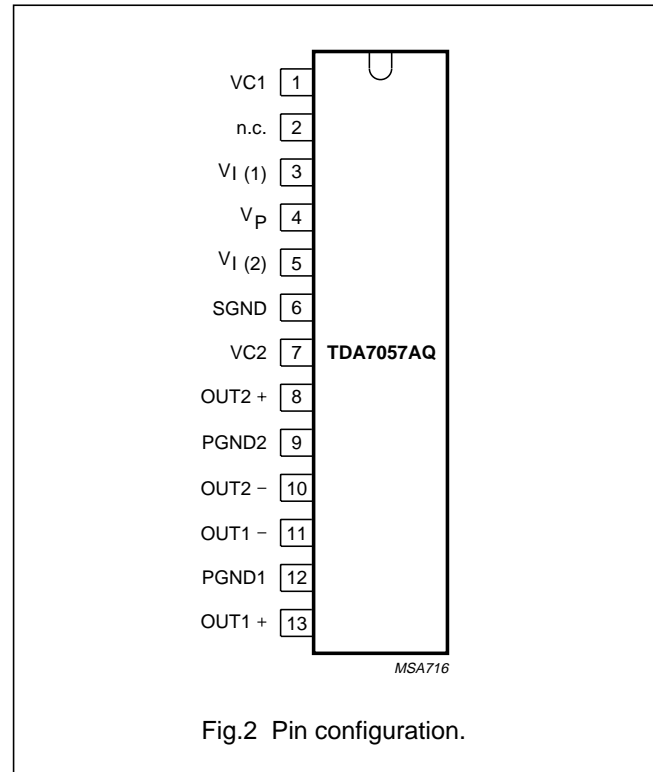
Fig.1 Block diagram.

2 × 8 W stereo BTL audio output amplifier with DC volume control

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PINNING

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume control 1
n.c.	2	not connected
$V_{I(1)}$	3	voltage input 1
V_P	4	positive supply voltage
$V_{I(2)}$	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume control 2
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2-	10	negative output 2
OUT1-	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1



FUNCTIONAL DESCRIPTION

The TDA7057AQ is a stereo output amplifier with two DC volume control stages. The device is designed for TVs and monitors, but is also suitable for battery-fed portable recorders and radios.

In conventional DC volume control circuits the control or input stage is AC-coupled to the output stage via external capacitors to keep the offset voltage low.

In the TDA7057AQ the two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and a low offset voltage is still maintained. The minimum supply voltage also remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from +40.5 dB to -33 dB. If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is a short-circuit protected to ground, V_P and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.

Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{case} < 60\text{ °C}$	–	22.5	W
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	150	°C
t_{sc}	short-circuit time		–	1	hr
V_n	input voltage pins 1, 3, 5 and 7		–	5	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-c}$	thermal resistance from junction to case	4	K/W
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	40	K/W

Power dissipation

Assume $V_P = 12\text{ V}$ and $R_L = 16\ \Omega$. The maximum sine wave dissipation is $2 \times 1.8\text{ W} = 3.6\text{ W}$.

At $T_{amb(max)} = 60\text{ °C}$:

$$R_{th\ tot} = (150 - 60)/3.6 = 25\text{ K/W.}$$

$$R_{th\ tot} = R_{th\ j-c} + R_{th\ c-hs} + R_{th\ hs}$$

$$R_{th\ c-hs} + R_{th\ hs} = 25 - 4 = 21\text{ K/W.}$$

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CHARACTERISTICS

$V_P = 12\text{ V}$; $T_{\text{amb}} = 25\text{ °C}$; $f_i = 1\text{ kHz}$; $R_L = 16\text{ }\Omega$; unless otherwise specified (see Fig.13).

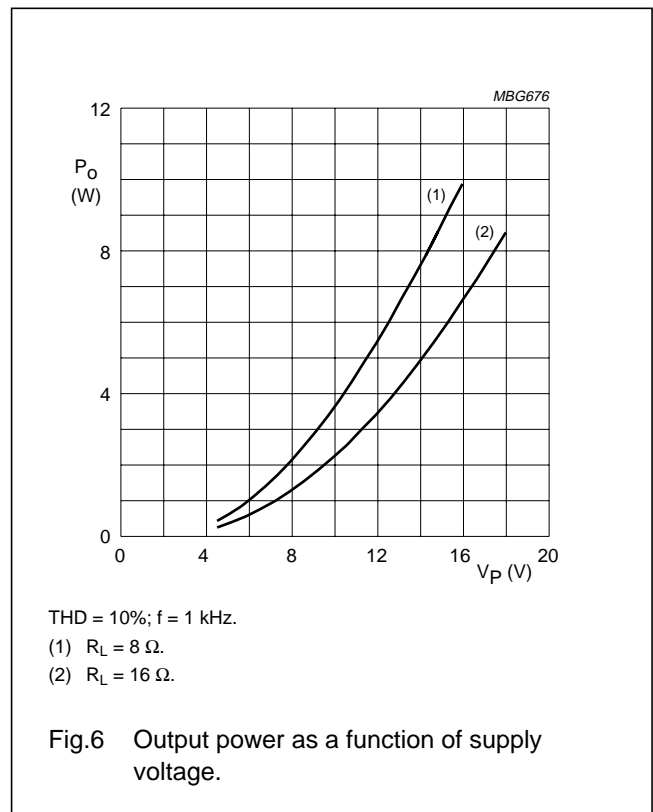
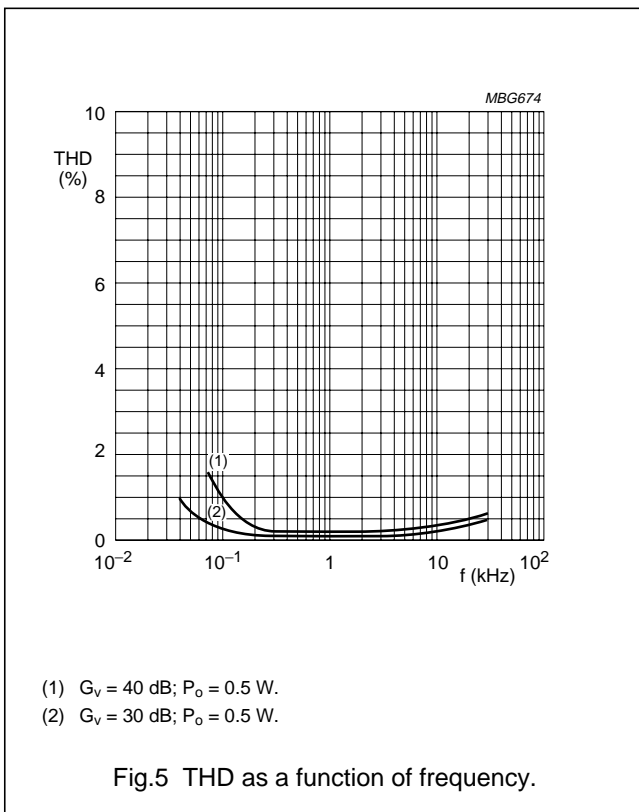
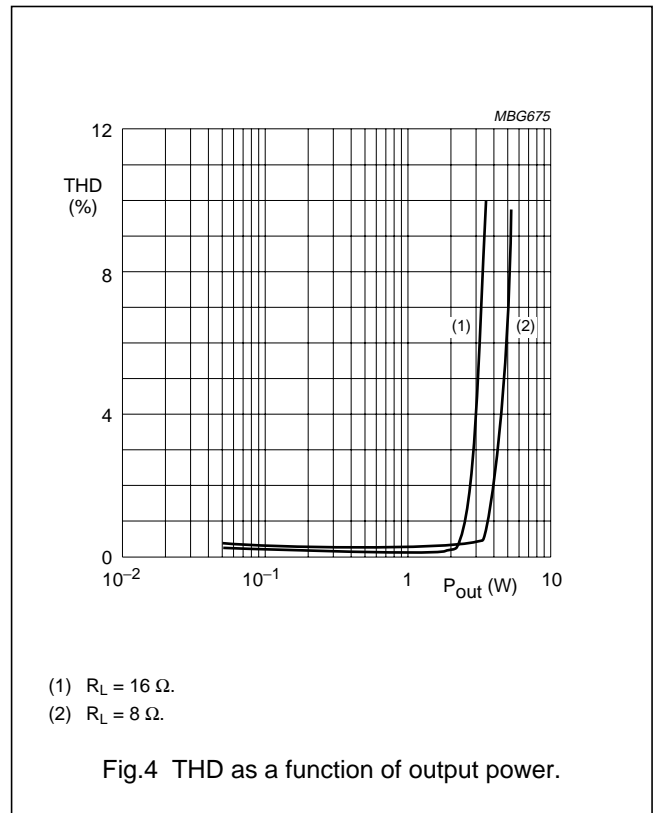
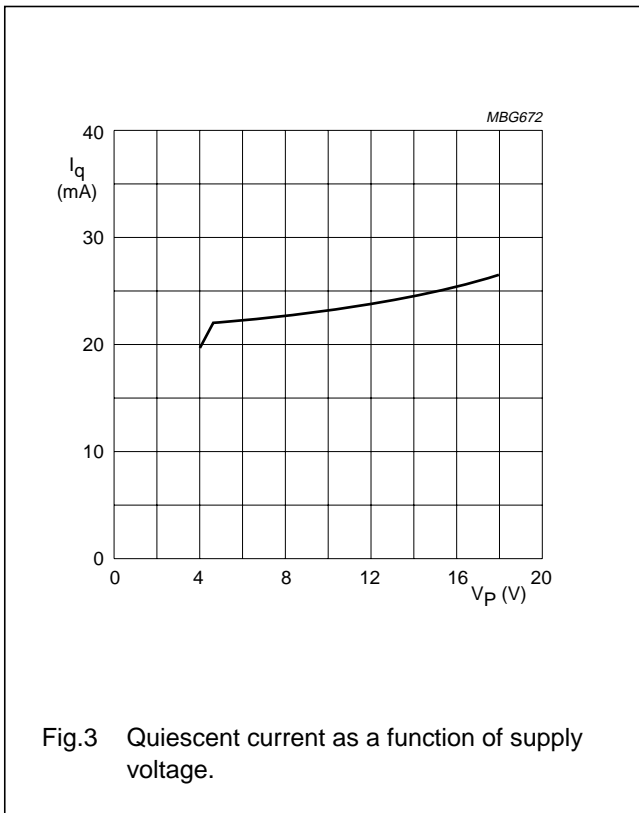
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	voltage supply		4.5	–	18.5	V
$I_{q(\text{tot})}$	total quiescent current	$V_P = 12\text{ V}$; $R_L = \infty$; note 1	–	22	25	mA
Maximum gain; $V_{1,7} \geq 1.4\text{ V}$						
P_o	output power	THD = 10%; $R_L = 16\text{ }\Omega$	3.0	3.5	–	W
		THD = 10%; $R_L = 8\text{ }\Omega$	–	5.3	–	W
		THD=10%; $R_L = 8\text{ }\Omega$; $V_P = 15\text{ V}$	–	8	–	W
THD	total harmonic distortion	$P_o = 0.5\text{ W}$	–	0.3	1	%
G_V	voltage gain		39.5	40.5	41.5	dB
$V_{i(\text{rms})}$	input signal handling (RMS value)	$G_V = 0\text{ dB}$; THD < 1%	1	–	–	V
$V_{o(n)}$	noise output voltage	$f_i = 500\text{ kHz}$; note 2	–	210	–	μV
B	bandwidth	at –1 dB	–	note 3	–	dB
SVRR	supply voltage ripple rejection	note 4	34	38	–	dB
$ V_{OS} $	DC output offset voltage	$ V_{13} - V_{11} $ and $ V_{10} - V_8 $	–	0	200	mV
Z_i	input impedance (pins 3 and 5)		15	20	25	$\text{k}\Omega$
α_{CS}	channel separation	$R_S = 5\text{ k}\Omega$	40	–	–	dB
$ G_V $	channel unbalance	note 5	–	–	1	dB
		$G_1 = 0\text{ dB}$; note 6	–	–	1	dB
Mute position; $V_1 = V_7 = 0.4\text{ V} \pm 30\text{ mV}$						
$V_{o(\text{mute})}$	output voltage in mute position	$V_i = 1.0\text{ V}$; note 7	–	35	45	μV
DC volume control						
ΔG_V	gain control range		68	73.5	–	dB
I_{DC}	volume control current	$V_1 = V_7 = 0\text{ V}$	–20	–25	–30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L .
2. The noise output voltage (RMS value) at $f_i = 500\text{ kHz}$ is measured with $R_S = 0\text{ }\Omega$ and bandwidth = 5 kHz.
3. 20 Hz to 300 kHz (typical).
4. The ripple rejection is measured with $R_S = 0\text{ }\Omega$ and $f = 100\text{ Hz}$ to 10 kHz. The ripple voltage ($V_{\text{ripple}} = 200\text{ mV RMS}$) is applied to the positive supply rail.
5. The channel unbalance is measured with $V_{DC1} = V_{DC2}$.
6. The channel unbalance at $G_1 = 0\text{ dB}$ is measured with $V_{DC1} = V_{DC2}$.
7. The noise output voltage (RMS value) is measured with $R_S = 5\text{ k}\Omega$ unweighted.

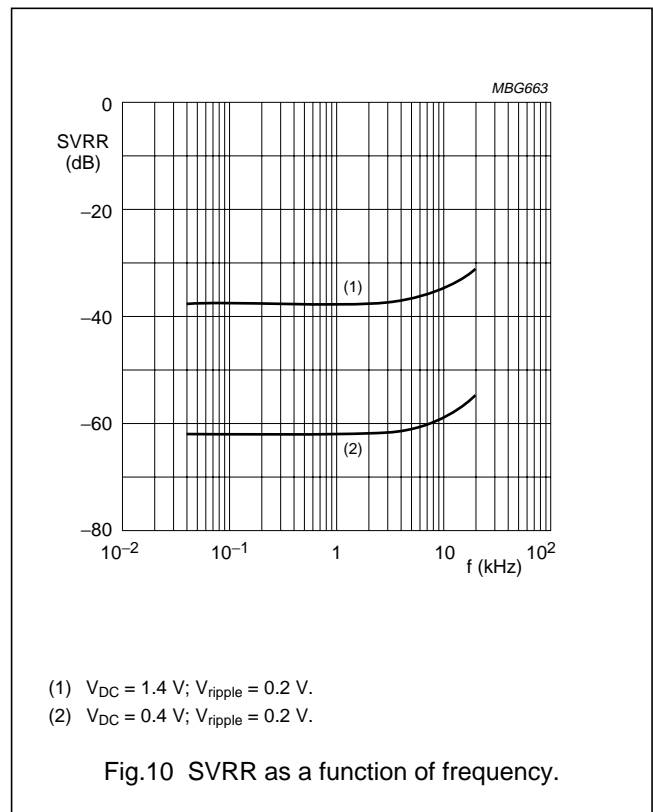
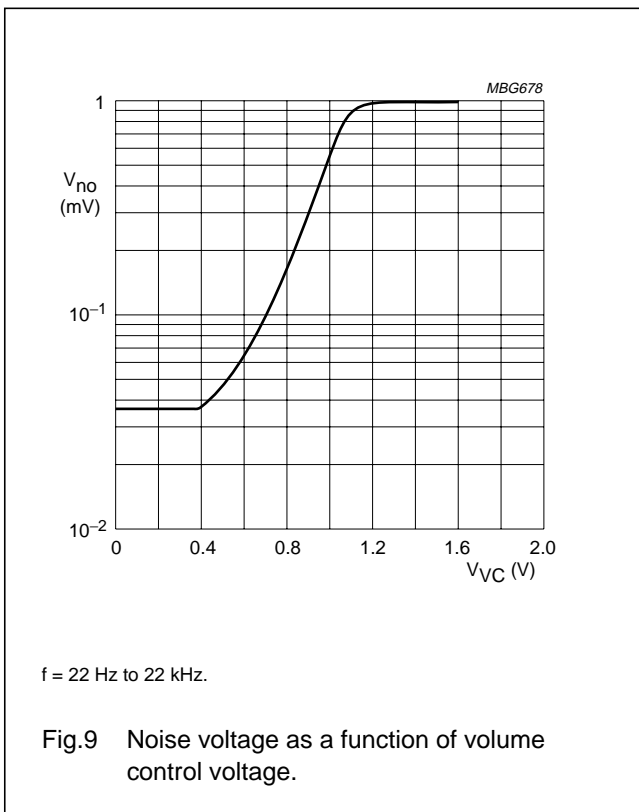
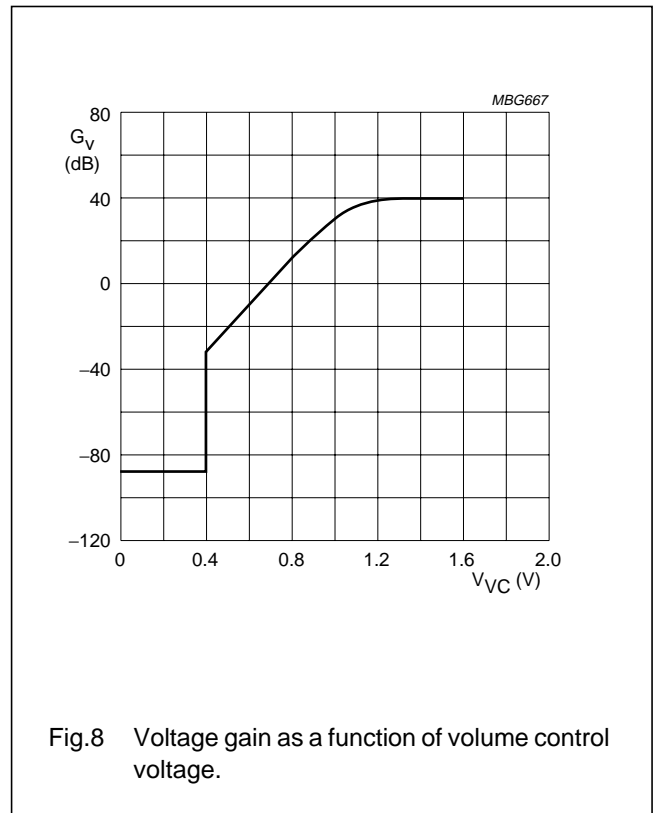
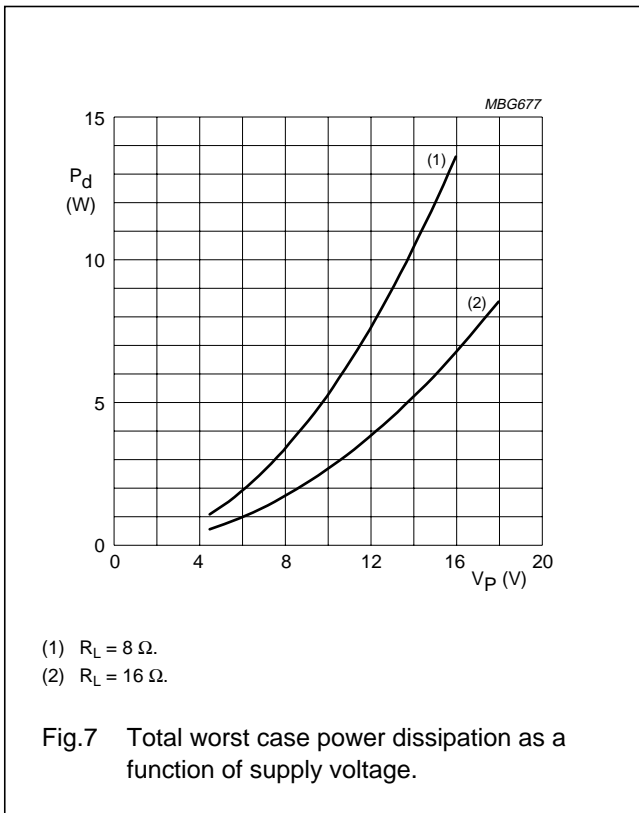
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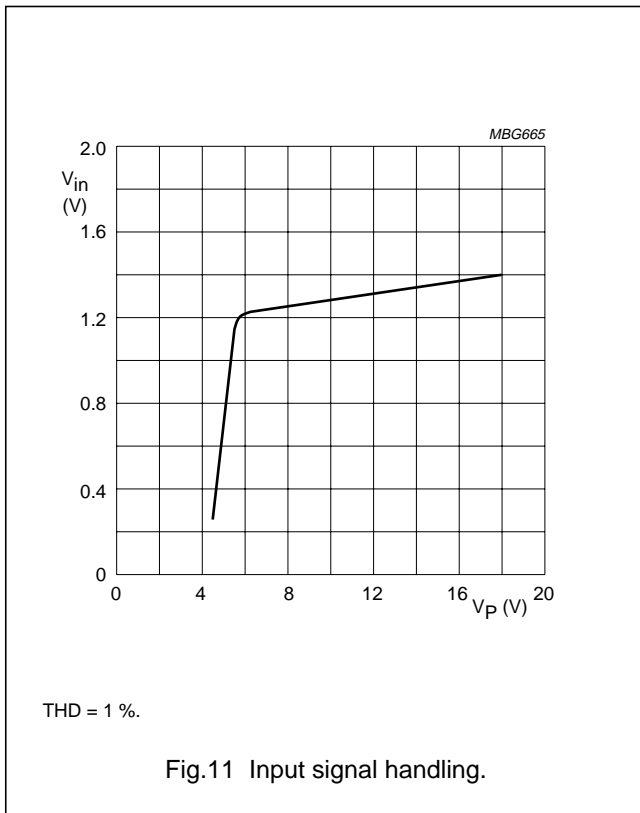


Fig.11 Input signal handling.

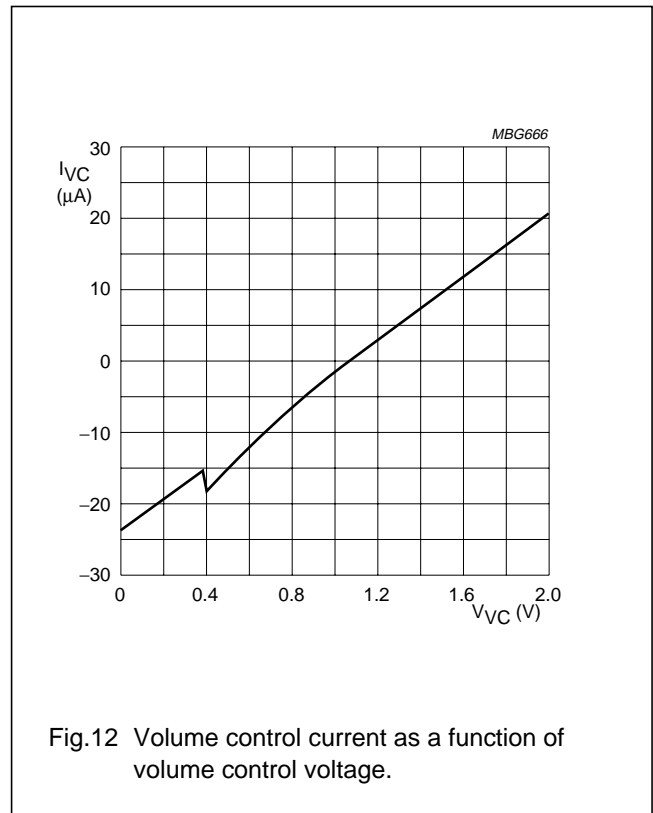


Fig.12 Volume control current as a function of volume control voltage.

APPLICATION INFORMATION

The application diagram is illustrated in Fig.13.

Test conditions

$T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified; $V_P = 12\text{ V}$;
 $V_{DC} = 1.4\text{ V}$; $f_i = 1\text{ kHz}$; $R_L = 16\text{ }\Omega$.

The quiescent current has been measured without load impedance.

The output power as a function of the supply voltage has been measured at THD = 10%. The maximum output power is limited by the maximum power dissipation and the maximum available output current.

The maximum input signal voltage is measured at THD = 1% at the output with a voltage gain of 0 dB.

To avoid instabilities and too high a distortion, the input ground and power ground must be separated as far as possible and connected as close as possible to the IC.

The DC volume control can be applied in several ways. Two possible circuits are shown below the main application diagram. The circuits at the control pin will influence the switch-on and switch-off behaviour and the maximum voltage gain.

For single-end applications the output peak current must not exceed 100 mA. At higher output currents the short-circuit protection (MCL) will be active.

Thermal considerations:

At high junction temperatures ($>125\text{ }^\circ\text{C}$) the voltage gain will decrease when it is higher than 0 dB. This results in a decrease of the output voltage and an increase of the distortion level. Thus for an optimal performance of the IC the heatsink has to be designed properly.

Calculation example for application: $V_P = 15\text{ V}$; $R_L = 8\text{ }\Omega$, stereo sine wave; worst case sine wave power dissipation is 12 W.

For $T_{amb(max)} = 40\text{ }^\circ\text{C}$ the thermal resistance from junction to ambient $R_{th\ j-a} = \frac{(125 - 40)}{12} = 7.1\text{ K/W}$

The thermal resistance of the heatsink becomes:

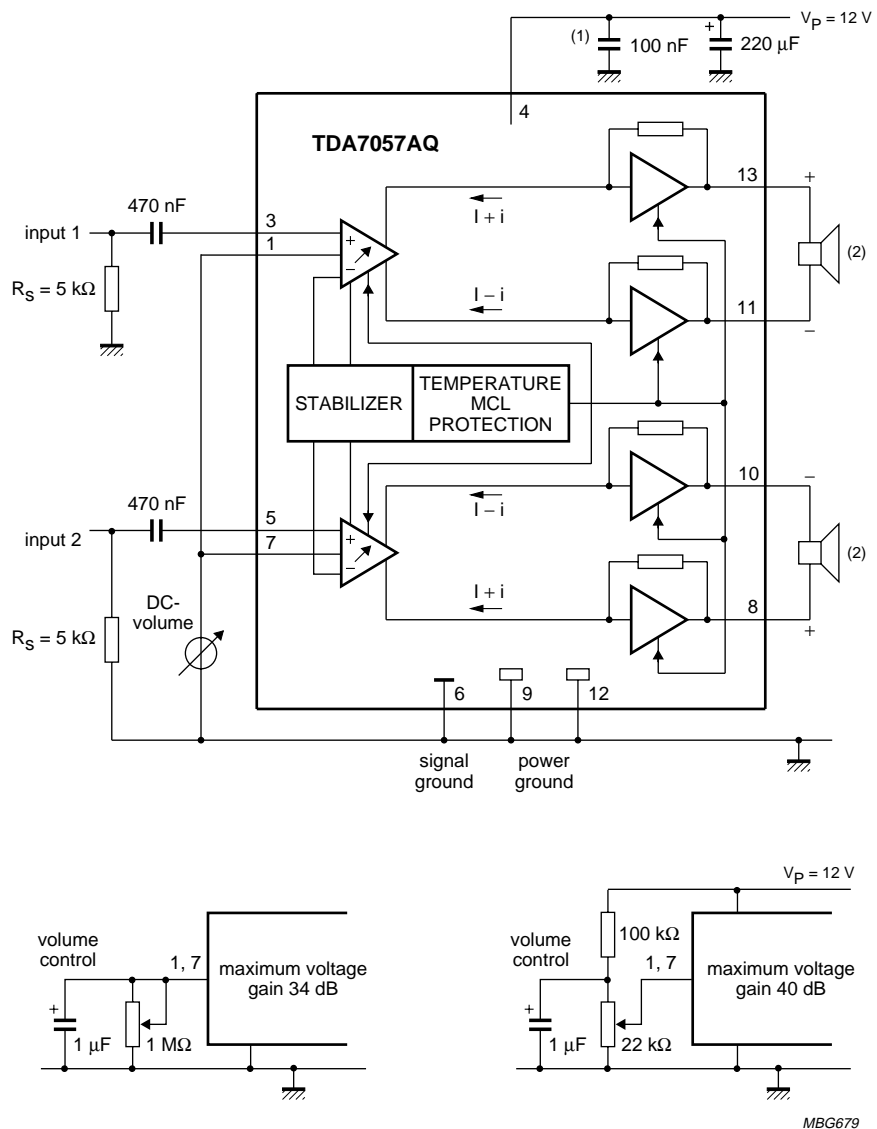
$$R_{th\ h-a} = R_{th\ j-a} - (R_{th\ j-c} + R_{th\ c-h});$$

$$R_{th\ h-a} = 7.1 - (4 + 0.1) = 3\text{ K/W}.$$

It should be noted that for 'music power' the power dissipation will be approximately half of the sine wave dissipation. Thus a smaller heatsink can be used.

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- (1) This capacitor can be omitted if the 220 μF electrolytic capacitor is connected close to pin 5.
- (2) $R_L = 16 \Omega$.

Fig.13 Test and application diagram.

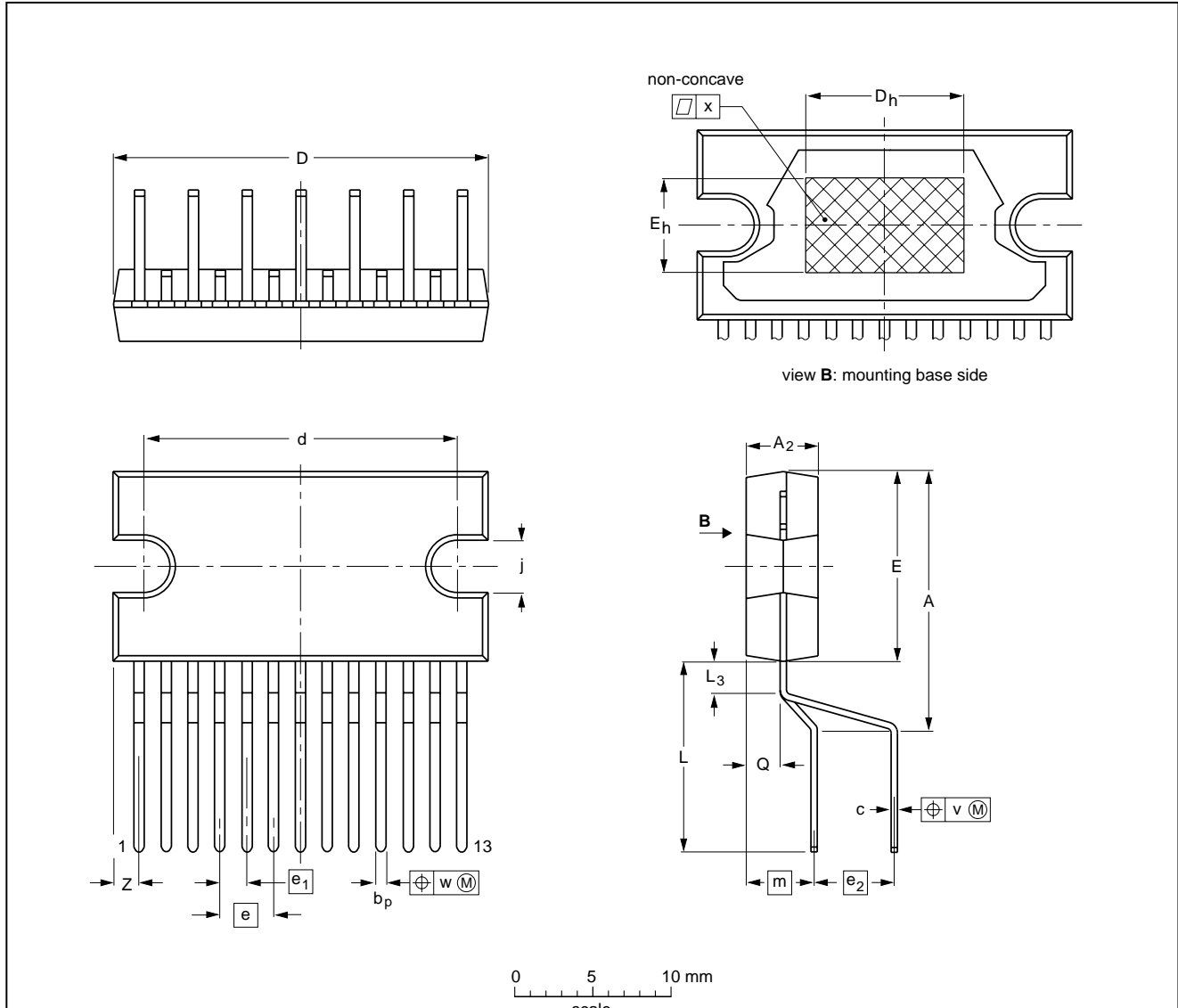
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PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)

SOT141-6



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	z ⁽¹⁾
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						95-03-11 97-12-16

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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NOTES

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010, Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

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Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762, Tel. +65 350 2538, Fax. +65 251 6500

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381

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