



THE DATASHEET OF AD8509ARUZ-REEL



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REVISION HISTORY

2/06—Rev. C

Added LFCSP Package	Universal
Added Pin Configurations and Function Descriptions Section ...	5
Updated Outline Dimensions	9
Changes to Ordering Guide	9

1/05—Rev. A to Rev. B

Changed Maximum Operating Voltage.....	Universal
Change to Features List.....	1
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9/04—Rev. 0 to Rev. A

Format Updated.....	Universal
Added Pb-Free Part.....	Universal
Changed Temperature Range.....	Universal
Changed Applications Section.....	1
Changes to Ordering Guide	8

10/97—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				20	mV
Input Bias Current	I_B				50	nA
Voltage Gain	A_{VO}		0.985			V/V
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_{LOAD} = +20\text{ mA}$	4.8			V
Output Voltage Low	V_{OL}	$I_{LOAD} = -20\text{ mA}$			200	mV
Output Short-Circuit Current	I_{SC}		120	350		mA
POWER SUPPLY						
Load Regulation		$V_{IN} = 0.5\text{ V to }4.5\text{ V}$, $I_{SOURCE} = 20\text{ mA}$ $V_{IN} = 0.5\text{ V to }4.5\text{ V}$, $I_{SINK} = 20\text{ mA}$		7		mV
Supply Current	I_{SY}	AD8509, $V_{IN} = 2.5\text{ V}$ AD8511, $V_{IN} = 2.5\text{ V}$		7	8.5	mV mA
Supply Voltage Range	V_S		3.3		10 6.5	mA V
DYNAMIC PERFORMANCE						
Slew Rate		$C_L = 15\text{ pF}$ $R_L = 250\ \Omega$		7		V/ μs
Settling Time	t_S	IDC = 13 mA (sink/source)		6.2		V/ μs
				3	6	μs
LOGIC INPUT CHARACTERISTICS						
Input Current Low	I_{IL}				1.0	μA
Input Current High	I_{IH}				1.5	μA
Input Voltage Low	V_{IL}				0.8	V
Input Voltage High	V_{IH}		2.0			V

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	7 V
Input Voltage	GND to V_S
Storage Temperature Range TSSOP (RV-48)	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range TSSOP (RV-48) Package	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead, Pb-Free SSOP (RV-48)	115	42	°C/W
48-Lead, Pb-Free LFCSP (CP-48-1)	125	29	°C/W

Table 4. MUX Function

A/B Select	Input
Logic High	INAx
Logic Low	INBx

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

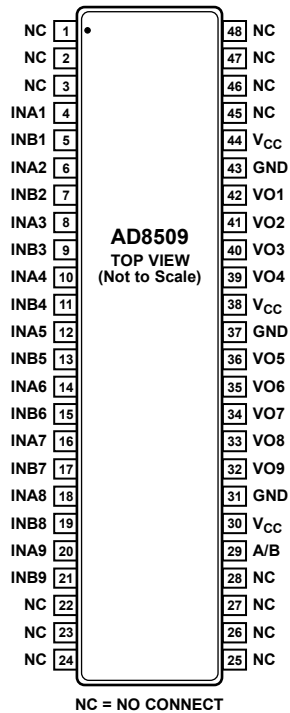


Figure 4. AD8509
48-Lead TSSOP (RV Suffix)

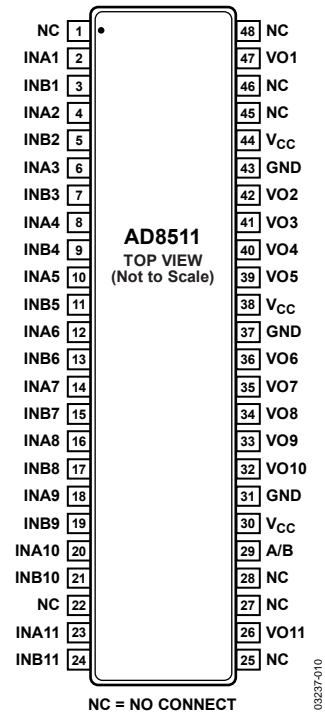


Figure 5. AD8511
48-Lead TSSOP (RV Suffix)

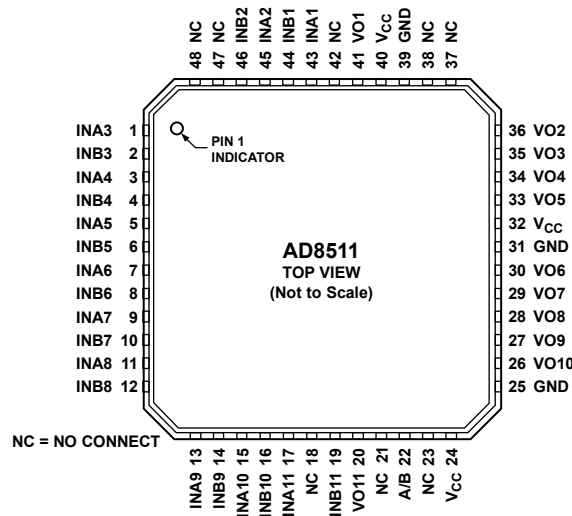


Figure 6. AD8511 (48-Lead LFCSP)

Table 5. Pin Function Descriptions

Pin No.			Mnemonic	Description
AD8509 (TSSOP)	AD8511 (TSSOP)	AD8511 (LFCSP)		
4, 6, 8, 10, 12, 14, 16, 18, 20	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 23	1, 3, 5, 7, 9, 11, 13, 15, 17, 43, 45	INAx	MUX Input
5, 7, 9, 11, 13, 15, 17, 19, 21	3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 24	2, 4, 6, 8, 10, 12, 14, 16, 19, 44, 46	INBx	MUX Input
32 to 36, 39 to 42	26, 32 to 36, 39 to 42, 47	20, 26 to 30, 33 to 36, 41	VOx	MUX Output
29	29	22	A/B	Input Selection Pin
30, 38, 44	30, 38, 44	24, 32, 40	Vcc	Bias
31, 37, 43	31, 37, 43	25, 31, 39	GND	Ground
1 to 3, 22 to 28, 45 to 48	1, 22, 25, 27, 28, 45, 46, 48	18, 21, 23, 37, 38, 42, 47, 48	NC	No Connection

TYPICAL PERFORMANCE CHARACTERISTICS

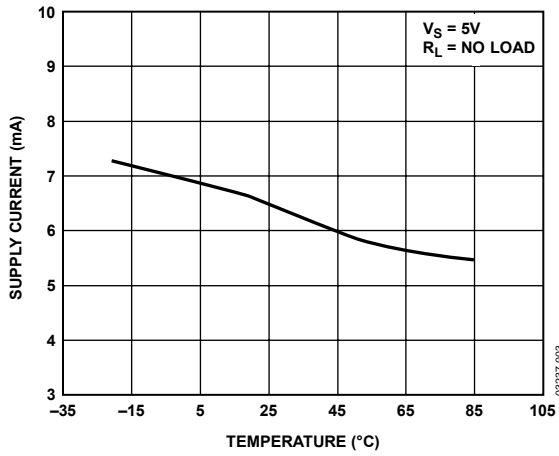


Figure 7. Supply Current vs. Temperature

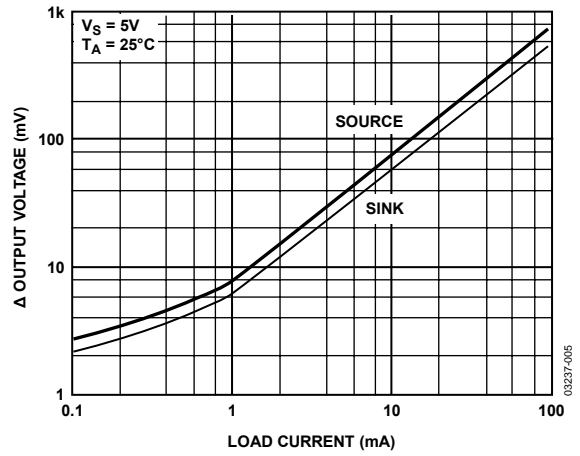


Figure 9. Output Voltage to Supply Rail vs. Load Current

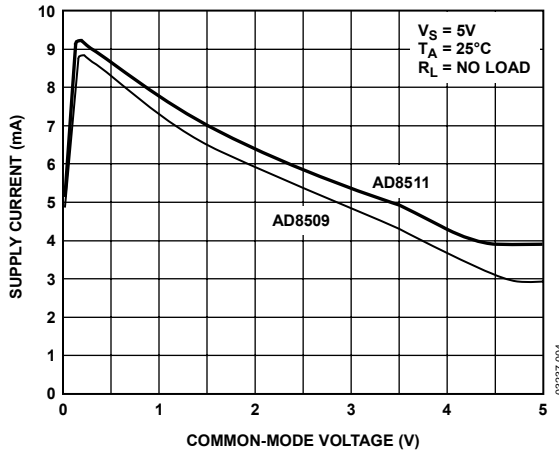


Figure 8. Supply Current vs. Common-Mode Voltage

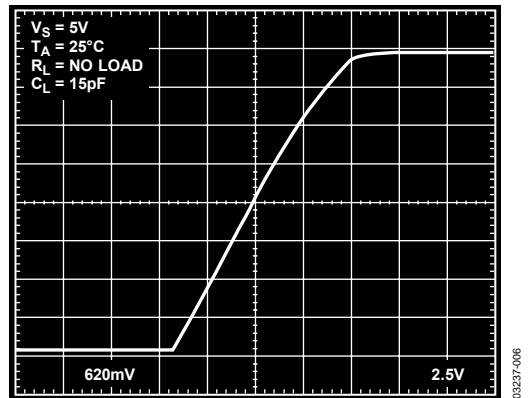


Figure 10. Large Signal Transient Response—Rising

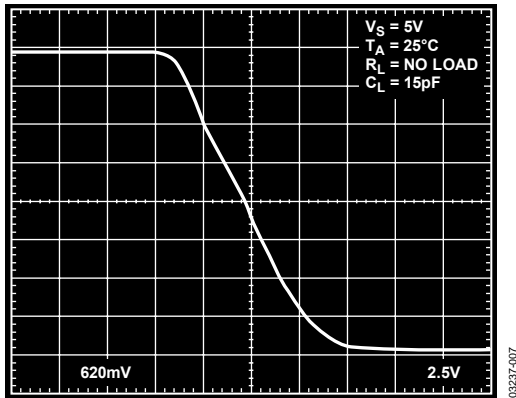


Figure 11. Large Signal Transient Response—Falling

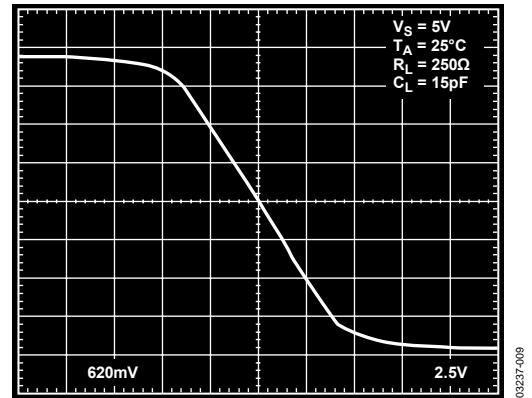


Figure 13. Large Signal Transient Response—Falling

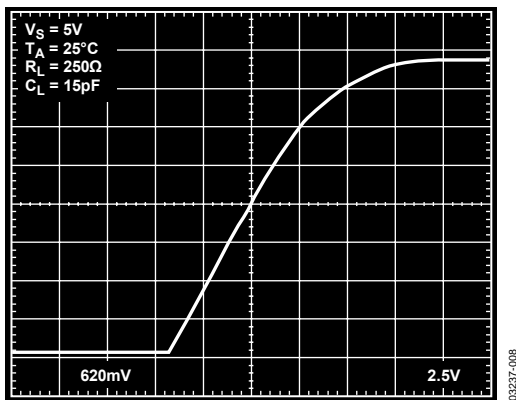


Figure 12. Large Signal Transient Response—Rising

APPLICATIONS

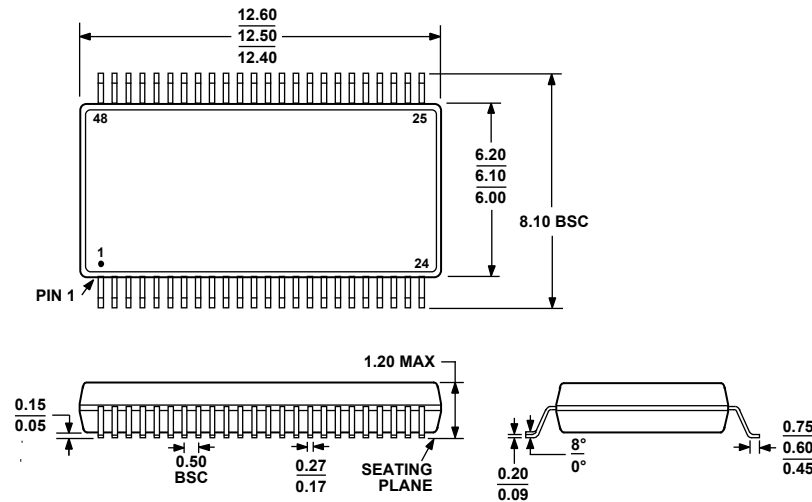
The AD8509 and AD8511 are CMOS buffers with A/B inputs that are used to select between two different reference voltages set up by an external resistor ladder. Input bias currents are orders of magnitude less than competitive parts. This allows very large resistor ladders to be used to save supply current. A guaranteed value of 50 nA is much higher than actual values and is limited by leakage in the test system.

Buffer outputs are designed to drive resistive loads. They are also stable with capacitive loads, so no resistors should be used in series with these outputs to attain the best display performance. Outputs have high slew rates and 6 μ s settling times. Each output can deliver a minimum of 120 mA, assuring fast response to varying loads.

The AD8509 is a 9-channel buffer and is similar to the LMC6009 in functionality. The AD8511 is an 11-channel buffer similar to the CL-FP6131. However, the control to select either 9- or 11-channel operation, the EN_11 pin of the CL-FP6131, is not available on the AD8511. If 9-channel operation is desired, use the AD8509.

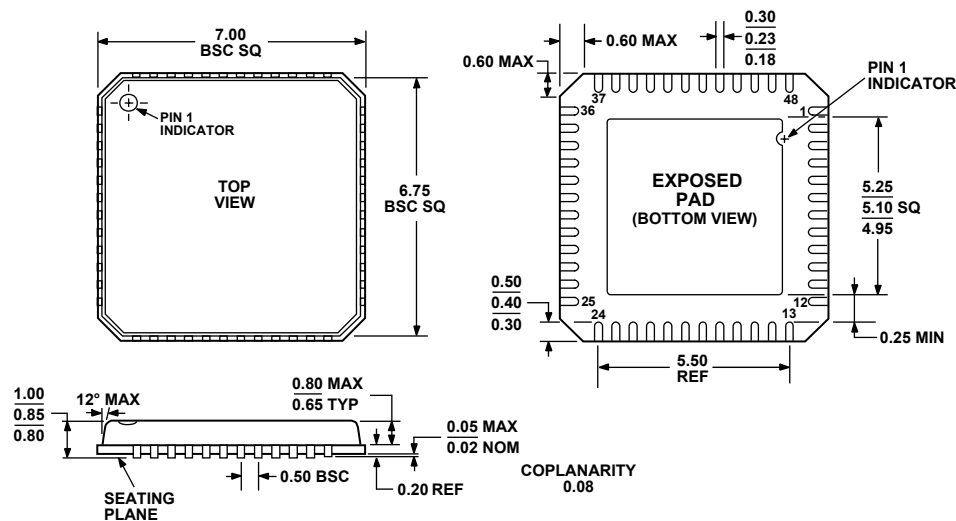
Power supply pins on the AD8509 and AD8511 have multiple ground and V_{CC} connections. Because of the high peak currents that these buffers can deliver, it is strongly recommended to connect all of the ground and V_{CC} pins, and suitably bypass the V_{CC} pins.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-ED

Figure 14. 48-Lead Thin Shrink Small Outline Package [TSSOP]
(RV-48)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKGD-2

Figure 15. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm x 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD8509ARU-REEL	-40°C to +85°C	48-Lead Thin Shrink Small Outline Package [TSSOP]	RV-48
AD8509ARUZ-REEL ²	-40°C to +85°C	48-Lead Thin Shrink Small Outline Package [TSSOP]	RV-48
AD8511ARU-REEL	-40°C to +85°C	48-Lead Thin Shrink Small Outline Package [TSSOP]	RV-48
AD8511ARUZ-REEL ²	-40°C to +85°C	48-Lead Thin Shrink Small Outline Package [TSSOP]	RV-48
AD8511ACPZ-REEL ²	-40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1

¹ All models only available in 2,500-piece reels.

² Z = Pb-free part.

AD8509/AD8511

NOTES

NOTES

AD8509/AD8511

NOTES

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- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management