THE DATASHEET OF

MAX9259GCB/V+

EVALUATION KIT AVAILABLE

MAX9259/MAX9260

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

General Description

The MAX9259 serializer pairs with the MAX9260 deserializer for joint transmission of high-speed video, audio, and control data.

The MAX9259/MAX9260 operate up to 3.125Gbps for a 15m shielded twisted-pair (STP) cable. This serial link supports display panels from QVGA (320 x 240) up to XGA (1280 x 768), or dual-view WVGA (2 x 854 x 480).

The embedded audio channel supports I²S up to 32 bits per sample and at a 192kHz sample rate. The embedded control channel forms a full-duplex, differential 100kbps to 1Mbps UART link between the serializer and deserializer. The host electronic control unit (ECU) or microcontroller (µC) resides either on the MAX9259 or on the MAX9260. In addition, the control channel enables ECU/µC control of peripherals in the remote side of the serial link through I²C/UART.

Preemphasis and channel equalization extend the link length and enhance the link reliability. Spread spectrum is available to reduce EMI on the serial and parallel output data signals. The differential link complies with the ISO 10605 and IEC 61000-4-2 ESD-protection standards.

The core supplies for the MAX9259/MAX9260 are 1.8V and 3.3V, respectively. Both devices use an I/O supply from 1.8V to 3.3V. These devices are available in a 64-pin TQFP package (10mm x 10mm) and a 56-pin TQFN/QFND package (8mm x 8mm x 0.75mm) with an exposed pad. Electrical performance is guaranteed over the -40°C to +105°C automotive temperature range.

Applications

High-Resolution Automotive Navigation

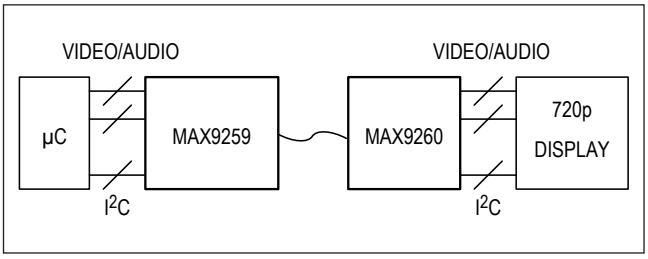
Rear-Seat Infotainment

Megapixel Camera Systems

Features

- **Ideal for Digital Video Applications**
  - **Up to XGA (1280 x 768) or Dual-View WVGA (2 x 854 x 480) Panels with 18- or 24-Bit Color**
  - **Pre/Deemphasis Allows 15m Cable at Full Speed**
  - **Up to 192kHz, 32-Bit Sample I²S**
- **Multiple Data Rates for System Flexibility**
  - **Up to 3.12Gbps Serial-Bit Rate**
  - **6.25MHz to 104MHz Pixel Clock**
  - **Up to 1Mbps UART/UART-to-I²C Control Channel**
- **Reduces EMI and Shielding Requirements**
  - **Serial Output Programmable for 100mV to 400mV**
  - **Programmable Spread Spectrum Reduces EMI**
  - **Bypasses Input PLL for Jitter Attenuation**
- **Peripheral Features for System Verification**
  - **Built-In Serial Link PRBS BER Tester**
  - **Interrupt Transmission from Deserializer to Serializer**
  - **Meets AEC-Q100 Requirements**
  - **-40°C to +105°C Operating Temperature Range**
  - **±10kV Contact and 25kV Air ISO 10605 and ±10kV IEC 61000-4-2 ESD Protection**

Simplified Diagram



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9259GCB/V+	-40°C to +105°C	64 TQFP-EP*
MAX9259GCB/V+T	-40°C to +105°C	64 TQFP-EP*
MAX9259GTN/V+T	-40°C to +105°C	56 TQFN-EP*
MAX9259GGN/VY+	-40°C to +105°C	56 QFND-EP*
MAX9260GCB/V+	-40°C to +105°C	64 TQFP-EP*
MAX9260GCB/V+T	-40°C to +105°C	64 TQFP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Typical Applications Circuit appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-4968; Rev 4; 10/14

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND
- MAX9259 ..... -0.5V to +1.9V
- MAX9260 ..... -0.5V to +3.9V

DVDD to GND (MAX9259) ..... -0.5V to +1.9V
DVDD to DGND (MAX9260) ..... -0.5V to +3.9V
IOVDD to GND (MAX9259) ..... -0.5V to +3.9V
IOVDD to IOGND (MAX9260) ..... -0.5V to +3.9V
Any Ground to Any Ground ..... -0.5V to +0.5V
OUT+, OUT- to AGND (MAX9259) ..... -0.5V to +1.9V
IN+, IN- to AGND (MAX9260) ..... -0.5V to +1.9V
LMN_ to GND (MAX9259)
- (60kΩ source impedance) ..... -0.5V to +3.9V

All Other Pins to GND (MAX9259) ..... -0.5V to (IOVDD + 0.5V)
All Other Pins to IOGND (MAX9260) ... -0.5V to (IOVDD + 0.5V)
OUT+, OUT- Short Circuit to Ground or Supply (MAX9259) ..... Continuous
IN+, IN- Short Circuit to Ground or Supply (MAX9260) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
- 64-Pin TQFP (derate 31.3mW/°C above +70°C) 2508mW
- 56-Pin TQFN (derate 47.6mW/°C above +70°C) 3809.5mW
- 56-Pin QFND (derate 42.7mW/°C above +70°C) 3148mW

Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

64 TQFP
- Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 31.9°C/W
- Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

56 TQFN
- Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 21°C/W
- Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

56 QFND
- Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 23.4°C/W
- Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1.6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAX9259 DC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (DIN_, PCLKIN, $\overline{PWDN}$, SSEN, BWS, ES, DRS, MS, CDS, $\overline{AUTOS}$, SD, SCK, WS)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}		-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUT (INT)							
High-Level Output Voltage	V_{OH1}	I_{OH} = -2mA		V_{IOVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS}	V_O = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	

MAX9259 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²C AND UART I/O, OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2)		-110		+5	µA
Low-Level Open-Drain Output Voltage	V_{OL2}	I_{OL} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
DIFFERENTIAL OUTPUT (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)		300	400	500	mV_{P-P}
		3.3dB preemphasis setting, $V_{OD(P)}$ (Figure 2)		350		610	
		3.3dB deemphasis setting, $V_{OD(D)}$ (Figure 2)		240		425	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}					15	mV
Output Offset Voltage, (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}					15	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-60			mA
		V_{OUT+} or V_{OUT-} = 1.9V				25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V				25	mA
Output Termination Resistance (Internal)	R_O	From OUT+, OUT- to V_{AVDD}		45	54	63	Ω
REVERSE CONTROL-CHANNEL RECEIVER (OUT+, OUT-)							
High Switching Threshold	V_{CHR}					27	mV
Low Switching Threshold	V_{CLR}			-27			mV
LINE-FAULT-DETECTION INPUT (LMN_)							
Short-to-GND Threshold	V_{TG}	Figure 3				0.3	V
Normal Thresholds	V_{TN}	Figure 3		0.57		1.07	V
Open Thresholds	V_{TO}	Figure 3		1.45		V_{IO+} 0.06	V
Open Input Voltage	V_{IO}	Figure 3		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	Figure 3		2.47			V
POWER SUPPLY							
Worst-Case Supply Current (Figure 4)	I_{WCS}	BWS = GND	f_{PCLKIN} = 16.6MHz		100	125	mA
			f_{PCLKIN} = 33.3MHz		105	145	
			f_{PCLKIN} = 66.6MHz		116	155	
			f_{PCLKIN} = 104MHz		135	175	
Sleep-Mode Supply Current	I_{CCS}				40	110	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = GND			5	70	µA

MAX9259 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

ESD PROTECTION					
OUT+, OUT- (Pin to EP)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±8	kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge	±10	
			Air discharge	±12	
		IEC 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge	±10	
			Air discharge	±25	
All Other Pins (to EP or Supply)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±4	µA

MAX9259 AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PARALLEL CLOCK INPUT (PCLKIN)							
Clock Frequency	f_{PCLKIN}	V_{BWS} = V_{GND}, V_{DRS} = V_{IOVDD}		8.33		16.66	MHz
		V_{BWS} = V_{GND}, V_{DRS} = V_{GND}		16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}		6.25		12.5	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{GND}		12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 5)		35	50	65	%
Clock Transition Time	t_R, t_F	(Figure 5)				4	ns
Clock Jitter	t_J	3.125Gbps, 300kHz sinusoidal jitter				800	$ps_{(P-P)}$
I²C/UART PORT TIMING (Note 3)							
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD		20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD		20		150	ns
Input Setup Time	t_{SET}	I²C only (Figure 6)		100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 6)		0			ns
SWITCHING CHARACTERISTICS (Note 3)							
Differential Output Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial-data rate = 3.125Gbps			90	150	ps
Total Serial Output Jitter	t_{TSOJ1}	3.125Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)			0.25		UI
Deterministic Serial Output Jitter	t_{DSOJ2}	3.125Gbps PRBS signal			0.15		UI
Parallel Data Input Setup Time	t_{SET}	(Figure 8)		1			ns
Parallel Data Input Hold Time	t_{HOLD}	(Figure 8)		1.5			ns
Serializer Delay (Note 4)	t_{SD}	(Figure 9)	Spread spectrum enabled			2830	Bits
			Spread spectrum disabled			270	
Link Start Time	t_{LOCK}	(Figure 10)				3.5	ms
Power-Up Time	t_{PU}	(Figure 11)				3.5	ms
I²S INPUT TIMING							
WS Frequency	f_{WS}	(Table 2)		8		192	kHz
Sample Word Length	n_{WS}	(Table 2)		4		32	Bits
SCK Frequency	f_{SCK}	f_{SCK} = f_{WS} x n_{WS} x 2		(8 x 4) x 2		(192 x 32) x 2	kHz
SCK Clock High Time (Note 3)	t_{HC}	V_{SCK} ≥ V_{IH}, t_{SCK} = 1/f_{SCK}		0.35 x t_{SCK}			ns
SCK Clock Low Time (Note 3)	t_{LC}	V_{SCK} ≤ V_{IL}, t_{SCK} = 1/f_{SCK}		0.35 x t_{SCK}			ns
SD, WS Setup Time	t_{SET}	(Figure 12, Note 3)		2			ns
SD, WS Hold Time	t_{HOLD}	(Figure 12, Note 3)		2			ns

MAX9260 DC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS ($\overline{ENABLE}$, INT, $\overline{PWDN}$, SSEN, BWS, ES, DRS, MS, CDS, EQS, DCS)								
High-Level Input Voltage	V_{IH1}				0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}						0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}			-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA					-1.5	V
SINGLE-ENDED OUTPUTS (DOUT_, SD, WS, SCK, PCLKOUT)								
High-Level Output Voltage	V_{OH}	I_{OH} = -2mA	V_{DCS} = V_{IOGND}		V_{IOVDD} - 0.3			V
			V_{DCS} = V_{IOVDD}		V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2mA	V_{DCS} = V_{IOGND}				0.3	V
			V_{DCS} = V_{IOVDD}				0.2	
Output Short-Circuit Current	I_{OS}	DOUT_, SD, WS, SCK	V_O = 0V, V_{DCS} = V_{IOGND}	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
				V_{IOVDD} = 1.7V to 1.9V	3	7	13	
			V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
				V_{IOVDD} = 1.7V to 1.9V	5	10	21	
		PCLKOUT	V_O = 0V, V_{DCS} = V_{IOGND}	V_{IOVDD} = 3.0V to 3.6V	15	33	50	
				V_{IOVDD} = 1.7V to 1.9V	5	10	17	
			V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 3.0V to 3.6V	30	54	97	
				V_{IOVDD} = 1.7V to 1.9V	9	16	32	
I²C AND UART I/O, OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL, $\overline{ERR}$, GPIO_, LOCK)								
High-Level Input Voltage	V_{IH2}				0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}						0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2)	RX/SDA, TX/SCL		-110		+1	µA
			GPIO, $\overline{ERR}$, LOCK		-80		+1	
Low-Level Open-Drain Output Voltage	V_{OL2}	I_{OL} = 3mA	V_{IOVDD} = 1.7V to 1.9V				0.4	V
			V_{IOVDD} = 3.0V to 3.6V				0.3	V

MAX9260 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIFFERENTIAL OUTPUTS FOR REVERSE CONTROL CHANNEL (IN+, IN-)							
Differential High Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROH}	No high-speed data transmission (Figure 13)		30		60	mV
Differential Low Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROL}	No high-speed data transmission (Figure 13)		-60		-30	mV
DIFFERENTIAL INPUTS (IN+, IN-)							
Differential High Input Threshold (Peak), (V_{IN}+) - (V_{IN}-)	$V_{IDH(P)}$	(Figure 14)			40	90	mV
Differential Low Input Threshold (Peak), (V_{IN}+) - (V_{IN}-)	$V_{IDL(P)}$	(Figure 14)		-90	-40		mV
Input Common-Mode Voltage, ((V_{IN}+) + (V_{IN}-))/2	V_{CMR}			1	1.3	1.6	V
Differential Input Resistance (Internal)	R_I			80	100	130	Ω
POWER SUPPLY							
Worst-Case Supply Current (Figure 15)	I_{WCS}	V_{BWS} = V_{IOGND}, $f_{PCLKOUT}$ = 16.6MHz	2% spread spectrum active		113	166	mA
			Spread spectrum disabled		105	155	
		V_{BWS} = V_{IOGND}, $f_{PCLKOUT}$ = 33.3MHz	2% spread spectrum active		122	181	
			Spread spectrum disabled		110	165	
		V_{BWS} = V_{IOGND}, $f_{PCLKOUT}$ = 66.6MHz	2% spread spectrum active		137	211	
			Spread spectrum disabled		120	188	
		V_{BWS} = V_{IOGND}, $f_{PCLKOUT}$ = 104MHz	2% spread spectrum active		159	247	
			Spread spectrum disabled		135	214	
Sleep-Mode Supply Current	I_{CCS}				80	130	µA
Power-Down Supply Current	I_{CCZ}	$V_{\overline{PWDN}}$ = V_{IOGND}			19	70	µA

MAX9260 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

ESD PROTECTION					
IN+, IN- (Pin to EP)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±8	kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge	±8	
			Air discharge	±10	
		IEC 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge	±8	
			Air discharge	±20	
All Other Pins (to EP or Supply)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±4	µA

MAX9260 AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)							
Clock Frequency	$f_{PCLKOUT}$	V_{BWS} = V_{IOGND}, V_{DRS} = V_{IOVDD}		8.33		16.66	MHz
		V_{BWS} = V_{IOGND}, V_{DRS} = V_{IOGND}		16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}		6.25		12.5	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOGND}		12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 16)		40	50	60	%
Clock Jitter	t_J	Period jitter, RMS, spread off, 3.125Gbps, PRBS pattern, UI = 1/$f_{PCLKOUT}$			0.05		UI
I²C/UART PORT TIMING							
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD		20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD		20		150	ns
Input Setup Time	t_{SET}	I²C only		100			ns
Input Hold Time	t_{HOLD}	I²C only		0			ns
SWITCHING CHARACTERISTICS							
PCLKOUT Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.4		2.2	ns
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.5		2.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.25		1.7	
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.3		2.0	
Parallel Data Rise-and-Fall Time (Figure 17)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.5		3.1	ns
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.6		3.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.3		2.2	
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.4		2.4	
Deserializer Delay	t_{SD}	Spread spectrum enabled (Figure 18)				2880	Bits
		Spread spectrum disabled (Figure 18)				750	
Lock Time	t_{LOCK}	Spread spectrum enabled (Figure 19)				1500	µs
		Spread spectrum off (Figure 19)				1000	
Power-Up Time	t_{PU}	(Figure 20)				2500	µs
Reverse Control-Channel Output Rise Time	t_R	No high-speed transmission (Figure 13)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No high-speed transmission (Figure 13)		180		400	ns

MAX9260 AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

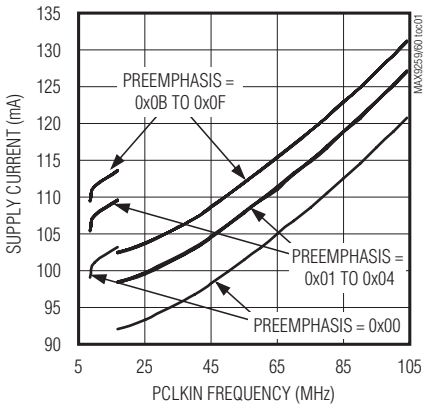
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²S OUTPUT TIMING							
WS Jitter	t_{AJ-WS}	t_{WS} = 1/f_{WS}, rising (falling) edge to falling (rising) edge (Note 5)	f_{WS} = 48kHz or 44.1kHz		0.4e - 3 x t_{WS}	0.5e - 3 x t_{WS}	ns
			f_{WS} = 96kHz		0.8e - 3 x t_{WS}	1e - 3 x t_{WS}	
			f_{WS} = 192kHz		1.6e - 3 x t_{WS}	2e - 3 x t_{WS}	
SCK Jitter	t_{AJ-SCK}	t_{SCK} = 1/f_{SCK}, rising edge to rising edge	n_{WS} = 16 bits, f_{WS} = 48kHz or 44.1kHz		13e - 3 x t_{SCK}	16e - 3 x t_{SCK}	ns
			n_{WS} = 24 bits, f_{WS} = 96kHz		39e - 3 x t_{SCK}	48e - 3 x t_{SCK}	
			n_{WS} = 32 bits, f_{WS} = 192kHz		0.1 x t_{SCK}	0.13 x t_{SCK}	
Audio Skew Relative to Video	ASK	Video and audio synchronized			3 x t_{WS}	4 x t_{WS}	µs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.3		3.1	ns
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.4		3.8	ns
SD, WS Valid Time Before SCK	t_{DVB}	t_{SCK} = 1/f_{SCK} (Figure 21)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{DVA}	t_{SCK} = 1/f_{SCK} (Figure 21)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns

Note 2: Minimum I_{IN} due to voltage drop across the internal pullup resistor.
Note 3: Not production tested.
Note 4: Bit time = 1/(30 x $f_{RXCLKIN}$) (BWS = 0), = 1/(40 x $f_{RXCLKIN}$) (BWS = V_{IOVDD}).
Note 5: Rising to rising edge jitter can be twice as large.

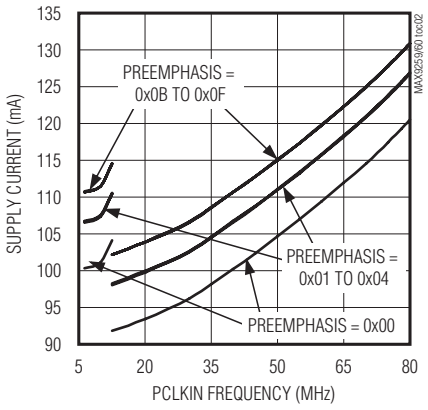
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V (MAX9259), V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V (MAX9260), T_A = +25°C, unless otherwise noted.)

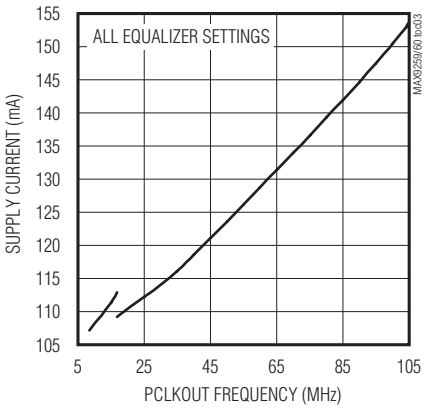
MAX9259 SUPPLY CURRENT vs. PCLKIN FREQUENCY (24-BIT MODE)



MAX9259 SUPPLY CURRENT vs. PCLKIN FREQUENCY (32-BIT MODE)



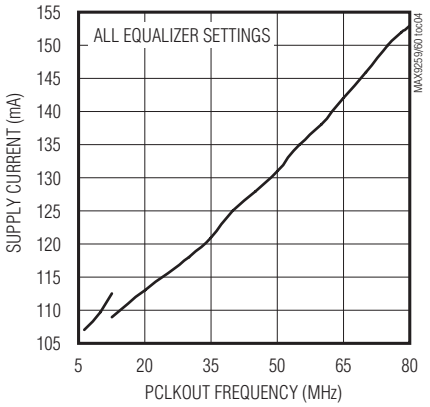
MAX9260 SUPPLY CURRENT vs. PCLKOUT FREQUENCY (24-BIT MODE)



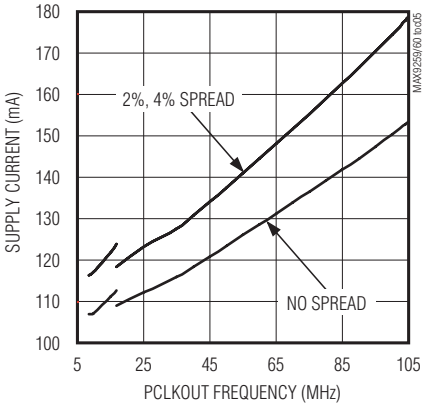
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V (MAX9259), V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V (MAX9260), T_A = +25°C, unless otherwise noted.)

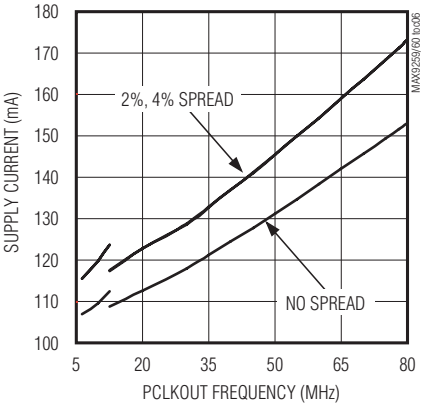
MAX9260 SUPPLY CURRENT vs. PCLKOUT FREQUENCY (32-BIT MODE)



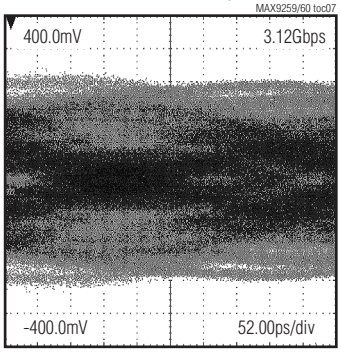
MAX9260 SUPPLY CURRENT vs. PCLKOUT FREQUENCY (24-BIT MODE)



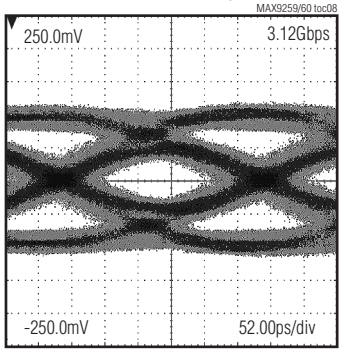
MAX9260 SUPPLY CURRENT vs. PCLKOUT FREQUENCY (32-BIT MODE)



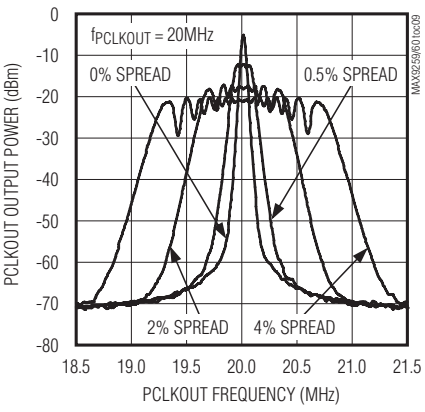
SERIAL LINK SWITCHING PATTERN WITHOUT PREEMPHASIS (PARALLEL BIT RATE = 104MHz, 10m STP CABLE)



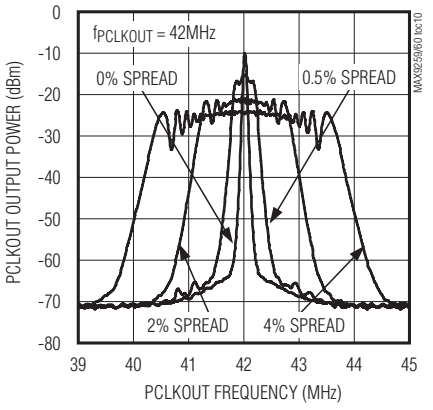
SERIAL LINK SWITCHING PATTERN WITH 14dB PREEMPHASIS (PARALLEL BIT RATE = 104MHz, 10m STP CABLE)



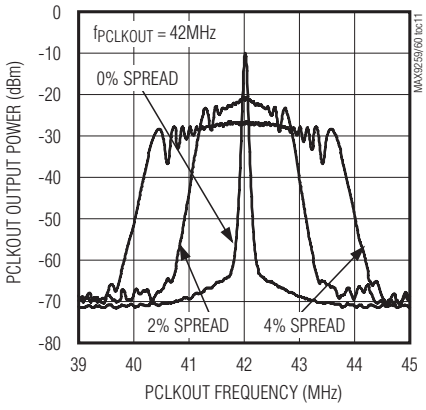
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (MAX9259 SPREAD ON, MAX9260 SPREAD OFF)



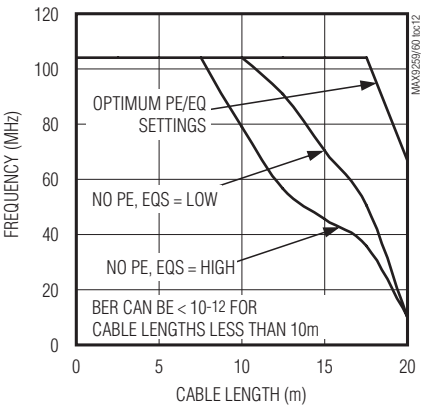
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (MAX9259 SPREAD ON, MAX9260 SPREAD OFF)



OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (MAX9260 SPREAD ON, MAX9259 SPREAD OFF)

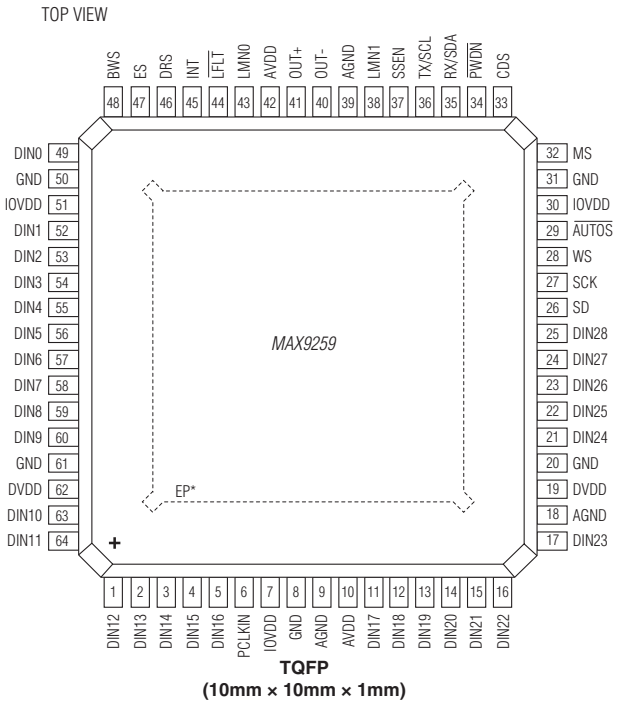


MAXIMUM PCLKIN FREQUENCY vs. STP CABLE LENGTH (BER < 10^{-9})

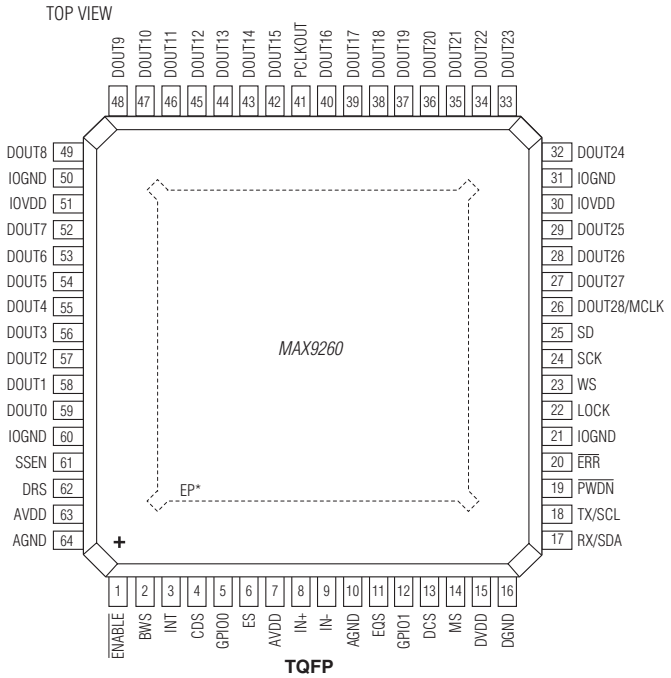


Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

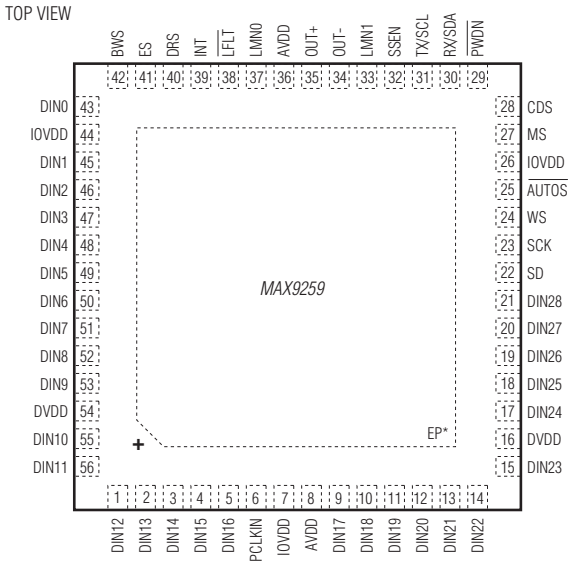
Pin Configurations



TQFP
(10mm × 10mm × 1mm)



TQFP
(10mm × 10mm × 1mm)



TQFN/QFND
(8mm x 8mm x 0.75mm)

*CONNECT EP TO GROUND PLANE

MAX9259 Pin Description

PIN		NAME	FUNCTION
TQFP	TQFN/QFND		
1–5, 11–17, 21–25, 49, 52–60, 63, 64	1–5, 9–15, 17–21, 43, 45–53, 55, 56	DIN0–DIN28	Data Input[0:28]. Parallel data inputs. All pins internally pulled down to GND. Selected edge of PCLKIN latches input data. Set BWS = low (24-bit mode) to use DIN0–DIN20 (RGB and SYNC). DIN21–DIN28 are not used in 24-bit mode. Set BWS = high (32-bit mode) to use DIN0–DIN28 (RGB, SYNC, and two extra inputs).
6	6	PCLKIN	Parallel Clock Input. Latches parallel data inputs and provides the PLL reference clock.
7, 30, 51	7, 26, 44	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to IOVDD.
8, 20, 31, 50, 61	—	GND	Digital and I/O Ground
9, 18, 39	—	AGND	Analog Ground
10, 42	8, 36	AVDD	1.8V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to AVDD.
19, 62	16, 54	DVDD	1.8V Digital Power Supply. Bypass DVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
26	22	SD	I^2S Serial-Data Input with Internal Pulldown to GND. Disable I^2S to use SD as an additional data input latched on the selected edge of PCLKIN.
27	23	SCK	I^2S Serial-Clock Input with Internal Pulldown to GND
28	24	WS	I^2S Word-Select Input with Internal Pulldown to GND
29	25	$\overline{AUTOS}$	Autostart Setting. Active-low power-up mode selection input requires external pulldown or pullup resistors. Set $\overline{AUTOS}$ = high to power up the device with no link active. Set $\overline{AUTOS}$ = low to have the MAX9259 power up the serial link with autorange detection (see Tables 11 and 12).
32	27	MS	Mode Select. Control-link mode-selection input requires external pulldown or pullup resistors. Set MS = low, to select base mode. Set MS = high to select the bypass mode.
33	28	CDS	Control-Direction Selection. Control-link-direction selection input requires external pulldown or pullup resistors. Set CDS = low for µC use on the MAX9259 side of the serial link. Set CDS = high for µC use on the MAX9260 side of the serial link.
34	29	$\overline{PWDN}$	Power-Down. Active-low power-down input requires external pulldown or pullup resistors.
35	30	RX/SDA	Receive/Serial Data. UART receive or I^2C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the MAX9259's UART. In I^2C mode, RX/SDA is the SDA input/output of the MAX9259's I^2C master.

MAX9259 Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	TQFN/QFND		
36	31	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the MAX9259's UART. In I²C mode, TX/SCL is the SCL output of the MAX9259's I²C master.
37	32	SSEN	Spread-Spectrum Enable. Serial link spread-spectrum enable input requires external pulldown or pullup resistors. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±0.5% spread spectrum on the serial link. Set SSEN = low to use the serial link without spread spectrum.
38	33	LMN1	Line-Fault Monitor Input 1 (see Figure 3 for details)
40, 41	34, 35	OUT-, OUT+	Differential CML Output –/+. Differential outputs of the serial link.
43	37	LMN0	Line-Fault Monitor Input 0 (see Figure 3 for details)
44	38	$\overline{LFLT}$	Line Fault. Active-low open-drain line-fault output with a 60kΩ internal pullup resistor. $\overline{LFLT}$ = low indicates a line fault. $\overline{LFLT}$ is output high when $\overline{PWDN}$ = low.
45	39	INT	Interrupt Output to Indicate Remote Side Requests. INT = low upon power-up and when $\overline{PWDN}$ = low. A transition on the INT input of the MAX9260 toggles the MAX9259's INT output.
46	40	DRS	Data-Rate Select. Data-rate range-selection input requires external pulldown or pullup resistors. Set DRS = high for parallel input data rates of 8.33MHz to 16.66MHz (24-bit mode) or 6.25MHz to 12.5MHz (32-bit mode). Set DRS = low for parallel input data rates of 16.66MHz to 104MHz (24-bit mode) or 12.5MHz to 78MHz (32-bit mode).
47	41	ES	Edge Select. PCLKIN trigger edge-selection input requires external pulldown or pullup resistors. Set ES = low to trigger on the rising edge of PCLKIN. Set ES = high to trigger on the falling edge of PCLKIN.
48	42	BWS	Bus-Width Select. Parallel input bus-width selection input requires external pulldown or pullup resistors. Set BWS = low for 24-bit bus mode. Set BWS = high for 32-bit bus mode.
—	—	EP	Exposed Pad. EP internally connected to AGND (TQFP package) or AGND and GND (TQFN package). **MUST** externally connect EP to the AGND plane to maximize thermal and electrical performance.

MAX9260 Pin Description

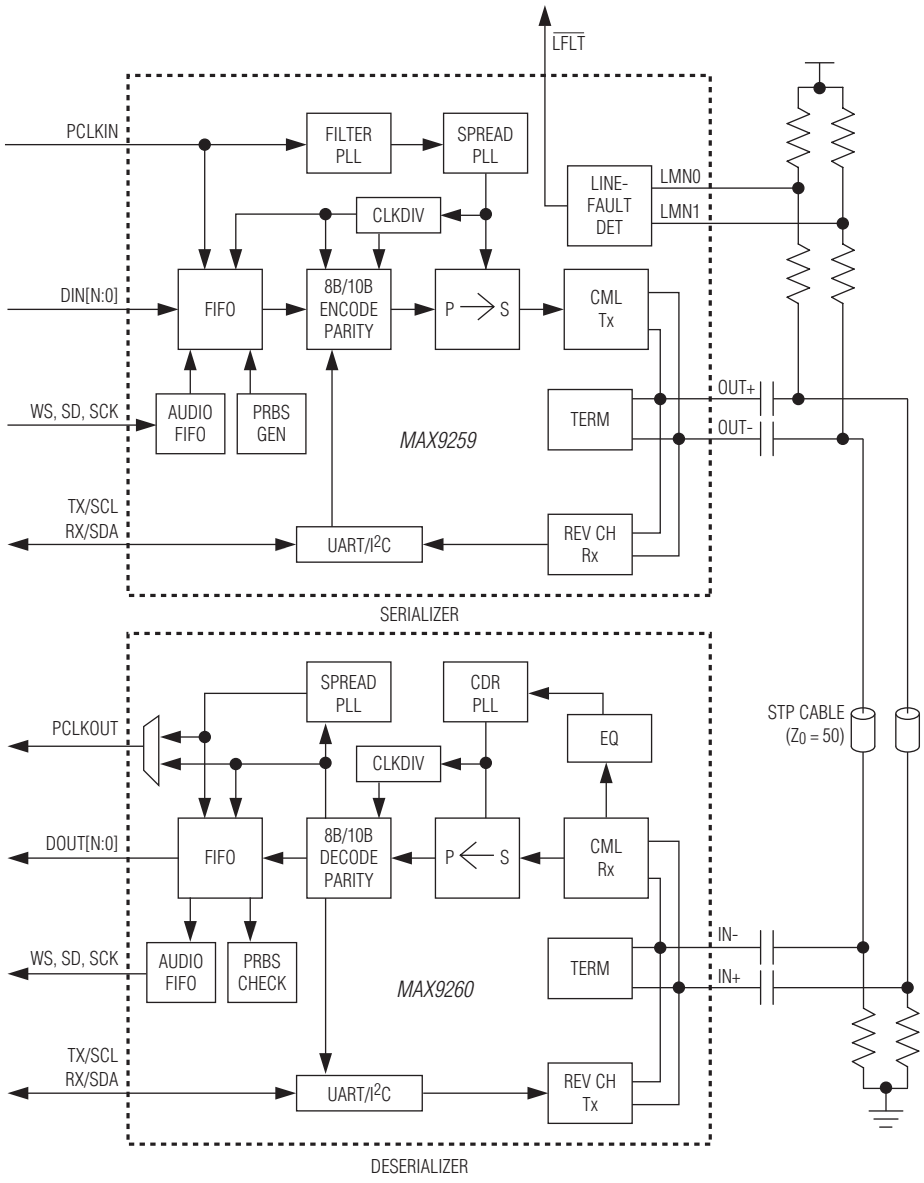
PIN	NAME	FUNCTION
1	$\overline{\text{ENABLE}}$	Enable. Active-low parallel output-enable input requires external pulldown or pullup resistors. Set $\overline{\text{ENABLE}}$ = low to enable PCLKOUT, SD, SCK, WS, and the parallel outputs, DOUT_. Set $\overline{\text{ENABLE}}$ = high to put PCLKOUT, SD, SCK, WS, and DOUT_ to high impedance.
2	BWS	Bus-Width Select. Parallel output bus-width selection input requires external pulldown or pullup resistors. Set BWS = low for 24-bit bus mode. Set BWS = high for 32-bit bus mode.
3	INT	Interrupt. Interrupt input requires external pulldown or pullup resistors. A transition on the INT input of the MAX9260 toggles the MAX9259's INT output.
4	CDS	Control-Direction Selection. Control-link-direction selection input requires external pulldown or pullup resistors. Set CDS = low for µC use on the MAX9259 side of the serial link. Set CDS = high for µC use on the MAX9260 side of the serial link.
5	GPIO0	GPIO0. Open-drain general-purpose input/output with internal 60kΩ pullup resistors to IOVDD. GPIO0 is high impedance during power-up and when $\overline{\text{PWDN}}$ = low.
6	ES	Edge Select. PCLKOUT edge-selection input requires external pulldown or pullup resistors. Set ES = low for a rising-edge trigger. Set ES = high for a falling-edge trigger.
7, 63	AVDD	3.3V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to AVDD.
8 , 9	IN+, IN-	Differential CML Input +/−. Differential inputs of the serial link.
10, 64	AGND	Analog Ground
11	EQS	Equalizer Select. Deserializer equalizer-selection input requires external pulldown or pullup resistors. The state of EQS latches upon power-up or rising edge of $\overline{\text{PWDN}}$. Set EQS = low for 10.7dB equalizer boost (EQTUNE = 1001). Set EQS = high for 5.2dB equalizer boost (EQTUNE = 0100).
12	GPIO1	GPIO1. Open-drain general-purpose input/output with internal 60kΩ pullup resistors to IOVDD. GPIO1 is high impedance during power-up and when $\overline{\text{PWDN}}$ = low.
13	DCS	Drive Current Select. Driver current-selection input requires external pulldown or pullup resistors. Set DCS = high for stronger parallel data and clock output drivers. Set DCS = low for normal parallel data and clock drivers (see the *MAX9260 DC Electrical Characteristics* table).
14	MS	Mode Select. Control-link mode-selection/autostart mode selection input requires external pulldown or pullup resistors. MS sets the control-link mode when CDS = high (see the *Control-Channel and Register Programming* section). Set MS = low to select base mode. Set MS = high to select the bypass mode. MS sets autostart mode when CDS = low (see Tables 11 and 12).
15	DVDD	3.3V Digital Power Supply. Bypass DVDD to DGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
16	DGND	Digital Ground
17	RX/SDA	Receive/Serial Data. UART receive or I^2C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the MAX9260's UART. In I^2C mode, RX/SDA is the SDA input/output of the MAX9259's I^2C master.

MAX9260 Pin Description (continued)

PIN	NAME	FUNCTION
18	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the MAX9259's UART. In I²C mode, TX/SCL is the SCL output of the MAX9260's I²C master.
19	$\overline{PWDN}$	Power-Down. Active-low power-down input requires external pulldown or pullup resistors.
20	$\overline{ERR}$	Error. Active-low open-drain video data error output with internal pullup to IOVDD. $\overline{ERR}$ goes low when the number of decoding errors during normal operation exceed a programmed error threshold or when at least one PRBS error is detected during PRBS test. $\overline{ERR}$ is output high when $\overline{PWDN}$ = low.
21, 31, 50, 60	IOGND	Input/Output Ground
22	LOCK	Open-Drain Lock Output with Internal Pullup to IOVDD. LOCK = high indicates PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates PLLs are not locked or incorrect serial-word-boundary alignment. LOCK remains low when the configuration link is active. LOCK is output high when $\overline{PWDN}$ = low.
23	WS	Word Select. I²S word-select output.
24	SCK	Serial Clock. I²S serial-clock output
25	SD	Serial Data. I²S serial-data output. Disable I²S to use SD as an additional data output latched on the selected edge of PCLKOUT.
26–29, 32–40, 42–49, 52–59	DOUT0–DOUT27, DOUT28/MCLK	Data Output[0:28]. Parallel data outputs. Output data can be strobed on the selected edge of PCLKOUT. Set BWS = low (24-bit mode) to use DOUT0–DOUT20 (RGB and SYNC). DOUT21–DOUT28 are not used in 24-bit mode and are set to low. Set BWS = high (32-bit mode) to use DOUT0–DOUT28 (RGB, SYNC, and two extra outputs). DOUT28 can be used to output MCLK (see the *Additional MCLK Output for Audio Applications* section).
30, 51	IOVDD	1.8V to 3.3V Logic I/O Power Supply. Bypass IOVDD to IOGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to IOVDD.
41	PCLKOUT	Parallel Clock Output. Used for DOUT0–DOUT28.
61	SSEN	Spread-Spectrum Enable. Parallel output spread-spectrum enable input requires external pulldown or pullup resistors. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±2% spread spectrum on the parallel outputs. Set SSEN = low to use the parallel outputs without spread spectrum.
62	DRS	Data-Rate Select. Data-rate range-selection input requires external pulldown or pullup resistors. Set DRS = high for parallel input data rates of 8.33MHz to 16.66MHz (24-bit mode) or 6.25MHz to 12.5MHz (32-bit mode). Set DRS = low for parallel input data rates of 16.66MHz to 104MHz (24-bit mode) or 12.5MHz to 78MHz (32-bit mode).
—	EP	Exposed Pad. EP internally connected to AGND. **MUST** externally connect EP to the AGND plane to maximize thermal and electrical performance.

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

Functional Diagram



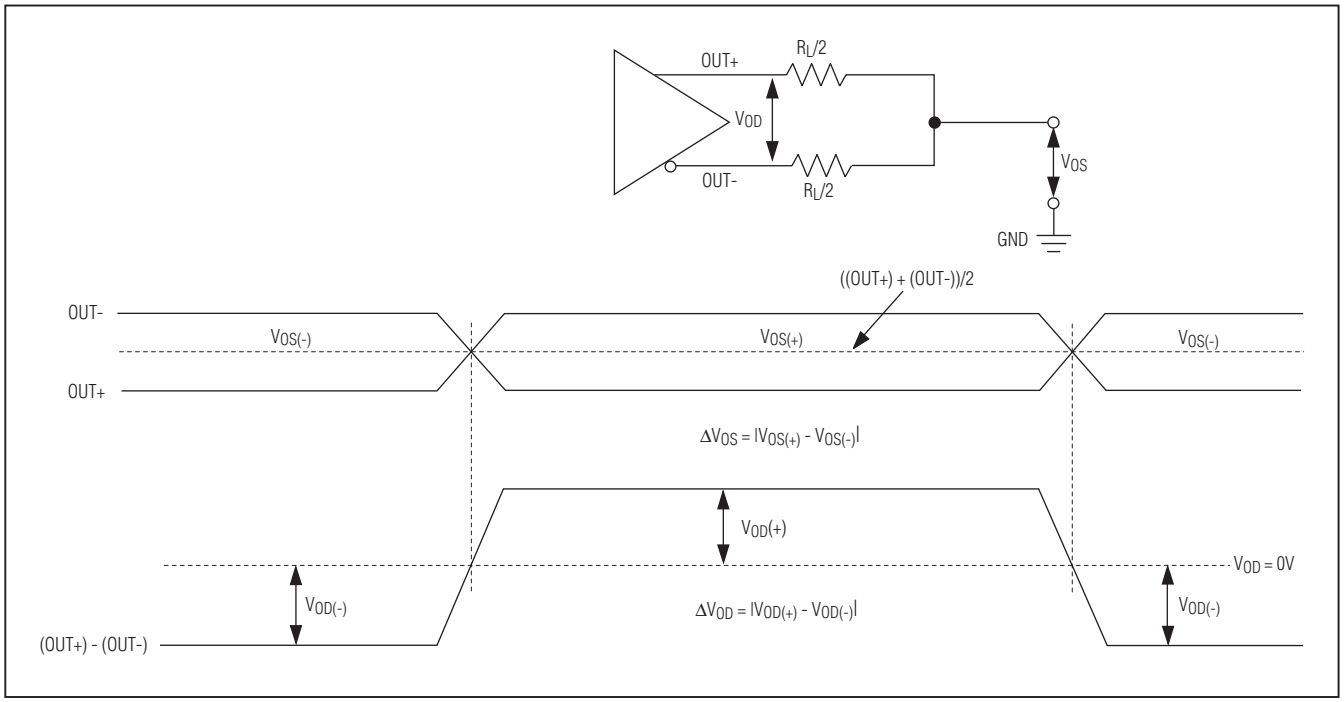


Figure 1. MAX9259 Serial Output Parameters

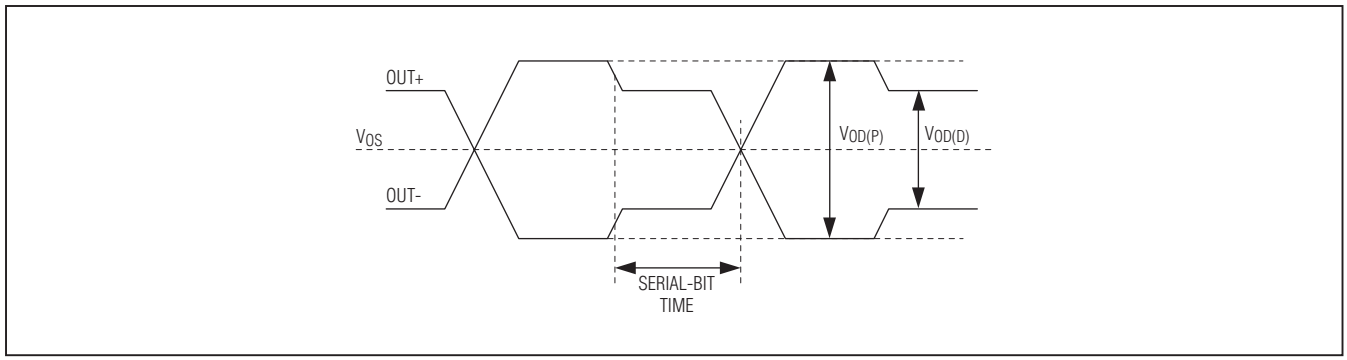


Figure 2. Output Waveforms at OUT+ and OUT-

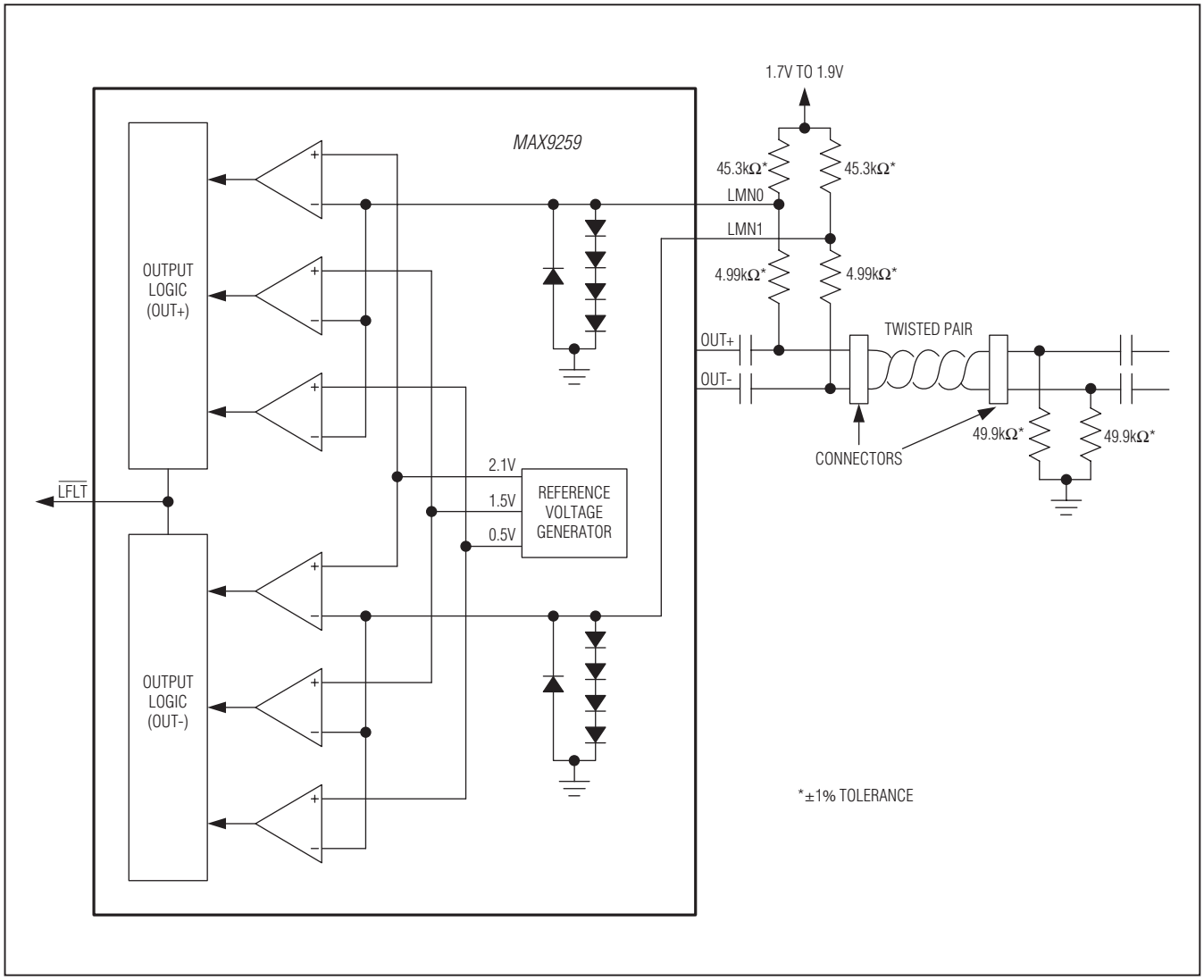


Figure 3. Fault-Detector Circuit

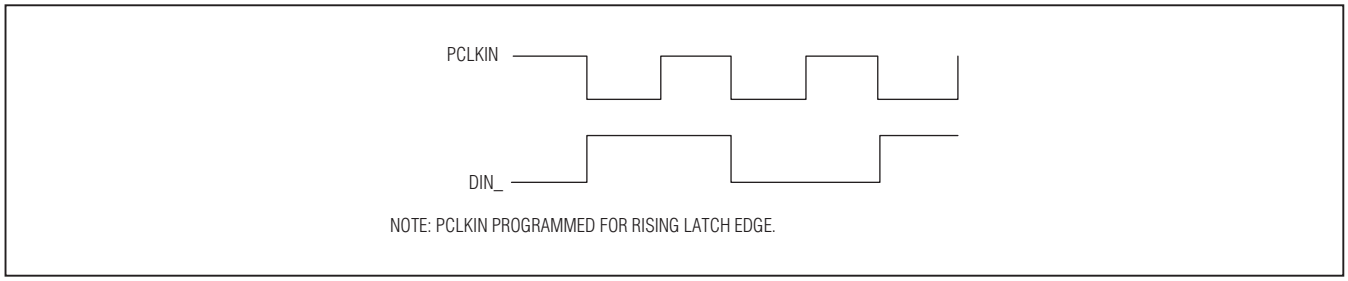


Figure 4. MAX9259 Worst-Case Pattern Input

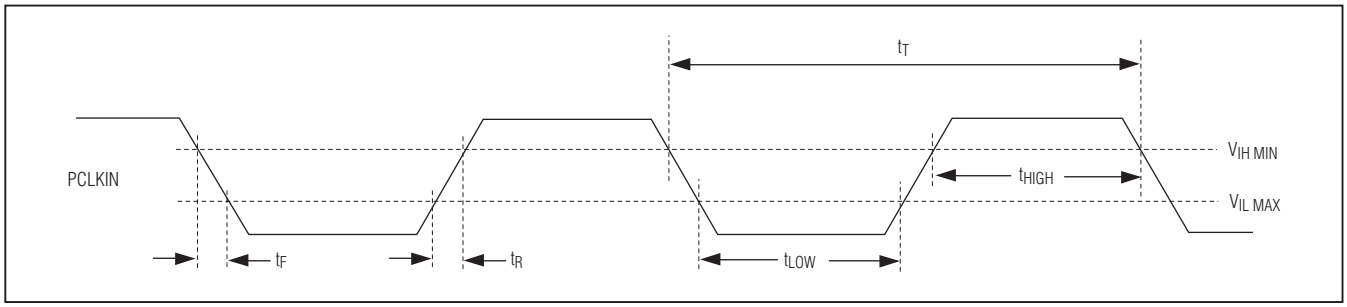


Figure 5. MAX9259 Parallel Input Clock Requirements

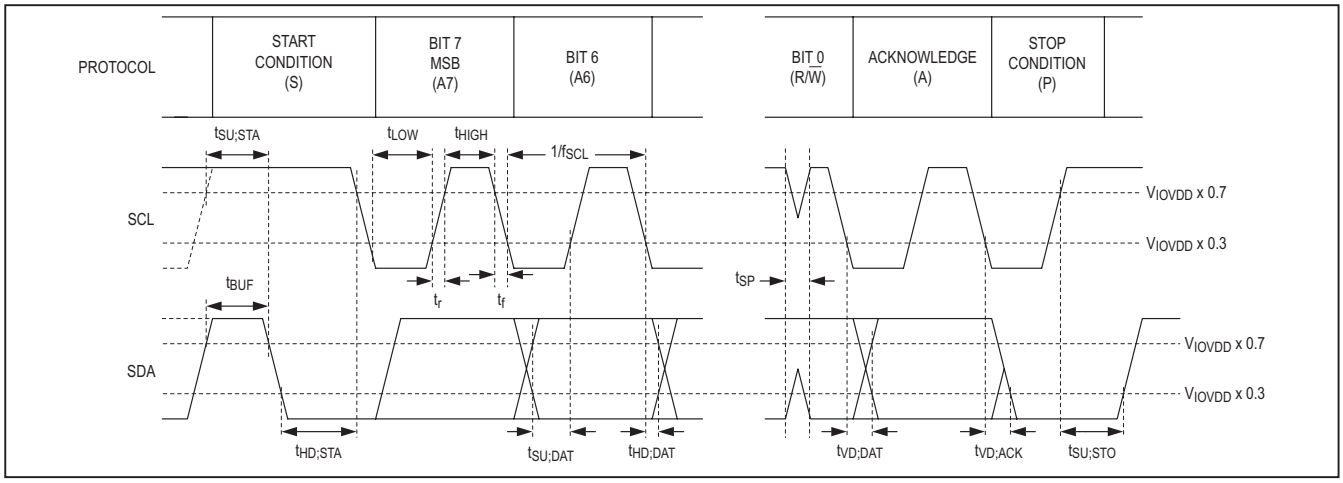


Figure 6. I²C Timing Parameters

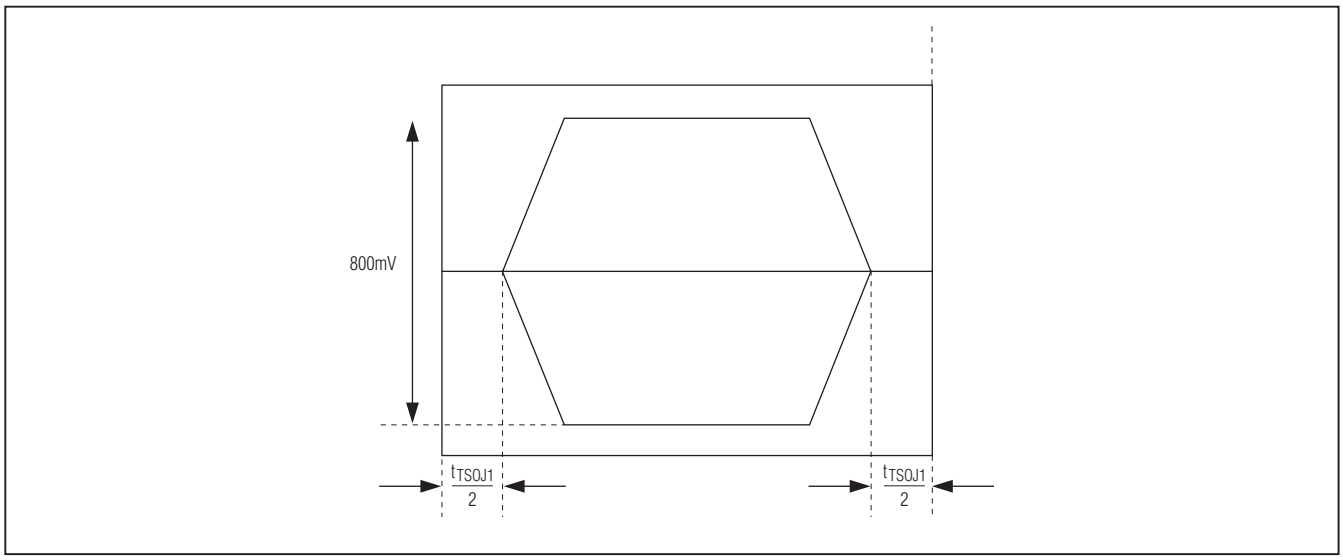


Figure 7. Differential Output Template

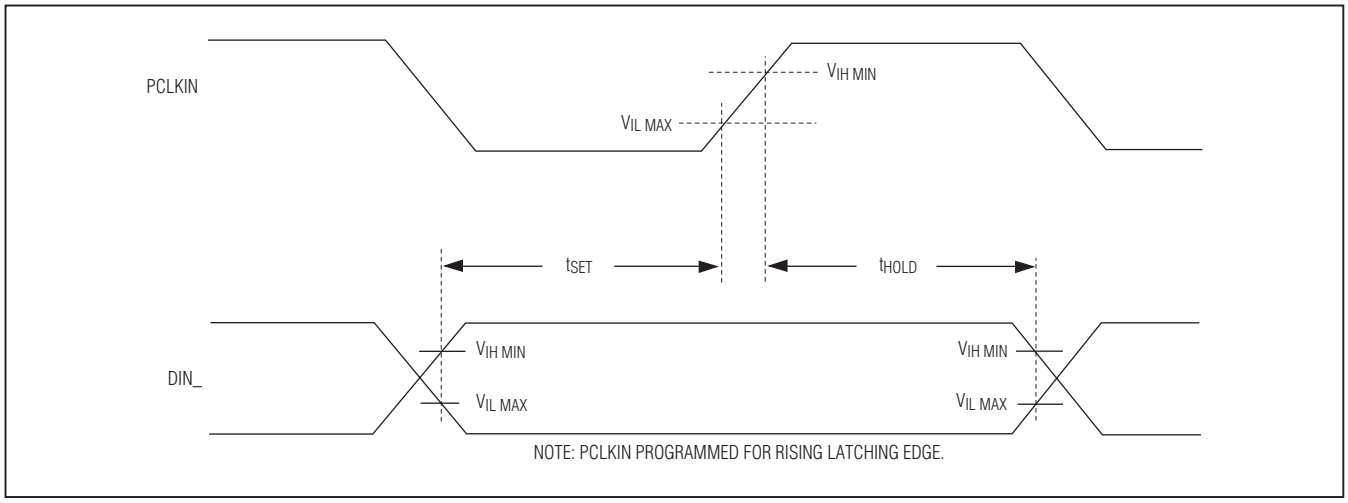


Figure 8. MAX9259 Input Setup-and-Hold Times

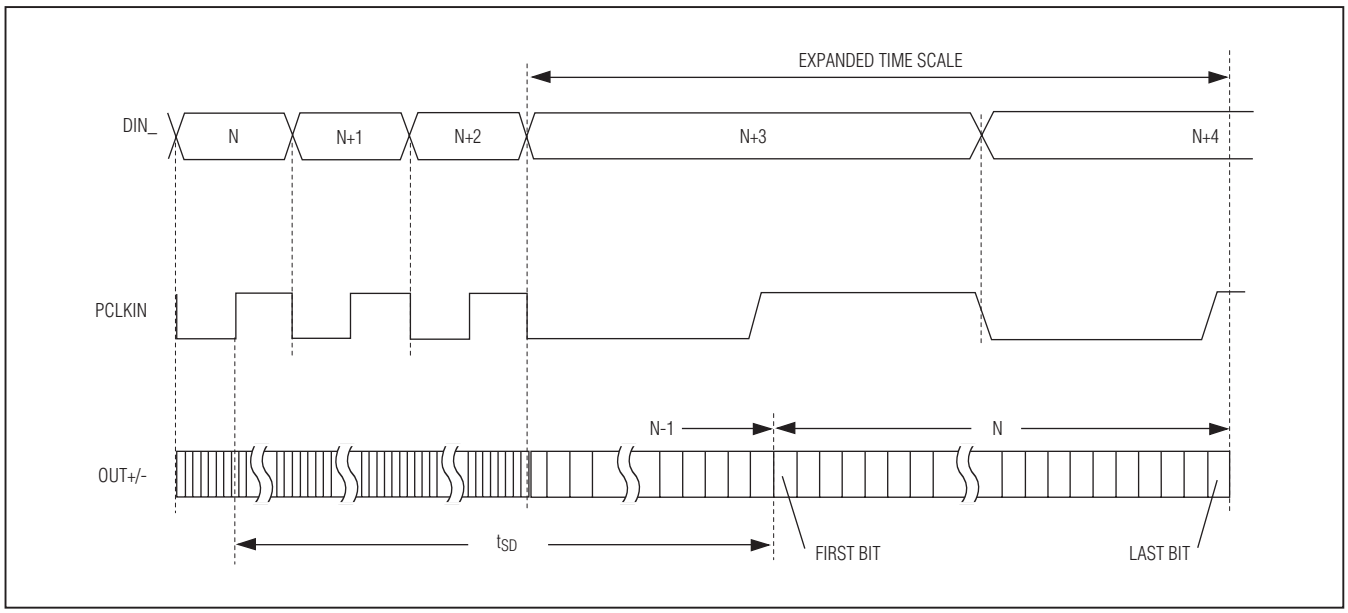


Figure 9. MAX9259 Serializer Delay

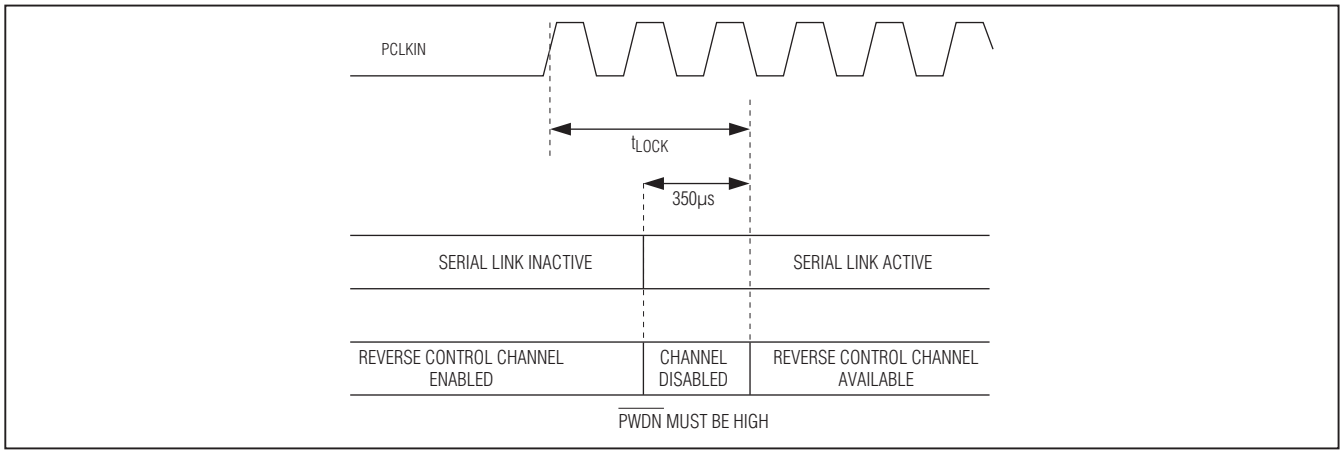


Figure 10. MAX9259 Link Startup Time

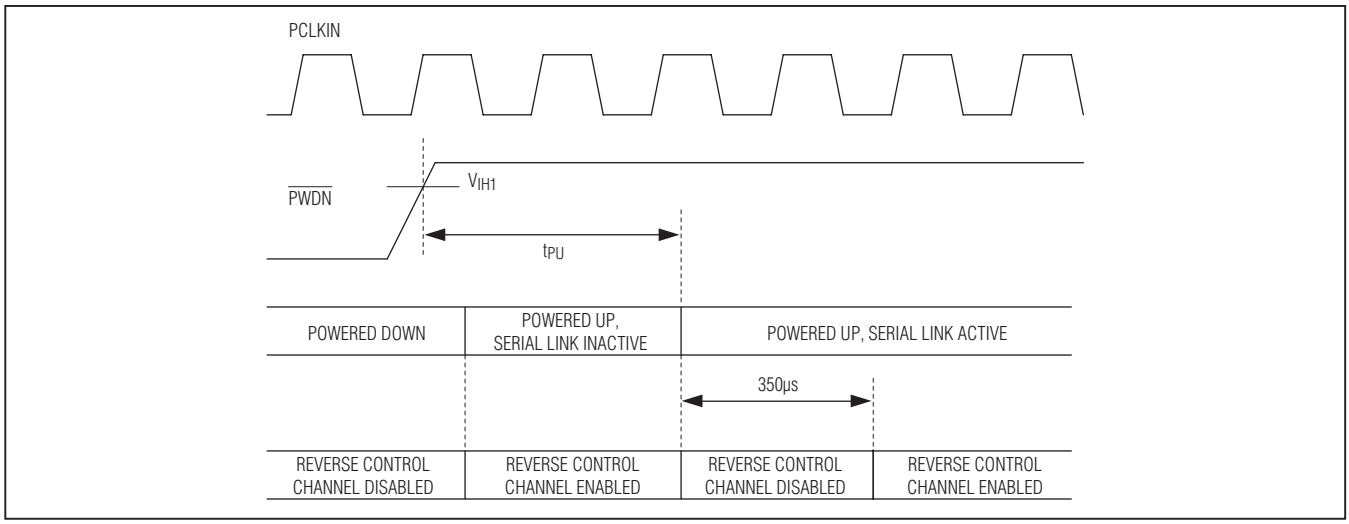


Figure 11. MAX9259 Power-Up Delay

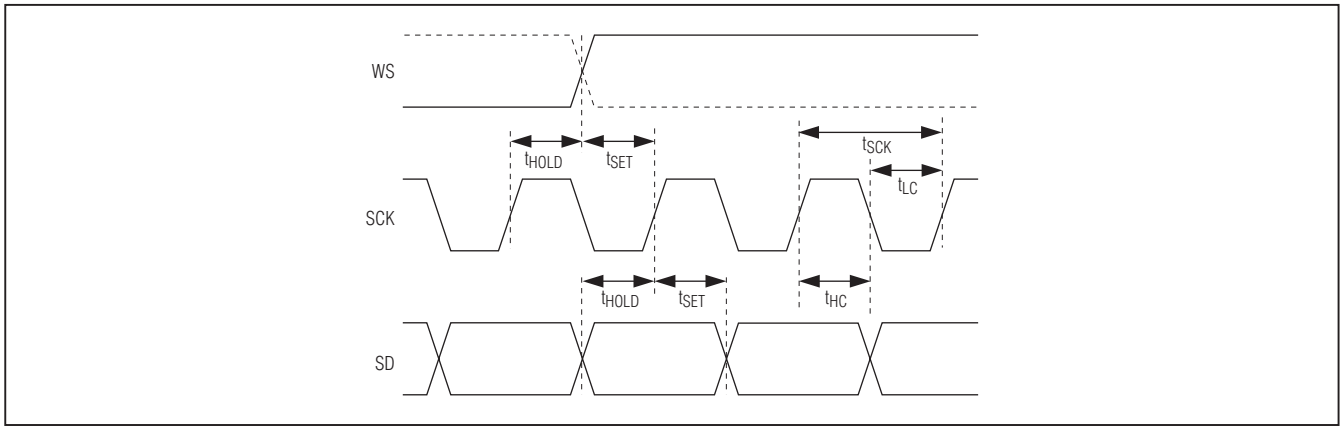


Figure 12. MAX9259 Input I²S Timing Parameters

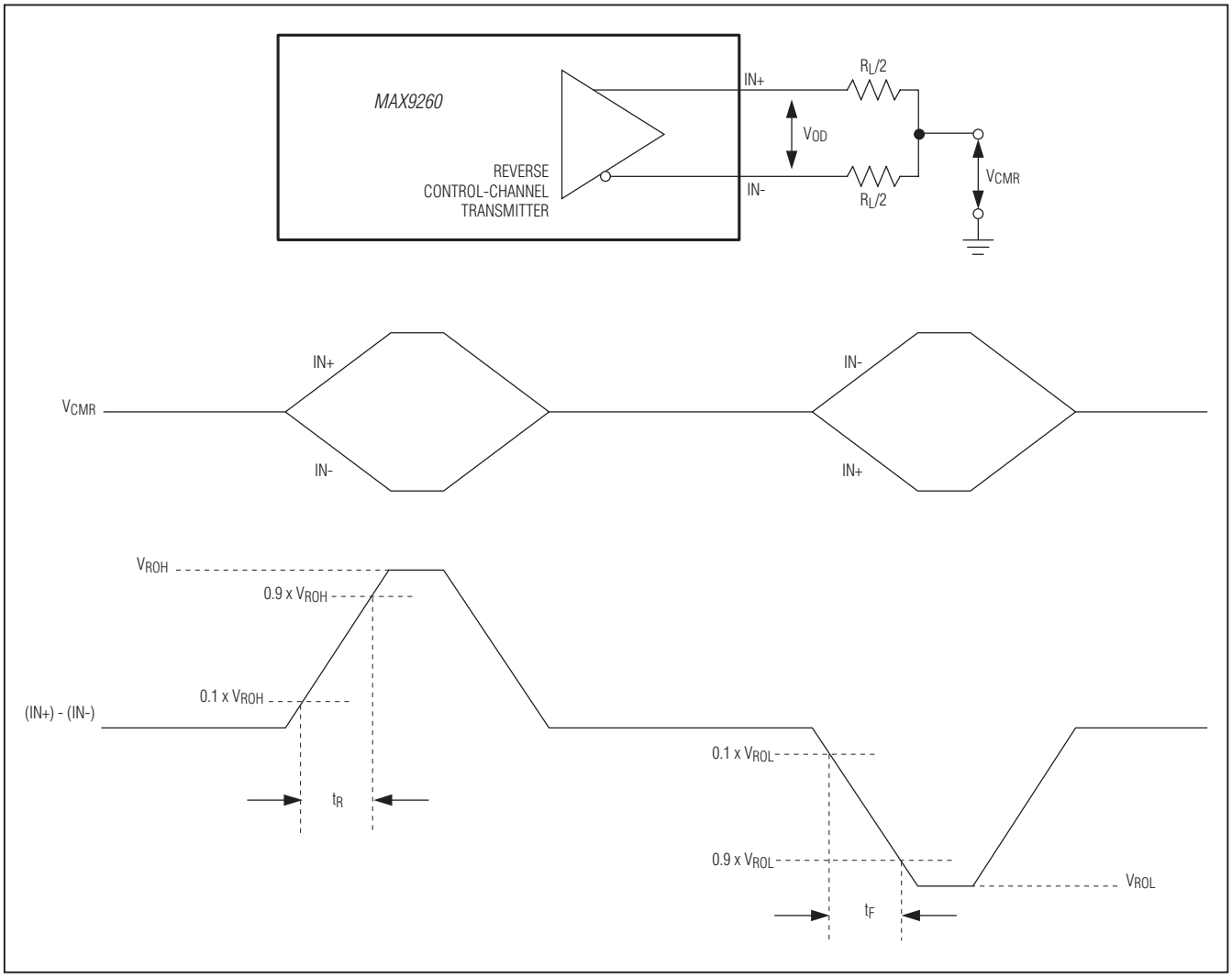


Figure 13. MAX9260 Reverse Control-Channel Output Parameters

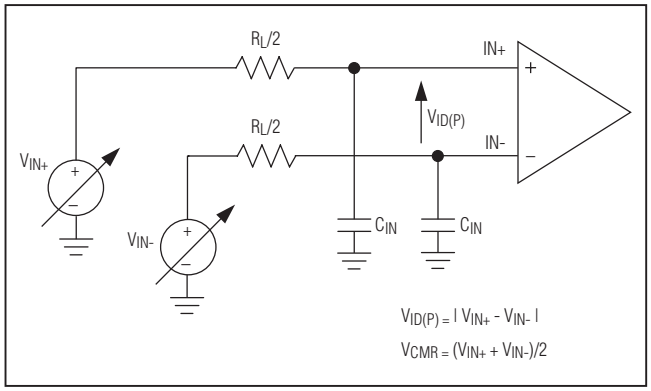


Figure 14. MAX9260 Test Circuit for Differential Input Measurement

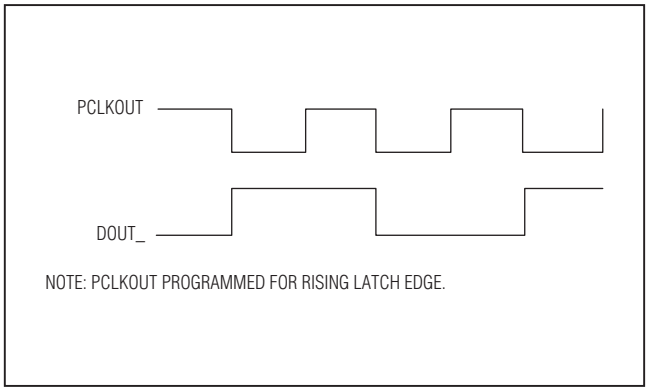


Figure 15. MAX9260 Worst-Case Pattern Output

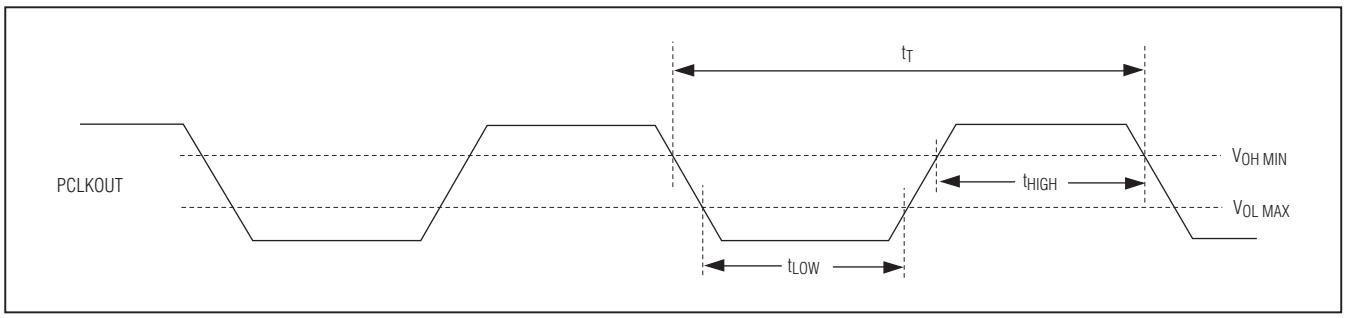


Figure 16. MAX9260 Clock Output High-and-Low Times

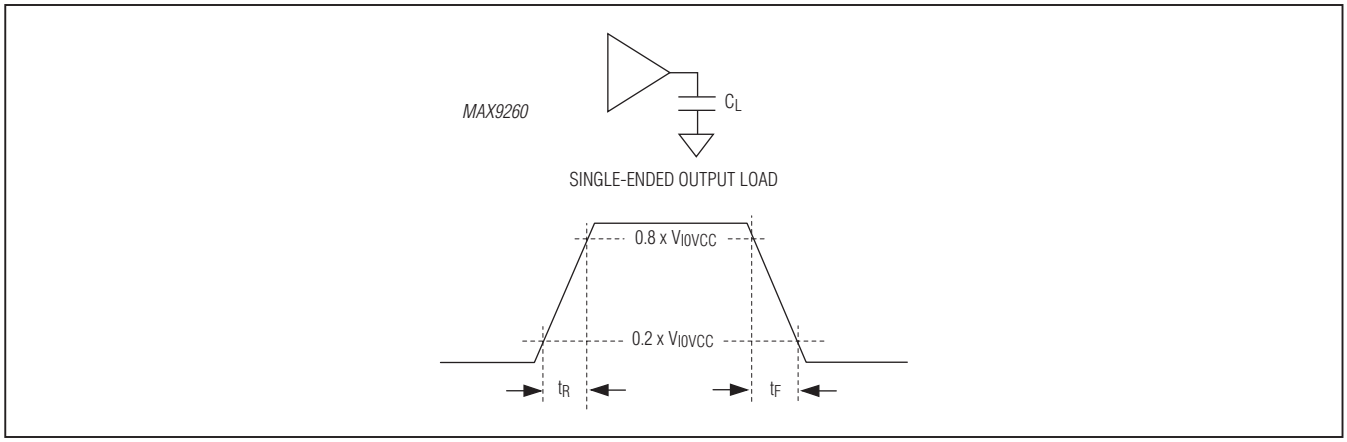


Figure 17. MAX9260 Output Rise-and-Fall Times

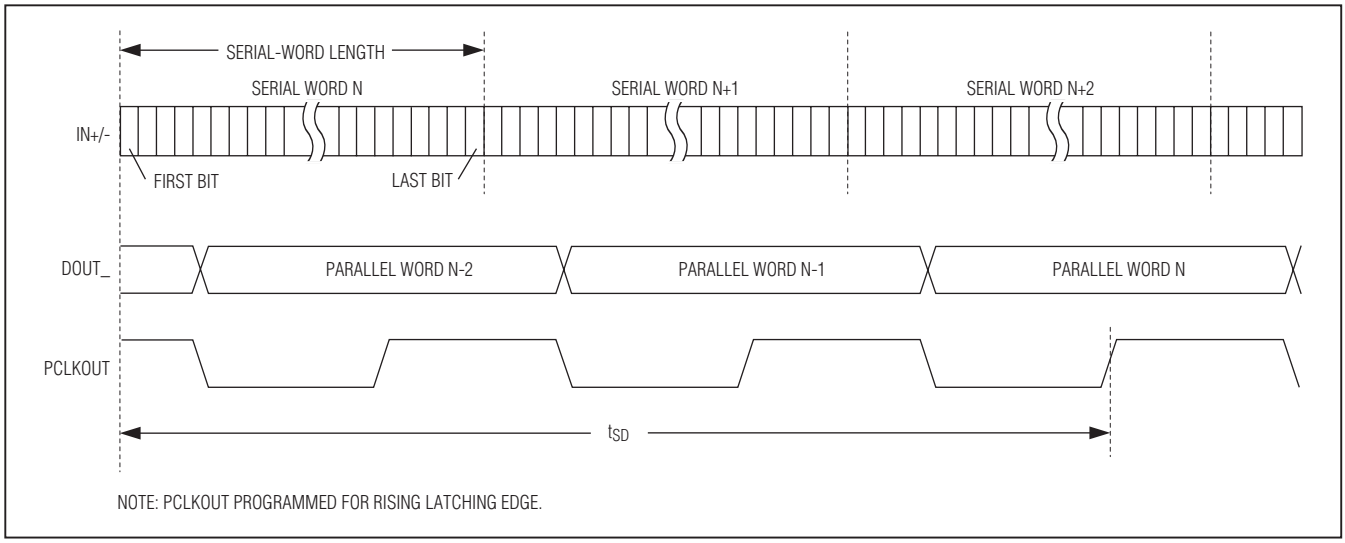


Figure 18. MAX9260 Deserializer Delay

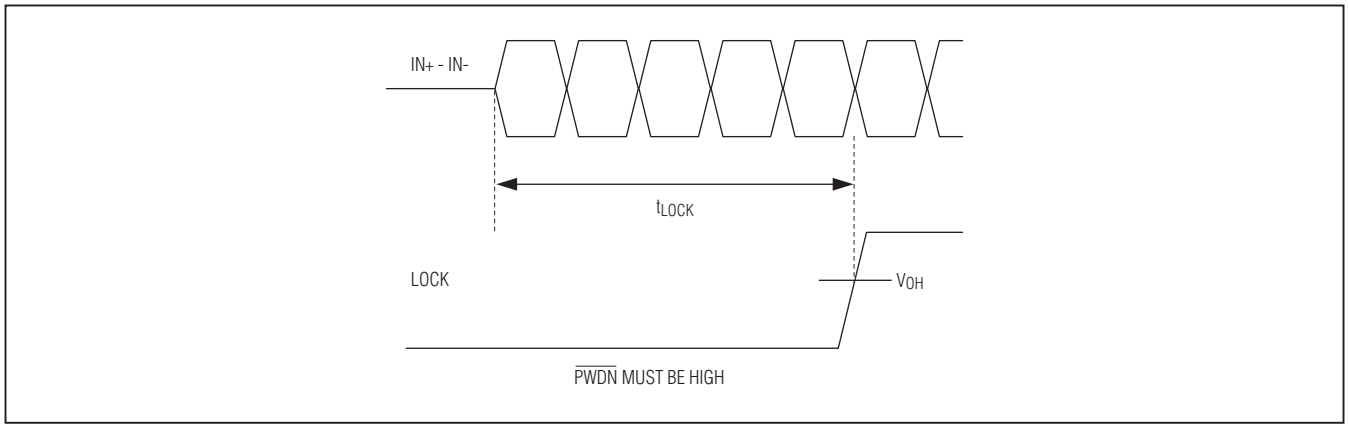


Figure 19. MAX9260 Lock Time

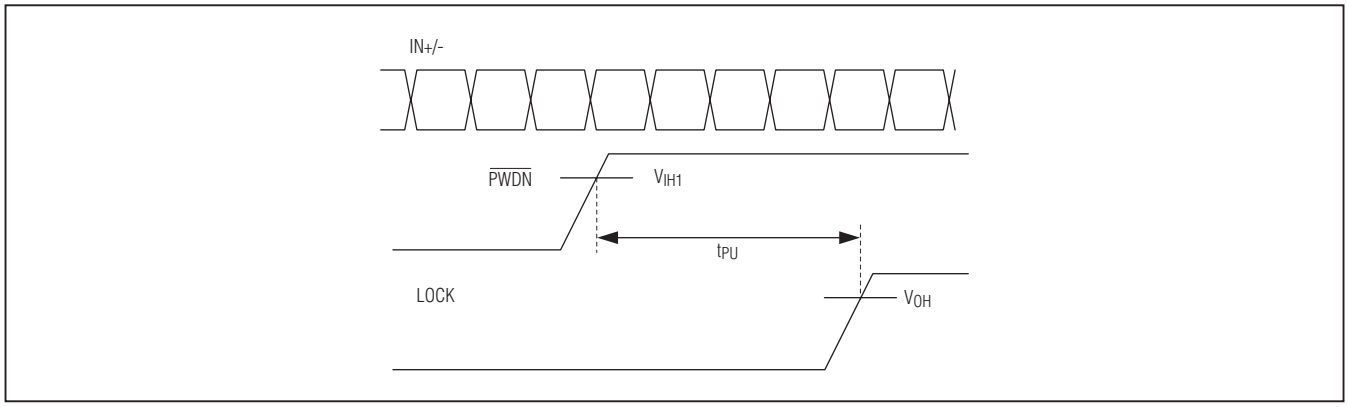


Figure 20. MAX9260 Power-Up Delay

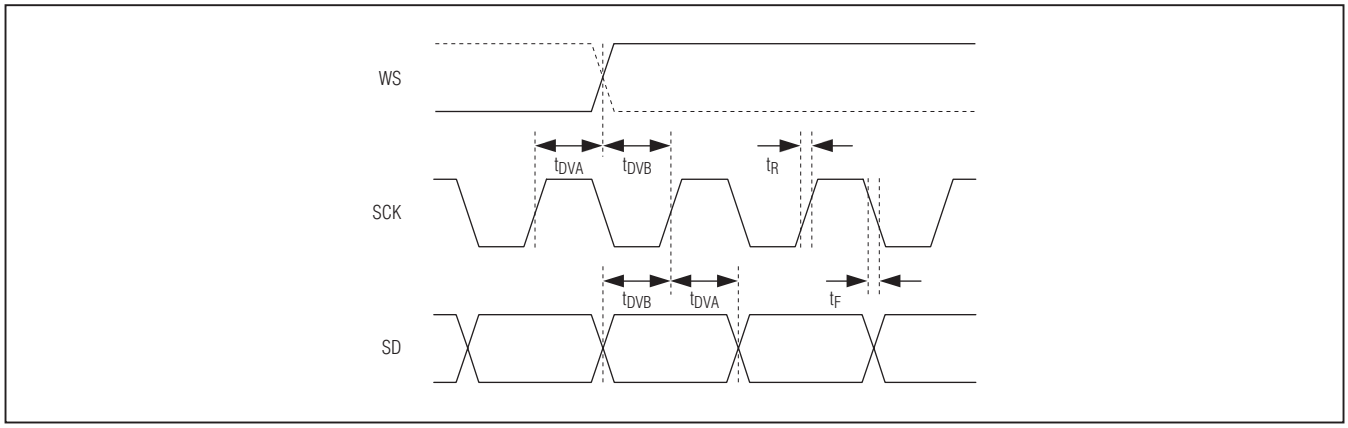


Figure 21. MAX9260 Output I²S Timing Parameters

Detailed Description

The MAX9259/MAX9260 chipset presents Maxim's GMSL technology. The MAX9259 serializer pairs with the MAX9260 deserializer to form a complete digital serial link for joint transmission of high-speed video, audio, and control data for video-display or image-sensing applications. The serial-payload data rate can reach up to 2.5Gbps for a 15m STP cable. The parallel interface is programmable for 24-bit or 32-bit width modes at the maximum bus clock of 104MHz or 78MHz, respectively. The minimum bus clock is 6.25MHz for the 32-bit mode and 8.33MHz for the 24-bit mode. With such a flexible data configuration, the GMSL is able to support XGA (1280 x 768) or dual-view WVGA (2 x 854 x 480) display panels. For image sensing, it supports three 10-bit camera links simultaneously with a pixel clock up to 78MHz. The 24-bit mode handles 21-bit data and control signals plus an I²S audio signal. The 32-bit mode handles 29-bit data and control signals plus an I²S audio signal. Any combination and sequence of color video data, video sync, and control signals make up the 21-bit or 29-bit parallel data on DIN_ and DOUT_. The I²S port supports the sampled audio data at a rate from 8kHz to 192kHz and the audio word length of anywhere between 4 to 32 bits. The embedded control channel forms a UART link between the serializer and deserializer. The UART link can be set to half-duplex mode or full-duplex mode depending on the application. The GMSL supports UART rates from 100kbps to 1Mbps. Using this control link, a host ECU or µC communicates with the serializer and deserializer, as well as the peripherals in the remote side, such as backlight control, grayscale gamma correction, camera module, and touch screen. All serial communication (forward and reverse) uses differential signaling. The peripheral programming uses I²C format or the default GMSL UART format. A separate bypass mode enables communication using a full-duplex, user-defined UART format. The control link between the MAX9259 and MAX9260 allows µC connectivity to either device or peripherals to support video-display or image-sensing applications.

The AC-coupled serial link uses 8B/10B coding. The MAX9259 serializer features a programmable driver preemphasis and the MAX9260 deserializer features a programmable channel equalizer to extend the link length and enhance the link reliability. Both devices have a programmable spread-spectrum feature for reducing EMI on the serial link output (MAX9259) and parallel data outputs (MAX9260). The differential serial link input and output pins comply with the ISO 10605 and IEC 61000-4-2 ESD-protection standards. The core supplies for the MAX9259/MAX9260 are 1.8V and 3.3V, respectively. Both devices use an I/O supply from 1.8V to 3.3V

Register Mapping

The µC configures various operating conditions of the GMSL through registers in the MAX9259/MAX9260. The default device addresses stored in the R0 and R1 registers of the MAX9259/MAX9260 are 0x80 and 0x90, respectively. Write to the R0/R1 registers in both devices to change the device address of the MAX9259 or MAX9260.

Parallel Inputs and Outputs

The parallel bus uses two selectable bus widths, 24 bits and 32 bits. BWS selects the bus width according to Table 1. In 24-bit mode, DIN21–DIN28 are not used and are internally pulled down. For both modes, SD, SCK, and WS pins are dedicated for I²S audio data. The assignments of the first 21 or 29 signals are interchangeable and appear in the same order at both sides of the serial link. In image-sensing applications, disabling the I²S audio channel (through the MAX9259 and MAX9260 internal registers) allows the MAX9259 to serialize three 10-bit camera data streams through DIN[0:28] plus SD inputs. The parallel bus accepts data clock rates from 8.33MHz to 104MHz for the 24-bit mode and 6.25MHz to 78MHz for the 32-bit mode.

Serial Link Signaling and Data Format

The MAX9259 high-speed data serial output uses CML signaling with programmable preemphasis and AC-coupling. The MAX9260 high-speed receiver uses AC-coupling and programmable channel equalization. Together, the GMSL operates at up to 3.125Gbps over STP cable lengths up to 15m.

The serializer scrambles and encodes the parallel input bits, and sends the 8B/10B coded signal through the serial link. The deserializer recovers the embedded serial clock and then samples, decodes, and descrambles the data onto the parallel output bus. Figures 22 and 23 show the serial-data packet format prior to scrambling and 8B/10B coding. For the 24-bit or 32-bit mode, the first 21 or 29 serial bits come from DIN[20:0] or DIN[28:0], respectively. The audio channel bit (ACB) contains an encoded audio signal derived from the three I²S inputs (SD, SCK, and WS). The forward control channel (FCC) bit carries the forward control data. The last bit (PCB) is the parity bit of the previous 23 or 31 bits.

Reverse Control Channel

The MAX9259/MAX9260 use the reverse control channel to send I²C/UART and interrupt signals in the opposite direction of the video stream from the deserializer to the serializer. The reverse control channel and forward video data coexist on the same twisted pair forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 500µs after power-up. The MAX9259 temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

Table 1. Bus-Width Selection Using BWS

BWS INPUT STATE	BUS WIDTH	PARALLEL BUS SIGNALS USED
Low	24	DIN[0:20]/DOUT[0:20], WS, SCK, SD
High	32	DIN[0:28]/DOUT[0:28], WS, SCK, SD

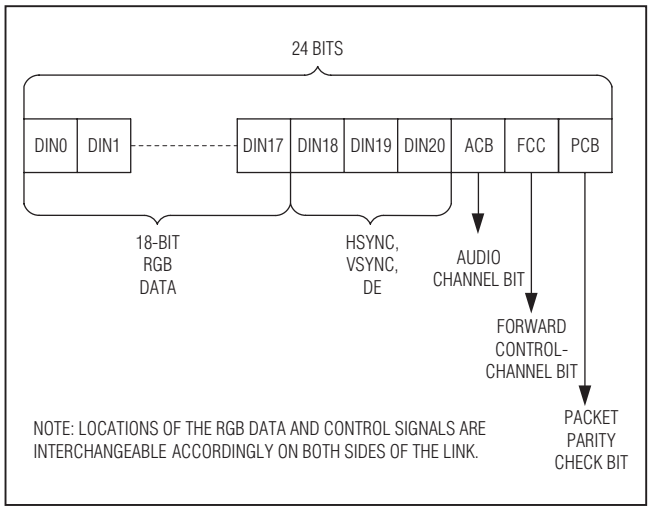


Figure 22. 24-Bit Mode Serial Link Data Format

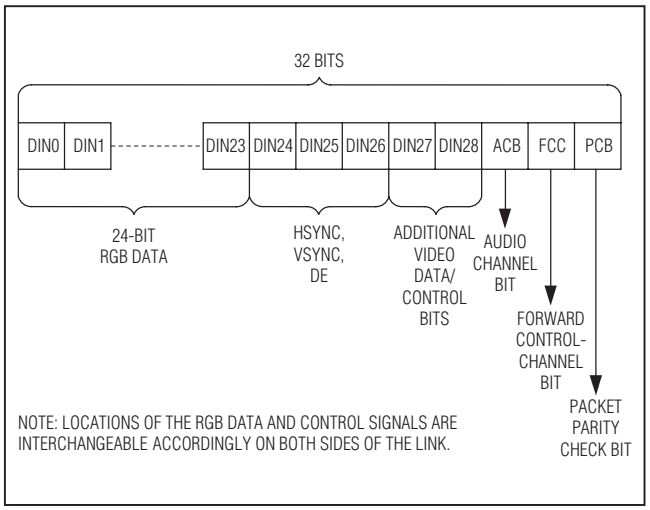


Figure 23. 32-Bit Mode Serial Link Data Format

Table 2. Maximum Audio Sampling Rates for Various PCLK_ Frequencies

WORD LENGTH (Bits)	PCLK_ FREQUENCY (DRS = LOW) (MHz)				PCLK_ FREQUENCY (DRS = HIGH) (MHz)			
	12.5	15	16.6	> 20	6.25	7.5	8.33	> 10
8	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
16	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
18	185.5	> 192	> 192	> 192	185.5	> 192	> 192	> 192
20	174.6	> 192	> 192	> 192	174.6	> 192	> 192	> 192
24	152.2	182.7	> 192	> 192	152.2	182.7	> 192	> 192
32	123.7	148.4	164.3	> 192	123.7	148.4	164.3	> 192

Parallel Data-Rate Selection

The MAX9259/MAX9260 use the DRS inputs to set the parallel data rate. Set DRS high to use a low-speed parallel data rate in the range of 6.25MHz to 12.5MHz (32-bit mode) or 8.33MHz to 16.66MHz (24-bit mode). Set DRS low for normal operation with parallel data rates higher than 12.5MHz (32-bit mode) or 16.66MHz (24-bit mode).

Audio Channel

The I²S audio channel supports audio sampling rates from 8kHz to 192kHz and audio word lengths from 4 bits to 32 bits. The audio bit clock (SCK) does not need to be synchronized with PCLKIN. The MAX9259 automatically encodes audio data into a single bit stream synchronous with PCLKIN. The MAX9260 decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I²S format. The audio channel is enabled by default. When the audio channel is disabled, the SD pins on both sides are treated as a regular parallel data pin.

PCLK_ frequencies can limit the maximum supported audio sampling rate. Table 2 lists the maximum audio sampling rate for various PCLK_ frequencies. Spread-spectrum settings do not affect the I²S data rate or WS clock frequency.

Additional MCLK Output for Audio Applications

Some audio DACs such as the MAX9850 do not require a synchronous main clock (MCLK), while other DACs require MCLK to be a specific multiple of WS. If an audio DAC chip needs the MCLK to be a multiple of WS, synchronize the I²S audio data with PCLK_ of the GMSL, which is typical for most applications. Select the PCLK_ to be the multiple of WS, or use a clock synthesis chip, such as the MAX9491, to regenerate the required MCLK from PCLK_ or SCK.

For audio applications that cannot directly use the PCLKOUT output, the MAX9260 provides a divided MCLK output on DOUT28 at the expense of one less parallel line in 32-bit mode (24-bit mode is not affected). By default, DOUT28 operates as a parallel data output and MCLK is turned off. Set MCLKDIV (MAX9260 register 0x12, D[6:0]) to a non-zero value to enable the MCLK output. Set MCLKDIV to 0x00 to disable MCLK and set DOUT28 as a parallel data output.

The output MCLK frequency is:

$$f_{MCLK} = \frac{f_{SRC}}{MCLKDIV}$$

where f_{SRC} is the MCLK source frequency (Table 3) and MCLKDIV is the divider ratio from 1 to 127.

Table 3. MAX9260 f_{SRC} Settings

MCLKSRC SETTING (REGISTER 0x12, D7)	DATA-RATE SETTING	BIT-WIDTH SETTING	MCLK SOURCE FREQUENCY (f_{SRC})
0	High speed	24-bit mode	3 x $f_{PCLKOUT}$
		32-bit mode	4 x $f_{PCLKOUT}$
	Low speed	24-bit mode	6 x $f_{PCLKOUT}$
		32-bit mode	8 x $f_{PCLKOUT}$
1	—	—	Internal oscillator (120MHz typ)

Choose MCLKDIV values so that f_{MCLK} is not greater than 60MHz. MCLK frequencies derived from PCLK_ (MCLKSRC = 0) are not affected by spread-spectrum settings in the deserializer (MAX9260). Enabling spread spectrum in the serializer (MAX9259), however, introduces spread spectrum into MCLK. Spread-spectrum settings of either device do not affect MCLK frequencies derived from the internal oscillator. The internal oscillator frequency ranges from 100MHz to 150MHz over all process corners and operating conditions.

Control-Channel and Register Programming

The µC uses the control link to send and receive control data over the STP link simultaneously with the high-speed data. Configuring the CDS pin allows the µC to control the link from either the MAX9259 or the MAX9260 side to support video-display or image-sensing applications.

The control link between the µC and the MAX9259 or MAX9260 runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control link and the bypass mode is a full-duplex control link. In base mode, the µC is the host and accesses the registers of both the MAX9259 and MAX9260 from either side of the link by using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the MAX9259 or MAX9260, with UART packets converted to I²C by the device on the remote side of the link (MAX9260 for LCD or MAX9259 for image-sensing applications). The µC communicates with a UART peripheral in base mode (through INTTYPE register settings) using the half-duplex default GMSL UART protocol of the MAX9259 and MAX9260. The device addresses of the MAX9259 and MAX9260 in the base mode are programmable. The default values are 0x80 and 0x90, respectively.

In base mode, when the peripheral interface uses I²C (default), the MAX9259/MAX9260 only convert packets that have device addresses different from those of the MAX9259 or MAX9260 to I²C. The converted I²C bit rate is the same as the original UART bit rate.

In bypass mode, the µC bypasses the MAX9259/MAX9260 and communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the MAX9259/MAX9260's registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one PCLK_ period of jitter due to the asynchronous sampling of the UART signal by PCLK_.

The MAX9259 embeds control signals going to the MAX9260 in the high-speed forward link. Do not send a low value longer than 100µs in either base or bypass mode. The MAX9260 uses a proprietary differential line coding to send signals back towards the MAX9259. The speed of the control link ranges from 100kbps to 1Mbps in both directions. The MAX9259/MAX9260 automatically detect the control-channel bit rate in base mode. Packet bit rates can vary up to 3.5x from the previous bit rate (see the *Changing the Data Frequency* section). Figure 24 shows the UART protocol for writing and reading in base mode between the µC and the MAX9259/MAX9260.

Figure 25 shows the UART data format. Even parity is used. Figures 26 and 27 detail the formats of the SYNC byte (0x79) and ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Certain events such as device wake-up and interrupt generate signals on the control path and should be ignored by the µC. All data written to the internal registers do not take affect until after the acknowledge byte is sent. This allows the µC to verify that write commands are processed without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART data rate automatically. If the INT or MS inputs of the MAX9260 toggles while there is control-channel communication, the control-channel communication can be corrupted. In the event of a missed acknowledge, the µC should

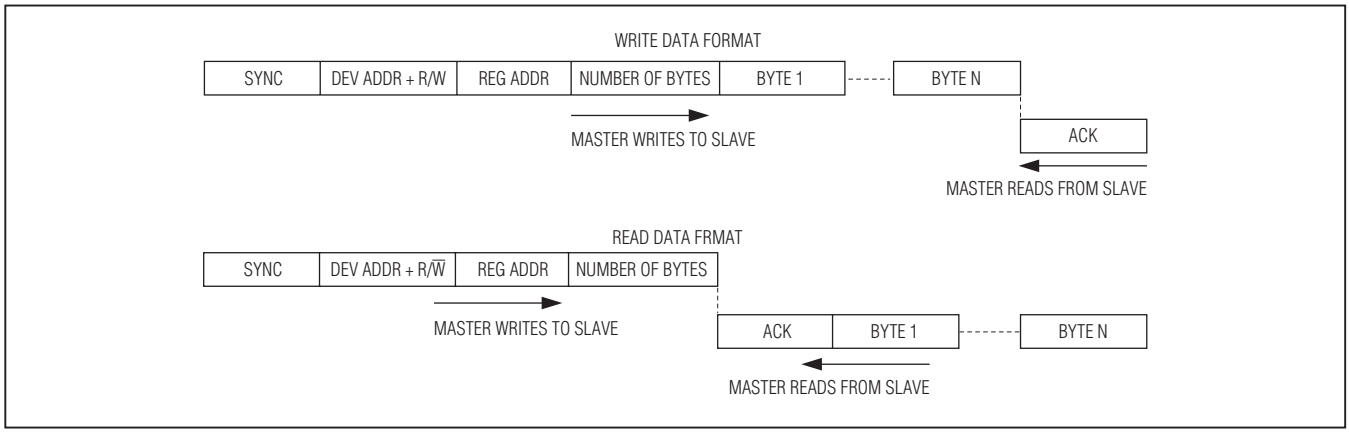


Figure 24. UART Protocol for Base Mode

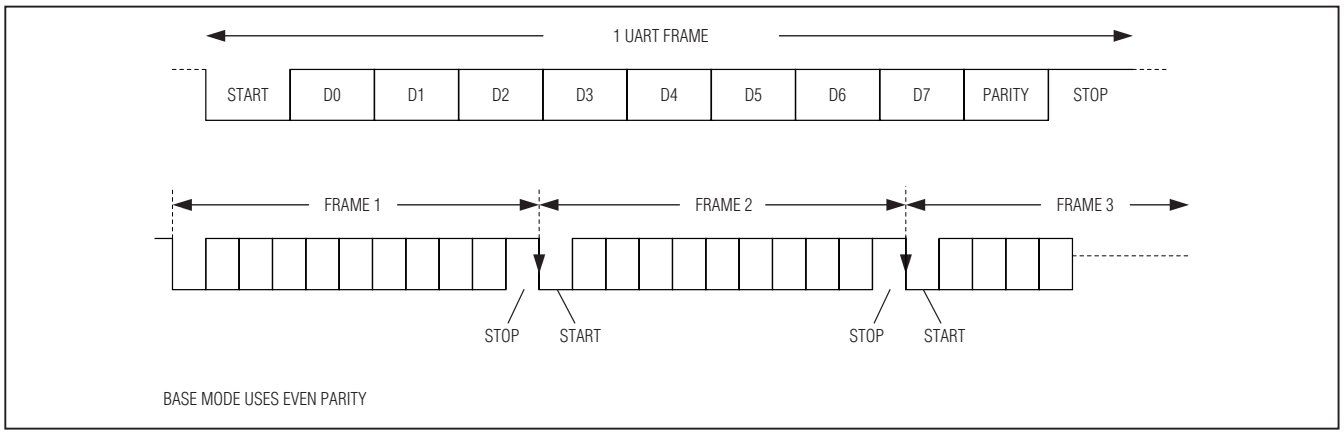


Figure 25. UART Data Format for Base Mode

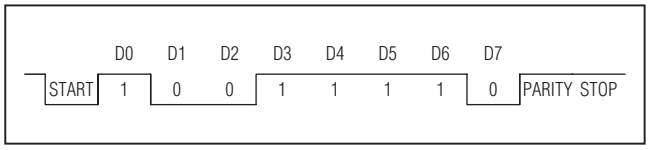


Figure 26. SYNC Byte (0x79)

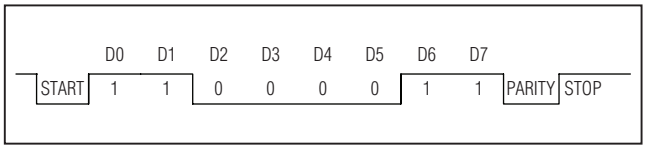


Figure 27. ACK Byte (0xC3)

assume there was an error in the packet transmission or response. In base mode, the µC must keep the UART Tx/Rx lines high no more than four bit times between bytes in a packet. Keep the UART Tx/Rx lines high for at least 16 bit times before starting to send a new packet.

As shown in Figure 28, the remote-side device converts the packets going to or coming from the peripherals from the UART format to the I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C's data rate is the same as the UART data rate.

Interfacing Command-Byte-Only I²C Devices

The MAX9259/MAX9260 UART-to-I²C conversion interfaces with devices that do not require register addresses, such as the MAX7324 GPIO expander. Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 29).

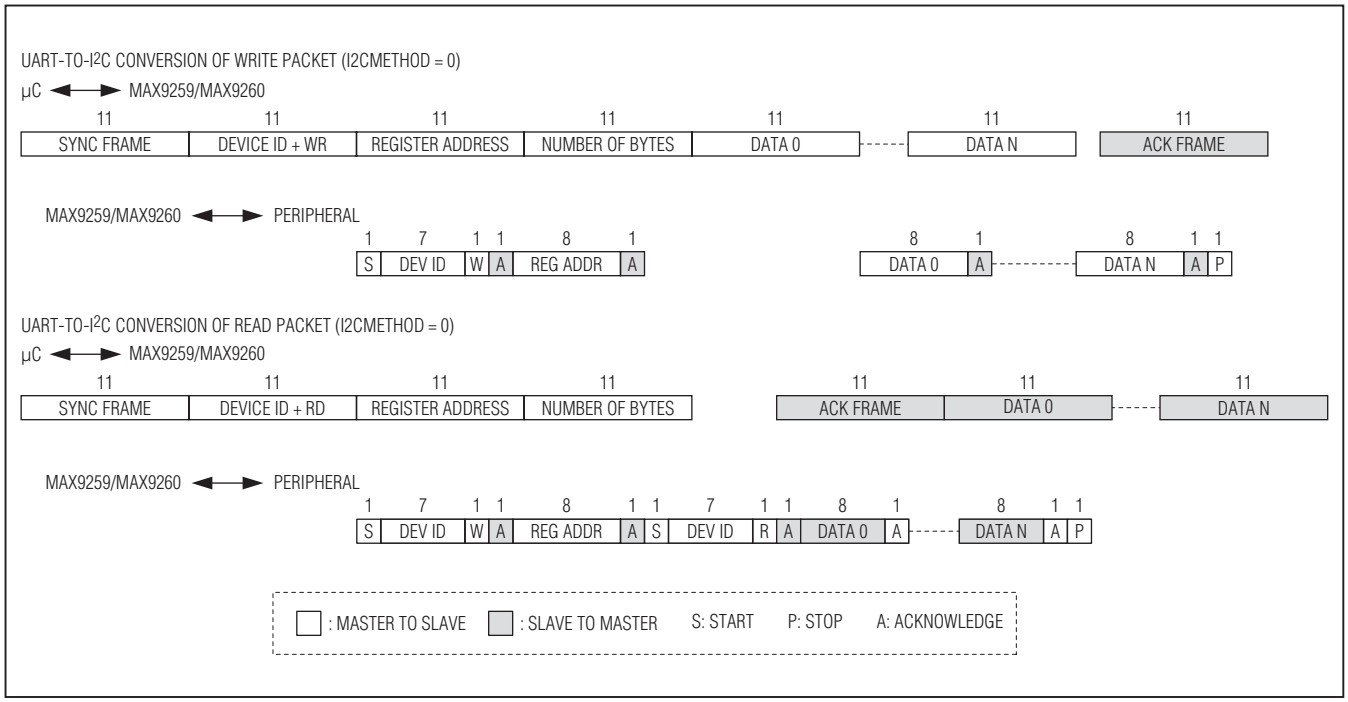


Figure 28. Format Conversion between UART and I²C with Register Address (I2CMETHOD = 0)

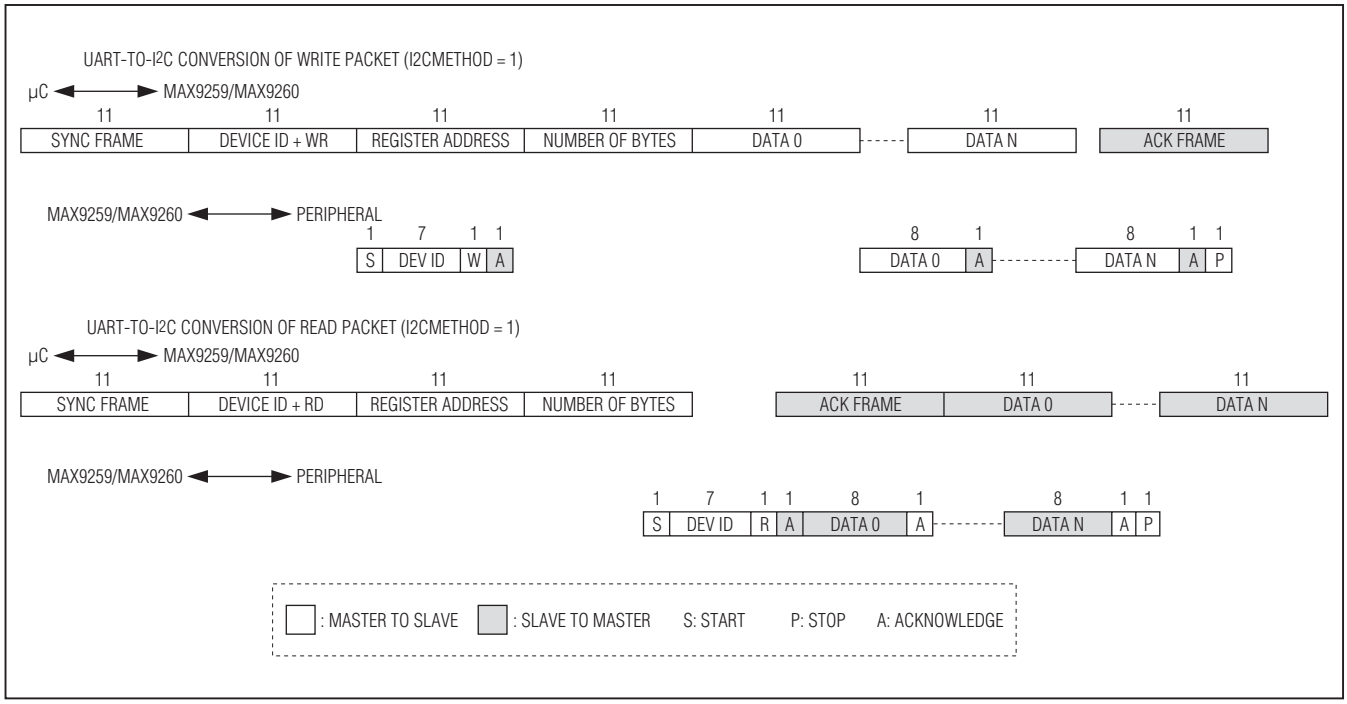


Figure 29. Format Conversion between UART and I²C in Command-Byte-Only Mode (I2CMETHOD = 1)

Table 4. MAX9259 CML Driver Strength (Default Level, CMLLVL = 11)

PREEMPHASIS LEVEL (dB)*	PREEMPHASIS SETTING (0x05, D[3:0])	I_{CML} (mA)	I_{PRE} (mA)	SINGLE-ENDED VOLTAGE SWING	
				MAX (mV)	MIN (mV)
-6.0	0100	12	4	400	200
-4.1	0011	13	3	400	250
-2.5	0010	14	2	400	300
-1.2	0001	15	1	400	350
0	0000	16	0	400	400
1.1	1000	16	1	425	375
2.2	1001	16	2	450	350
3.3	1010	16	3	475	325
4.4	1011	16	4	500	300
6.0	1100	15	5	500	250
8.0	1101	14	6	500	200
10.5	1110	13	7	500	150
14.0	1111	12	8	500	100

**Negative preemphasis levels denote deemphasis.*

Interrupt Control

The INT of the MAX9259 is the interrupt output and the INT of the MAX9260 is the interrupt input. The interrupt output on the MAX9259 follows the transitions at the interrupt input of the MAX9260. This interrupt function supports remote-side functions such as touch-screen peripherals, remote power-up, or remote monitoring. Interrupts that occur during periods where the reverse control channel is disabled, such as link startup/shutdown, are automatically resent once the reverse control channel becomes available again. Bit D4 of register 0x06 in the MAX9260 also stores the interrupt input state. Writing to the SETINT register bit also sets the INT output of the MAX9259. In addition, the µC sets the INT output of the MAX9259 by writing to the SETINT register bit. In normal operation, the state of the interrupt output changes when the interrupt input on the MAX9260 toggles.

Preemphasis Driver

The serial line driver in the MAX9259 employs current-mode logic (CML) signaling. The driver generates an adjustable preemphasized waveform according to the cable length and characteristics. There are 13 preemphasis settings, as shown in Table 4. Negative preemphasis levels are deemphasis levels in which the preemphasized swing level is the same as normal swing, but the no-transition data is deemphasized. Program the preemphasis levels through register 0x05 D[3:0] of the MAX9259. This preemphasis function compensates the high-frequency loss of the cable and enables reliable transmission over longer link distances. Additionally, a lower power drive mode can be entered by programming CMLLVL bits (0x05 D[5:4]) to reduce the driver strength down to 75% (CMLLVL = 10), or 50% (CMLLVL = 01) from 100% (CMLLVL = 11, default).

Line Equalizer

The MAX9260 includes an adjustable line equalizer to further compensate cable attenuation at high frequencies. The cable equalizer has 11 selectable levels of compensation from 2.1dB to 13dB (Table 5). The EQS input selects the default equalization level at power-up. The state of EQS is latched upon power-up or when resuming from power-down mode. To select other equalization levels, set the corresponding register bits in the MAX9260 (0x05 D[3:0]). Use equalization in the MAX9260, together with preemphasis in the MAX9259 to create the most reliable link for a given cable.

Table 5. MAX9260 Cable Equalizer Boost Levels

BOOST SETTING (0x05 D[3:0])	TYPICAL BOOST GAIN (dB)
0000	2.1
0001	2.8
0010	3.4
0011	4.2
0100	5.2 **Power-up default (EQS = high)**
0101	6.2
0110	7
0111	8.2
1000	9.4
1001	10.7 **Power-up default (EQS = low)**
1010	11.7
1011	13

Spread Spectrum

To reduce the EMI generated by the transitions on the serial link and parallel outputs, both the MAX9259 and MAX9260 support spread spectrum. Turning on spread spectrum on the MAX9260 spreads the parallel video outputs. Turning on spread spectrum on the MAX9259 spreads the serial link, along with the MAX9260 parallel outputs. Do not enable spread spectrum for both the MAX9259 and MAX9260. The six selectable spread-spectrum rates at the MAX9259 serial output are ±0.5%, ±1%, ±1.5%, ±2%, ±3%, and ±4% (Table 6). Some spread-spectrum rates can only be used at lower PCLK_ frequencies (Table 7). There is no PCLK_ frequency limit for the 0.5% spread rate. The two selectable spread-spectrum rates at the MAX9260 parallel outputs are ±2% and ±4% (Table 8).

Set the MAX9259 SSEN input high to select 0.5% spread at power-up and SSEN input low to select no spread at power-up. Set the MAX9260 SSEN input high to select 2% spread at power-up and SSEN input low to select no spread at power-up. The state of SSEN is latched upon power-up or when resuming from power-down mode. Whenever the MAX9259 spread spectrum is turned on

Table 6. Serial Output Spread

SS	SPREAD (%)
000	No spread spectrum. **Power-up default when SSEN = low.**
001	±0.5% spread spectrum. **Power-up default when SSEN = high.**
010	±1.5% spread spectrum
011	±2% spread spectrum
100	No spread spectrum
101	±1% spread spectrum
110	±3% spread spectrum
111	±4% spread spectrum

Table 7. MAX9259 Spread-Spectrum Rate Limitations

24-BIT MODE PCLKIN FREQUENCY (MHz)	32-BIT MODE PCLKIN FREQUENCY (MHz)	SERIAL LINK BIT RATE (Mbps)	AVAILABLE SPREAD RATES
< 33.3	< 25	< 1000	All rates available
33.3 to < 66.7	20 to < 50	1000 to < 2000	1.5%, 1.0%, 0.5%
66.7+	50+	2000+	0.5%

Table 8. MAX9260 Parallel Output Spread

SS	SPREAD (%)
00	No spread spectrum. **Power-up default when SSEN = low.**
01	±2% spread spectrum. **Power-up default when SSEN = high.**
10	No spread spectrum
11	±4% spread spectrum

Table 9. MAX9259 Modulation Coefficients and Maximum SDIV Settings

BIT-WIDTH MODE	SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT (decimal)	SDIV UPPER LIMIT (decimal)
32-Bit	1	104	40
	0.5	104	63
	3	152	27
	1.5	152	54
	4	204	15
	2	204	30
24-Bit	1	80	52
	0.5	80	63
	3	112	37
	1.5	112	63
	4	152	21
	2	152	42

Table 10. MAX9260 Modulation Coefficients and Maximum SDIV Settings

SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT (decimal)	SDIV UPPER LIMIT (decimal)
4	208	15
2	208	30

or off, the serial link automatically restarts and remains unavailable while the MAX9260 relocks to the serial data.

Turning on spread spectrum on either the MAX9259 or MAX9260 side does not affect the audio data stream. Changes in the MAX9259 spread settings only affect MCLK output if it is derived from PCLK_ (MCLKSRC = 0).

Both devices include a sawtooth divider to control the spread-modulation rate. Autodetection or manual programming of the PCLK_ operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV, 0x03 D[5:0]) allows the user to set a specific modulation frequency for a specific PCLK_ rate. Always keep the modulation frequency between 20kHz to 40kHz to ensure proper operation.

Manual Programming of the Spread-Spectrum Divider

The modulation rates for the MAX9259 or the MAX9260 relate to the PCLK_ frequency as follows:

$$f_M = (1 + DRS)\frac{f_{PCLK\_}}{MOD \times SDIV}$$

where:

f_M = Modulation frequency

DRS = DRS pin input value (0 or 1)

$f_{PCLK\_}$ = Parallel clock frequency (12.5MHz to 104MHz)

MOD = Modulation coefficient given in Table 9 for the MAX9259 and Table 10 for the MAX9260

SDIV = 6-bit (MAX9259) or 5-bit (MAX9260) SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the part number and desired bit-width and spread-spectrum settings. Solve the above equation for SDIV using the desired parallel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Tables 9 or 10, set SDIV to the maximum value.

Sleep Mode

The serializer/deserializer include a low-power sleep mode to reduce power consumption on the device not attached to the µC (MAX9260 in LCD applications and MAX9259 in camera applications). Set the corresponding remote IC's SLEEP bit to 1 to initiate sleep mode. The MAX9259 sleeps immediately after setting its SLEEP = 1. The MAX9260 sleeps after serial link inactivity or 8ms (whichever arrives first) after setting its SLEEP = 1. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

The µC side device cannot enter into sleep mode, and its SLEEP bit remains at 0. Use the $\overline{PWDN}$ input pin to bring the µC side device into a low-power state.

Configuration Link Mode

The MAX9259/MAX9260 include a low-speed configuration link to allow control-data connection between the two devices in the absence of a valid parallel clock input. In either display or camera applications, the configuration link can be used to program equalizer/preemphasis or other registers before establishing the video link. An internal oscillator provides PCLK_ for establishing the serial configuration link between the MAX9259 and MAX9260. The parallel output clock and data lines are disabled in the MAX9260. The LOCK output remains low even after a successful configuration link lock. Set CLINKEN = 1 on the MAX9259 to turn on the configuration link. The configuration link remains active as long as the video link has not been enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Startup Procedure

Table 11 lists four startup cases for video-display applications. Table 12 lists two startup cases for image-sensing applications. In either display or image-sensing applications, the control link is always available after the high-speed data link or the configuration link is established and the MAX9259/MAX9260 registers or the peripherals are ready for programming.

Video-Display Applications

For the video-display application, with a remote display unit, connect the µC to the serializer (MAX9259) and set CDS = low for both the MAX9259 and MAX9260. Table 11 summarizes the four startup cases based on the settings of $\overline{AUTOS}$ and MS.

Case 1: Autostart Mode

After power-up or when $\overline{PWDN}$ transitions from low to high for both the serializer and deserializer, the serial link establishes if a stable PCLK_ is present. The MAX9259 locks to PCLK_ and sends the serial data to the MAX9260. The MAX9260 then detects activity on the serial link and locks to the input serial data.

Case 2: Standby Start Mode

After power-up, or when $\overline{PWDN}$ transitions from low to high for both the serializer and deserializer, the MAX9260 starts up in sleep mode, and the MAX9259 stays in standby mode (does not send serial data). Use the µC and program the MAX9259 to set SEREN = 1 to establish a video link or CLINKEN = 1 to establish the configuration link. After locking to a stable PCLK_ (for SEREN = 1) or the internal oscillator (for CLINKEN = 1), the MAX9259 sends a wake-up signal to the deserializer. The MAX9260 exits sleep mode after locking to the serial data and sets SLEEP = 0. If after 8ms the deserializer does not lock to the input serial data, the MAX9260 goes back to sleep, and the internal sleep bit remains uncleared (SLEEP = 1).

Case 3: Remote Side Autostart Mode

After power-up, or when $\overline{PWDN}$ transitions from low to high, the remote device (MAX9260) starts up and tries to lock to an incoming serial signal with sufficient power. The host side (MAX9259) is in standby mode and does not try to establish a link. Use the µC and program the MAX9259 to set SEREN = 1 (and apply a stable PCLK_) to establish a video link, or CLINKEN = 1 to establish the configuration link. In this case, the MAX9260 ignores the short wake-up signal sent from the MAX9259.

Case 4: Remote Side in Sleep Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the remote device (MAX9260) starts up in sleep mode. The high-speed link establishes automatically after MAX9259 powers up with a stable PCLK_ and sends a wake-up signal to the MAX9260. Use this mode in applications where the MAX9260 powers up before the MAX9259.

Table 11. Startup Selection for Video-Display Applications (CDS = Low)

CASE	$\overline{\text{AUTOS}}$ (MAX9259)	MAX9259 POWER-UP STATE	MS (MAX9260)	MAX9260 POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Low	Normal (SLEEP = 0)	Both devices power up with serial link active (autostart)
2	High	Serialization disabled	High	Sleep mode (SLEEP = 1)	Serial link is disabled and the MAX9260 powers up in sleep mode. Set SEREN = 1 or CLINKEN = 1 in the MAX9259 to start the serial link and wake up the MAX9260.
3	High	Serialization disabled	Low	Normal (SLEEP = 0)	Both devices power up in normal mode with the serial link is disabled. Set SEREN = 1 or CLINKEN = 1 in the MAX9259 to start the serial link.
4	Low	Serialization enabled	High	Sleep mode (SLEEP = 1)	MAX9260 starts in sleep mode. Link autostarts upon MAX9259 power-up. Use this case when the MAX9260 powers up before the MAX9259.

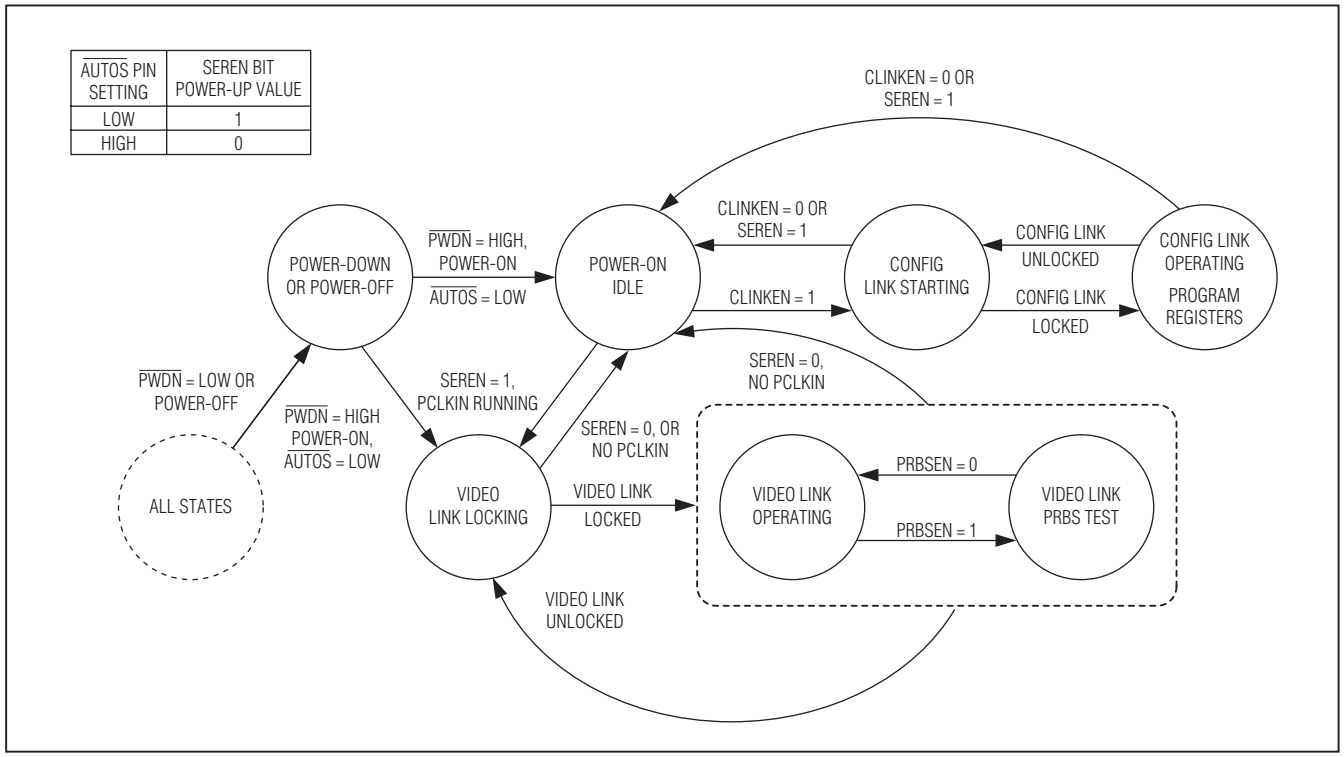


Figure 30. MAX9259 State Diagram, CDS = Low (LCD Application)

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

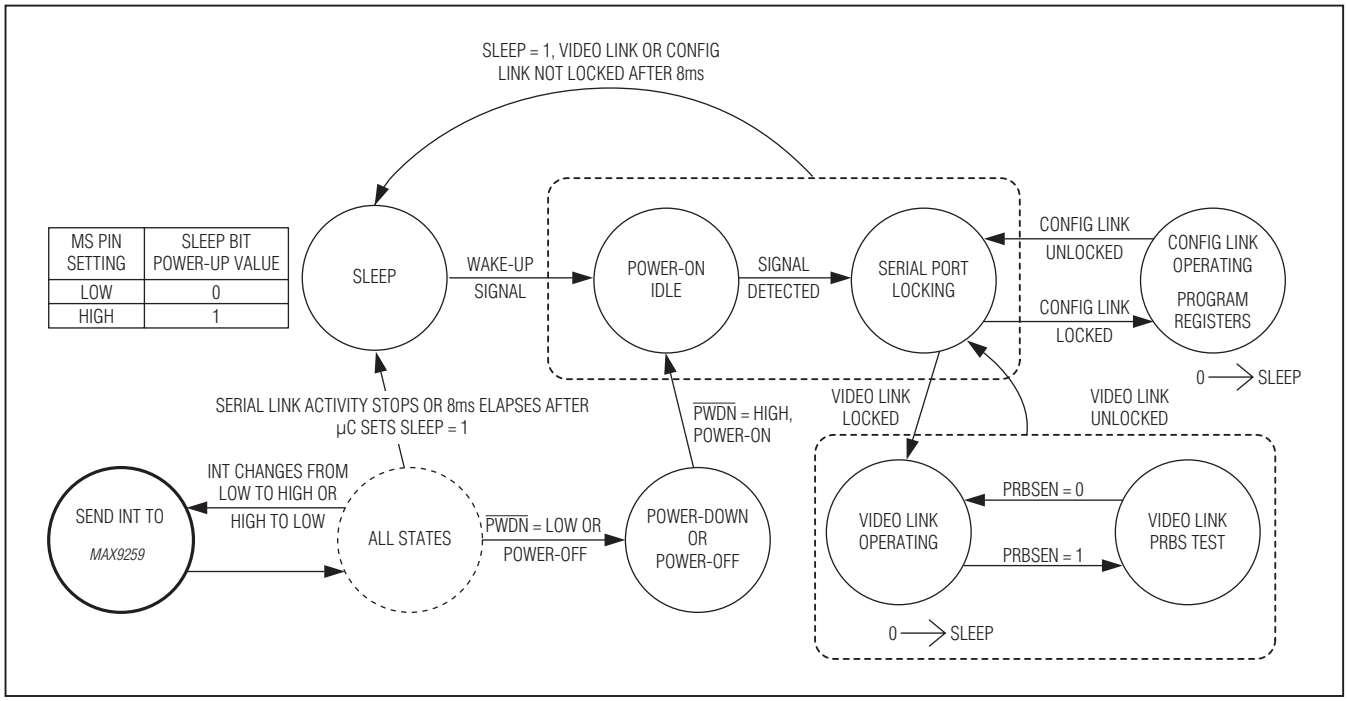


Figure 31. MAX9260 State Diagram, CDS = Low (LCD Application)

Image-Sensing Applications

For image-sensing applications, with remote camera unit(s), connect the µC to the deserializer (MAX9260) and set CDS = high for both the MAX9259 and MAX9260. The MAX9260 powers up normally (SLEEP = 0) and continuously tries to lock to a valid serial input. Table 12 summarizes the two startup cases, based on the state of the MAX9259 $\overline{AUTOS}$ pin.

Case 1: Autostart Mode

After power-up, or when $\overline{PWDN}$ transitions from low to high, the MAX9259 locks to a stable PCLKIN and sends the high-speed data to the MAX9260. The MAX9260 locks to the serial data and outputs the parallel video data and PCLKOUT.

Case 2: Sleep Mode

After power-up, or when $\overline{PWDN}$ transitions from low to high, the MAX9259 starts up in sleep mode. To wake up the MAX9259, use the µC to send a regular UART frame containing at least three rising edges (e.g., 0x66), at a bit rate no greater than 1Mbps. The low-power wake-up receiver of the MAX9259 detects the wake-up frame over the reverse control channel and powers up. Reset the sleep bit (SLEEP = 0) of the MAX9259 using a regular control-channel write packet to power up the device fully. Send the sleep bit write packet at least 500µs after the wake-up frame. The MAX9259 goes back to sleep mode if its sleep bit is not cleared within 8ms (typ) after detecting a wake-up frame.

Table 12. Startup Selection for Image-Sensing Applications (CDS = High)

CASE	$\overline{AUTOS}$ (MAX9259)	MAX9259 POWER-UP STATE	MAX9260 POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Normal (SLEEP = 0)	Autostart
2	High	Sleep mode (SLEEP = 1)	Normal (SLEEP = 0)	MAX9259 is in sleep mode. Wake up the MAX9259 through the control channel (µC attached to MAX9260).

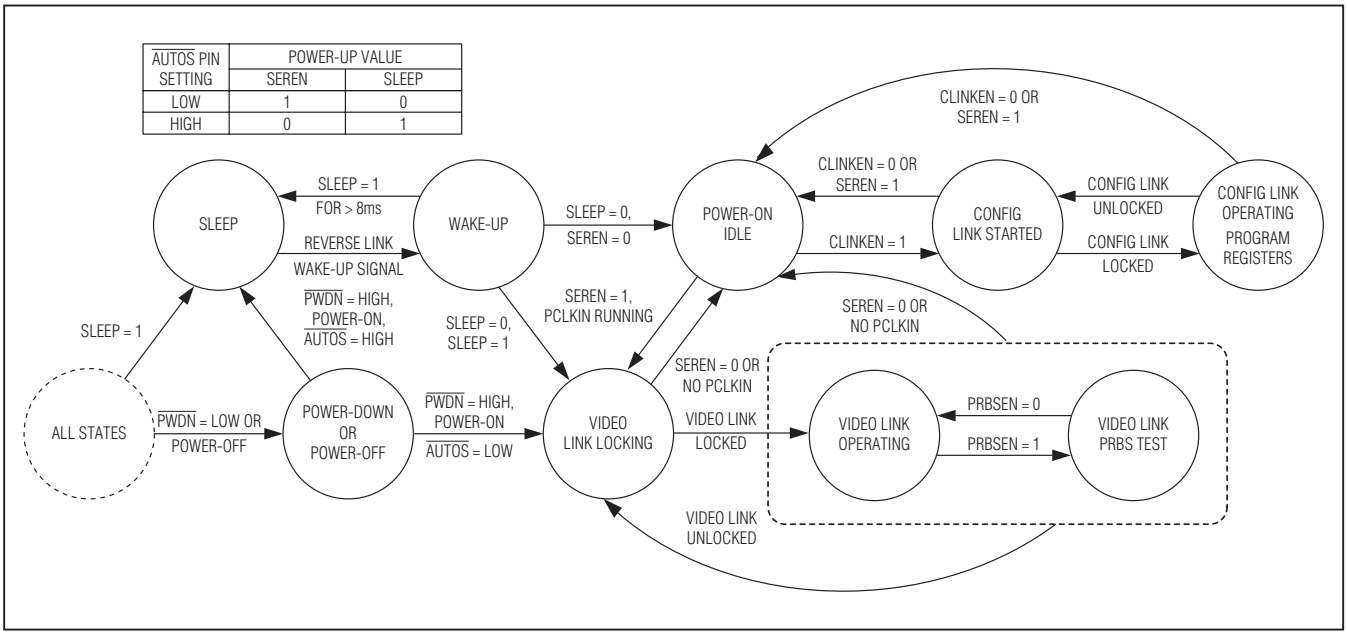


Figure 32. MAX9259 State Diagram, CDS = High (Camera Application)

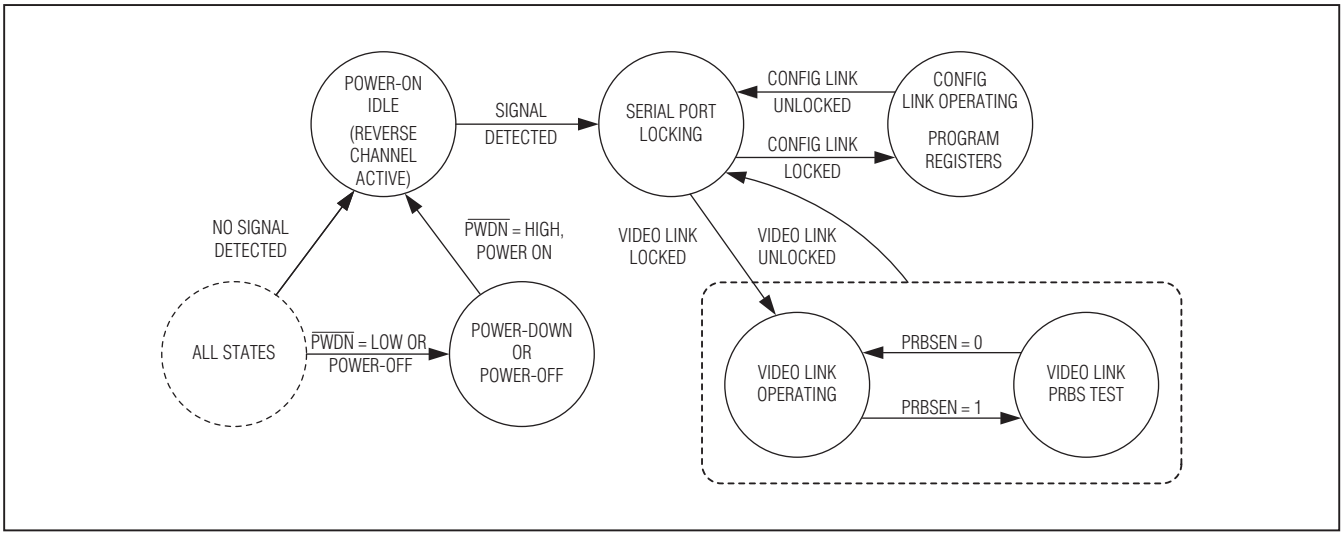


Figure 33. MAX9260 State Diagram, CDS = High (Camera Application)

Applications Information

MAX9260 Error Checking

The MAX9260 checks the serial link for errors and stores the number of detected decoding errors in the 8-bit register (DECERR, 0x0D). If a large number of decoding errors are detected within a short duration, the deserializer loses lock and stops the error counter. The deserializer then attempts to relock to the serial data. DECERR resets upon successful video link lock, successful readout of DECERR (through UART), or whenever autoerror reset is enabled. The MAX9260 does not check for decoding errors during the internal PRBS test and DECERR is reset to 0x00.

$\overline{ERR}$ Output

The MAX9260 has an open-drain $\overline{ERR}$ output. This output asserts low whenever the number of decoding errors exceed the error threshold (ERRTHR, 0x0C) during normal operation, or when at least one PRBS error is detected during PRBS test. $\overline{ERR}$ reasserts high whenever DECERR (0x0D) resets, due to DECERR readout, video link lock, or autoerror reset.

Autoerror Reset

The default method to reset errors is to read the respective error registers in the MAX9260 (0x0D, 0x0E). Autoerror reset clears the decoding-error counter (DECERR) and the $\overline{ERR}$ output ~1µs after $\overline{ERR}$ goes low. Autoerror reset is disabled on power-up. Enable autoerror reset through AUTORST (0x06 D6). Autoerror reset does not run when the device is in PRBS test mode.

Self PRBS Test

The MAX9259/MAX9260 link includes a PRBS pattern generator and bit-error verification function. Set PRBSEN = 1 (0x04 D5) first in the MAX9259 and then the MAX9260 to start the PRBS test. Set PRBSEN = 0 (0x04 D5) first in the MAX9260 and then the MAX9259 to exit the PRBS self test. The MAX9260 uses an 8-bit register (0x0E) to count the number of detected errors. The control link also controls the start and stop of the error counting. During PRBS mode, the device does not count decoding errors and the $\overline{ERR}$ output reflects PRBS errors only. Autoerror reset does not run when the device is in PRBS mode.

Microcontrollers on Both Sides of the GMSL Link (Dual µC Control)

Usually the µC is either on the serializer (MAX9259) side for video-display applications, or on the deserializer (MAX9260) side for image-sensing applications. For the former case, both the CDS pins of the MAX9259/MAX9260 are set to low, and for the later case, the CDS pins are set to high. However, if the CDS pin of the MAX9259 is low and the CDS pin of the MAX9260 is high, then the MAX9259/MAX9260 can both connect to µCs simultaneously. In such a case, the µCs on either side can communicate with the MAX9259/MAX9260 UART protocol.

Contentions of the control link may happen if the µCs on both sides are using the link at the same time. The MAX9259/MAX9260 do not provide the solution for contention avoidance. The serializer/deserealizer do not send an acknowledge frame when communication fails due to contention. Users can always implement a higher-layer protocol to avoid the contention. In addition, if UART communication across the serial link is not required, the µCs can disable the forward and reverse control channel through the FWDCCEN and REVCCEN bits (0x04 D[1:0]) in the MAX9259/MAX9260. UART communication across the serial link is stopped and contention between µCs no longer occurs. During the dual µC operation, if one of the CDS pins on either side changes state, the link resumes the corresponding state described in the *Link Startup Procedure* section.

As an example of dual µC use in an image-sensing link, the MAX9259 may be in sleep mode and waiting to be waked up by the MAX9260. After wake-up, the serializer-side µC sets the MAX9259 CDS pin low and assumes master control of the MAX9259 registers.

Jitter-Filtering PLL

In some applications, the parallel bus input clock to the MAX9259 (PCLKIN) includes noise, which reduces link reliability. The MAX9259 has a narrow-band jitter-filtering PLL to attenuate frequency components outside the PLL's bandwidth (< 100kHz typ). Enable the jitter-filtering PLL by setting DISFPLL = 0 (0x05 D6).

Changing the Data Frequency

Both the video data rate ($f_{PCLK\_}$) and the control data rate (f_{UART}) can be changed on-the-fly to support applications with multiple clock speeds. Slow speed/performance modes allow significant power savings when a system's full capabilities are not required. Enable the MAX9259/MAX9260 link after PCLK_ stabilizes. Stop PCLKIN for 5µs and restart the serial link or toggle SEREN after each change in the parallel clock frequency to recalibrate any automatic settings if a clean frequency change cannot be guaranteed. The reverse control channel remains unavailable for 350µs after serial link start or stop. Limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device

Table 13. MAX9259 Line-Fault Mapping

REGISTER ADDRESS	BITS	NAME	VALUE	LINE-FAULT TYPE
0x08	D[3:2]	LFNEG	00	Negative cable wire shorted to battery
			01	Negative cable wire shorted to ground
			10	Normal operation
			11	Negative cable wire open
	D[1:0]	LFPOS	00	Positive cable wire shorted to battery
			01	Positive cable wire shorted to ground
			10	Normal operation
			11	Positive cable wire open

Table 14. Staggered Output Delay

OUTPUT	OUTPUT DELAY RELATIVE TO DOUT0 (ns)	
	DISSTAG = 0	DISSTAG = 1
DOUT0–DOUT5, DOUT21, DOUT22	0	0
DOUT6–DOUT10, DOUT23, DOUT24	0.5	0
DOUT11–DOUT15, DOUT25, DOUT26	1	0
DOUT16–DOUT20, DOUT27, DOUT28	1.5	0
PCLKOUT	0.75	0

recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps and then at 100kbps to have reduction ratios of 3 and 3.333, respectively.

LOCK Output Loopback

Connect the LOCK output to the INT input of the MAX9260 to loopback LOCK to the MAX9259. The interrupt output on the MAX9259 follows the transitions at the LOCK output of the MAX9260. Reverse-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the video link. LOCK asserts for video link only and not for the configuration link.

MAX9260 GPIOs

The MAX9260 has two open-drain GPIOs available. GPIO1OUT and GPIO0OUT (0x06 D3, D1) set the output state of the GPIOs. The GPIO input buffers are always enabled. The input states are stored in GPIO1 and GPIO0 (0x06 D2, D0). Set GPIO1OUT/GPIO0OUT to 1 when using GPIO1/GPIO0 as an input.

Line-Fault Detection

The line-fault detector in the MAX9259 monitors for line failures such as short to ground, short to power supply, and open link for system fault diagnosis. Figure 3 shows the required external resistor connections. $\overline{LFLT}$ = low when a line fault is detected and $\overline{LFLT}$ = high when the line returns to normal. The line-fault type is stored in 0x08 D[3:0] of the MAX9259. The fault-detector threshold voltages are referenced to the MAX9259 ground. Additional passive components set the DC level of the cable (Figure 3). If the MAX9259 and MAX9260 grounds are different, the link DC voltage during normal operation can vary and cross one of the fault-detection thresholds. For the fault-detection circuit, select the resistor's power rating to handle a short to the battery. Table 13 lists the mapping for line-fault types.

Staggered Parallel Data Outputs

The MAX9260 staggers the parallel data outputs to reduce EMI and noise. Staggering outputs also reduce the power-supply transient requirements. By default, the deserializer staggers outputs according to Table 14. Disable output staggering through the DISSTAG bit (0x06 D7)

Choosing I²C/UART Pullup Resistors

Both I²C/UART open-drain lines require pullup resistors to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time $t_R = 0.85 \times R_{PULLUP} \times C_{BUS} < 300ns$. The waveforms

are not recognized if the transition time becomes too slow. The MAX9259/MAX9260 support I²C/UART rates up to 1Mbps.

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Four capacitors—two at the serializer output and two at the deserializer input—are needed for proper link operation and to provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML receiver termination resistor (R_{TR}), the CML driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (R_{TD} + R_{TR}))/4. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω). This leaves the capacitor selection to change the system time constant. Use at least 0.22µF (100V) high-frequency surface-mount ceramic capacitors to pass the lower speed reverse-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The MAX9259 uses an AVDD and DVDD of 1.7V to 1.9V. The MAX9260 uses an AVDD and DVDD of 3.0V to 3.6V. All single-ended inputs and outputs on the MAX9259/MAX9260 derive power from an IOVDD of 1.7V to 3.6V. The input levels or output levels scale with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic-field canceling effects. Balanced cables pick up noise as common mode rejected by the CML receiver. Table 15 lists the suggested cables and connectors used in the GMSL link.

Board Layout

Separate the parallel signals and CML high-speed serial signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML, and digital signals. Layout PCB traces close to each other and have a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer.

Route the PCB traces for a CML channel (there are two conductors per CML channel) in parallel to maintain the differential characteristic impedance. Avoid vias. If vias must be used, use only one pair per CML channel and place the via for each line at the same point along the length of the PCB traces. This way, any reflections occur at the same time. Do not make vias into test points for

Table 15. Suggested Connectors and Cables for GMSL

SUPPLIER	CONNECTOR	CABLE
JAE Electronics, Inc.	MX38-FF	A-BW-Lxxxxx
Nissei Electric Co., Ltd.	GT11L-2S	F-2WME AWG28
Rosenberger Hochfrequenztechnik GmbH	D4S10A-40ML5-Z	Dacar 538

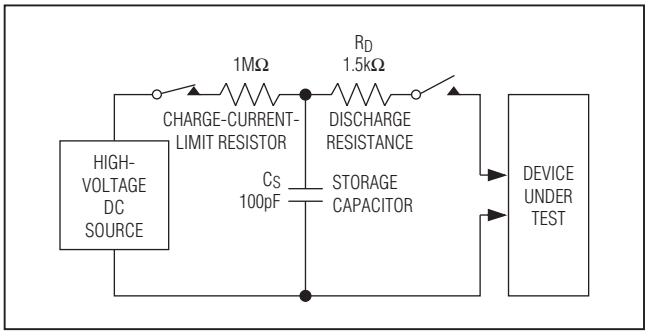


Figure 34. Human Body Model ESD Test Circuit

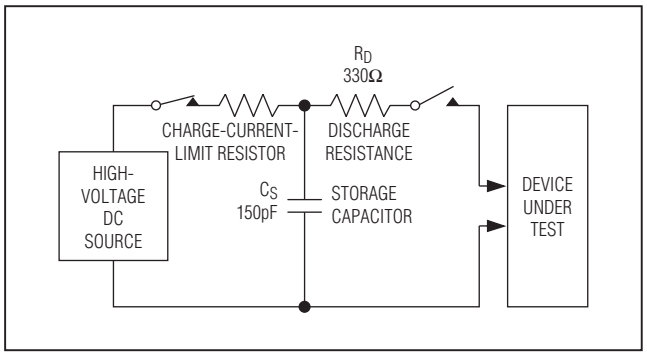


Figure 35. IEC 61000-4-2 Contact Discharge ESD Test Circuit

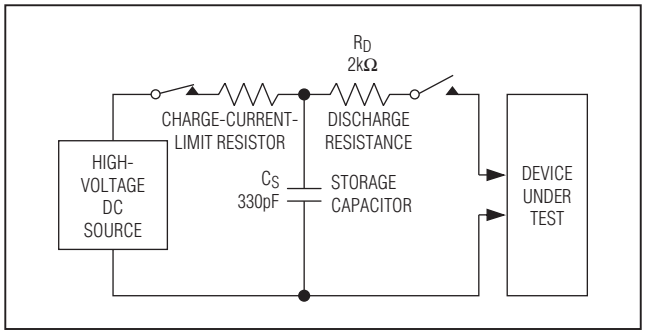


Figure 36. ISO 10605 Contact Discharge ESD Test Circuit

ATE. Keep PCB traces that make up a differential pair equal in length to avoid skew within the differential pair.

ESD Protection

The MAX9259/MAX9260 ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. Serial outputs on the MAX9259 and serial inputs on the MAX9260 meet ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All other pins meet the Human Body Model ESD tolerances. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 34). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 35). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 36).

Table 16. MAX9259 Register Table

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address	1000000
	D0	—	0	Reserved	0
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address	1001000
	D0	—	0	Reserved	0
0x02	D[7:5]	SS	**000**	No spread spectrum. **Power-up default when SSEN = low**.	000, 001
			001	±0.5% spread spectrum. **Power-up default when SSEN = high**.	
			010	±1.5% spread spectrum	
			011	±2% spread spectrum	
			100	No spread spectrum	
			101	±1% spread spectrum	
			110	±3% spread spectrum	
			111	±4% spread spectrum	
	D4	AUDIOEN	0	Disable I^2S channel	1
			1	Enable I^2S channel	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock	11
			01	25MHz to 50MHz pixel clock	
			10	50MHz to 104MHz pixel clock	
			11	Automatically detect the pixel clock range	
	D[1:0]	SRNG	00	0.5 to 1Gbps serial-data rate	11
			01	1 to 2Gbps serial-data rate	
			10	2 to 3.125Gbps serial-data rate	
			11	Automatically detect serial-data rate	
0x03	D[7:6]	AUTOFM	00	Calibrate spread-modulation rate only once after locking	00
			01	Calibrate spread-modulation rate every 2ms after locking	
			10	Calibrate spread-modulation rate every 16ms after locking	
			11	Calibrate spread-modulation rate every 256ms after locking	
	D[5:0]	SDIV	000000	Autocalibrate sawtooth divider	000000
			XXXXXX	Manual SDIV setting (see the *Manual Programming of the Spread-Spectrum Divider* section)	

Table 16. MAX9259 Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x04	D7	SEREN	**0**	Disable serial link. **Power-up default when $\overline{\text{AUTOS}}$ = high**. Reverse-channel communication remains unavailable for 350µs after the MAX9259 starts/stops the serial link.	0, 1
			1	Enable serial link. **Power-up default when $\overline{\text{AUTOS}}$ = low**. Reverse-channel communication remains unavailable for 350µs after the MAX9259 starts/stops the serial link.	
	D6	CLINKEN	0	Disable configuration link	0
			1	Enable configuration link	
	D5	PRBSEN	0	Disable PRBS test	0
			1	Enable PRBS test	
	D4	SLEEP	0	Normal mode. Default value depends on CDS and $\overline{\text{AUTOS}}$ pin values at power-up.	0, 1
			1	Activate sleep mode. Default value depends on CDS and $\overline{\text{AUTOS}}$ pin values at power-up.	
	D[3:2]	INTTYPE	00	Base mode uses I^2C peripheral interface	00
			01	Base mode uses UART peripheral interface	
			10, 11	Base mode peripheral interface disabled	
	D1	REVCCEN	0	Disable reverse control channel from deserializer (receiving)	1
			1	Enable reverse control channel from deserializer (receiving)	
	D0	FWDCCEN	0	Disable forward control channel to deserializer (sending)	1
			1	Enable forward control channel to deserializer (sending)	

Table 16. MAX9259 Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D7	I2CMETHOD	0	I²C conversion sends the register address	0
			1	Disable sending of I²C register address (command-byte-only mode)	
	D6	DISFPLL	0	Filter PLL active	1
			1	Filter PLL disabled	
	D[5:4]	CMLLVL	00	Do not use	11
			01	200mV CML signal level	
			10	300mV CML signal level	
			11	400mV CML signal level	
	D[3:0]	PREEMP	0000	Preemphasis off	0000
			0001	-1.2dB preemphasis	
			0010	-2.5dB preemphasis	
			0011	-4.1dB preemphasis	
			0100	-6.0dB preemphasis	
			0101	Do not use	
			0110	Do not use	
			0111	Do not use	
			1000	1.1dB preemphasis	
			1001	2.2dB preemphasis	
			1010	3.3dB preemphasis	
			1011	4.4dB preemphasis	
			1100	6.0dB preemphasis	
			1101	8.0dB preemphasis	
			1110	10.5dB preemphasis	
			1111	14.0dB preemphasis	
0x06	D[7:0]	—	01000000	Reserved	01000000
0x07	D[7:0]	—	00100010	Reserved	00100010
0x08	D[7:4]	—	0000	Reserved	0000 (read only)
	D[3:2]	LFNEG	00	Negative cable wire shorted to battery	10 (read only)
			01	Negative cable wire shorted to ground	
			10	Normal operation	
			11	Negative cable wire open	
	D[1:0]	LFPOS	00	Positive cable wire shorted to battery	10 (read only)
			01	Positive cable wire shorted to ground	
			10	Normal operation	
			11	Positive cable wire open	

Table 16. MAX9259 Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0D	D7	SETINT	0	Set INT low when SETINT transitions from 1 to 0	0
			1	Set INT high when SETINT transitions from 0 to 1	
	D[6:4]	—	000	Reserved	000
	D[3:0]	—	1111	Reserved	1111
0x1E	D[7:0]	ID	00000001	Device identifier (MAX9259 = 0x01)	00000001 (read only)
0x1F	D[7:4]	—	0000	Reserved	0000 (read only)
	D[3:0]	REVISION	XXXX	Device revision	(read only)

X = Don't care.

Table 17. MAX9260 Register Table

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address	1000000
	D0	—	0	Reserved	0
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address	1001000
	D0	—	0	Reserved	0
0x02	D[7:6]	SS	**00**	No spread spectrum. **Power-up default when SSEN = low**.	00, 01
			01	±2% spread spectrum. **Power-up default when SSEN = high**.	
			10	No spread spectrum	
			11	±4% spread spectrum	
	D5	—	0	Reserved	0
	D4	AUDIOEN	0	Disable I^2S channel	1
			1	Enable I^2S channel	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock	11
			01	25MHz to 50MHz pixel clock	
			10	50MHz to 104MHz pixel clock	
			11	Automatically detect the pixel clock range	
	D[1:0]	SRNG	00	0.5 to 1Gbps serial-data rate	11
			01	1 to 2Gbps serial-data rate	
			10	2 to 3.125Gbps serial-data rate	
			11	Automatically detect serial-data rate	

Table 17. MAX9260 Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x03	D[7:6]	AUTOFM	00	Calibrate spread-modulation rate only once after locking	00
			01	Calibrate spread-modulation rate every 2ms after locking	
			10	Calibrate spread-modulation rate every 16ms after locking	
			11	Calibrate spread-modulation rate every 256ms after locking	
	D5	—	0	Reserved	0
	D[4:0]	SDIV	00000	Autocalibrate sawtooth divider	00000
			XXXXX	Manual SDIV setting (see the *Manual Programming of the Spread-Spectrum Divider* section)	
0x04	D7	LOCKED	0	LOCK output is low	0 (read only)
			1	LOCK output is high	
	D6	OUTENB	0	Enable DOUT_, PCLKOUT, and I²S outputs. A transition on $\overline{\text{ENABLE}}$ changes the state of OUTENB.	0, 1
			1	Disable DOUT_, PCLKOUT, and I²S outputs. A transition on $\overline{\text{ENABLE}}$ changes the state of OUTENB.	
	D5	PRBSEN	0	Disable PRBS test	0
			1	Enable PRBS test	
	D4	SLEEP	0	Normal mode default value depends on CDS and MS pin values at power-up)	0, 1
			1	Activate sleep mode default value depends on CDS and MS pin values at power-up)	
	D[3:2]	INTTYPE	00	Base mode uses I²C peripheral interface	00
			01	Base mode uses UART peripheral interface	
			10, 11	Base mode peripheral interface disabled	
	D1	REVCCEN	0	Disable reverse control channel to serializer (sending)	1
			1	Enable reverse control channel to serializer (sending)	
	D0	FWDCCEN	0	Disable forward control channel from serializer (receiving)	1
			1	Enable forward control channel from serializer (receiving)	

Table 17. MAX9260 Register Table (continued)

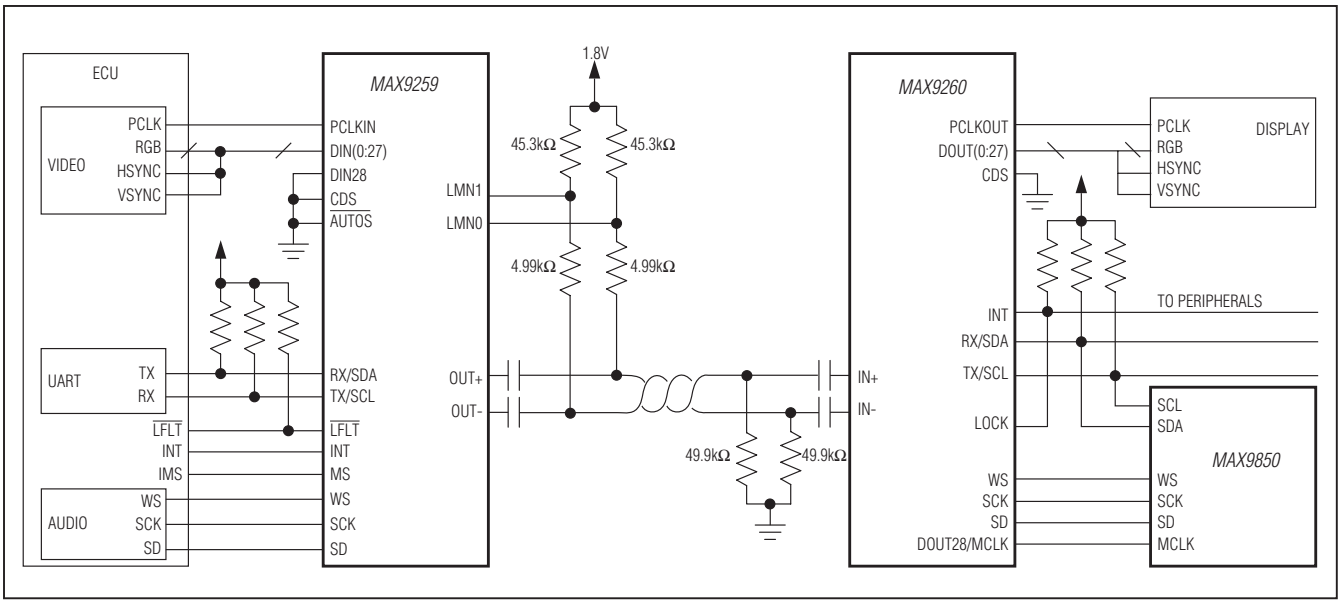
REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D7	I2CMETHOD	0	I²C conversion sends the register address	0
			1	Disable sending of I²C register address (command-byte-only mode)	
	D[6:5]	HPFTUNE	00	7.5MHz Equalizer highpass cutoff frequency	01
			01	3.75MHz cutoff frequency	
			10	2.5MHz cutoff frequency	
			11	1.87MHz cutoff frequency	
	D4	PDHF	0	High-frequency boosting enabled	0
			1	High-frequency boosting disabled	
	D[3:0]	EQTUNE	0000	2.1dB equalizer boost gain	0100, 1001
			0001	2.8dB equalizer boost gain	
			0010	3.4dB equalizer boost gain	
			0011	4.2dB equalizer boost gain	
			0100	5.2dB equalizer boost gain. **Power-up default when EQS = high**.	
			0101	6.2dB equalizer boost gain	
			0110	7dB equalizer boost gain	
			0111	8.2dB equalizer boost gain	
			1000	9.4dB equalizer boost gain	
			1001	10.7dB equalizer boost gain. **Power-up default when EQS = low**.	
			1010	11.7dB equalizer boost gain	
			1011	13dB equalizer boost gain	
			11XX	Do not use	
0x06	D7	DISSTAG	0	Enable staggered outputs	0
			1	Disable staggered outputs	
	D6	AUTORST	0	Do not automatically reset error registers and outputs	0
			1	Automatically reset error registers and outputs	
	D5	DISINT	0	Enable interrupt transmission to serializer	0
			1	Disable interrupt transmission to serializer	
	D4	INT	0	INT input = low (read only)	0 (read only)
			1	INT input = high (read only)	
	D3	GPIO1OUT	0	Output low to GPIO1	1
			1	Output high to GPIO1	
	D2	GPIO1	0	GPIO1 is low	1 (read only)
			1	GPIO1 is high	
	D1	GPIO0OUT	0	Output low to GPIO0	1
			1	Output high to GPIO0	
	D0	GPIO0	0	GPIO0 is low	1 (read only)
			1	GPIO0 is high	

Table 17. MAX9260 Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x07	D[7:0]	—	01010100	Reserved	01010100
0x08	D[7:0]	—	00110000	Reserved	00110000
0x09	D[7:0]	—	11001000	Reserved	11001000
0x0A	D[7:0]	—	00010010	Reserved	00010010
0x0B	D[7:0]	—	00100000	Reserved	00100000
0x0C	D[7:0]	ERRTHR	XXXXXXXX	Error threshold for decoding errors. $\overline{ERR}$ = low when DECERR > ERRTHR.	00000000
0x0D	D[7:0]	DECERR	XXXXXXXX	Decoding error counter. This counter remains zero while the device is in PRBS test mode.	00000000 (read only)
0x0E	D[7:0]	PRBSERR	XXXXXXXX	PRBS error counter	00000000 (read only)
0x12	D7	MCLKSRC	0	MCLK derived from PCLKOUT (see Table 3)	0
			1	MCLK derived from internal oscillator	
	D[6:0]	MCLKDIV	0000000	MCLK disabled	0000000
			XXXXXXX	MCLK divider	
0x1E	D[7:0]	ID	00000010	Device identifier (MAX9260 = 0x02)	00000010 (read only)
0x1F	D[7:4]	—	0000	Reserved	0000 (read only)
	D[3:0]	REVISION	XXXX	Device revision	(read only)

X = Don't care.

Typical Application Circuit



Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5688+2	21-0135	90-0046
64 TQFP-EP	C64E+10	21-0084	90-0329
56 QFND-EP	G5688Y+1	21-0704	90-0423

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/09	Initial release	—
1	7/10	Added clarification of fault thresholds and updated *Pin Description* table	3, 4, 8, 11, 12, 13, 15, 16, 17, 25, 28, 33, 39, 44, 48
2	11/10	Added TQFN package to *Ordering Information, Absolute Maximum Ratings*, *Pin Configurations*, *Pin Description*, and *Package Information*	1, 2, 10, 11, 50
3	1/11	Added Patent Pending to *Features*	1
4	10/14	Updated *General Description* and *Features* sections and Figure 6, clarified function, added QFND package, removed Tables 1 and 2, and renumbered subsequent tables	1, 2, 4, 6, 10–12, 18, 24, 26–30, 32–34, 36 37, 40, 41, 43–50

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