THE DATASHEET OF

ADN4667ARUZ

3 V LVDS Quad CMOS Differential Line Driver

Data Sheet

ADN4667

FEATURES

- ±15 kV ESD protection on output pins
- 400 Mbps (200 MHz) switching rates
- Flow through pinout simplifies PCB layout
- 300 ps typical differential skew
- 400 ps maximum differential skew
- 1.7 ns maximum propagation delay
- 3.3 V power supply
- ±310 mV differential signaling
- Low power dissipation (10 mW typical)
- Interoperable with existing 5 V LVDS receivers
- High impedance on LVDS outputs on power-down
- Conforms to TIA/EIA-644 LVDS standards
- Industrial operating temperature range: −40°C to +85°C
- Available in surface-mount (SOIC) and low profile TSSOP package
- Qualified for automotive applications

APPLICATIONS

- Backplane data transmission
- Cable data transmission
- Clock distribution

FUNCTIONAL BLOCK DIAGRAM

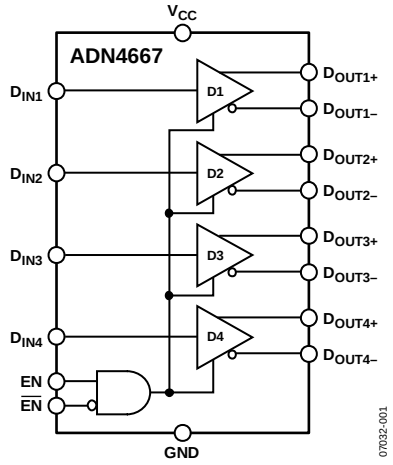

Figure 1.

GENERAL DESCRIPTION

The ADN4667 is a quad, CMOS, low voltage differential signaling (LVDS) line driver offering data rates of over 400 Mbps (200 MHz) and ultralow power consumption. It features a flow through pinout for easy PCB layout and separation of input and output signals.

The device accepts low voltage TTL/CMOS logic signals and converts them to a differential current output of typically ±3.1 mA for driving a transmission medium such as a twisted pair cable. The transmitted signal develops a differential voltage of typically ±310 mV across a termination resistor at the receiving end. This is converted back to a TTL/CMOS logic level by an LVDS receiver, such as the ADN4668.

The ADN4667 also offers active high and active low enable/disable inputs (EN and $\overline{EN}$). These inputs control all four drivers and turn off the current outputs in the disabled state to reduce the quiescent power consumption to typically 10 mW.

The ADN4667 and its companion LVDS receiver, the ADN4668, offer a new solution to high speed, point-to-point data transmission, and a low power alternative to emitter-coupled logic (ECL) or positive emitter-coupled logic (PECL).

Rev. B

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1/08—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V; R_L = 100 Ω; C_L = 15 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are given for V_{CC} = +3.3 V, T_A = +25°C.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Comments[1, 2]
LVDS OUTPUTS (D_{OUT+}, D_{OUT-})						
Differential Output Voltage	V_{OD}	250	310	450	mV	See Figure 2 and Figure 4
Change in Magnitude of V_{OD} for Complementary Output States	ΔV_{OD}		1	35	|mV|	See Figure 2 and Figure 4
Offset Voltage	V_{OS}	1.125	1.17	1.375	V	See Figure 2 and Figure 4
Change in Magnitude of V_{OS} for Complementary Output States	ΔV_{OS}		1	25	|mV|	See Figure 2 and Figure 4
Output High Voltage	V_{OH}		1.33	1.6	V	See Figure 2 and Figure 4
Output Low Voltage	V_{OL}	0.90	1.02		V	See Figure 2 and Figure 4
INPUTS (D_{IN}, EN, $\overline{EN}$)						
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Input Low Voltage	V_{IL}	GND		0.8	V	
Input High Current	I_{IH}	−10	+2	+10	µA	$V_{IN} = V_{CC}$ or 2.5 V
Input Low Current	I_{IL}	−10	+2	+10	µA	V_{IN} = GND or 0.4 V
Input Clamp Voltage	V_{CL}	−1.5	−0.8		V	I_{CL} = −18 mA
LVDS OUTPUT PROTECTION (D_{OUT+}, D_{OUT-})						
Output Short-Circuit Current[3]	I_{OS}		−4.2	−9.0	mA	Enabled, $D_{IN} = V_{CC}$, D_{OUT+} = 0 V or D_{IN} = GND, D_{OUT-} = 0 V
Differential Output Short-Circuit Current[3]	I_{OSD}		−4.2	−9.0	mA	Enabled, V_{OD} = 0 V
LVDS OUTPUT LEAKAGE (D_{OUT+}, D_{OUT-})						
Power-Off Leakage	I_{OFF}	−20	±1	+20	µA	V_{OUT} = 0 V or 3.6 V, V_{CC} = 0 V or open
Output Three-State Current	I_{OZ}	−10	±1	+10	µA	EN = 0.8 V and $\overline{EN}$ = 2.0 V, V_{OUT} = 0 V or V_{CC}
POWER SUPPLY						
No Load Supply Current, Drivers Enabled	I_{CC}		4.0	8.0	mA	$D_{IN} = V_{CC}$ or GND
Loaded Supply Current, Drivers Enabled	I_{CCL}		20	30	mA	R_L = 100 Ω all channels, $D_{IN} = V_{CC}$ or GND (all inputs)
No Load Supply Current, Drivers Disabled	I_{CCZ}		2.2	6.0	mA	$D_{IN} = V_{CC}$ or GND, EN = GND, $\overline{EN} = V_{CC}$
ESD PROTECTION						
D_{OUT+}, D_{OUT-}			±15		kV	Human body model
All Pins Except D_{OUT+}, D_{OUT-}			±4		kV	Human body model

[1] Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}, ΔV_{OD}, and ΔV_{OS}.
[2] The ADN4667 is a current mode device and functions within data sheet specifications only when a resistive load is applied to the driver outputs. Typical range is 90 Ω to 110 Ω.
[3] Output short-circuit current (I_{OS}) is specified as magnitude only; minus sign indicates direction only.

AC CHARACTERISTICS

V_{CC} = 3.0 V to 3.6 V; R_L = 100 Ω; C_L[1] = 15 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are given for V_{CC} = +3.3 V, T_A = +25°C.

Table 2.

Parameter[2]	Min	Typ	Max	Unit	Conditions/Comments[3, 4]
Differential Propagation Delay, High to Low, t_{PHLD}	0.5	0.9	1.7	ns	See Figure 3 and Figure 4
Differential Propagation Delay, Low to High, t_{PLHD}	0.5	1.2	1.7	ns	See Figure 3 and Figure 4
Differential Pulse Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$, t_{SKD1}[5]	0	0.3	0.4	ns	See Figure 3 and Figure 4
Channel-to-Channel Skew, t_{SKD2}[6]	0	0.4	0.5	ns	See Figure 3 and Figure 4
Differential Part-to-Part Skew, t_{SKD3}[7]	0		1.0	ns	See Figure 3 and Figure 4
Differential Part-to-Part Skew, t_{SKD4}[8]	0		1.2	ns	See Figure 3 and Figure 4
Rise Time, t_r		0.5	1.5	ns	See Figure 3 and Figure 4
Fall Time, t_f		0.5	1.5	ns	See Figure 3 and Figure 4
Disable Time High to Inactive, t_{PHZ}		2	5	ns	See Figure 5 and Figure 6
Disable Time Low to Inactive, t_{PLZ}		2	5	ns	See Figure 5 and Figure 6
Enable Time Inactive to High, t_{PZH}		3	7	ns	See Figure 5 and Figure 6
Enable Time Inactive to Low, t_{PZL}		3	7	ns	See Figure 5 and Figure 6
Maximum Operating Frequency, f_{MAX}[9]	200	250		MHz	See Figure 5 and Figure 6

[1] C_L includes probe and jig capacitance.
[2] AC parameters are guaranteed by design and characterization.
[3] Generator waveform for all tests unless otherwise specified: f = 50 MHz, Z_O = 50 Ω, $t_r \le 1$ ns, and $t_f \le 1$ ns.
[4] All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.
[5] $t_{SKD1} = \lvert t_{PHLD} - t_{PLHD} \rvert$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
[6] t_{SKD2} is the differential channel-to-channel skew of any event on the same device.
[7] t_{SKD3}, differential part-to-part skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
[8] t_{SKD4}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperatures and voltage ranges, and across process distribution. t_{SKD4} is defined as |maximum − minimum| differential propagation delay.
[9] f_{MAX} generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% to 55%, $V_{OD} > 250$ mV, all channels switching.

Test Circuits and Timing Diagrams

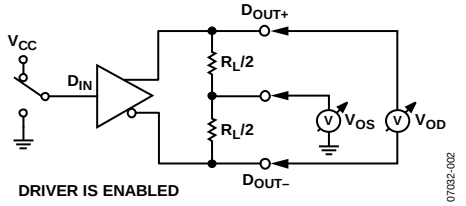


Figure 2. Test Circuit for Driver V_{OD} and V_{OS}

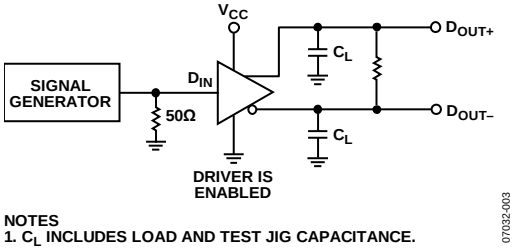


Figure 3. Test Circuit for Driver Propagation Delay and Transition Time

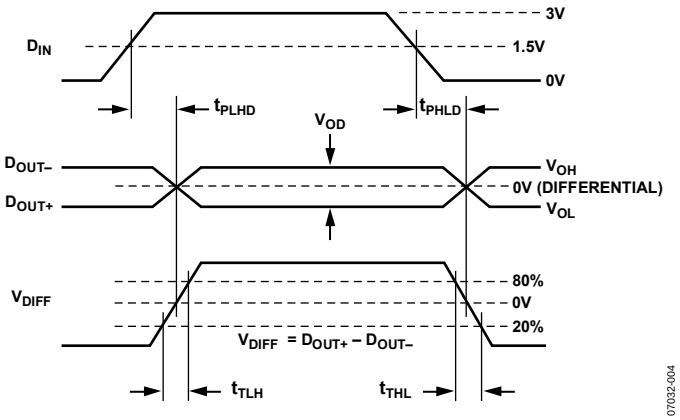


Figure 4. Driver Propagation Delay and Transition Time Waveforms

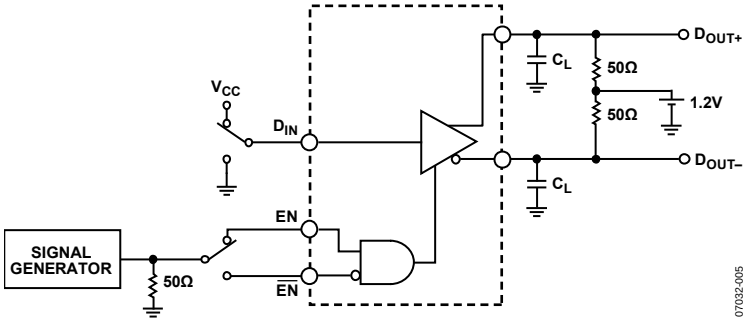


Figure 5. Test Circuit for Driver Three-State Delay

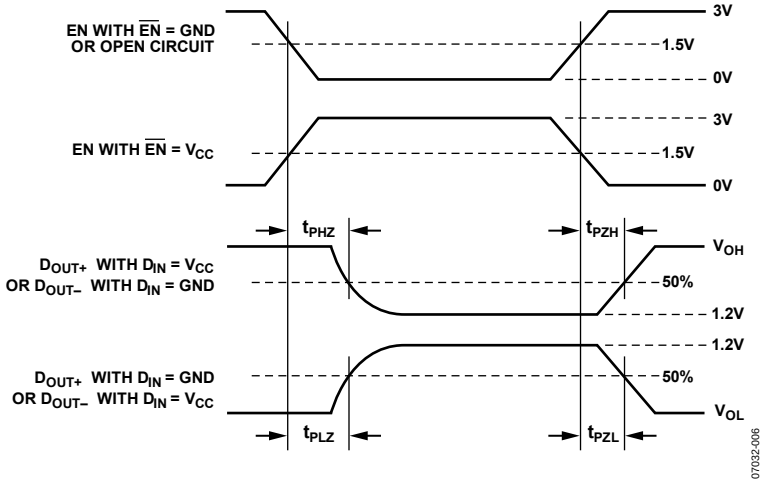


Figure 6. Driver Three-State Delay Waveforms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.3 V to +4 V
Input Voltage (D_{IN}) to GND	−0.3 V to V_{CC} + 0.3 V
Enable Input Voltage (EN, $\overline{EN}$) to GND	−0.3 V to V_{CC} + 0.3 V
Output Voltage (D_{OUT+}, D_{OUT-}) to GND	−0.3 V to V_{CC} + 0.3 V
Short-Circuit Duration (D_{OUT+}, D_{OUT-}) to GND	Continuous
Industrial Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	
TSSOP Package	150.4°C/W
SOIC Package	125°C/W
Reflow Soldering Peak Temperature (10sec)	260°C max

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

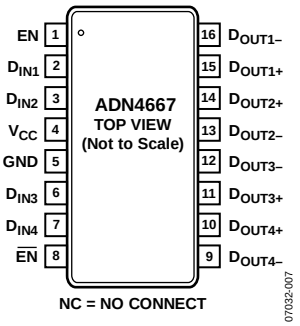


Figure 7. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Active High Enable and Power-Down Input (3 V TTL/CMOS). If $\overline{EN}$ is held low or open circuit, EN enables the drivers when high and disables the drivers when low.
2	D_{IN1}	Driver Channel 1 Logic Input.
3	D_{IN2}	Driver Channel 2 Logic Input.
4	V_{CC}	Power Supply Input. These parts can be operated from 3.0 V to 3.6 V. The supply should be decoupled with a 10 µF solid tantalum capacitor in parallel with a 0.1 µF capacitor to GND.
5	GND	Ground Reference Point for All Circuitry on the Part.
6	D_{IN3}	Driver Channel 3 Logic Input.
7	D_{IN4}	Driver Channel 4 Logic Input.
8	$\overline{EN}$	Active Low Enable and Power-Down Input with Pull-Down (3 V TTL/CMOS). If EN is held high, $\overline{EN}$ enables the drivers when low or open circuit and disables the drivers and powers down the device when high.
9	D_{OUT4-}	Channel 4 Inverting Output Current Driver. When D_{IN4} is high, current flows into D_{OUT4-}. When D_{IN4} is low, current flows out of D_{OUT4-}.
10	D_{OUT4+}	Channel 4 Noninverting Output Current Driver. When D_{IN4} is high, current flows out of D_{OUT4+}. When D_{IN4} is low, current flows into D_{OUT4+}.
11	D_{OUT3+}	Channel 3 Noninverting Output Current Driver. When D_{IN3} is high, current flows out of D_{OUT3+}. When D_{IN3} is low, current flows into D_{OUT3+}.
12	D_{OUT3-}	Channel 3 Inverting Output Current Driver. When D_{IN3} is high, current flows into D_{OUT3-}.When D_{IN3} is low, current flows out of D_{OUT3-}.
13	D_{OUT2-}	Channel 2 Inverting Output Current Driver. When D_{IN2} is high, current flows into D_{OUT2-}. When D_{IN2} is low, current flows out of D_{OUT2-}.
14	D_{OUT2+}	Channel 2 Noninverting Output Current Driver. When D_{IN2} is high, current flows out of D_{OUT2+}. When D_{IN2} is low, current flows into D_{OUT2+}.
15	D_{OUT1+}	Channel 1 Noninverting Output Current Driver. When D_{IN1} is high, current flows out of D_{OUT1+}. When D_{IN1} is low, current flows into D_{OUT1+}.
16	D_{OUT1-}	Channel 1 Inverting Output Current Driver. When D_{IN1} is high, current flows into D_{OUT1-}. When D_{IN1} is low, current flows out of D_{OUT1-}.

TYPICAL PERFORMANCE CHARACTERISTICS

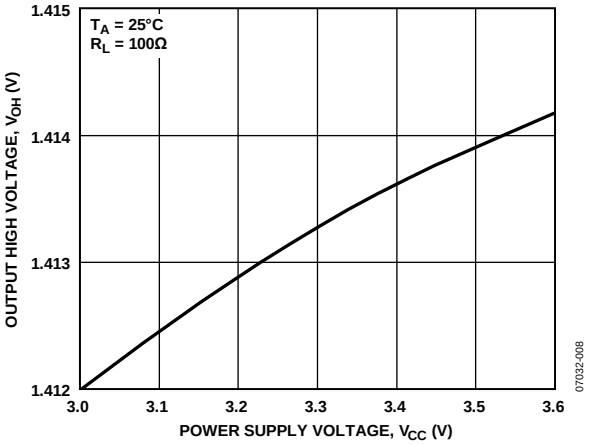


Figure 8. Output High Voltage vs. Power Supply Voltage

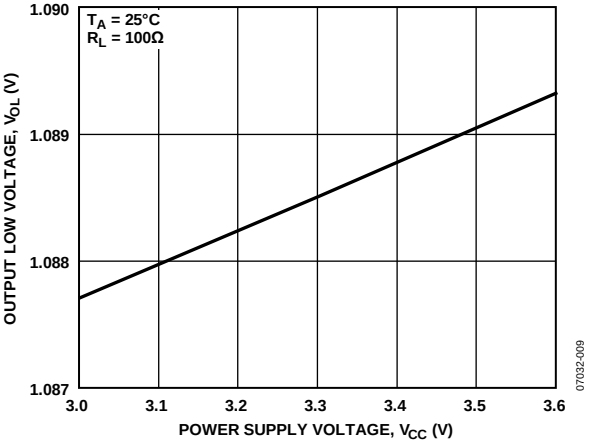


Figure 9. Output Low Voltage vs. Power Supply Voltage

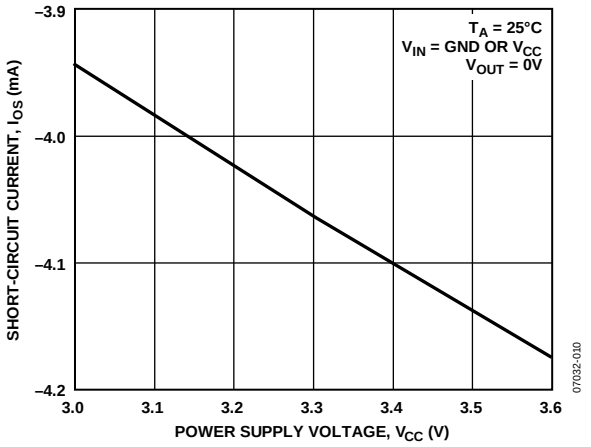


Figure 10. Output Short-Circuit Current vs. Power Supply Voltage

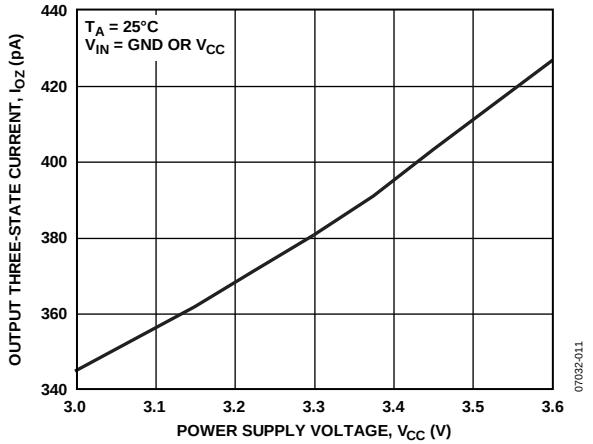


Figure 11. Output Three-State Current vs. Power Supply Voltage

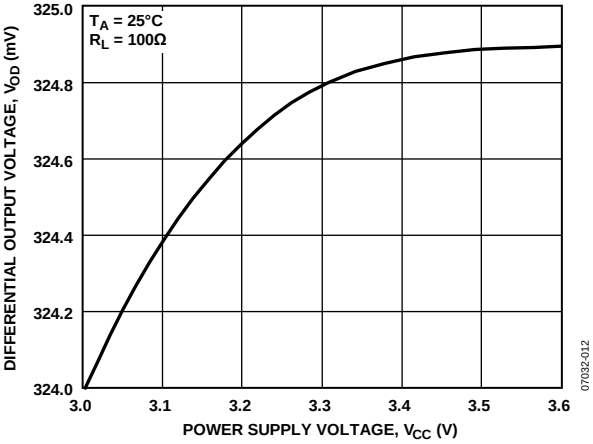


Figure 12. Differential Output Voltage vs. Power Supply Voltage

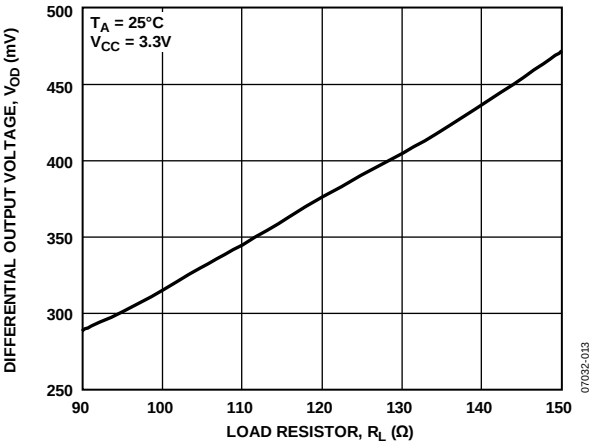


Figure 13. Differential Output Voltage vs. Load Resistor

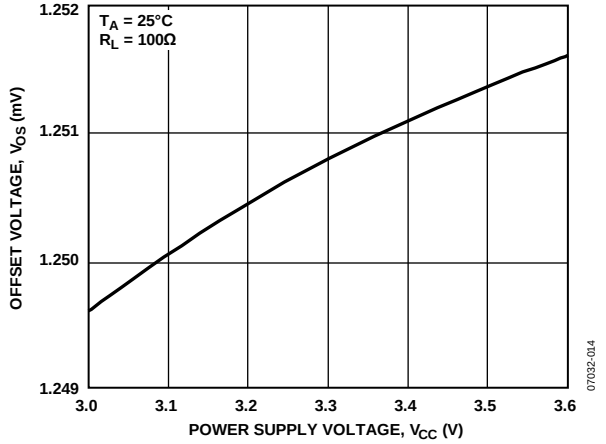


Figure 14. Offset Voltage vs. Power Supply Voltage

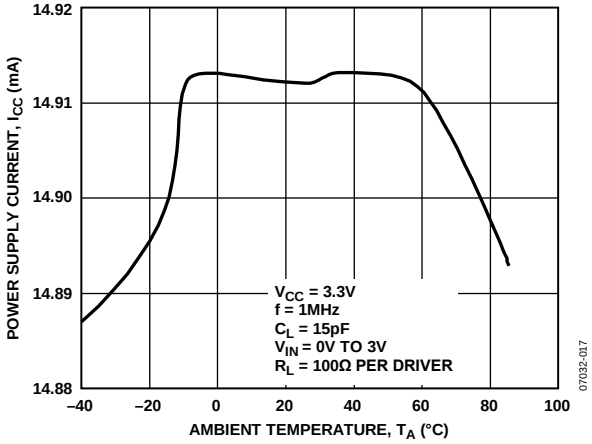


Figure 17. Power Supply Current vs. Ambient Temperature

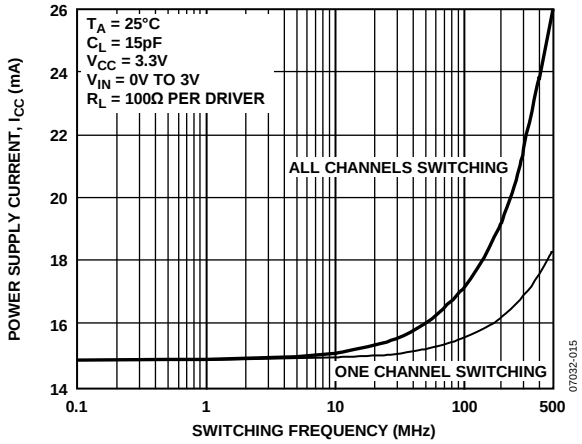


Figure 15.Power Supply Current vs. Switching Frequency

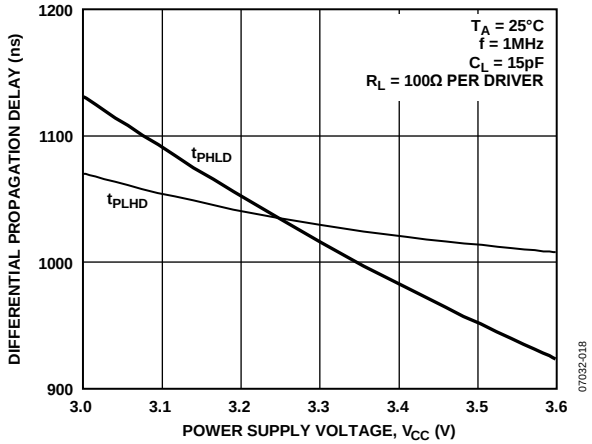


Figure 18. Differential Propagation Delay vs. Power Supply Voltage

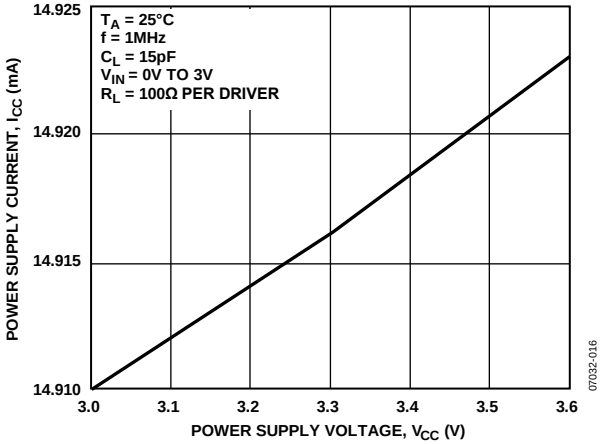


Figure 16. Power Supply Current vs. Power Supply Voltage

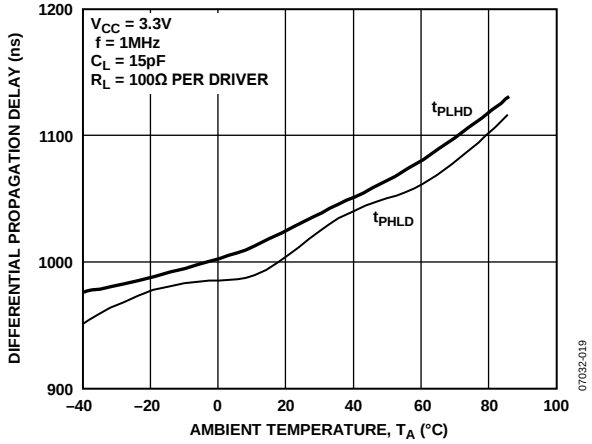


Figure 19. Differential Propagation Delay vs. Ambient Temperature

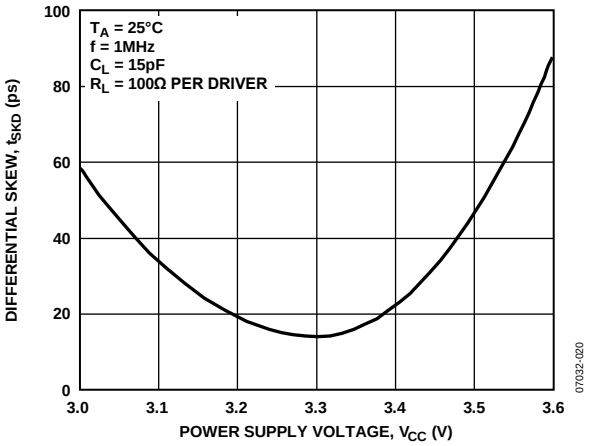


Figure 20. Differential Skew vs. Supply Voltage

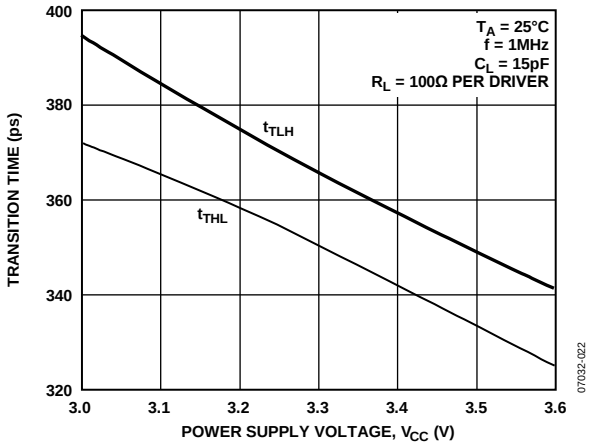


Figure 22. Transition Time vs. Supply Voltage

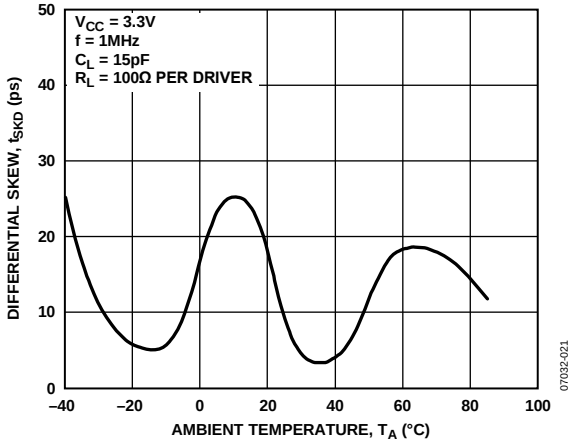


Figure 21. Differential Skew vs. Ambient Temperature

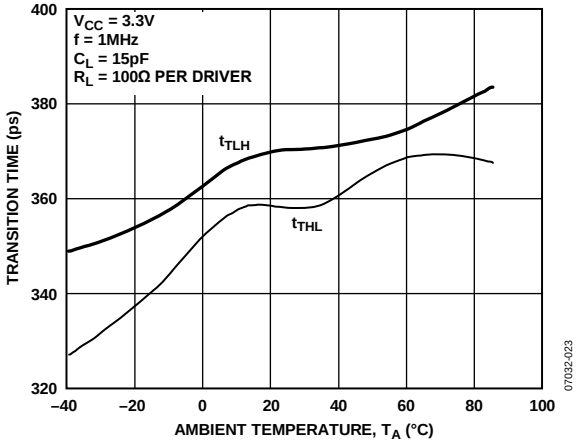


Figure 23. Transition Time vs. Ambient Temperature

THEORY OF OPERATION

The ADN4667 is a quad line driver for low voltage differential signaling. It takes a single-ended 3 V logic signal and converts it to a differential current output. The data can then be transmitted for considerable distances, over media such as a twisted pair cable or PCB backplane, to an LVDS receiver like the ADN4668, where it develops a voltage across a terminating resistor, R_T. This resistor is chosen to match the characteristic impedance of the medium, typically around 100 Ω. The differential voltage is detected by the receiver and converted back into a single-ended logic signal.

When D_{IN} is high (Logic 1), current flows out of the D_{OUT+} pin (current source) through R_T and back into the D_{OUT-} pin (current sink). At the receiver, this current develops a positive differential voltage across R_T (with respect to the inverting input) and gives a Logic 1 at the receiver output. When D_{IN} is low, D_{OUT+} sinks current and D_{OUT-} sources current; a negative differential voltage across R_T gives a Logic 0 at the receiver output.

The output drive current is between ±2.5 mA and ±4.5 mA (typically ±3.1 mA), developing between ±250 mV and ±450 mV across a 100 Ω termination resistor. The received voltage is centered around the receiver offset of 1.2 V. Therefore, the noninverting receiver input is typically (1.2 V + [310 mV/2]) = 1.355 V, and the inverting receiver input is (1.2 V − [310 mV/2]) = 1.045 V for Logic 1. For Logic 0, the inverting and noninverting output voltages are reversed. Note that because the differential voltage reverses polarity, the peak-to-peak voltage swing across R_T is twice the differential voltage.

Current mode drivers offer considerable advantages over voltage mode drivers such as RS-422 drivers. The operating current remains fairly constant with increased switching frequency, whereas that of voltage mode drivers increase exponentially in most cases. This is caused by the overlap as internal gates switch between high and low, which causes currents to flow from the device power supply to ground. A current mode device simply reverses a constant current between its two outputs, with no significant overlap currents.

This is similar to emitter-coupled logic (ECL) and positive emitter-coupled logic (PECL), but without the high quiescent current of ECL and PECL.

ENABLE INPUTS

The active high and active low enable inputs deactivate all the current drivers when in the disabled state. This also powers down the device and reduces the current consumption from typically 20 mA to typically 2.2 mA. A truth table for the enable inputs is shown in Table 5.

Table 5. Enable Inputs Truth Table

EN	$\overline{EN}$	D_{IN}	D_{OUT+}	D_{OUT-}
H	L or open	L	I_{SINK}	I_{SOURCE}
H	L or open	H	I_{SOURCE}	I_{SINK}
Any other combination of EN and $\overline{EN}$		X	Inactive	Inactive

APPLICATIONS INFORMATION

Figure 24 shows a typical application for point-to-point data transmission using the ADN4667 as the driver and the ADN4668 as the receiver.

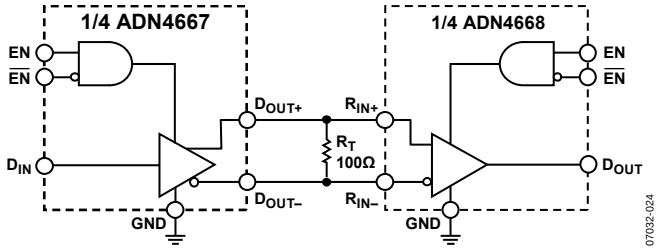
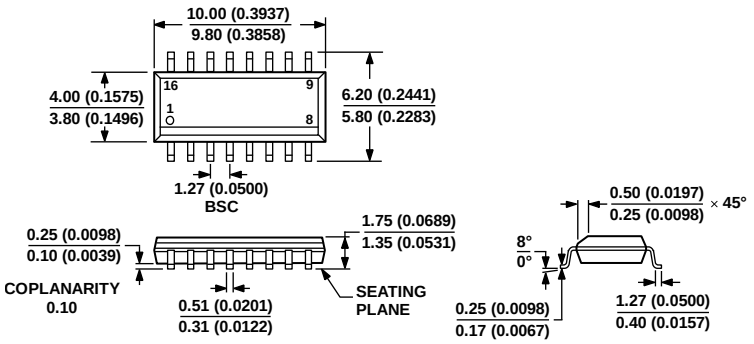


Figure 24. Typical Application Circuit

OUTLINE DIMENSIONS

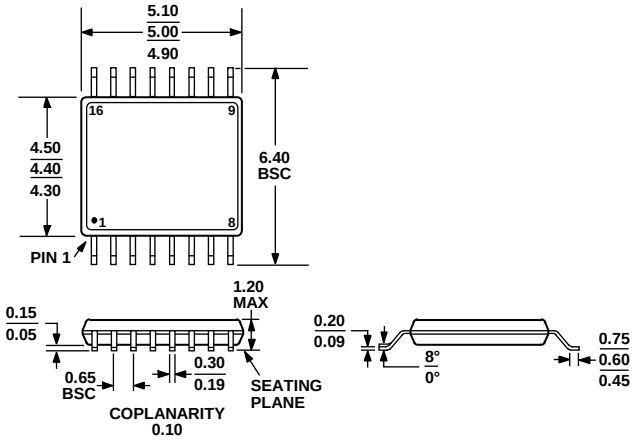


COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 25. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 26. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADN4667ARZ	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADN4667ARZ-REEL7	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADN4667ARUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADN4667ARUZ-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADN4667WARZ-REEL7	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications

AUTOMOTIVE PRODUCTS

The ADN4667W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.

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