



**THE DATASHEET OF  
PE43204MLIBA-Z**



**Product Description**

The PE43204 is a 50Ω, HaRP™-enhanced, high linearity, 2-bit RF Digital Step Attenuator (DSA) covering an 18 dB attenuation range in 6 dB steps. With a parallel control interface, it maintains high attenuation accuracy, fast switching speed, low insertion loss and low power consumption. This next generation Peregrine DSA is available in a 3x3 mm 12-lead QFN footprint.

The PE43204 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

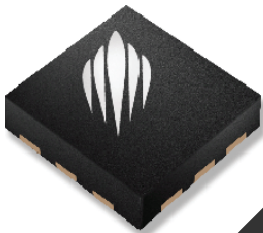
**50 Ω RF Digital Attenuator**  
**2-bit; 0, 6, 12, and 18 dB States**

**Features**

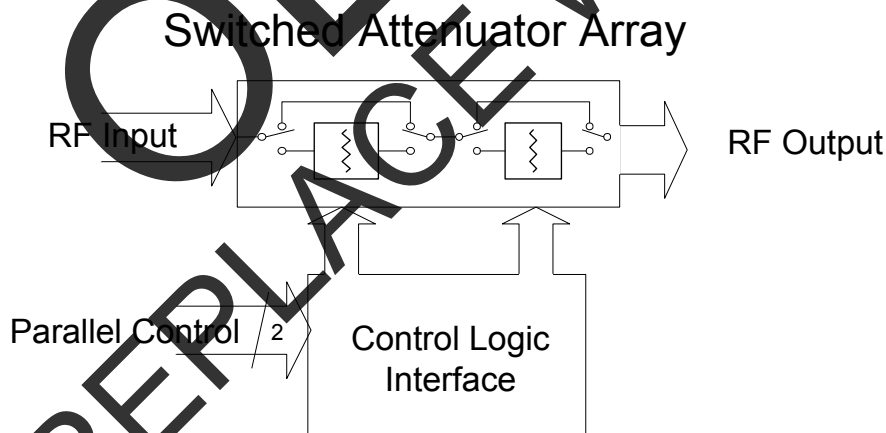
- HaRP™-enhanced UltraCMOS™ device
- Fast switching speed: Typical 26 ns
- High Linearity: Typical +61 dBm IP3
- Small α-Error
- Best in class 2000 V HBM ESD tolerance
- Attenuation: 6, 12, and 18 dB States
- Parallel Control
- CMOS Compatible
- Packaged in a 12-lead 3x3x0.85 mm QFN

**Figure 1. Package Type**

12-lead 3x3x0.85 mm QFN Package



**Figure 2. Functional Schematic Diagram**

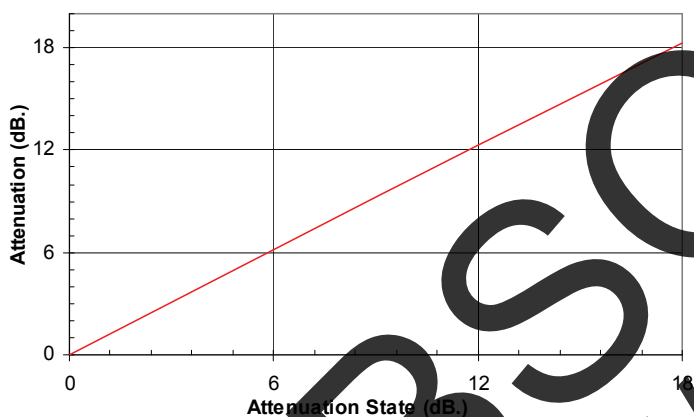


**Table 1. Electrical Specifications @ +25°C, V<sub>DD</sub> = 3.3 V**

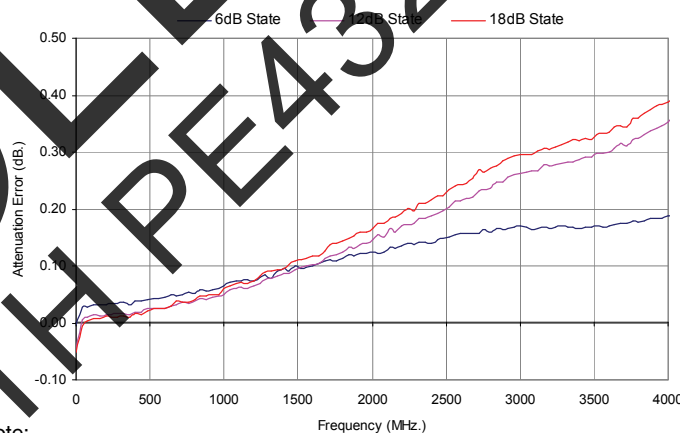
Parameter	Test Conditions	Min	Typical	Max	Units
Frequency Range			50 - 3000		MHz
Attenuation Range	6 dB, 12 dB and 18 dB steps		0 - 18		dB
Insertion Loss			0.6	0.7	dB
Attenuation Error	0 dB - 18 dB Attenuation Settings 50 MHz to < 2000 MHz 2000 MHz - 3000 MHz		+0.1	-0.25 / + 0.40	dB
			+0.2	-0.10 / +0.50	dB
Return Loss			15		dB
Relative Phase	All States		11		deg
P1dB	Input	+28	+30		dBm
IIP3	IIP3 Two tones at +18 dBm, 20 MHz spacing		+61		dBm
Switching Speed	50% DC CTRL to 10% / 90% RF		26		ns

**Performance Plots**

**Figure 3. Attenuation vs. Attenuation Setting**

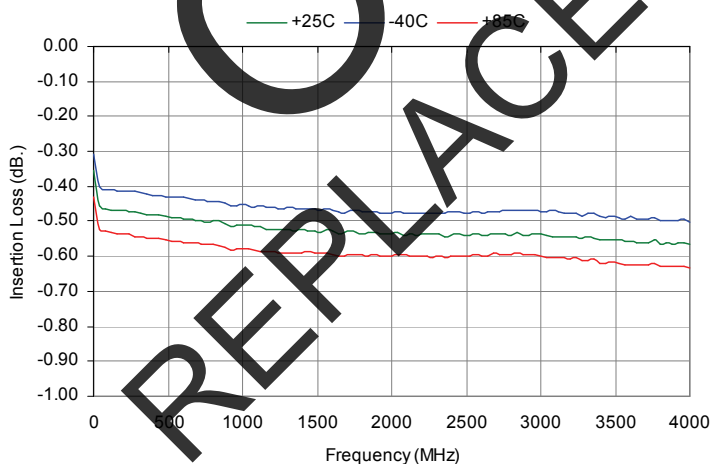


**Figure 4. Attenuation Error vs. Frequency @ T = +25°C**

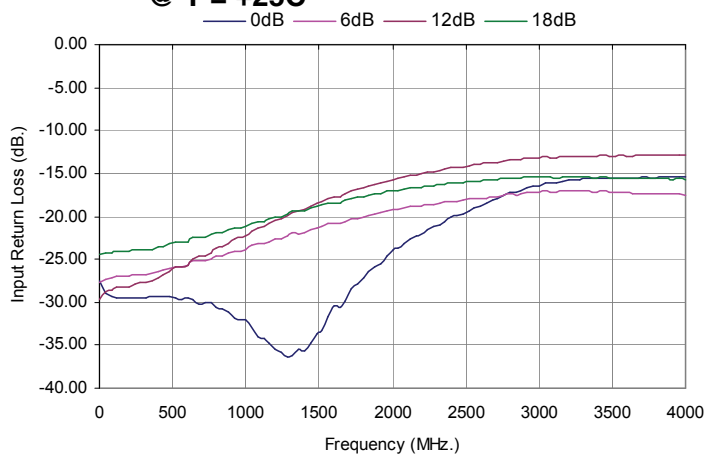


Note:  
Attenuation Error Equation -  $AE = [ ABS \{ ABS(Insertion Loss @ Attenuation Setting) - ABS(Reference Loss) \} ] - [ ABS(Attenuation Setting) ]$

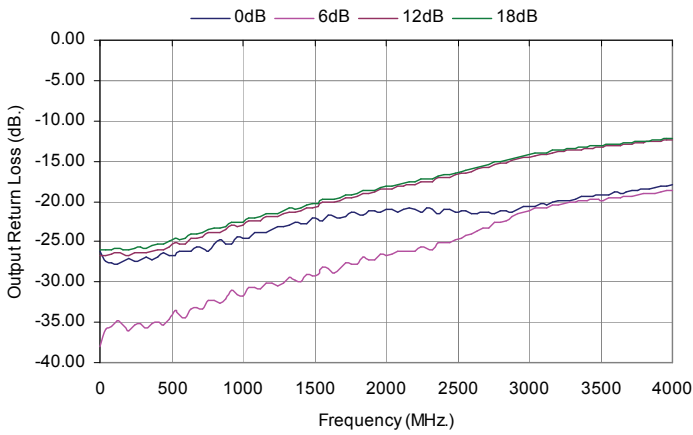
**Figure 5. Insertion Loss vs. Temperature**



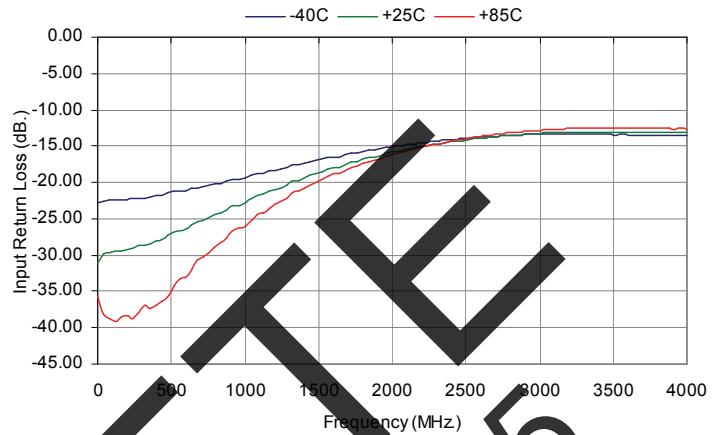
**Figure 6. Input Return Loss vs Attenuation @ T = +25°C**



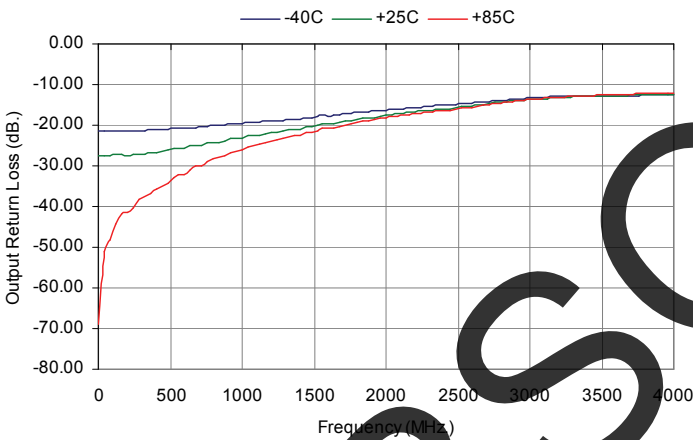
**Figure 7. Output Return Loss vs Attenuation @ T = +25C**



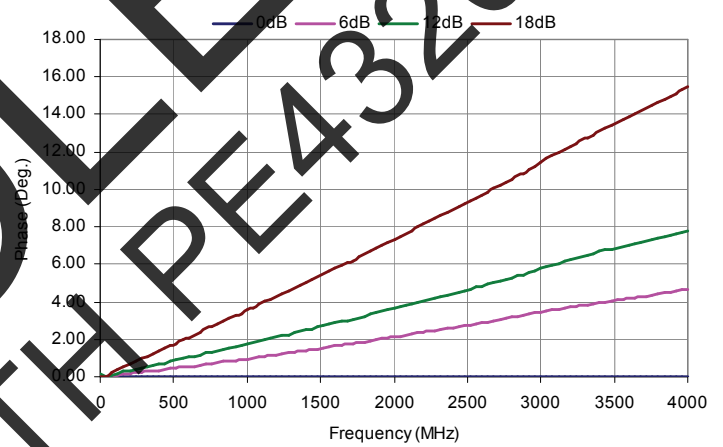
**Figure 8. Input Return Loss vs Temperature @ 12dB State**



**Figure 9. Output Return Loss vs Temperature @ 12dB State**

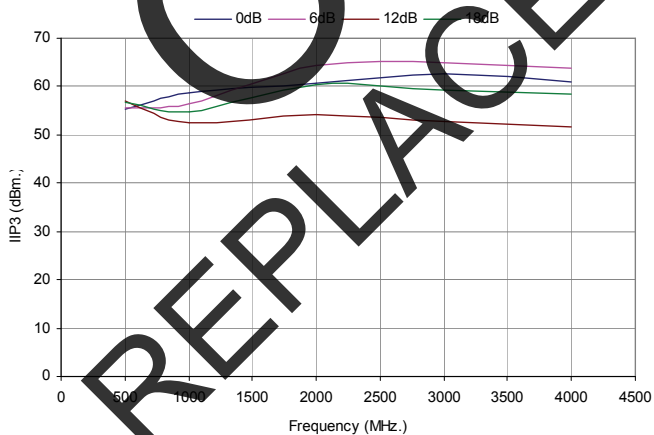


**Figure 10. Relative Phase\* vs Frequency @ T = +25C**



\*Relative Phase = Phase (attenuation state) – Phase (Insertion Loss state)

**Figure 11. Input IP3 vs Attenuation Setting @ T = +25C**



**Figure 12. Attenuation Error vs. Attenuation Setting @ 3000 MHz**

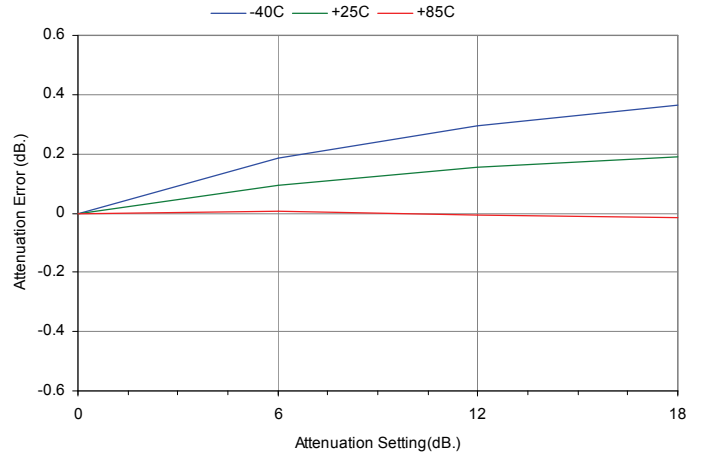


Figure 13. Pin Configuration (Top View)

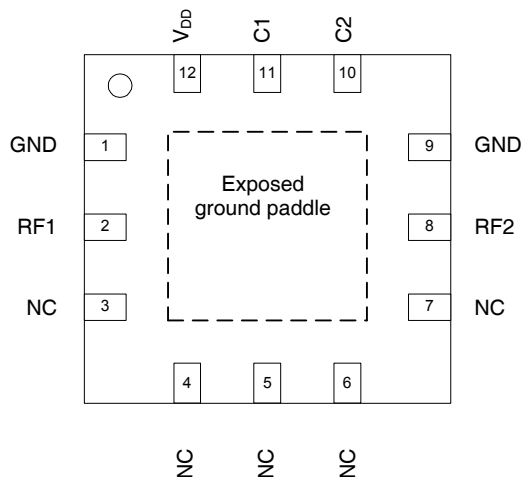


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	GND	Ground
2	RF1 <sup>2</sup>	RF1 port
3	NC <sup>1</sup>	No Connect
4	NC <sup>1</sup>	No Connect
5	NC <sup>1</sup>	No Connect
6	NC <sup>1</sup>	No Connect
7	NC <sup>1</sup>	No Connect
8	RF2 <sup>2</sup>	RF2 port
9	GND	Ground
10	C2	Attenuation control bit, 12 dB
11	C1	Attenuation control bit, 6 dB
12	V <sub>DD</sub>	Power Supply Pin

Notes: 1. Pins 3 through 7 may be tied to ground if desired, but they are not connected to ground internal to the package.  
2. All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

### Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Table 3. Attenuation Word Truth Table

C1	C2	Attenuation Setting RF1-RF2
L	L	Reference I.L.
H	L	6 dB
L	H	12 dB
H	H	18 dB

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Units
V <sub>DD</sub> Power Supply Voltage	3.0	3.3	3.6	V
I <sub>DD</sub> Power Supply Current		8	200	μA
Digital Input High	0.7xV <sub>DD</sub>		3.6	V
Digital Input Low	0		0.3xV <sub>DD</sub>	V
Digital Input Leakage			10	μA
P <sub>IN</sub> Input power (50Ω) 20 MHz ≤ f < 4.0 GHz			+23	dBm
T <sub>OP</sub> Operating temperature range	-40	25	85	°C

Table 5. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V <sub>DD</sub>	Power supply voltage	-0.3	4.0	V
V <sub>I</sub>	Voltage on any Digital input	-0.3	V <sub>DD</sub> +0.3	V
T <sub>ST</sub>	Storage temperature range	-65	150	°C
P <sub>IN</sub>	Input power (50Ω) 20 MHz ≤ f < 4.0 GHz		+23	dBm
V <sub>ESD</sub>	ESD voltage (Human Body Model, MIL-STD-883 Method 3015.7)		2000	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

### Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

### Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

### Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE43204 in the 12-lead 3x3 QFN package is MSL1.

### Switching Frequency

The PE43204 has a maximum 25 kHz switching rate. Switching rate is defined to be the speed at which the DSA can be toggled across attenuation states.

## Evaluation Kit

The 2-bit DSA EK Board was designed to ease customer evaluation of Peregrine's PE43204.

For automated programming, connect the test harness provided with the EVK to the parallel port of the PC and to the 6-pin header of the PCB. Connect the loose wire of the supplied cable to a power supply set at 3.3V DC. Set the SP3T switches S1 and S2 to the 'MIDDLE' toggle position. After downloading and installing the DSA EVK software from [www.psemi.com](http://www.psemi.com), run the software and select 'PE43204' from the drop down menu. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

For manual programming, disconnect the test harness provided with the EVK. Apply 3.3V to the Vdd header pin and Ground to the GND header pin. The DUT can be controlled two ways:

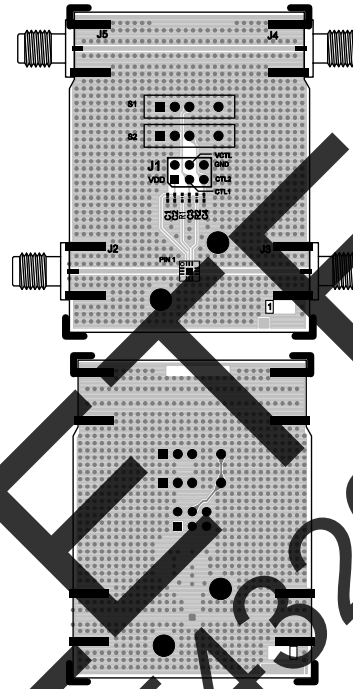
1. *The mechanical switches in conjunction with the VCTL pin can be used.* Apply desired control voltage to VCTL header pin. The top mechanical switch controls the 6dB stage, the bottom mechanical switch controls the 12dB stage. For each switch, the left position is the 0V condition, while the right position is the Vctrl condition. The middle position leaves the control pin floating.
2. *The CTL1 and CTL2 pins on the header can be used.* Each pin directly controls the 6dB and 12dB stage respectively. The VCTL pin on the header is left open. The mechanical switches may be left uninstalled or must be kept in the middle position.

Note: To minimize switching time, C3 and C4 can be removed.

## Power-up Control Settings

The PE43204 will always power up into the state determined by the voltages on the 2 control pins. The DSA can be preset to any state within the 18 dB range by pre-setting the parallel control pins prior to power-up. There is a 10µs delay between the time the DSA is powered-up to the time the desired state is set. If the control pins are left floating during power-up, the device will default to the minimum attenuation setting (insertion loss state).

**Figure 14. Evaluation Board Layouts**  
Peregrine Specification 101/0344



**Figure 15. Evaluation Board Schematic**  
Peregrine Specification 102/0416

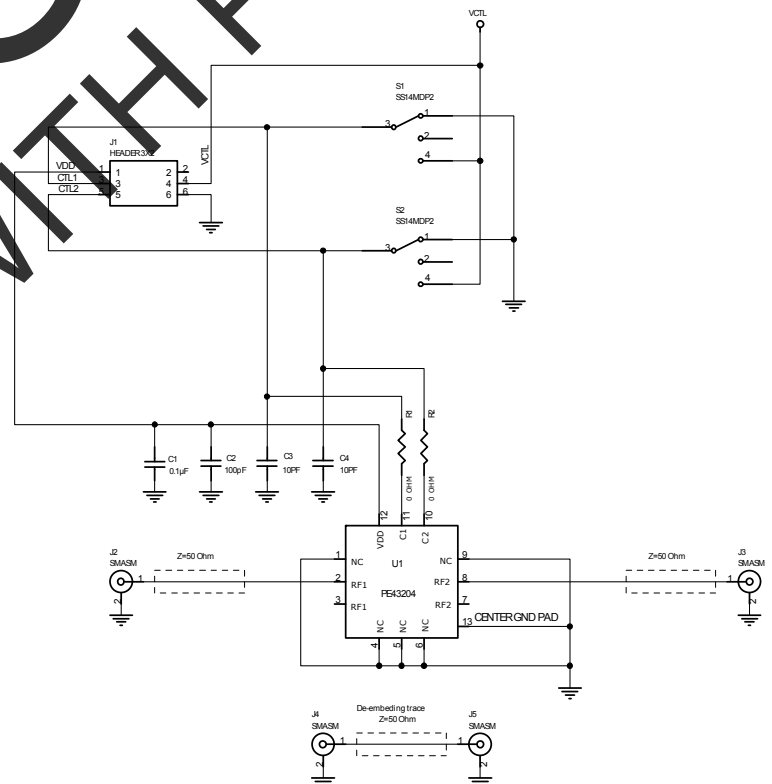
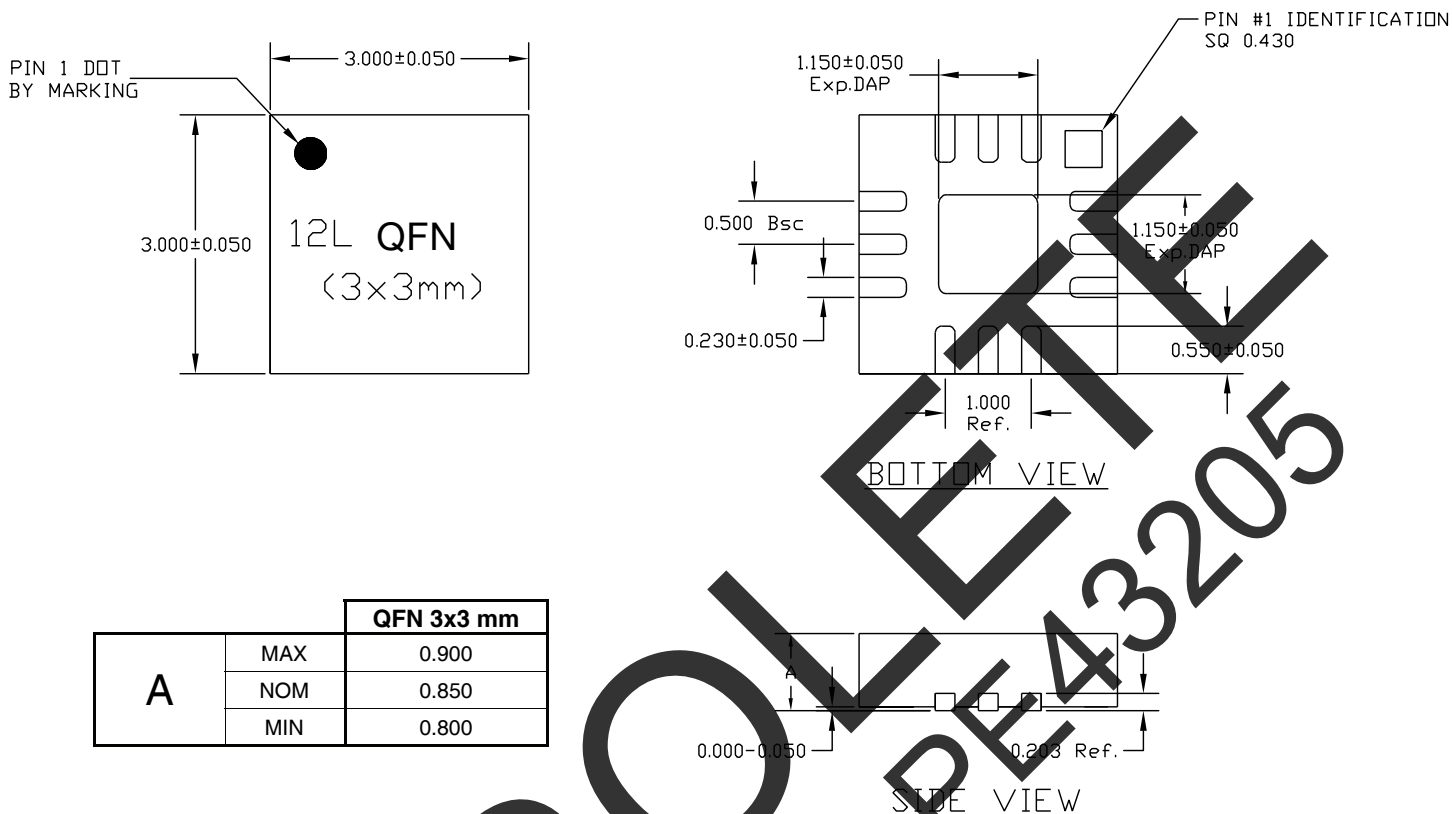


Figure 16. Package Drawing

3x3 mm 12-lead QFN, BOM 19/0104



QFN 3x3 mm		
A	MAX	0.900
	NOM	0.850
	MIN	0.800

Note: Pin 1 Identification tab is electrically connected to the exposed ground paddle

OBSOLETE  
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The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

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