THE DATASHEET OF

AD8307AN

Low Cost, DC to 500 MHz, 92 dB Logarithmic Amplifier

Data Sheet **AD8307**

FEATURES

- Complete multistage logarithmic amplifier
- 92 dB dynamic range: −75 dBm to +17 dBm to −90 dBm using matching network
- Single supply of 2.7 V minimum at 7.5 mA typical
- DC to 500 MHz operation, ±1 dB linearity
- Slope of 25 mV/dB, intercept of −84 dBm
- Highly stable scaling over temperature
- Fully differential dc-coupled signal path
- 100 ns power-up time, 150 µA sleep current

APPLICATIONS

- Conversion of signal level to decibel form
- Transmitter antenna power measurement
- Receiver signal strength indication (RSSI)
- Low cost radar and sonar signal processing
- Network and spectrum analyzers (to 120 dB)
- Signal level determination down to 20 Hz
- True decibel ac mode for multimeters

GENERAL DESCRIPTION

The AD8307 is the first logarithmic amplifier made available in an 8-lead SOIC_N package. It is a complete 500 MHz monolithic demodulating logarithmic amplifier based on the progressive compression (successive detection) technique, providing a dynamic range of 92 dB to ±3 dB law conformance and 88 dB to a tight ±1 dB error bound at all frequencies up to 100 MHz. The AD8307 is extremely stable and easy to use, requiring no significant external components. A single-supply voltage of 2.7 V to 5.5 V at 7.5 mA is needed. A fast acting CMOS-compatible control pin can disable the AD8307 to a standby current of 150 µA.

The AD8307 operates over the industrial temperature range of −40°C to +85°C and is available in an 8-lead SOIC package and an 8-lead PDIP.

FUNCTIONAL BLOCK DIAGRAM

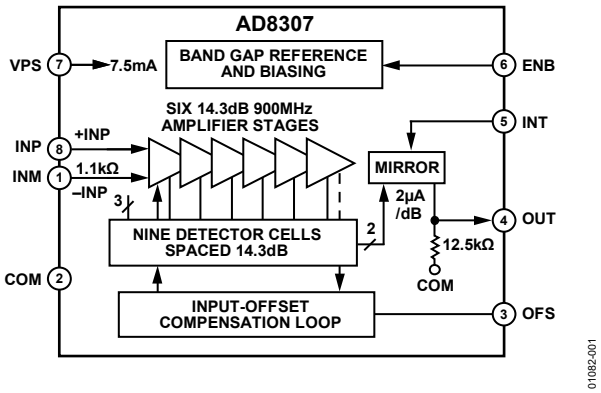

Figure 1.

Table 1. Next Generation Upgrades for the AD8307

Device No.	Product Description
AD8310	15 ns Response Time, Buffered Output
ADL5513	Lower Input Range (80 dB), Operation to 4 GHz, Higher Power Consumption
AD8309	Higher Input Range (100 dB), Limiter Output

Rev. F
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9/2015—Rev. D to Rev. E

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10/2006—Rev. B to Rev. C

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6/2003—Rev. A to Rev. B

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SPECIFICATIONS

V_S = 5 V, T_A = 25°C, R_L ≥ 1 MΩ, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
GENERAL CHARACTERISTICS					
Input Range (±3 dB Error)	From noise floor to maximum input		92		dB
Input Range (±1 dB Error)	From noise floor to maximum input		88		dB
Logarithmic Conformance	f ≤ 100 MHz, central 80 dB		±0.3	±1	dB
	f = 500 MHz, central 75 dB		±0.5		dB
Logarithmic Slope	Unadjusted[1]	23	25	27	mV/dB
vs. Temperature		23		27	mV/dB
Logarithmic Intercept	Sine amplitude, unadjusted[2]		20		μV
	Equivalent sine power in 50 Ω	−87	−84	−77	dBm
vs. Temperature		−88		−76	dBm
Input Noise Spectral Density	Inputs shorted		1.5		nV/√Hz
Operating Noise Floor	R_{SOURCE} = 50 Ω/2		−78		dBm
Output Resistance	Pin 4 to ground	10	12.5	15	kΩ
Internal Load Capacitance			3.5		pF
Response Time	Small signal, 10% to 90%, 0 mV to 100 mV, C_L = 2 pF		400		ns
	Large signal, 10% to 90%, 0 V to 2.4 V, C_L = 2 pF		500		ns
Upper Usable Frequency			500		MHz
Lower Usable Frequency	AC-coupled input		10		Hz
AMPLIFIER CELL CHARACTERISTICS					
Cell Bandwidth	−3 dB		900		MHz
Cell Gain			14.3		dB
INPUT CHARACTERISTICS					
DC Common-Mode Voltage	AC-coupled input		3.2		V
Common-Mode Range	Either input (small signal)	−0.3	+1.6	V_S − 1	V
DC Input Offset Voltage[3]	R_{SOURCE} ≤ 50 Ω		50	500	μV
	Drift		0.8		μV/°C
Incremental Input Resistance	Differential		1.1		kΩ
Input Capacitance	Either pin to ground		1.4		pF
Bias Current	Either input		10	25	μA
POWER INTERFACES					
Supply Voltage		2.7		5.5	V
Supply Current	V_{ENB} ≥ 2 V		8	10	mA
Disabled	V_{ENB} ≤ 1 V		150	750	μA

[1] This can be adjusted downward by adding a shunt resistor from the output to ground. A 50 kΩ resistor reduces the nominal slope to 20 mV/dB.
[2] This can be adjusted in either direction by a voltage applied to Pin 5, with a scale factor of 8 dB/V.
[3] Normally nulled automatically by internal offset correction loop and can be manually nulled by a voltage applied between Pin 3 and ground; see the Applications Information section.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
Supply	7.5 V
Input Voltage (Pin 1 and Pin 8)	V_{SUPPLY}
Storage Temperature Range (N, R)	−65°C to +125°C
Ambient Temperature Range, Rated Performance Industrial, AD8307AN, AD8307AR	−40°C to +85°C
Lead Temperature Range (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

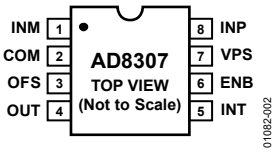


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INM	Signal Input Minus Polarity. Normally at $V_{POS}/2$.
2	COM	Common Pin (Usually Grounded).
3	OFS	Offset Adjustment. External capacitor connection.
4	OUT	Logarithmic (RSSI) Output Voltage. R_{OUT} = 12.5 kΩ.
5	INT	Intercept Adjustment, ±3 dB. (See the Slope and Intercept Adjustments section.)
6	ENB	CMOS-Compatible Chip Enable. Active when high.
7	VPS	Positive Supply: 2.7 V to 5.5 V.
8	INP	Signal Input Plus Polarity. Normally at $V_{POS}/2$. Due to the symmetrical nature of the response, there is no special significance to the sign of the two input pins. DC resistance from INP to INM = 1.1 kΩ.

TYPICAL PERFORMANCE CHARACTERISTICS

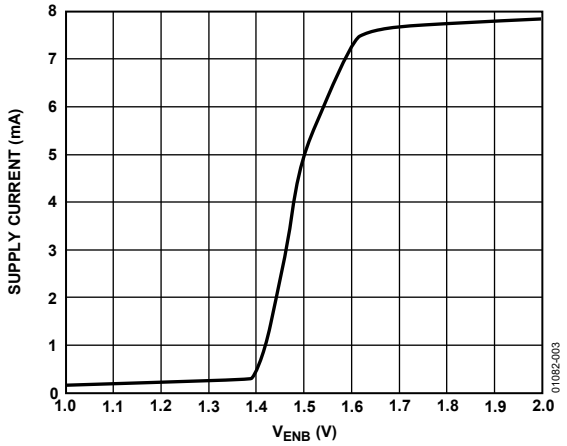


Figure 3. Supply Current vs. V_{ENB} (5 V)

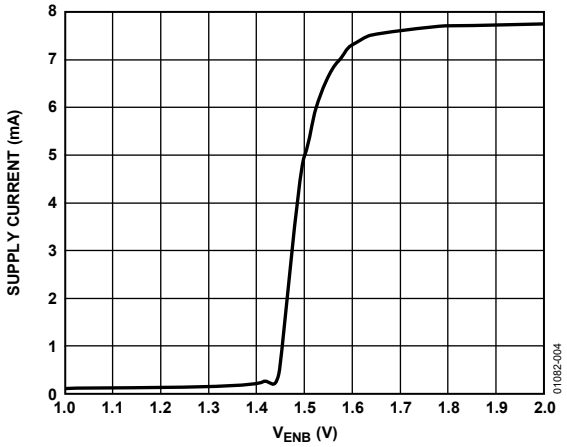


Figure 4. Supply Current vs. V_{ENB} (3 V)

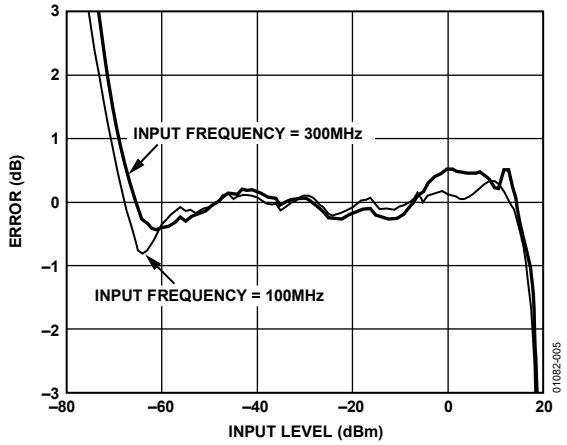


Figure 5. Log Conformance vs. Input Level (dBm), 100 MHz and 300 MHz

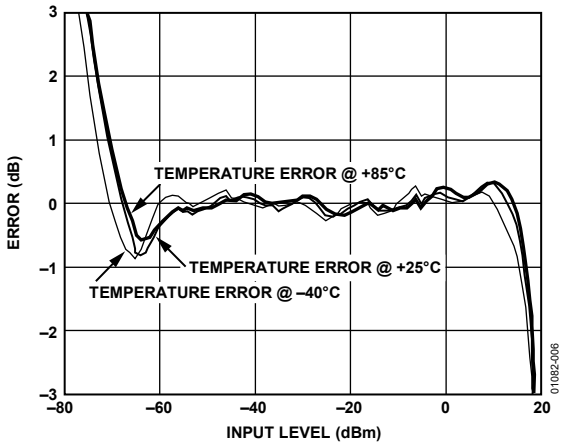


Figure 6. Log Conformance vs. Input Level (dBm) at –40°C, +25°C, and +85°C

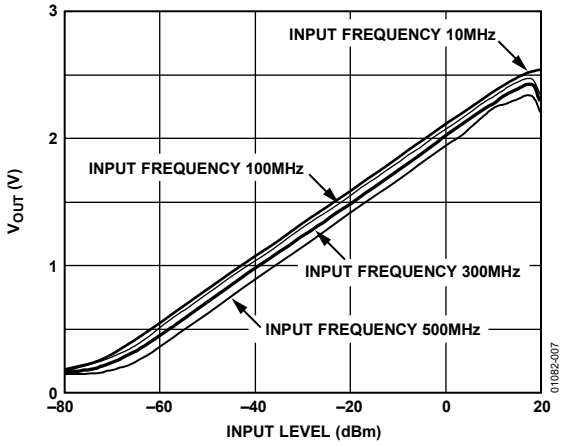


Figure 7. V_{OUT} vs. Input Level (dBm) at Various Frequencies

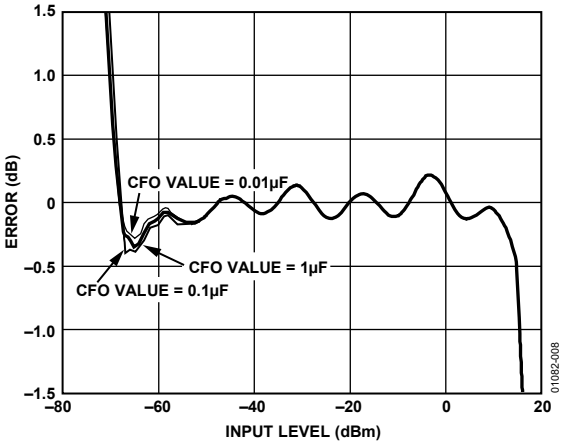


Figure 8. Log Conformance vs. CFO Values at 1 kHz Input Frequency

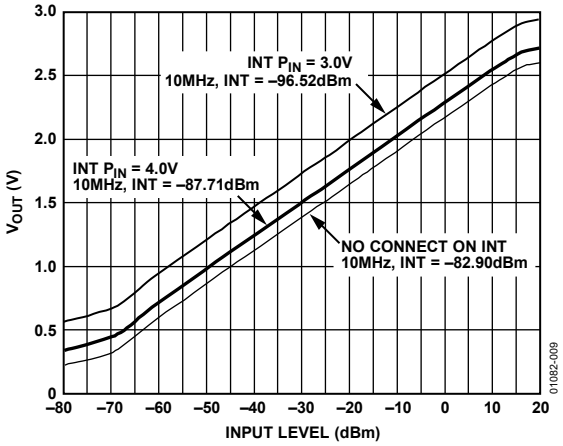


Figure 9. V_{OUT} vs. Input Level at 5 V Supply; Showing Intercept Adjustment

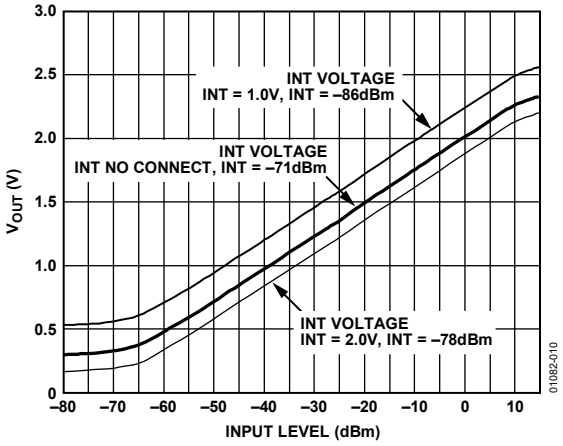


Figure 10. V_{OUT} vs. Input Level at 3 V Supply Using AD820 as Buffer, Gain = +2; Showing Intercept Adjustment

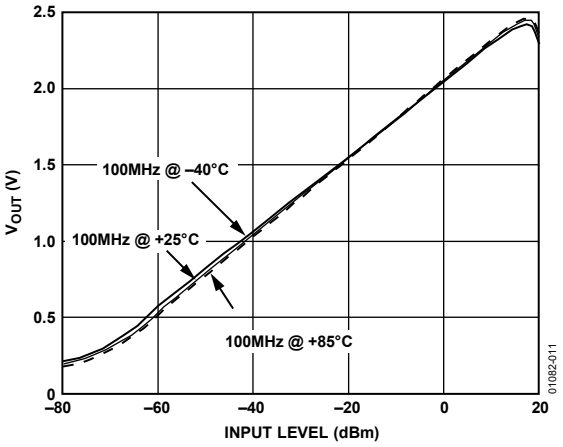


Figure 11. V_{OUT} vs. Input Level at Three Temperatures (−40°C, +25°C, +85°C)

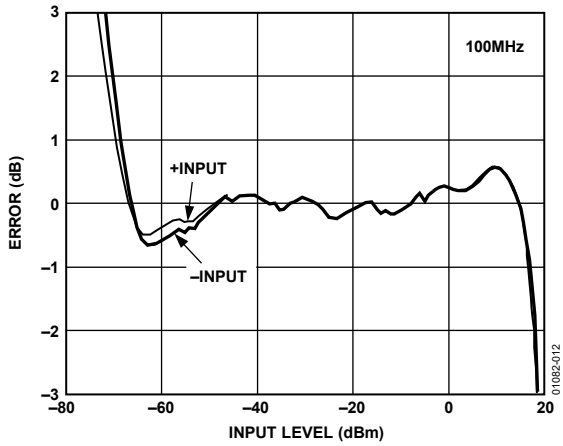


Figure 12. Log Conformance vs. Input Level at 100 MHz Showing Response to Alternative Inputs

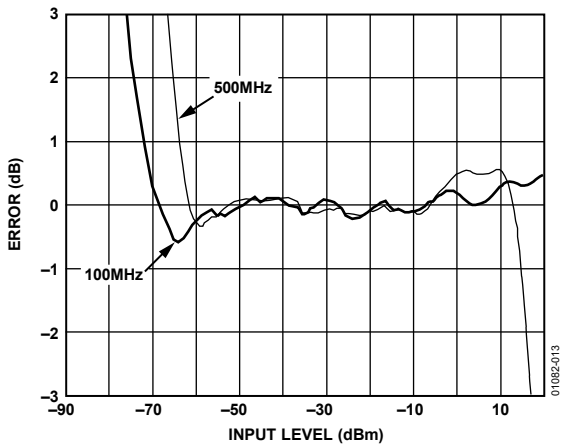


Figure 13. Log Conformance vs. Input Level at 100 MHz and 500 MHz; Input Driven Differentially Using Transformer

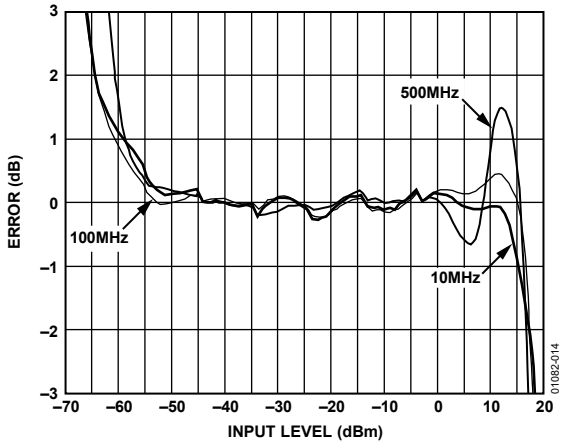


Figure 14. Log Conformance vs. Input Level at 3 V Supply Using AD820 as Buffer, Gain = +2

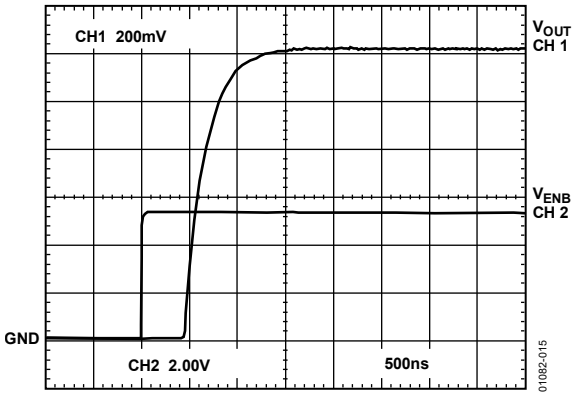


Figure 15. Power-Up Response Time

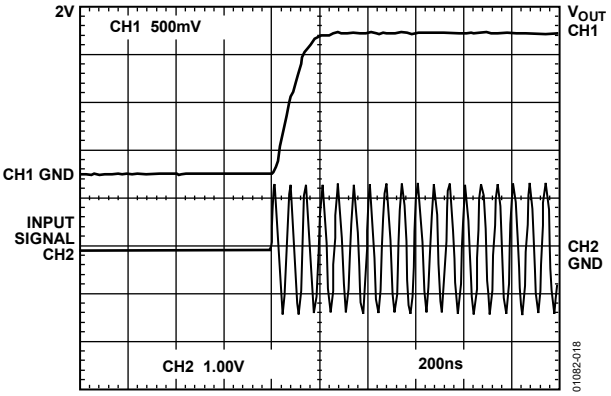


Figure 18. V_{OUT} Rise Time

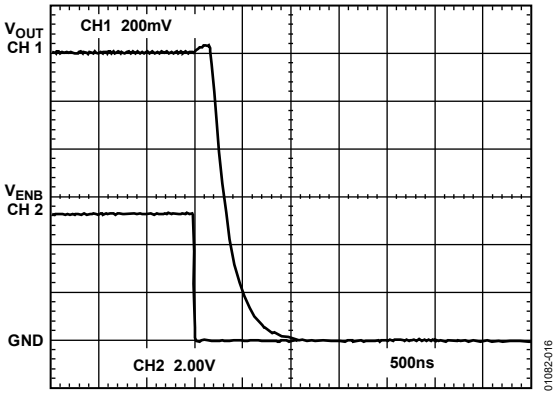


Figure 16. Power-Down Response Time

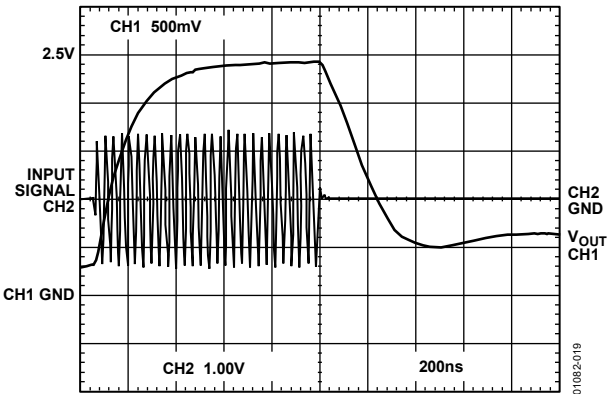


Figure 19. Large Signal Response Time

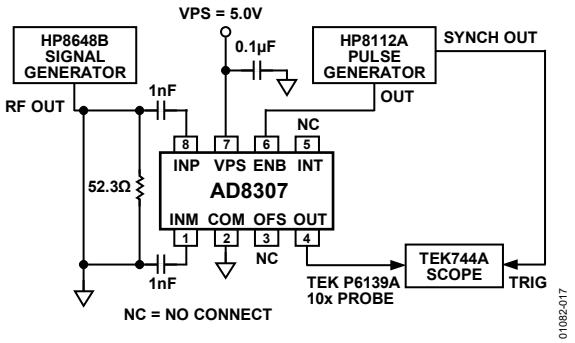


Figure 17. Test Setup for Power-Up/Power-Down Response Time

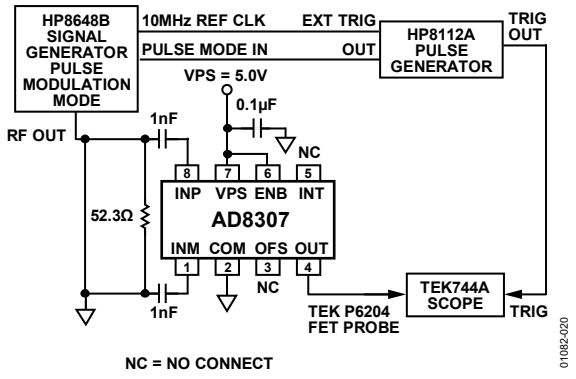


Figure 20. Test Setup for V_{OUT} Pulse Response

LOG AMP THEORY

Logarithmic amplifiers perform a more complex operation than that of classical linear amplifiers, and their circuitry is significantly different. A good grasp of what log amps do and how they work can prevent many pitfalls in their application. The essential purpose of a log amp is not to amplify, though amplification is utilized to achieve the function. Rather, it is to compress a signal of wide dynamic range to its decibel equivalent. It is thus a measurement device. A better term may be logarithmic converter, because its basic function is the conversion of a signal from one domain of representation to another via a precise nonlinear transformation.

Logarithmic compression leads to situations that can be confusing or paradoxical. For example, a voltage offset added to the output of a log amp is equivalent to a gain increase ahead of its input. In the usual case where all the variables are voltages, and regardless of the particular structure, the relationship between the variables can be expressed as

$$V_{OUT} = V_Y \log(V_{IN}/V_X) \quad (1)$$

where:
V_{OUT} is the output voltage.
V_Y is the slope voltage; the logarithm is usually taken to base 10 (in which case V_Y is also the volts per decade).
V_{IN} is the input voltage.
V_X is the intercept voltage.

All log amps implicitly require two references, in this example, V_X and V_Y, which determine the scaling of the circuit. The absolute accuracy of a log amp cannot be any better than the accuracy of its scaling references. Equation 1 is mathematically incomplete in representing the behavior of a demodulating log amp, such as the AD8307, where V_{IN} has an alternating sign. However, the basic principles are unaffected, and this can be safely used as the starting point in the analyses of log amp scaling.

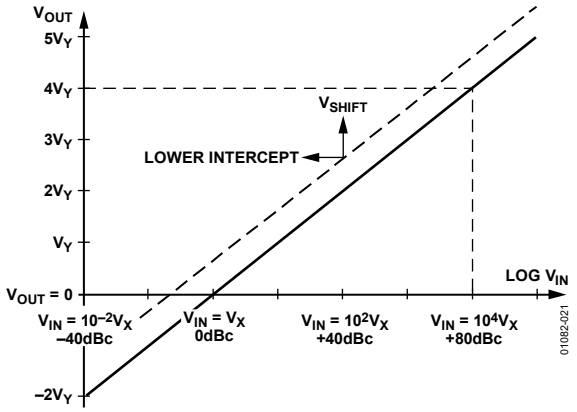


Figure 21. Ideal Log Amp Function

Figure 21 shows the input/output relationship of an ideal log amp, conforming to Equation 1. The horizontal scale is logarithmic and spans a wide dynamic range, shown in Figure 21 as over 120 dB, or six decades. The output passes through zero (the log intercept) at the unique value $V_{IN} = V_X$ and ideally becomes negative for inputs below the intercept. In the ideal case, the straight line describing V_{OUT} for all values of V_{IN} continues indefinitely in both directions. The dotted line shows that the effect of adding an offset voltage, V_{SHIFT}, to the output is to lower the effective intercept voltage, V_X. Exactly the same alteration can be achieved by raising the gain (or signal level) ahead of the log amp by the factor, V_{SHIFT}/V_Y. For example, if V_Y is 500 mV per decade (25 mV/dB), an offset of 150 mV added to the output appears to lower the intercept by two-tenths of a decade, or 6 dB. Adding an offset to the output is thus indistinguishable from applying an input level that is 6 dB higher.

The log amp function described by Equation 1 differs from that of a linear amplifier in that the incremental gain $\delta V_{OUT}/\delta V_{IN}$ is a very strong function of the instantaneous value of V_{IN}, as is apparent by calculating the derivative. For the case where the logarithmic base is δ,

$$\frac{\delta V_{OUT}}{\delta V_{IN}} = \frac{V_Y}{V_{IN}} \quad (2)$$

That is, the incremental gain is inversely proportional to the instantaneous value of the input voltage. This remains true for any logarithmic base, which is chosen as 10 for all decibel related purposes. It follows that a perfect log amp is required to have infinite gain under classical small signal (zero amplitude) conditions. Less ideally, this result indicates that whatever means are used to implement a log amp, accurate response under small signal conditions (that is, at the lower end of the dynamic range) demands the provision of a very high gain bandwidth product. A further consequence of this high gain is that in the absence of an input signal, even very small amounts of thermal noise at the input of a log amp cause a finite output for zero input. This results in the response line curving away from the ideal shown in Figure 21 toward a finite baseline, which can be either above or below the intercept. Note that the value given for this intercept can be an extrapolated value, in which case the output cannot cross zero, or even reach it, as is the case for the AD8307.

While Equation 1 is fundamentally correct, a simpler formula is appropriate for specifying the calibration attributes of a log amp like the AD8307, which demodulates a sine wave input.

$$V_{OUT} = V_{SLOPE}(P_{IN} - P_0) \quad (3)$$

where:
V_{OUT} is the demodulated and filtered baseband (video or RSSI) output.
V_{SLOPE} is the logarithmic slope, now expressed in V/dB (typically between 15 mV/dB and 30 mV/dB).
P_{IN} is the input power, expressed in decibels relative to some reference power level.
P_0 is the logarithmic intercept, expressed in decibels relative to the same reference level.

The most widely used reference in RF systems is decibels above 1 mW in 50 Ω, written dBm. Note that the quantity ($P_{IN} - P_0$) is

just dB. The logarithmic function disappears from the formula because the conversion has already been implicitly performed in stating the input in decibels. This is strictly a concession to popular convention; log amps manifestly do not respond to power (tacitly, power absorbed at the input), but rather to input voltage. The use of dBV (decibels with respect to 1 V rms) is more precise, though still incomplete, because waveform is involved as well. Because most users think about and specify RF signals in terms of power, more specifically, in dBm re: 50 Ω, this convention is used in specifying the performance of the AD8307.

PROGRESSIVE COMPRESSION

Most high speed, high dynamic range log amps use a cascade of nonlinear amplifier cells (see Figure 22) to generate the logarithmic function from a series of contiguous segments, a type of piecewise linear technique. This basic topology immediately opens up the possibility of enormous gain bandwidth products. For example, the AD8307 employs six cells in its main signal path, each having a small signal gain of 14.3 dB (×5.2) and a −3 dB bandwidth of about 900 MHz. The overall gain is about 20,000 (86 dB) and the overall bandwidth of the chain is some 500 MHz, resulting in the incredible gain bandwidth product (GBW) of 10,000 GHz, about a million times that of a typical op amp. This very high GBW is an essential prerequisite for accurate operation under small signal conditions and at high frequencies. In Equation 2, however, the incremental gain decreases rapidly as V_{IN} increases. The AD8307 continues to exhibit an essentially logarithmic response down to inputs as small as 50 µV at 500 MHz.

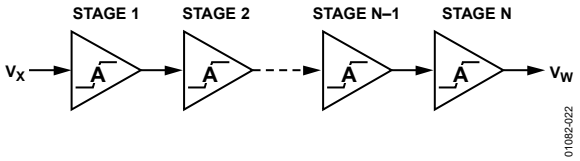


Figure 22. Cascade of Nonlinear Gain Cells

To develop the theory, first consider a scheme slightly different from that employed in the AD8307, but simpler to explain and mathematically more straightforward to analyze. This approach is based on a nonlinear amplifier unit, called an A/1 cell, with the transfer characteristic shown in Figure 23.

The local small signal gain $\delta V_{OUT}/\delta V_{IN}$ is A, maintained for all inputs up to the knee voltage E_K, above which the incremental gain drops to unity. The function is symmetrical: the same drop in gain occurs for instantaneous values of V_{IN} less than $-E_K$. The large signal gain has a value of A for inputs in the range $-E_K \le V_{IN} \le +E_K$, but falls asymptotically toward unity for very large inputs. In logarithmic amplifiers based on this amplifier function, both the slope voltage and the intercept voltage must be traceable to the one reference voltage, E_K. Therefore, in this fundamental analysis, the calibration accuracy of the log amp is dependent solely on this voltage. In practice, it is possible to separate the basic references used to determine V_Y and V_X and, in the case of the AD8307, V_Y is traceable to an on-chip band gap reference, whereas V_X is derived from the thermal voltage kT/q and is later temperature corrected.

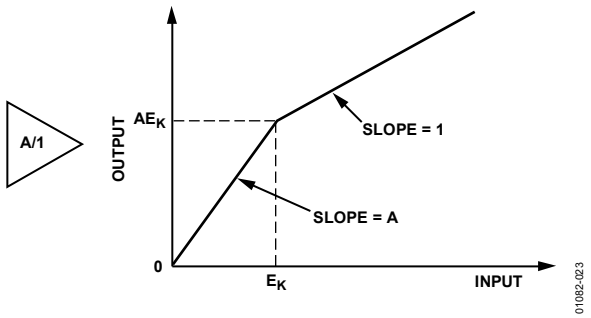


Figure 23. A/1 Amplifier Function

Let the input of an N-cell cascade be V_{IN}, and the final output be V_{OUT}. For small signals, the overall gain is simply A^N. A six-stage system in which A = 5 (14 dB) has an overall gain of 15,625 (84 dB). The importance of a very high small signal gain in implementing the logarithmic function has been noted; however, this parameter is only of incidental interest in the design of log amps.

From this point forward, rather than considering gain, analyze the overall nonlinear behavior of the cascade in response to a simple dc input, corresponding to the V_{IN} of Equation 1. For very small inputs, the output from the first cell is $V_1 = AV_{IN}$. The output from the second cell is $V_2 = A^2 V_{IN}$, and so on, up to $V_N = A^N V_{IN}$. At a certain value of V_{IN}, the input to the Nth cell, V_{N-1}, is exactly equal to the knee voltage E_K. Thus, $V_{OUT} = AE_K$ and because there are N − 1 cells of Gain A ahead of this node, calculate $V_{IN} = E_K/A^{N-1}$. This unique situation corresponds to the lin-log transition (labeled 1 in Figure 24). Below this input, the cascade of gain cells acts as a simple linear amplifier, whereas for higher values of V_{IN}, it enters into a series of segments that lie on a logarithmic approximation (dotted line).

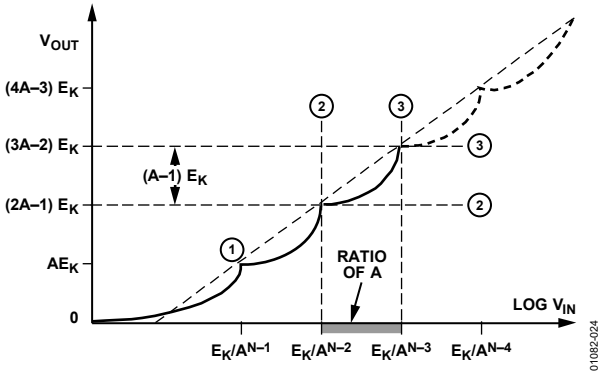


Figure 24. First Three Transitions

Continuing this analysis, the next transition occurs when the input to the N − 1 stage just reaches E_K, that is, when $V_{IN} = E_K/A^{N-2}$. The output of this stage is then exactly AE_K, and it is easily demonstrated (from the function shown in Figure 23) that the output of the final stage is $(2A - 1)E_K$ (labeled 2 in Figure 24). Thus, the output has changed by an amount $(A - 1)E_K$ for a change in V_{IN} from E_K/A^{N-1} to E_K/A^{N-2}, that is, a ratio change of A. At the next critical point (labeled 3 in Figure 24), the input is again A times larger and V_{OUT} has increased to $(3A - 2)E_K$, that is, by another linear increment of $(A - 1)E_K$.

Further analysis shows that right up to the point where the input to the first cell is above the knee voltage, V_{OUT} changes by $(A - 1)E_K$ for a ratio change of A in V_{IN}. This can be expressed as a certain fraction of a decade, which is simply $\log_{10}(A)$. For example, when A = 5, a transition in the piecewise linear output function occurs at regular intervals of 0.7 decade ($\log_{10}(A)$, or 14 dB divided by 20 dB). This insight immediately allows the user to write the volts per decade scaling parameter, which is also the scaling voltage, V_Y, when using base 10 logarithms, as

$$V_Y = \frac{Linear\ Change\ in\ V_{OUT}}{Decades\ Change\ in\ V_{IN}} = \frac{(A-1)E_K}{\log_{10}(A)} \quad (4)$$

Note that only two design parameters are involved in determining V_Y, namely, the cell gain A and the knee voltage, E_K, while N, the number of stages, is unimportant in setting the slope of the overall function. For A = 5 and E_K = 100 mV, the slope would be a rather awkward 572.3 mV per decade (28.6 mV/dB). A well designed log amp has rational scaling parameters.

The intercept voltage can be determined by using two pairs of transition points on the output function (consider Figure 24). The result is

$$V_X = \frac{E_K}{A^{(N+1/(A-1))}} \quad (5)$$

For the case under consideration, using N = 6, calculate V_Z = 4.28 µV. However, be careful about the interpretation of this parameter, because it was earlier defined as the input voltage at which the output passes through zero (see Figure 21). Clearly, in the absence of noise and offsets, the output of the amplifier chain shown in Figure 23 can be zero when, and only when, V_{IN} = 0. This anomaly is due to the finite gain of the cascaded amplifier, which results in a failure to maintain the logarithmic approximation below the lin-log transition (labeled 1 in Figure 24). Closer analysis shows that the voltage given by Equation 5 represents the extrapolated, rather than actual, intercept.

DEMODULATING LOG AMPS

Log amps based on a cascade of A/1 cells are useful in baseband applications because they do not demodulate their input signal. However, baseband and demodulating log amps alike can be made using a different type of amplifier stage, called an A/0 cell. Its function differs from that of the A/1 cell in that the gain above the knee voltage E_K falls to zero, as shown by the solid line in Figure 25. This is also known as the limiter function, and a chain of N such cells are often used to generate hard-limited output in recovering the signal in FM and PM modes.

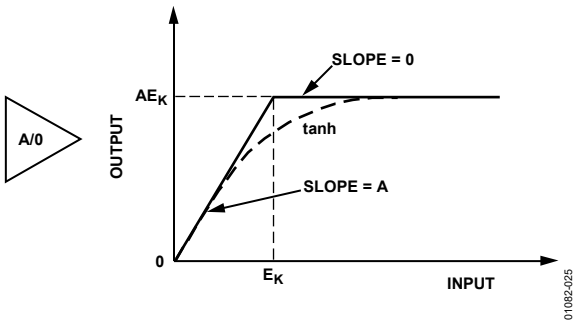


Figure 25. A/0 Amplifier Functions (Ideal and Tanh)

The AD640, AD606, AD608, AD8307, and various other Analog Devices, Inc., communications products incorporating a logarithmic intermediate frequency (IF) amplifier all use this technique. It becomes apparent that the output of the last stage can no longer provide the logarithmic output because this remains unchanged for all inputs above the limiting threshold, which occurs at $V_{IN} = E_K/A^{N-1}$. Instead, the logarithmic output is now generated by summing the outputs of all the stages. The full analysis for this type of log amp is only slightly more complicated than that of the previous case. It is readily shown that, for practical purposes, the intercept voltage, V_X, is identical to that given in Equation 5, while the slope voltage is

$$V_Y = \frac{AE_K}{\log_{10}(A)} \quad (6)$$

Preference for the A/0 style of log amp over one using A/1 cells stems from several considerations. The first is that an A/0 cell can be very simple. In the AD8307, it is based on a bipolar transistor differential pair, having resistive loads, R_L, and an emitter current source, I_E. This exhibits an equivalent knee voltage of E_K = 2 kT/q and a small signal gain of $A = I_E R_L/E_K$. The large signal transfer function is the hyperbolic tangent (see the dashed line in Figure 25). This function is very precise, and the deviation from an ideal A/0 form is not detrimental. In fact, the rounded shoulders of the tanh function result in a lower ripple in the logarithmic conformance than that obtained using an ideal A/0 function.

An amplifier composed of these cells is entirely differential in structure and can thus be rendered very insensitive to disturbances on the supply lines and, with careful design, to temperature variations. The output of each gain cell has an associated transconductance (g_m) cell that converts the differential output voltage of the cell to a pair of differential currents, which are summed simply by connecting the outputs of all the g_m (detector) stages in parallel. The total current is then converted back to a voltage by a transresistance stage to generate the logarithmic output. This scheme is depicted in single-sided form in Figure 26.

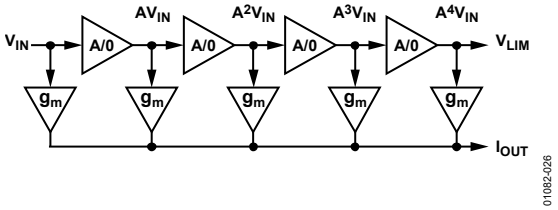


Figure 26. Log Amp Using A/0 Stages and Auxiliary Summing Cells

The chief advantage of this approach is that the slope voltage can now be decoupled from the knee voltage, $E_K = 2$ kT/q, which is inherently PTAT. By contrast, the simple summation of the cell outputs results in a very high temperature coefficient of the slope voltage given in Equation 6. To do this, the detector stages are biased with currents (not shown), which are rendered stable with temperature. These are derived either from the supply voltage (as in the AD606 and AD608) or from an internal band gap reference (as in the AD640 and AD8307). This topology affords complete control over the magnitude and temperature behavior of the logarithmic slope, decoupling it completely from E_K.

A further step is needed to achieve the demodulation response, required when the log amp converts an alternating input into a quasi-dc baseband output. This is achieved by altering the g_m cells used for summation purposes to also implement the rectification function. Early discrete log amps based on the progressive compression technique used half-wave rectifiers. This made postdetection filtering difficult. The AD640 was the first commercial monolithic log amp to use a full-wave rectifier, a practice followed in all subsequent Analog Devices types.

These detectors can be modeled as essentially linear g_m cells, but produce an output current independent of the sign of the voltage applied to the input of each cell; that is, they implement the absolute value function. Because the output from the later A/0 stages closely approximates an amplitude symmetric square wave for even moderate input levels (most stages of the amplifier chain operate in a limiting mode), the current output from each detector is almost constant over each period of the input. Somewhat earlier detector stages produce a waveform having only very brief dropouts, whereas the detectors nearest the input produce a low level, almost sinusoidal waveform at twice the input frequency. These aspects of the detector system result in a signal that is easily filtered, resulting in low residual ripple on the output.

INTERCEPT CALIBRATION

All monolithic log amps from Analog Devices include accurate means to position the intercept voltage, V_X (or equivalent power for a demodulating log amp). Using the scheme shown in Figure 26, the basic value of the intercept level departs considerably from that predicted by the simpler analyses given earlier. However, the intrinsic intercept voltage is still proportional to E_K, which is PTAT (see Equation 5). Recalling that the addition of an offset to the output produces an effect that is indistinguishable from a change in the position of the intercept, it is possible to cancel the left-right motion of V_X resulting from the temperature variation of E_K. Do this by adding an offset with the required temperature behavior.

The precise temperature shaping of the intercept positioning offset results in a log amp having stable scaling parameters, making it a true measurement device, for example, as a calibrated received signal strength indicator (RSSI). In this application, the user is more interested in the value of the output for an input waveform that is invariably sinusoidal. Although the input level can alternatively be stated as an equivalent power, in dBm, be sure to work carefully. It is essential to know the load impedance in which this power is presumed to be measured.

In radio frequency (RF) practice, it is generally safe to assume a reference impedance of 50 Ω in which 0 dBm (1 mW) corresponds to a sinusoidal amplitude of 316.2 mV (223.6 mV rms). The intercept can likewise be specified in dBm. For the AD8307, it is positioned at −84 dBm, corresponding to a sine amplitude of 20 μV. It is important to bear in mind that log amps do not respond to power, but to the voltage applied to their input.

The AD8307 presents a nominal input impedance much higher than 50 Ω (typically 1.1 kΩ low frequencies). A simple input matching network can considerably improve the sensitivity of this type of log amp. This increases the voltage applied to the input and thus alters the intercept. For a 50 Ω match, the voltage gain is 4.8 and the entire dynamic range moves down by 13.6 dB (see Figure 35). Note that the effective intercept is a function of waveform. For example, a square wave input reads 6 dB higher than a sine wave of the same amplitude and a Gaussian noise input 0.5 dB higher than a sine wave of the same rms value.

OFFSET CONTROL

In a monolithic log amp, direct coupling between the stages is used for several reasons. First, this avoids the use of coupling capacitors, which typically have a chip area equal to that of a basic gain cell, thus considerably increasing die size. Second, the capacitor values predetermine the lowest frequency at which the log amp can operate; for moderate values, this can be as high as 30 MHz, limiting the application range. Third, the parasitic (backplate) capacitance lowers the bandwidth of the cell, further limiting the applications.

However, the very high dc gain of a direct-coupled amplifier raises a practical issue. An offset voltage in the early stages of the chain is indistinguishable from a real signal. For example, if it were as high as 400 μV, it would be 18 dB larger than the smallest ac signal (50 μV), potentially reducing the dynamic range by this amount. This problem is averted by using a global feedback path from the last stage to the first, which corrects this offset in a similar fashion to the dc negative feedback applied around an op amp. The high frequency components of the signal must be removed to prevent a reduction of the HF gain in the forward path.

In the AD8307, this is achieved by an on-chip filter, providing sufficient suppression of HF feedback to allow operation above 1 MHz. To extend the range below this frequency, an external capacitor can be added. This permits the high-pass corner to be lowered to audio frequencies using a capacitor of modest value. Note that this capacitor has no effect on the minimum signal frequency for input levels above the offset voltage; this extends down to dc (for a signal applied directly to the input pins). The offset voltage varies from part to part; some exhibit essentially stable offsets of under 100 μV without the benefit of an offset adjustment.

EXTENSION OF RANGE

The theoretical dynamic range for the basic log amp shown in Figure 26 is A^N. For A = 5.2 (14.3 dB) and N = 6, it is 20,000 or 86 dB. The actual lower end of the dynamic range is largely determined by the thermal noise floor, measured at the input of the chain of amplifiers. The upper end of the range is extended upward by the addition of top-end detectors. The input signal is applied to a tapped attenuator, and progressively smaller signals are applied to three passive rectifying g_m cells whose outputs are summed with those of the main detectors. With care in design, the extension to the dynamic range can be seamless over the full frequency range. For the AD8307, it amounts to a further 27 dB.

Therefore, the total dynamic range is theoretically 113 dB. The specified range of 90 dB (−74 dBm to +16 dBm) is for high accuracy and calibrated operation, and includes the low end degradation due to thermal noise and the top end reduction due to voltage limitations. The additional stages are not redundant, but are needed to maintain accurate logarithmic conformance over the central region of the dynamic range, and in extending the usable range considerably beyond the specified range. In applications where log conformance is less demanding, the AD8307 can provide over 95 dB of range.

INTERFACES

The AD8307 comprises six main amplifier/limiter stages, each having a gain of 14.3 dB and small signal bandwidth of 900 MHz; the overall gain is 86 dB with a −3 dB bandwidth of 500 MHz. These six cells and their associated g_m styled full-wave detectors handle the lower two-thirds of the dynamic range. Three top-end detectors, placed at 14.3 dB taps on a passive attenuator, handle the upper third of the 90 dB range. Biasing for these cells is provided by two references: one determines their gain and the other is a band gap circuit that determines the logarithmic slope and stabilizes it against supply and temperature variations. The AD8307 can be enabled or disabled by a CMOS-compatible level at ENB (Pin 6). The first amplifier stage provides a low voltage noise spectral density (1.5 nV/√Hz).

The differential current-mode outputs of the nine detectors are summed and then converted to single-sided form in the output stage, nominally scaled 2 µA/dB. The logarithmic output voltage is developed by applying this current to an on-chip 12.5 kΩ resistor, resulting in a logarithmic slope of 25 mV/dB (that is, 500 mV/decade) at the OUT pin. This voltage is not buffered, allowing the use of a variety of special output interfaces, including the addition of postdemodulation filtering. The last detector stage includes a modification to temperature stabilize the log intercept, which is accurately positioned to make optimal use of the full output voltage range available. The intercept can be adjusted using the INT pin, which adds or subtracts a small current to the signal current.

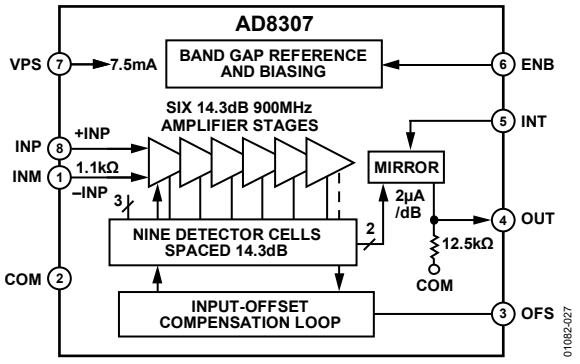


Figure 27. Main Features of the AD8307

The last gain stage also includes an offset sensing cell. This generates a bipolarity output current when the main signal path has an imbalance due to accumulated dc offsets. This current is integrated by an on-chip capacitor, which can be increased in value by an off-chip component at OFS. The resulting voltage is used to null the offset at the output of the first stage. Because it does not involve the signal input connections, whose ac-coupling capacitors otherwise introduce a second pole in the feedback path, the stability of the offset correction loop is assured.

The AD8307 is built on an advanced, dielectrically isolated, complementary bipolar process. Most resistors are thin film types having a low temperature coefficient of resistance (TCR) and high linearity under large signal conditions. Their absolute tolerance is typically within ±20%. Similarly, the capacitors have a typical tolerance of ±15% and essentially zero temperature or voltage sensitivity. Most interfaces have additional small junction capacitances associated with them due to active devices or ESD protection; these can be neither accurate nor stable. Component numbering in each of these interface diagrams is local.

ENABLE INTERFACE

The chip enable interface is shown in Figure 28. The currents in the diode-connected transistors control the turn-on and turn-off states of the band gap reference and the bias generator, and are a maximum of 100 µA when Pin 6 is taken to 5 V, under worst-case conditions. Left unconnected, or at a voltage below 1 V, the AD8307 is disabled and consumes a sleep current of under 50 µA; tied to the supply, or at a voltage above 2 V, it is fully enabled. The internal bias circuitry is very fast, typically <100 ns for either off or on. In practice, the latency period before the log amp exhibits its full dynamic range is more likely to be limited by factors relating to the use of ac coupling at the input or the settling of the offset control loop.

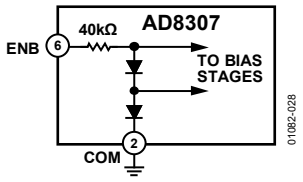


Figure 28. Enable Interface

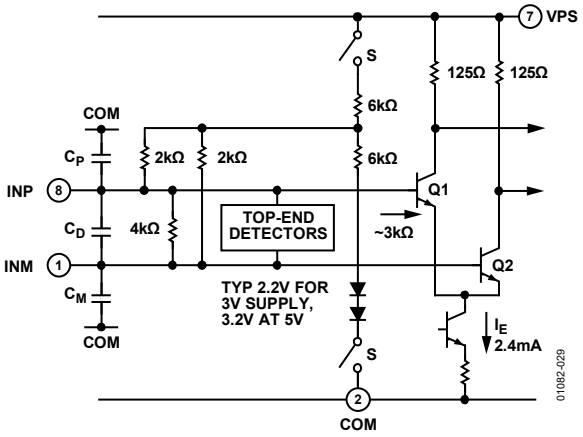


Figure 29. Signal Input Interface

INPUT INTERFACE

Figure 29 shows the essentials of the signal input interface. C_P and C_M are the parasitic capacitances to ground; C_D is the differential input capacitance, mostly due to Q1 and Q2. In most applications, both input pins are ac-coupled. The switches close when ENB is asserted. When disabled, the inputs float, bias current I_E is shut off, and the coupling capacitors remain charged. If the log amp is disabled for long periods, small leakage currents discharge these capacitors. If they are poorly matched, charging currents at power-up can generate a transient input

voltage that can block the lower reaches of the dynamic range until it has become much less than the signal.

In most applications, the signal is single sided and can be applied to either Pin 1 or Pin 8, with the other pin ac-coupled to ground. Under these conditions, the largest input signal that can be handled by the AD8307 is 10 dBm (sine amplitude of ±1 V) when operating from a 3 V supply; 16 dBm can be handled using a 5 V supply. The full 16 dBm can be achieved for supplies down to 2.7 V, using a fully balanced drive. For frequencies above about 10 MHz, this is most easily achieved using a matching network. Using such a network, having an inductor at the input, the input transient is eliminated. Occasionally, it is desirable to use the dc-coupled potential of the AD8307. The main challenge is to present signals to the log amp at the elevated common-mode input level, requiring the use of low noise, low offset buffer amplifiers. Using dual supplies of ±3 V, the input pins can operate at ground potential.

OFFSET INTERFACE

The input-referred dc offsets in the signal path are nulled via the interface associated with Pin 3, shown in Figure 30. Q1 and Q2 are the first stage input transistors, with their corresponding load resistors (125 Ω). Q3 and Q4 generate small currents, which can introduce a dc offset into the signal path. When the voltage on OFS is at about 1.5 V, these currents are equal and nominally 64 µA. When OFS is taken to ground, Q4 is off and the effect of the current in Q3 is to generate an offset voltage of 64 µV × 125 Ω = 8 mV. Because the first stage gain is ×5, this is equivalent to an input offset (INP to INM) of 1.6 mV. When OFS is taken to its most positive value, the input-referred offset is reversed to −1.6 mV. If true dc coupling is needed, down to very small inputs, this automatic loop must be disabled and the residual offset eliminated using a manual adjustment.

In normal operation, however, using an ac-coupled input signal, the OFS pin should be left open. Any residual input offset voltage is then automatically nulled by the action of the feedback loop. The g_m cell, which is gated off when the chip is disabled, converts any output offset (sensed at a point near the end of the cascade of amplifiers) to a current. This is integrated by the on-chip capacitor, C_{HP}, and any added external capacitance, C_{OFS}, to generate an error voltage, which is applied back to the input stage in the polarity needed to null the output offset. From a small signal perspective, this feedback alters the response of the amplifier, which, rather than behaving as a fully dc-coupled system, now exhibits a zero in its ac transfer function, resulting in a closed-loop high-pass corner at about 1.5 MHz.

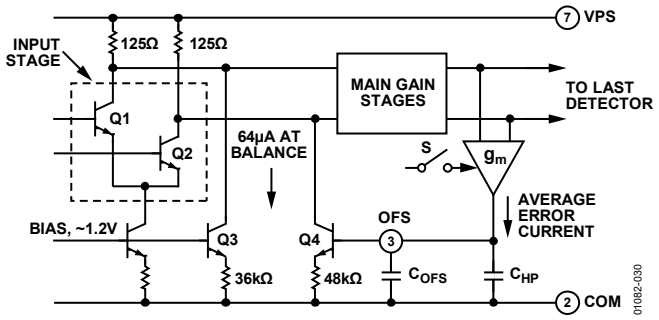


Figure 30. Offset Interface and Offset Nulling Path

The offset feedback is limited to a range of ±1.6 mV; signals larger than this override the offset control loop, which only affects performance for very small inputs. An external capacitor reduces the high-pass corner to arbitrarily low frequencies; using 1 µF, this corner is below 10 Hz. All Analog Devices log amps use an offset nulling loop; the AD8307 differs in using this single-sided form.

OUTPUT INTERFACE

The outputs from the nine detectors are differential currents, having an average value that is dependent on the signal input level, plus a fluctuation at twice the input frequency. The currents are summed at the LGP node and the LGM node in Figure 31. Further currents are added at these nodes, to position the intercept, by slightly raising the output for zero input, and to provide temperature compensation. Because the AD8307 is not laser trimmed, there is a small uncertainty in both the log slope and the log intercept. These scaling parameters can be adjusted.

For zero signal conditions, all the detector output currents are equal. For a finite input of either polarity, their difference is converted by the output interface to a single-sided unipolar current nominally scaled 2 µA/dB (40 µA/decade) at the OUT pin. An on-chip 12.5 kΩ resistor, R1, converts this current to a voltage of 25 mV/dB. C1 and C2 are effectively in shunt with R1 and form a low-pass filter pole with a corner frequency of about 5 MHz. The pulse response settles to within 1% of the final value within 300 ns. This integral low-pass filter provides adequate smoothing in many IF applications. At 10.7 MHz, the 2f ripple is 12.5 mV in amplitude, equivalent to ±0.5 dB, and only 0.5 mV (±0.02 dB) at f = 50 MHz. A filter capacitor, C_{FLT}, added from the OUT pin to ground lowers this corner frequency. Using 1 µF, the ripple is maintained to less than ±0.5 dB down to input frequencies of 100 Hz. Note that C_{OFS} should also be increased in low frequency applications, and is typically made equal to C_{FLT}.

It can be desirable to increase the speed of the output response, with the penalty of increased ripple. One way to do this is by connecting a shunt load resistor from the OUT pin to ground, which raises the low-pass corner frequency. This also alters the logarithmic slope, for example, to 7.5 mV/dB using a 5.36 kΩ resistor, while reducing the 10% to 90% rise time to 25 ns. The ripple amplitude for the 50 MHz input remains at 0.5 mV, but this is now equivalent to ±0.07 dB. If a negative supply is available, the output pin can be connected directly to the summing node of an external op amp connected as an inverting mode transresistance stage.

Note that while the AD8307 can operate down to supply voltages of 2.7 V, the output voltage limit is reduced when the supply drops below 4 V. This characteristic is the result of necessary headroom requirements, approximately two V_{BE} drops, in the design of the output stage.

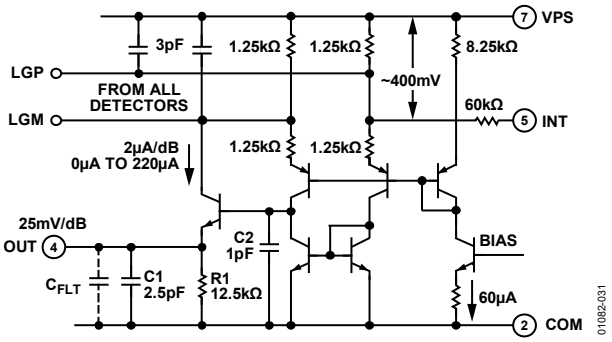


Figure 31. Simplified Output Interface

THEORY OF OPERATION

The AD8307 has very high gain and a bandwidth from dc to over 1 GHz, at which frequency the gain of the main path is still over 60 dB. Consequently, it is susceptible to all signals within this very broad frequency range that find their way to the input terminals. It is important to remember that these are indistinguishable from the wanted signal, and has the effect of raising the apparent noise floor (that is, lowering the useful dynamic range). For example, while the signal of interest can be an IF of 50 MHz, any of the following could easily be larger than the IF signal at the lower extremities of its dynamic range: 60 Hz hum (picked up due to poor grounding techniques), spurious coupling (from a digital clock source on the same PC board), and local radio stations, for example.

Careful shielding is essential. A ground plane should be used to provide a low impedance connection to the common pin, COM, for the decoupling capacitors used at VPS, and as the output ground. It is inadvisable to assume that the ground plane is equipotential. Neither of the inputs should be ac-coupled directly to the ground plane, but should be kept separate from it, being returned instead to the low associated with the source. This can mean isolating the low side of an input connector with a small resistance to the ground plane.

BASIC CONNECTIONS

Figure 32 shows the simple connections suitable for many applications. The inputs are ac coupled by C1 and C2, which should have the same value, for example, C_C. The coupling time constant is R_{IN} $C_C/2$, thus forming a high-pass corner with a 3 dB attenuation at $f_{HP} = 1/(pR_{IN}C_C)$. In high frequency applications, f_{HP} should be as large as possible to minimize the coupling of unwanted low frequency signals. Conversely, in low frequency applications, a simple RC network forming a low-pass filter should be added at the input for the same reason. For the case where the generator is not terminated, the signal range should be expressed in terms of the voltage response and should extend from −85 dBV to +6 dBV.

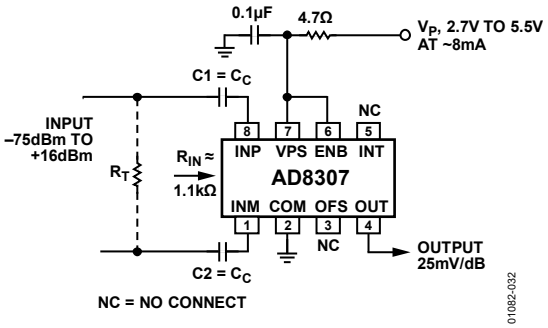


Figure 32. Basic Connections

Where it is necessary to terminate the source at a low impedance, the resistor R_T should be added, with allowance for the shunting effect of the basic 1.1 kΩ input resistance (R_{IN}) of the AD8307. For example, to terminate a 50 Ω source, a 52.3 Ω 1% tolerance resistor should be used. This can be placed on the input side or the log amp side of the coupling capacitors; in the former case, smaller capacitors can be used for a given frequency range; in the latter case, the effective R_{IN} is lowered directly at the log amp inputs.

Figure 33 shows the output vs. the input level, in dBm, when driven from a terminated 50 Ω generator, for sine inputs at 10 MHz, 100 MHz, and 500 MHz; Figure 34 shows the typical logarithmic conformance under the same conditions. Note that 10 dBm corresponds to a sine amplitude of 1 V, equivalent to an rms power of 10 mW in a 50 Ω termination. However, if the termination resistor is omitted, the input power is negligible. The use of dBm to define input level therefore needs to be considered carefully in connection with the AD8307.

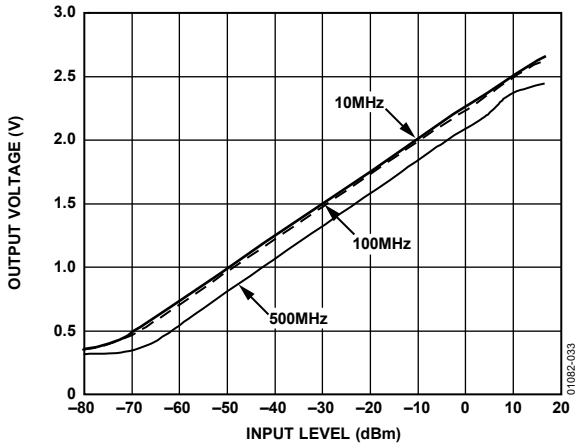


Figure 33. Log Response at 10 MHz, 100 MHz, and 500 MHz

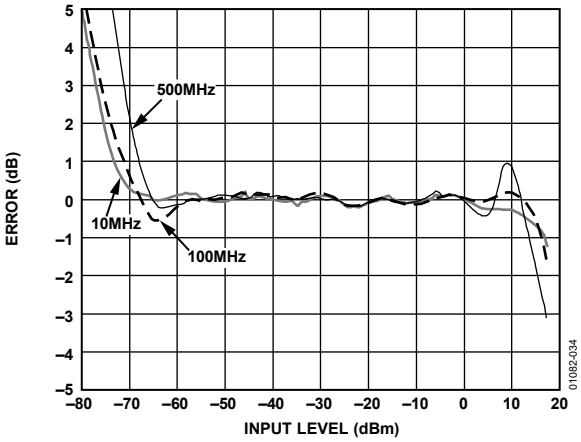


Figure 34. Logarithmic Law Conformance at 10 MHz, 100 MHz, and 500 MHz

INPUT MATCHING

Where higher sensitivity is required, an input matching network is valuable. Using a transformer to achieve the impedance transformation also eliminates the need for coupling capacitors, which lowers the offset voltage generated directly at the input, and balances the drives to the INP pin and the INM pin. The choice of turns ratio depends somewhat on the frequency. At frequencies below 50 MHz, the reactance of the input capacitance is much higher than the real part of the input impedance. In this frequency range, a turns ratio of about 1:4.8 lowers the input impedance to 50 Ω while raising the input voltage, thus lowering the effect of the short-circuit noise voltage by the same factor. There is a small contribution from the input noise current, so the total noise is reduced by a lesser factor. The intercept is also lowered by the turns ratio; for a 50 Ω match, it is reduced by 20 $\log_{10}$ (4.8) or 13.6 dB.

NARROW-BAND MATCHING

Transformer coupling is useful in broadband applications. However, a magnetically coupled transformer may not be convenient in some situations. At high frequencies, it is often preferable to use a narrow-band matching network, as shown in Figure 35.

Using a narrow-band matching network has several advantages. The same voltage gain is achieved, providing increased sensitivity, but a measure of selectivity is also introduced. The component count is low: two capacitors and an inexpensive chip inductor. Further, by making these capacitors unequal, the amplitudes at the INP pin and the INM pin can be equalized when driving from a single-sided source, that is, the network also serves as a balun.

Figure 36 shows the response for a center frequency of 100 MHz. Note the very high attenuation at low frequencies. The high frequency attenuation is due to the input capacitance of the log amp.

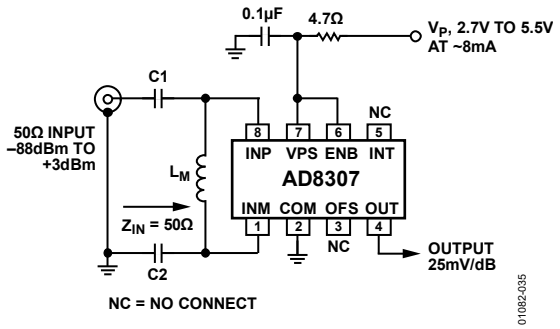


Figure 35. High Frequency Input Matching Network

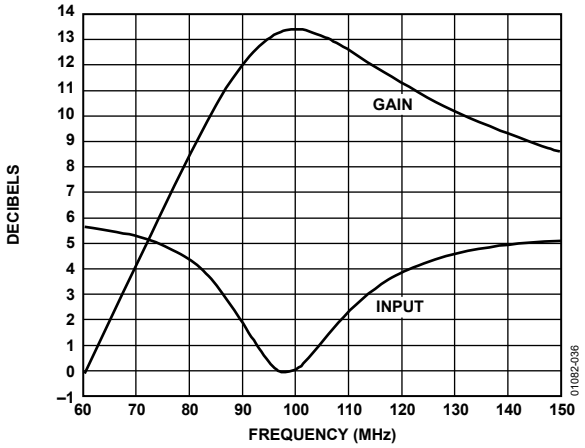


Figure 36. Response of 100 MHz Matching Network

Table 5 provides solutions for a variety of center frequencies (f_C) and matching impedances (Z_{IN}) of nominally 50 Ω and 100 Ω. The unequal capacitor values were chosen to provide a well-balanced differential drive and to allow better centering of the frequency response peak when using standard value components, which generally results in a Z_{IN} that is not exact. The full AD8307 HF input impedance and the inductor losses are included in the modeling.

Table 5. Narrow-Band Matching Values

f_C (MHz)	Z_{IN} (Ω)	C1 (pF)	C2 (pF)	L_M (nH)	Voltage Gain (dB)
10	45	160	150	3300	13.3
20	44	82	75	1600	13.4
50	46	30	27	680	13.4
100	50	15	13	330	13.4
150	57	10	8.2	220	13.2
200	57	7.5	6.8	150	12.8
250	50	6.2	5.6	100	12.3
500	54	3.9	3.3	39	10.9
10	103	100	91	5600	10.4
20	102	51	43	2700	10.4
50	99	22	18	1000	10.6
100	98	11	9.1	430	10.5
150	101	7.5	6.2	260	10.3
200	95	5.6	4.7	180	10.3
250	92	4.3	3.9	130	9.9
500	114	2.2	2.0	47	6.8

SLOPE AND INTERCEPT ADJUSTMENTS

Where higher calibration accuracy is needed, the adjustments shown in Figure 37 can be used, either singly or in combination. The log slope is lowered to 20 mV/dB by shunting the nominally 12.5 kΩ on-chip load resistor (see Figure 31) with 50 kΩ, adjusted by VR1. The calibration range is ±10% (18 mV/dB to 22 mV/dB), including full allowance for the variability in the value of the internal load. The adjustment can be made by alternately applying two input levels, provided by an accurate signal generator, spaced over the central portion of the log amp's dynamic range, for example, −60 dBm and 0 dBm. An AM modulated signal at the center of the dynamic range can also be used. For a modulation depth, M, expressed as a fraction, the decibel range between the peaks and troughs over one cycle of the modulation period is given by

$$\Delta dB = 20\log_{10}\frac{1+M}{1-M} \quad (7)$$

For example, using an rms signal level of −40 dBm with a 70% modulation depth (M = 0.7), the decibel range is 15 dB, as the signal varies from −47.5 dBm to −32.5 dBm.

The log intercept is adjustable over a ±3 dB range, which is sufficient to absorb the worst-case intercept error in the AD8307, plus some system level errors. For greater range, set R_S to zero. VR2 is adjusted while applying an accurately known CW signal near the lower end of the dynamic range to minimize the effect of any residual uncertainty in the slope. For example, to position the intercept to −80 dBm, a test level of −65 dBm can be applied and VR2 adjusted to produce a dc output of 15 dB above zero at 25 mV/dB, which is 0.3 V.

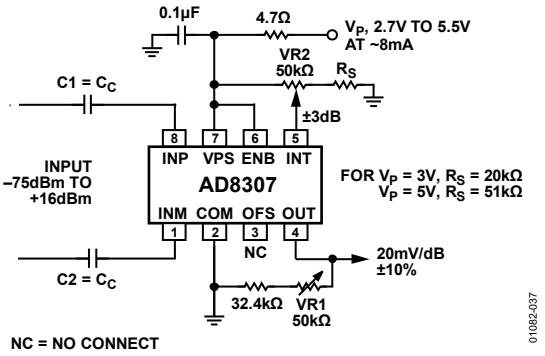


Figure 37. Slope and Intercept Adjustments

APPLICATIONS INFORMATION

The AD8307 is a highly versatile and easily applied log amp requiring very few external components. Most applications of this device can be accommodated using the simple connections shown in the preceding section.

BUFFERED OUTPUT

The output can be buffered and the slope optionally increased by using an op amp. If the single-supply capability is to be preserved, a suitable component is the AD8031. Like the AD8307, it is capable of operating from a 2.7 V supply and features a rail-to-rail output capability; it is available in a 5-lead version and in dual form as the 8-lead AD8032. Figure 38 shows how the slope can be increased to 50 mV/dB (1 V per decade), requiring a 5 V supply (90 dB times 50 mV is a 4.5 V swing). VR1 provides a ±10% slope adjustment; VR2 provides a ±3 dB intercept range. With R2 = 4.99 kΩ, the slope is adjustable to 25 mV/dB, allowing the use of a 2.7 V supply. Setting R2 to 80.6 kΩ, it is raised to 100 mV/dB, providing direct reading in decibels on a digital voltmeter. Because a 90 dB range now corresponds to a 9 V swing, a supply of at least this amount is needed for the op amp.

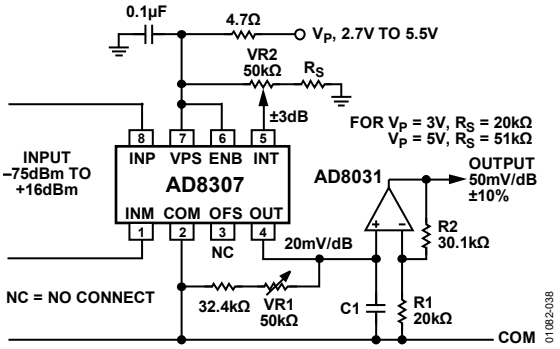


Figure 38. Log Amp with Buffered Output

C1 is optional; it lowers the corner frequency of the low-pass output filter. A value of 0.1 µF should be used for applications in which the output is measured on a voltmeter or other low speed device. On the other hand, when C1 is omitted, the 10% to 90% response time is under 200 ns and is typically 300 ns to 99% of the final value. To achieve faster response times, it is necessary to lower the load resistance at the output of the AD8307, then restore the scale using a higher gain in the op amp. Using 8.33 kΩ, the basic slope is 10 mV/dB; this can be restored to 25 mV/dB using a buffer gain of 2.5. The overall 10% to 90% response time is under 100 ns. Figure 39 shows how the output current capability can be augmented to drive a 50 Ω load; R_T optionally provides reverse termination, which halves the slope to 12.5 mV/dB.

FOUR-POLE FILTER

In low frequency applications, for example, audio down to 20 Hz, it is useful to employ the buffer amplifier as a multipole low-pass filter to achieve low output ripple while maintaining a rapid response time to changes in signal level.

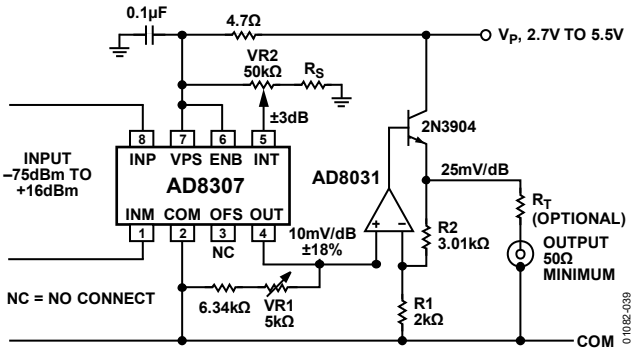


Figure 39. Cable Driving Log Amp

In Figure 40, the capacitor values are chosen for operation in the audio field, providing a corner frequency of 10 Hz, an attenuation of 80 dB/decade above this frequency, and a 1% settling time of 150 ms (0.1% in 175 ms). The residual ripple is 4 mV (±0.02 dB) when the input to the AD8307 is at 20 Hz. This filter can easily be adapted to other frequencies by proportional scaling of C5 to C7 (for example, for 100 kHz use 100 pF). Placed ahead of a digital multimeter, the convenient slope scaling of 100 mV/dB requires only a repositioning of the decimal point to read directly in decibels. The supply voltage for the filter must be large enough to support the dynamic range; a minimum of 9 V is needed for most applications; 12 V is recommended.

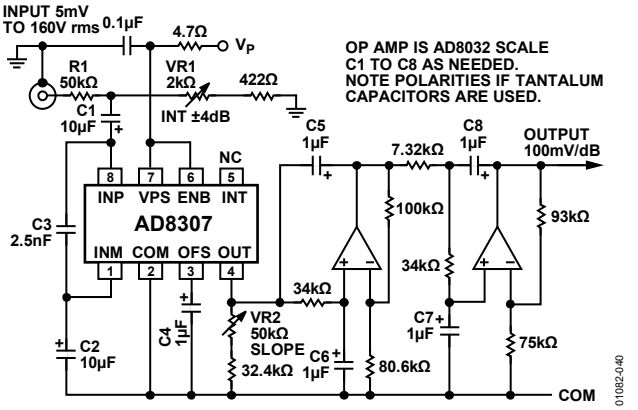


Figure 40. Log Amp with Four-Pole Low-Pass Filter

Figure 40 also shows the use of an input attenuator that can optionally be employed to produce a useful wide range ac voltmeter with direct decibel scaling. The basic range of –73 dBm to +17 dBm (that is, 50 µV rms to 1.6 V rms, for sine excitations) is shifted for illustrative purposes to 5 mV to 160 V rms (at which point the power in R1 is 512 mW). Because the basic input resistance of the AD8307 is not precise, VR1 is used to center the signal range at its input, doubling as a ±4 dB intercept adjustment. The low frequency response extends to 15 Hz; a higher corner frequency can be selected as needed by scaling C1 and C2. The shunt capacitor, C3, is used to lower the high frequency bandwidth to about 100 kHz, and thus lower the susceptibility to spurious signals. Other values should be chosen as needed for the coupling and filter capacitors.

1 µW TO 1 kW 50 Ω POWER METER

The front-end adaptation shown in Figure 41 provides the measurement of power being delivered from a transmitter final amplifier to an antenna. The range has been set to cover the power range −30 dBm (7.07 mV rms, or 1 µW) to +60 dBm (223 V rms, or 1 kW). A nominal voltage attenuation ratio of 158:1 (44 dB) is used; thus the intercept is moved from −84 dBm to −40 dBm and the AD8307, scaled 0.25 V/decade of power, now reads 1.5 V for a power level of 100 mW, 2.0 V at 10 W, and 2.5 V at 1 kW. The general expression is

$$P\,(\text{dBm}) = 40\,(V_{OUT} - 1)$$

The required attenuation can be implemented using a capacitive divider, providing a very low input capacitance, but it is difficult to ensure accurate values of small capacitors. A better approach is to use a resistive divider, taking the required precautions to minimize spurious coupling into the AD8307 by placing it in a shielded box with the input resistor passing through a hole in this box, as indicated in Figure 41. The coupling capacitors shown in Figure 41 are suitable for f ≥ 10 MHz. A capacitor can be added across the input pins of the AD8307 to reduce the response to spurious HF signals, which, as previously noted, extends to over 1 GHz.

The mismatch caused by the loading of this resistor is trivial; only 0.05% of the power delivered to the load is absorbed by the measurement system, a maximum of 500 mW at 1 kW. The postdemodulation filtering and slope calibration arrangements are chosen from other applications described in this data sheet to meet the particular system requirements. The 1 nF capacitor lowers the risk of HF signals entering the AD8307 via the load.

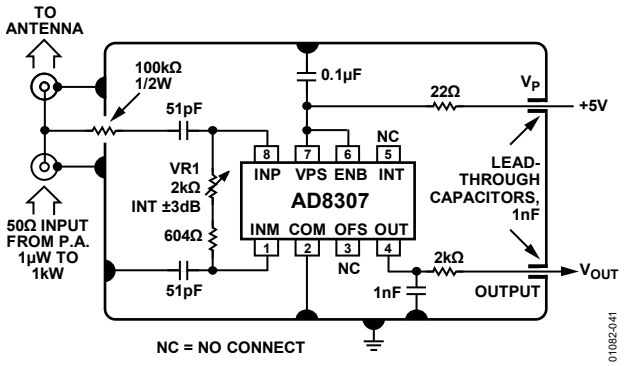


Figure 41. 1 µW to 1 kW, 50 Ω Power Meter

MEASUREMENT SYSTEM WITH 120 dB DYNAMIC RANGE

The dynamic range of the AD8307 can be extended further from 90 dB to over 120 dB by the addition of an X-AMP® such as the AD603. This type of variable gain amplifier exhibits a very exact exponential gain control characteristic, which is another way of stating that the gain varies by a constant number of decibels for a given change in the control voltage. For the AD603, this scaling factor is 40 dB/V, or 25 mV/dB. It is apparent that this property of a linear-in-dB response is characteristic of log amps; indeed, the AD8307 exhibits the same scaling factor.

The AD603 has a very low input-referred noise: 1.3 nV/√Hz at its 100 Ω input, or 0.9 nV/√Hz when matched to 50 Ω, equivalent to 0.4 µV rms, or −115 dBm, in a 200 kHz bandwidth. It is also capable of handling inputs in excess of 1.4 V rms, or +16 dBm. It is thus able to cope with a dynamic range of over 130 dB in this particular bandwidth.

If the gain control voltage for the X-AMP is derived from the output of the AD8307, the effect is to raise the gain of this front-end stage when the signal is small and lower it when it is large, but without altering the fundamental logarithmic nature of the response. This gain range is 40 dB, which, combined with the 90 dB range of the AD8307, again corresponds to a 130 dB range.

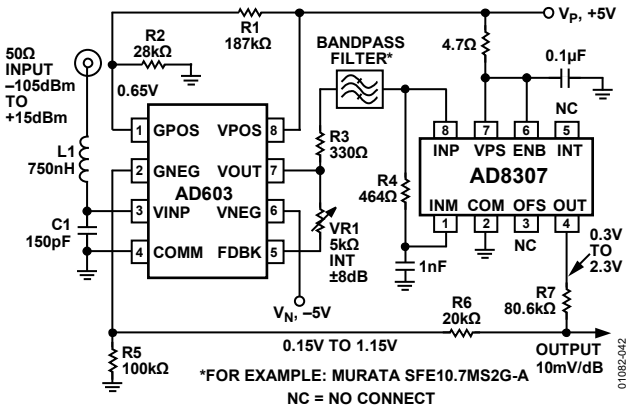


Figure 42. 120 dB Measurement System

Figure 42 shows how these two parts can work together to provide state-of-the-art IF measurements in applications such as spectrum/network analyzers and other high dynamic range instrumentation. To understand the operation, note first that the AD8307 is used to generate an output of about 0.3 V to 2.3 V. This 2 V span is divided by 2 in R5, R6, and R7 to provide the 1 V span needed by the AD603 to vary its gain by 40 dB. Note that an increase in the positive voltage applied at GNEG (Pin 2 of the AD603) lowers the gain. This feedback network is tapped to provide a convenient 10 mV/dB scaling at the output node, which can be buffered if necessary.

The center of the voltage range fed back to the AD603 is 650 mV, and the ±20 dB gain range is centered by R1/R2. Note that the intercept calibration of this system benefits from the use of a well-regulated 5 V supply. To absorb the insertion loss of the filter and center the full dynamic range, the intercept is adjusted by varying the maximum gain of the AD603, using VR1. Figure 43 shows the AD8307 output over the range −120 dBm to +20 dBm and the deviation from an ideal logarithmic response. The dotted line shows the increase in the noise floor that results when the filter is omitted; the decibel difference is about 10 $\log_{10}(50/0.2)$ or 24 dB, assuming a 50 MHz bandwidth from the AD603. An LC filter can be used in place of the ceramic filter used in this example.

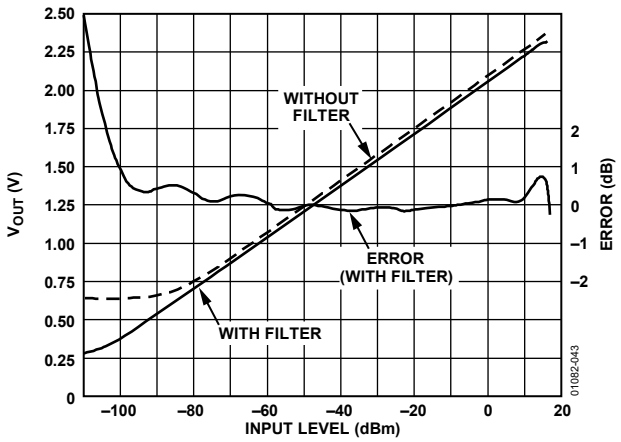


Figure 43. Results for 120 dB Measurement System

OPERATION AT LOW FREQUENCIES

The AD8307 provides excellent logarithmic conformance at signal frequencies that can be arbitrarily low, depending only on the values used for the input coupling capacitors. It can also be desirable to add a low-pass input filter to desensitize the log amp to HF signals. Figure 44 shows a simple arrangement, providing coupling with an attenuation of 20 dB; the intercept is shifted up by this attenuation, from −84 dBm to −64 dBm, and the input range is now 0.5 mV to 20 V (sine amplitude).

A high-pass 3 dB corner frequency of nominally 3 Hz is set by the 10 µF coupling capacitors, C1 and C2, which are preferably tantalum electrolytics (note the polarity) and a low-pass 3 dB corner frequency of 200 kHz (set by C3 and the effective resistance at the input of 1 kΩ). The −1% amplitude error points occur at 20 Hz and 30 kHz. These are readily altered to suit other applications by simple scaling. When C3 is zero, the low-pass corner is at 200 MHz. Note that the lower end of the dynamic range is improved by this capacitor, which essentially provides an HF short circuit at the input. This significantly lowers the wideband noise; the noise reduction is about 2 dB compared to when the AD8307 is driven from a 50 Ω source. Ensure that the output is free of postdemodulation ripple by lowering the low-pass filter time constant, which is provided by C5. With the value shown in Figure 44, the output time constant is 125 ms.

See Figure 40 for a more elaborate filter. To improve the law conformance at very low signal levels and at low frequencies, add C4 to the offset compensation loop.

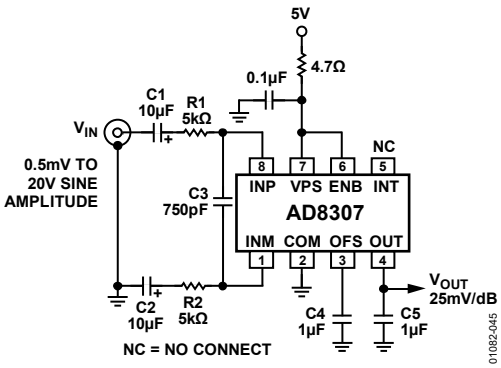
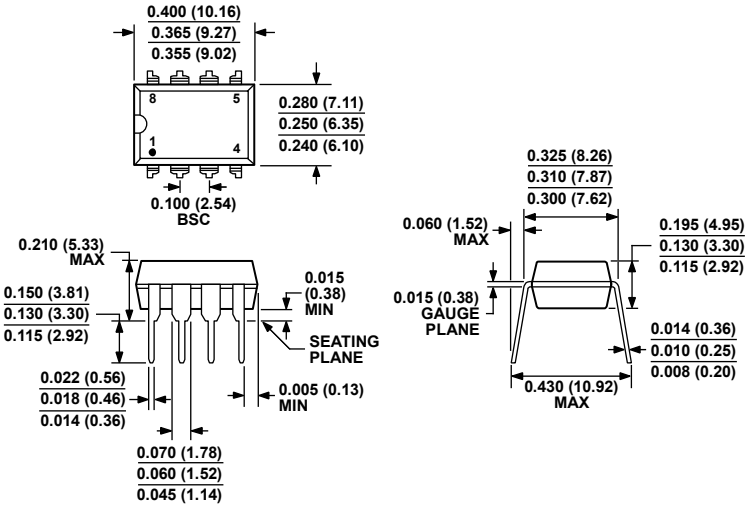


Figure 44. Connections for Low Frequency Operation

OUTLINE DIMENSIONS



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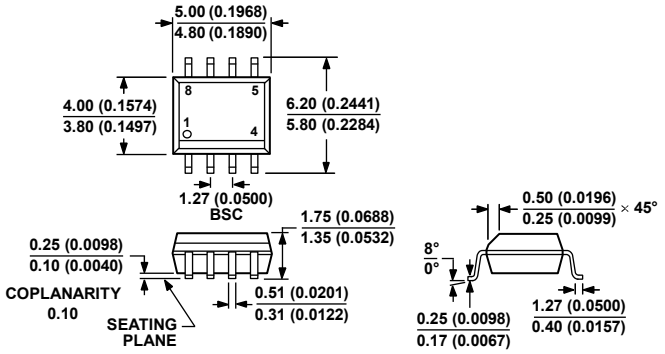
070606-A

Figure 45. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)



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012407-A

Figure 46. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8307ANZ	−40°C to +85°C	8-Lead PDIP	N-8
AD8307ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD8307ARZ-REEL	−40°C to +85°C	8-Lead SOIC_N 13" Tape and Reel	R-8
AD8307ARZ-RL7	−40°C to +85°C	8-Lead SOIC_N 7" Tape and Reel	R-8

[1] Z = RoHS Compliant Part.

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