THE DATASHEET OF

TS12A44513PWRG4

TEXAS INSTRUMENTS

TS12A44513, TS12A44514, TS12A44515

SCDS247B – OCTOBER 2008 – REVISED FEBRUARY 2016

TS12A4451x Low ON-State Resistance 4-Channel SPST CMOS Analog Switches

1 Features

- 2-V to 12-V Single-Supply Operation
- Specified ON-State Resistance:
  - 15-Ω Maximum With 12-V Supply
  - 20-Ω Maximum With 5-V Supply
  - 50-Ω Maximum With 3.3-V Supply
- ΔR_{ON} Matching
  - 2.5-Ω (Max) at 12 V
  - 3-Ω (Max) at 5 V
  - 3.5-Ω (Max) at 3.3 V
- Specified Low OFF-Leakage Currents:
  - 1 nA at 25°C
  - 10 nA at 85°C
- Specified Low ON-Leakage Currents:
  - 1 nA at 25°C
  - 10 nA at 85°C
- Low Charge Injection: 11.5 pC (12-V Supply)
- Fast Switching Speed:
  t_{ON} = 80 ns, t_{OFF} = 50 ns (12-V Supply)
- Break-Before-Make Operation ($t_{ON} > t_{OFF}$)
- TTL/CMOS-Logic Compatible With 5-V Supply
- Available in 14-Pin TSSOP Package or 14-Pin SOIC Package

2 Applications

- Data Acquisition Systems
- Communication Circuits
- Signal Routing
- Computer Peripherals

3 Description

The TS12A44513, TS12A44514, and TS12A44515 devices have four bidirectional single-pole single-throw (SPST) single-supply CMOS analog switches. The TS12A44513 has two normally closed (NC) switches and two normally open (NO) switches, the TS12A44514 has four NO switches, and the TS12A44515 has four NC switches.

These CMOS switches may operate continuously with a single supply from 2 V to 12 V and can handle rail-to-rail analog signals. The OFF-leakage current maximum is only 1 nA at 25°C or 10 nA at 85°C.

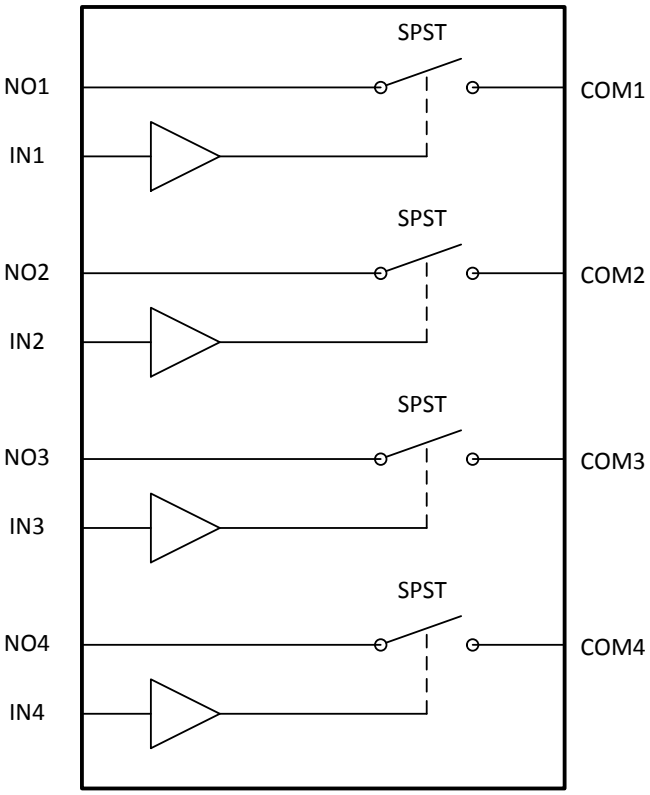
When using a 5-V supply, all digital inputs have 0.8-V to 2.4-V logic thresholds, ensuring TTL/CMOS-logic compatibility.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS12A44513, TS12A44514, TS12A44515	TSSOP (14)	5.00 mm x 4.4 mm
	SOIC (14)	8.65 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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Changes from Revision A (November 2014) to Revision B **Page**

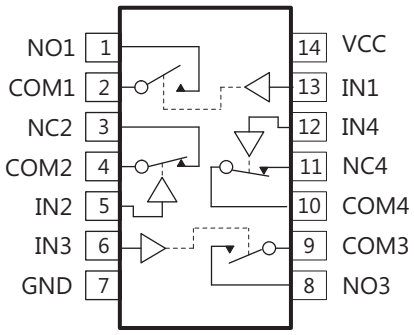
- Changed V_{CC} min value from 0 to 2 in *Recommended Operating Conditions* table ... 4
- Added Supply column back into all *Electrical Characteristics* tables ... 6

Changes from Original (October 2008) to Revision A **Page**

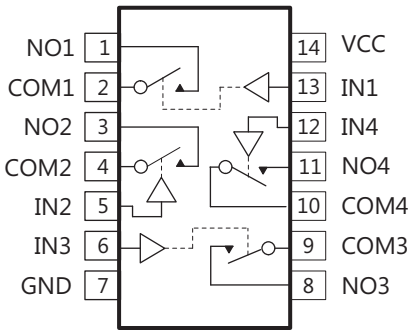
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

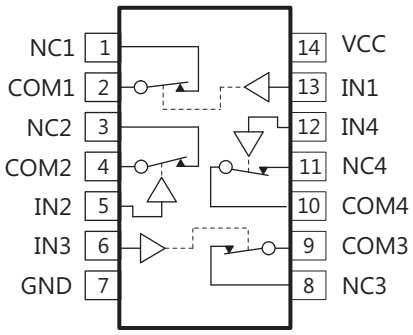
D OR PW PACKAGE...TS12A44513
(TOP VIEW)



D OR PW PACKAGE...TS12A44514
(TOP VIEW)



D OR PW PACKAGE...TS12A44515
(TOP VIEW)



Pin Functions

PIN				I/O	DESCRIPTION
NAME	TS12A44513	TS12A44514	TS12A44515		
COM	2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	I/O	Common
VCC	14	14	14	I	Power supply
IN	5, 6, 12, 13	5, 6, 12, 13	5, 6, 12, 13	I	Digital control to connect COM to NO or NC
GND	7	7	7	GND	Ground
NO	1, 8	1, 3, 8, 11	–	I/O	Normally open
NC	3, 11	–	1, 3, 8, 11	I/O	Normally closed

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)(3)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			–0.3	13	V
V_{NC} V_{NO} V_{COM}	Analog voltage (4)			–0.3	V_{CC} + 0.3	V
I_{NC} I_{NO} I_{COM} I_{IN}	Analog current			-20	20	mA
	Peak current (pulsed at 1 ms, 10% duty cycle)				±30	mA
T_A	Operating temperature			–40	85	°C
P_D	Power dissipation	Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, T_A = 25°C, T_J = 125°C	PW package		0.88	W
T_{stg}	Storage temperature			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) Voltages referenced to GND
(4) Voltages exceeding V_{CC} or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{CC}	2	12	V
V_{NC}, V_{NO}, V_{COM}, V_{IN}	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC (1)		TS12A44513, TS12A44514, TS12A44515		UNIT
		D	PW	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.8	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.6	48.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	61.3	
ψ_{JT}	Junction-to-top characterization parameter	13.8	5.7	
ψ_{JB}	Junction-to-board characterization parameter	44.1	60.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply(1)

V_{CC} = 4.5 V to 5.5 V, V_{INH} = 2.4 V, V_{INL} = 0.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP(2)	MAX	UNIT
ANALOG SWITCH							
V_{COM}, V_{NO}, V_{NC}	Analog signal range			0		V_{CC}	V
R_{on}	ON-state resistance	V_{CC} = 4.5 V, V_{COM} = 3.5 V, I_{COM} = 1 mA	25°C		12	20	Ω
			Full			30	
$R_{on(flat)}$	ON-state resistance flatness	V_{COM} = 1 V, 2 V, 3 V, I_{COM} = 1 mA	25°C		1	3	Ω
			Full			4	
ΔR_{on}	ON-state resistance matching between channels(3)	V_{CC} = 4.5 V, I_{COM} = 5 mA, V_{NO} or V_{NC} = 3 V	25°C			3	Ω
			T_{MIN} to T_{MAX}			4	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NO, NC OFF leakage current(4)	V_{CC} = 5.5 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 4.5 V	25°C			1	nA
			Full			10	
$I_{COM(OFF)}$	COM OFF leakage current(4)	V_{CC} = 5.5 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 4.5 V	25°C			1	nA
			Full			10	
$I_{COM(ON)}$	COM ON leakage current(4)	V_{CC} = 5.5 V, V_{COM} = 4.5 V, V_{NO} or V_{NC} = 4.5 V	25°C			1	nA
			Full			10	
DIGITAL CONTROL INPUT (IN)							
V_{IH}	Input logic high		Full	2.4		V_{CC}	V
V_{IL}	Input logic low		Full	0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = V_{CC}, 0 V	Full			0.01	µA
DYNAMIC							
t_{ON}	Turn-on time	see Figure 2	25°C		45	100	ns
			Full			125	
t_{OFF}	Turn-off time	see Figure 2	25°C		35	50	ns
			Full			70	
Q_C	Charge injection(5)	C_L = 1 nF, V_{NO} = 0 V, R_S = 0 Ω, See Figure 1	25°C		–1.5		pC
$C_{NO(OFF)}$, $C_{NC(OFF)}$	NO, NC OFF capacitance	f = 1 MHz, See Figure 4	25°C		8		pF
$C_{COM(OFF)}$	COM OFF capacitance	f = 1 MHz, See Figure 4	25°C		8		pF
$C_{COM(ON)}$	COM ON capacitance	f = 1 MHz, See Figure 4	25°C		19		pF
C_I	Digital input capacitance	V_{IN} = V_{CC}, 0 V	25°C		2		pF
BW	Bandwidth	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS},	25°C		530		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		–94		dB
THD	Total harmonic distortion	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		0.09%		
SUPPLY							
I_{CC}	Supply Current	V_{IN} = V_{CC}, 0 V	25°C		0.05		µA
			Full		0.1		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$
(4) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(5) Specified by design, not production tested

6.6 Electrical Characteristics for 12-V Supply(1)

V_{CC} = 11.4 V to 12.6 V, V_{INH} = 5 V, V_{INL} = 0.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP(2)	MAX	UNIT
ANALOG SWITCH							
V_{COM}, V_{NO}, V_{NC}	Analog signal range			0		V_{CC}	V
R_{on}	ON-state resistance	V_{CC} = 11.4 V, V_{COM} = 10 V, I_{COM} = 1 mA	25°C		6.5	10	Ω
			Full			15	
$R_{on(flat)}$	ON-state resistance flatness	V_{CC} = 11.4 V, V_{COM} = 2 V, 5 V, 10 V, I_{COM} = 1 mA	25°C		1.5	3	Ω
			Full			4	
ΔR_{on}	ON-state resistance matching between channels(3)	V_{CC} = 11.4 V, I_{COM} = 5 mA, V_{NO} or V_{NC} = 10 V	25°C			2.5	Ω
			T_{MIN} to T_{MAX}			3	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NO, NC OFF leakage current(4)	V_{CC} = 12.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 10 V	25°C			1	nA
			Full			10	
$I_{COM(OFF)}$	COM OFF leakage current(4)	V_{CC} = 12.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 10 V	25°C			1	nA
			Full			10	
$I_{COM(ON)}$	COM ON leakage current(4)	V_{CC} = 12.6 V, V_{COM} = 10 V, V_{NO} or V_{NC} = 10 V	25°C			1	nA
			Full			10	
DIGITAL CONTROL INPUT (IN)							
V_{IH}	Input logic high		Full	5		V_{CC}	V
V_{IL}	Input logic low		Full	0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = V_{CC}, 0 V	Full			0.001	μA
DYNAMIC							
t_{ON}	Turn-on time	See Figure 2	25°C		25	75	ns
			Full			80	
t_{OFF}	Turn-off time	See Figure 2	25°C		20	45	ns
			Full			50	
Q_C	Charge injection(5)	C_L = 1 nF, V_{NO} = 0 V, R_S = 0 Ω, See Figure 1	25°C		–10.5		pC
$C_{NO(OFF)}$, $C_{NC(OFF)}$	NO, NC OFF capacitance	f = 1 MHz, See Figure 4	25°C		8		pF
$C_{COM(OFF)}$	COM OFF capacitance	f = 1 MHz, See Figure 4	25°C		8		pF
$C_{COM(ON)}$	COM ON capacitance	f = 1 MHz, See Figure 4	25°C		21.5		pF
C_I	Digital input capacitance	V_{IN} = V_{CC}, 0 V	25°C		2		pF
BW	Bandwidth	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS},	25°C		530		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		–95		dB
THD	Total harmonic distortion	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		0.07%		
SUPPLY							
I_{CC}	Supply Current	V_{IN} = V_{CC}, 0 V	25°C		0.05		μA
			Full		0.2		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical Values are at T_A = 25°C.
(3) $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$
(4) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(5) Specified by design, not production tested

6.7 Electrical Characteristics for 3-V Supply(1)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP(2)	MAX	UNIT
ANALOG SWITCH							
V_{COM}, V_{NO}, V_{NC}	Analog signal range			0		V_{CC}	V
R_{on}	ON-state resistance	V_{CC} = 3 V, V_{COM} = 1.5 V, I_{NO} = 1 mA,	25°C		20	40	Ω
			Full			50	
$R_{on(flat)}$	ON-state resistance flatness	V_{CC} = 3 V, V_{COM} = 1 V, 1.5 V, 2 V, I_{COM} = 1 mA	25 °C		1	3	Ω
			Full			4	
ΔR_{on}	ON-state resistance matching between channels(3)	V_{CC} = 2.7 V, I_{COM} = 5 mA, V_{NO} or V_{NC} = 1.5 V	25°C			3.5	Ω
			T_{MIN} to T_{MAX}			4.5	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NO, NC OFF leakage current(4)	V_{CC} = 3.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 3 V	25°C			1	nA
			Full			10	
$I_{COM(OFF)}$	COM OFF leakage current(4)	V_{CC} = 3.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 3 V	25°C			1	nA
			Full			10	
$I_{COM(ON)}$	COM ON leakage current(4)	V_{CC} = 3.6 V, V_{COM} = 3 V, V_{NO} or V_{NC} = 3 V	25°C			1	nA
			Full			10	
DIGITAL CONTROL INPUT (IN)							
V_{IH}	Input logic high		Full	2.4		V_{CC}	V
V_{IL}	Input logic low		Full	0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = V_{CC}, 0 V	Full			0.01	µA
DYNAMIC							
t_{ON}	Turn-on time(5)	See Figure 2	25°C		70	120	ns
			Full			175	
t_{OFF}	Turn-off time(5)	See Figure 2	25°C		50	80	ns
			Full			120	
Q_C	Charge injection(5)	C_L = 1 nF, See Figure 1	25°C		–0.5		pC
$C_{NO(OFF)}$, $C_{NC(OFF)}$	NO, NC OFF capacitance	f = 1 MHz, See Figure 4	25°C		8		pF
$C_{COM(OFF)}$	COM OFF capacitance	f = 1 MHz, See Figure 4	25°C		8		pF
$C_{COM(ON)}$	COM ON capacitance	f = 1 MHz, See Figure 4	25°C		17		pF
C_I	Digital input capacitance	V_{IN} = V_{CC}, 0 V	25°C		2		pF
BW	Bandwidth	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		510		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		–94		dB
THD	Total harmonic distortion	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		0.27%		
SUPPLY							
I_{CC}	Supply Current	V_{IN} = V_{CC}, 0 V	25°C		0.05		µA
			Full		0.2		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$
(4) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(5) Specified by design, not production tested

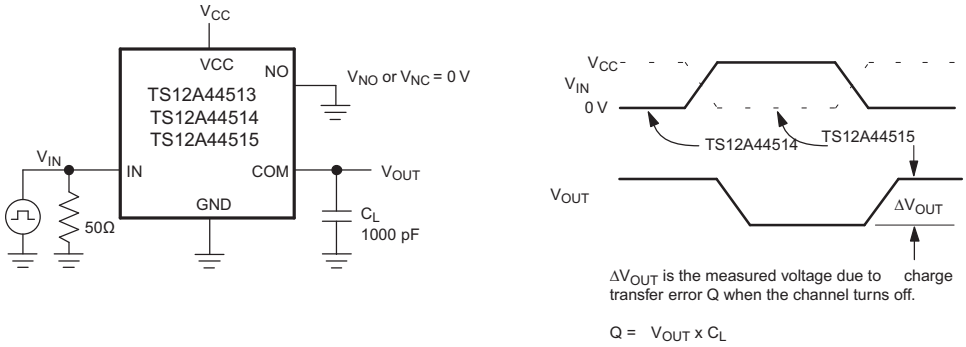


Figure 1. Charge Injection

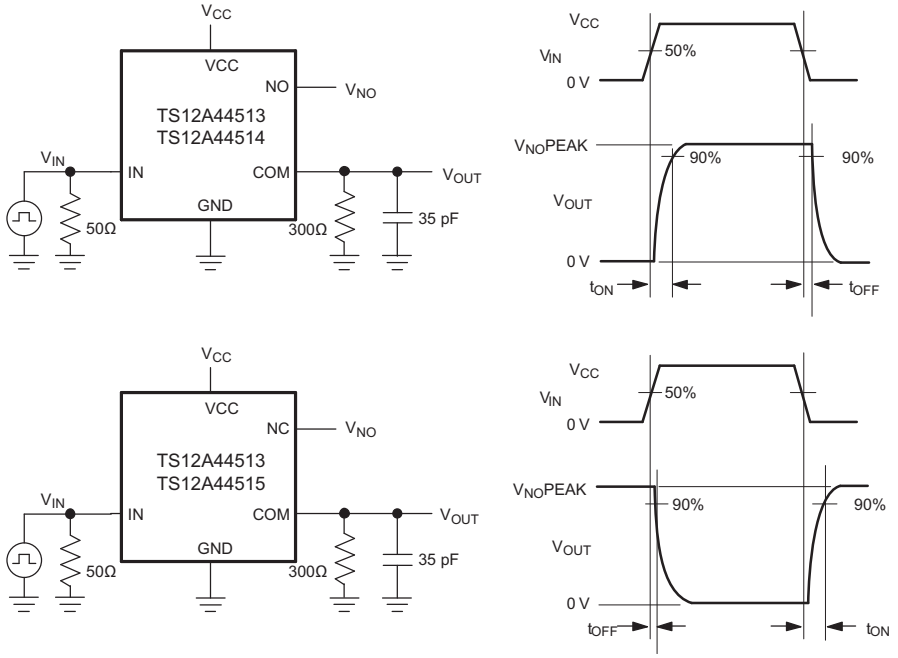
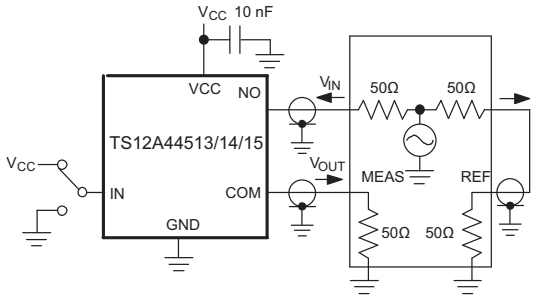


Figure 2. Switching Times



Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. ON loss is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF Isolation} = 20\log \frac{V_{OUT}}{V_{IN}}$$

$$\text{ON Loss} = 20\log \frac{V_{OUT}}{V_{IN}}$$

Figure 3. Off Isolation and On Loss

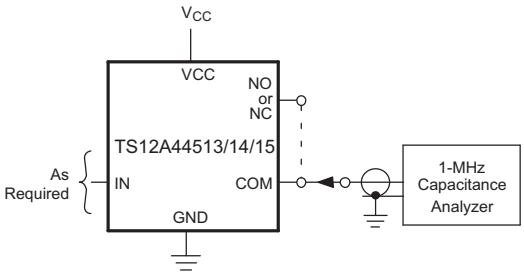


Figure 4. NO, NC, and COM Capacitance

6.8 Typical Characteristics

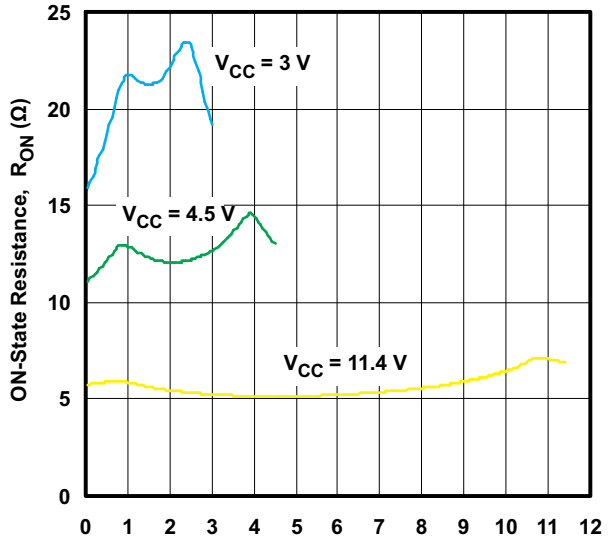


Figure 5. R_{ON} vs V_{COM} (T_A = 25°C)

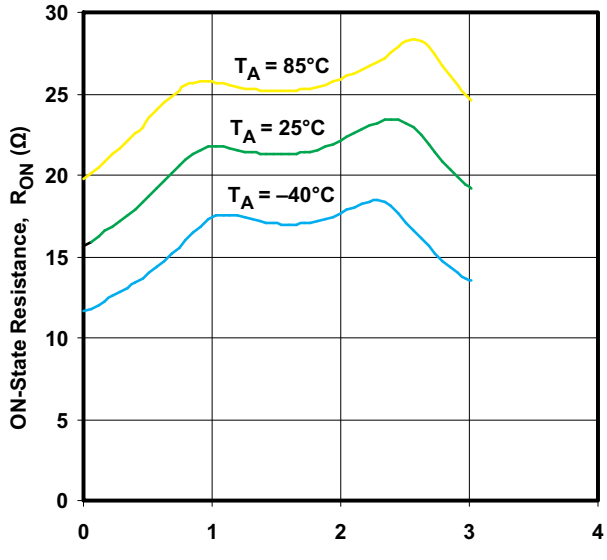


Figure 6. R_{ON} vs V_{COM} (V_{CC} = 3 V)

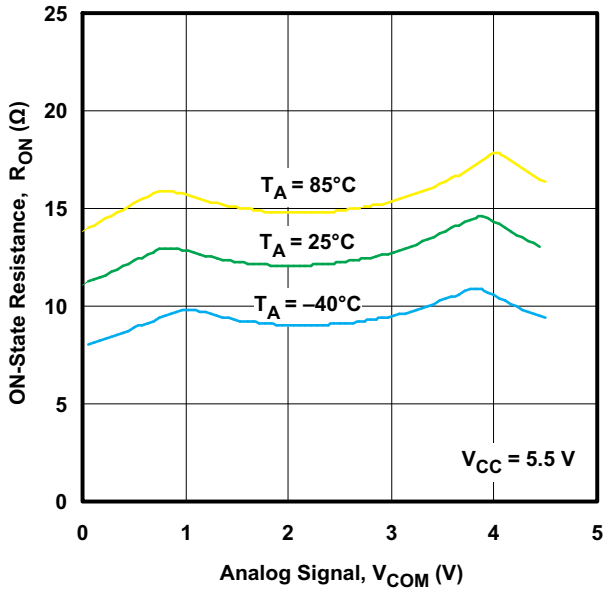


Figure 7. R_{ON} vs V_{COM} (V_{CC} = 4.5 V)

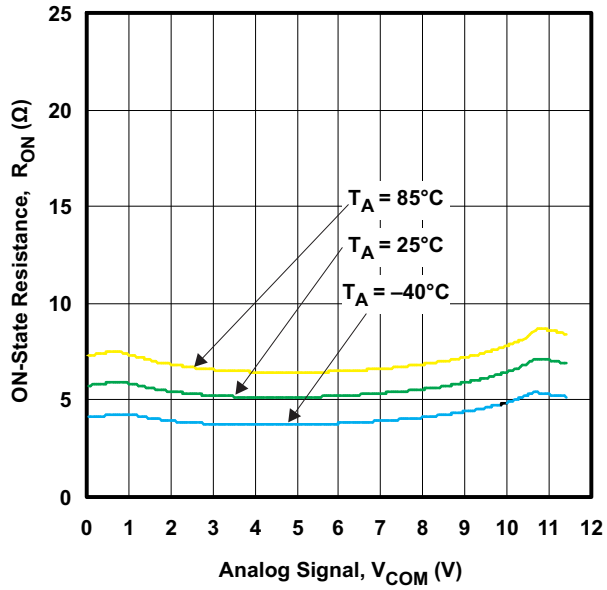


Figure 8. R_{ON} vs V_{COM} (V_{CC} = 11.4 V)

7 Detailed Description

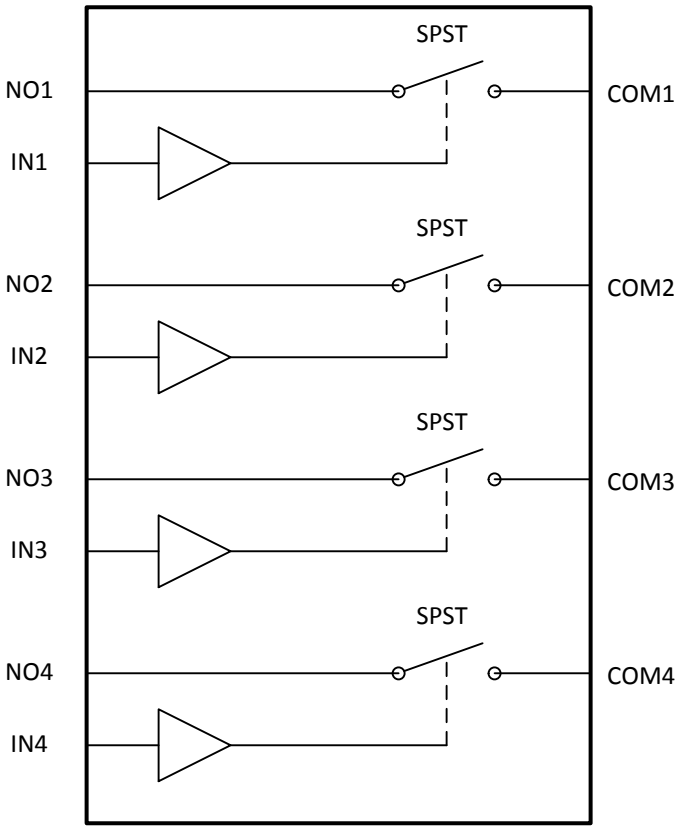
7.1 Overview

The TS12A4451x has 4 bidirectional single-pole single-throw (SPST) single-supply CMOS analog switches. The TS12A44513 has two normally closed (NC) switches and two normally open (NO) switches, the TS12A44514 has four normally open (NO) switches, and the TS12A44515 has four normally closed (NC) switches .

These CMOS switches can operate continuously with a single supply between 2 V and 12 V and can handle rail-to-rail analog signals. The OFF-leakage current maximum is only 1 nA at 25°C or 10 nA at 85°C.

When using a 5-V supply, all digital inputs have 0.8-V to 2.4-V logic thresholds, ensuring TTL/CMOS-logic compatibility.

7.2 Functional Block Diagram



7.3 Feature Description

The TS12A4451x is bidirectional with fast switching times in the 10's of ns range which allows data acquisition and communication between multiple devices.

With a 5-V supply these devices are compatible with standard 1.8-V TTL/CMOS logic.

7.4 Device Functional Modes

Table 1. Function Table

IN	NO TO COM, COM TO NO	NC TO COM, COM TO NC
L	OFF	ON
H	ON	OFF

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

8.1.1 Logic-Level Thresholds

The logic-level thresholds are CMOS/TTL compatible when V_{CC} is 5 V. As V_{CC} is raised, the level threshold increases slightly. When V_{CC} reaches 12 V, the level threshold is about 3 V – above the TTL-specified high-level minimum of 2.8 V, but still compatible with CMOS outputs.

CAUTION

Do not connect the TS12A44513/TS12A44514/MAS4515 V_{CC} to 3 V and then connect the logic-level pins to logic-level signals that operate from 5-V supply. Output levels can exceed 3 V and violate the absolute maximum ratings, damaging the part and/or external circuits.

8.2 Typical Application

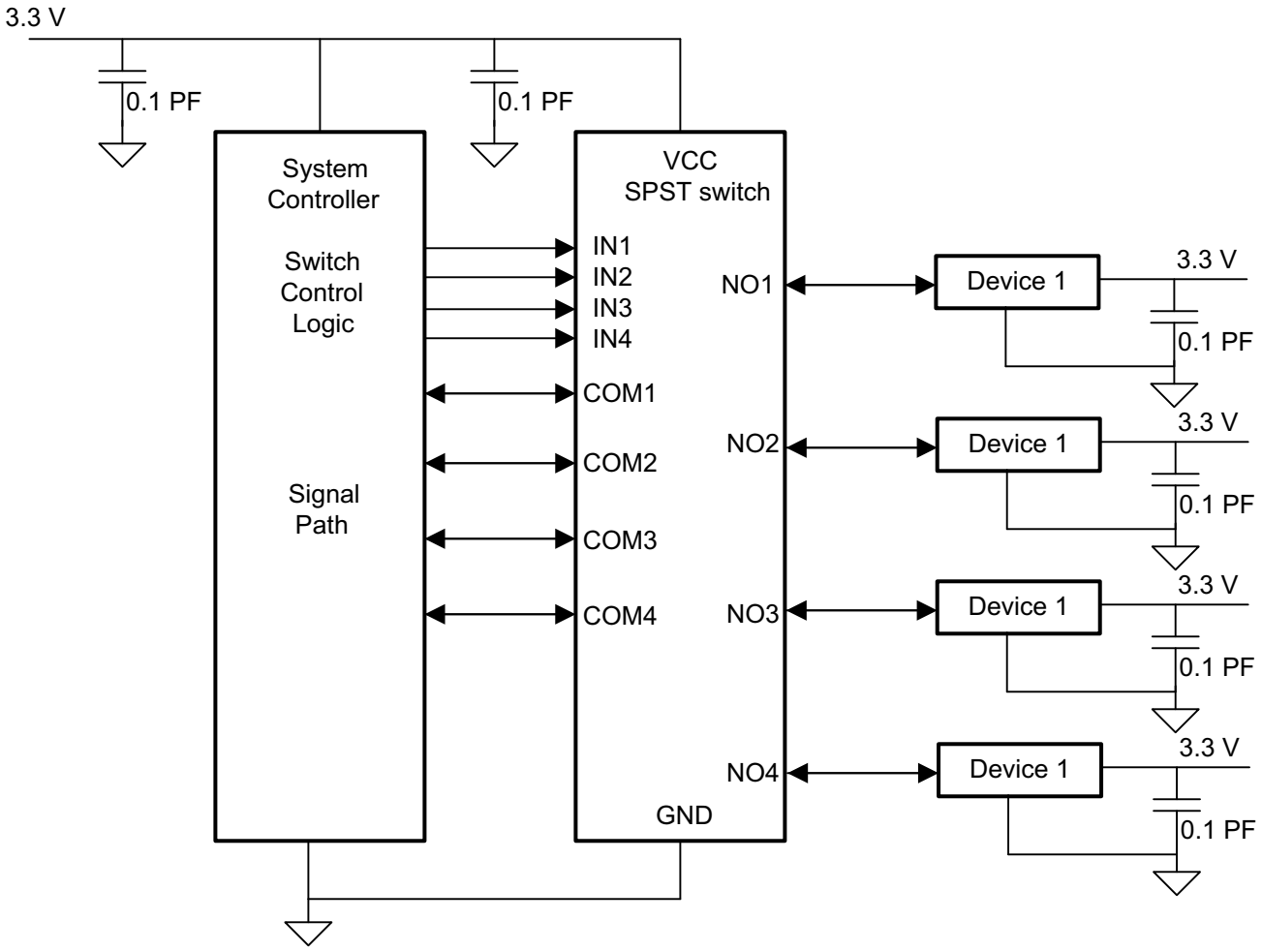


Figure 9. Typical Application Schematic

8.2.1 Design Requirements

Ensure that all of the signals passing through the switch are with in the specified ranges to ensure proper performance.

Table 2. Design Parameters

	MIN	MAX	UNIT
V_{CC}	0	12	V
V_{NC}, V_{NO}, V_{COM}, V_{IN}	0	V_{CC}	V

8.2.2 Detailed Design Procedure

The TS12A4451x can be properly operated without any external components. However, it is recommended that unused pins be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. It is also recommended that the digital control pins (INX) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

8.2.3 Application Curve

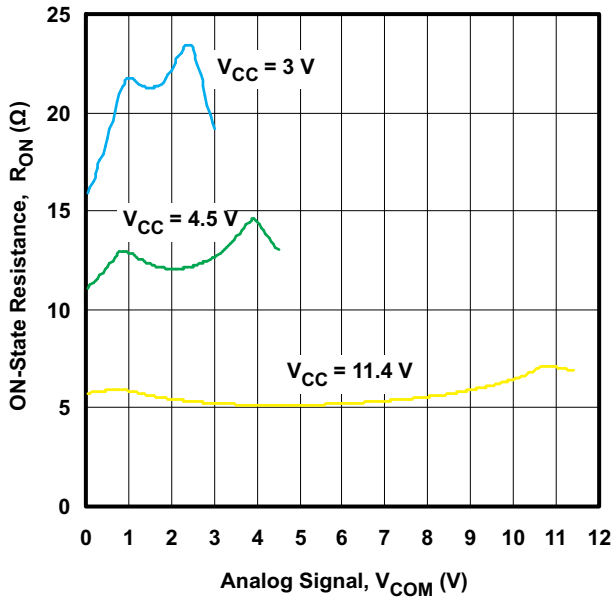


Figure 10. ON-State Resistance, R_{ON} vs Analog Signal, V_{COM}

9 Power Supply Recommendations

The TS12A4451x construction is typical of most CMOS analog switches, except that they have only two supply pins: VCC and GND. VCC and GND drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes connected in series are internally connected between each analog-signal pin and both VCC and GND. If an analog signal exceeds V_{CC} or GND, one of the diodes will be forward biased, but the other will be reverse biased preventing current flow.

Virtually all the analog leakage current comes from the ESD diodes to VCC or GND. Although the ESD diodes on a given signal pin are identical and, therefore, fairly well balanced, they are reverse biased differently. Each is biased by either V_{CC} or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the VCC and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no direct connection between the analog-signal paths and VCC or GND.

VCC and GND also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched V_{CC} and GND signals to drive the analog signal gates.

10 Layout

10.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

10.2 Layout Example

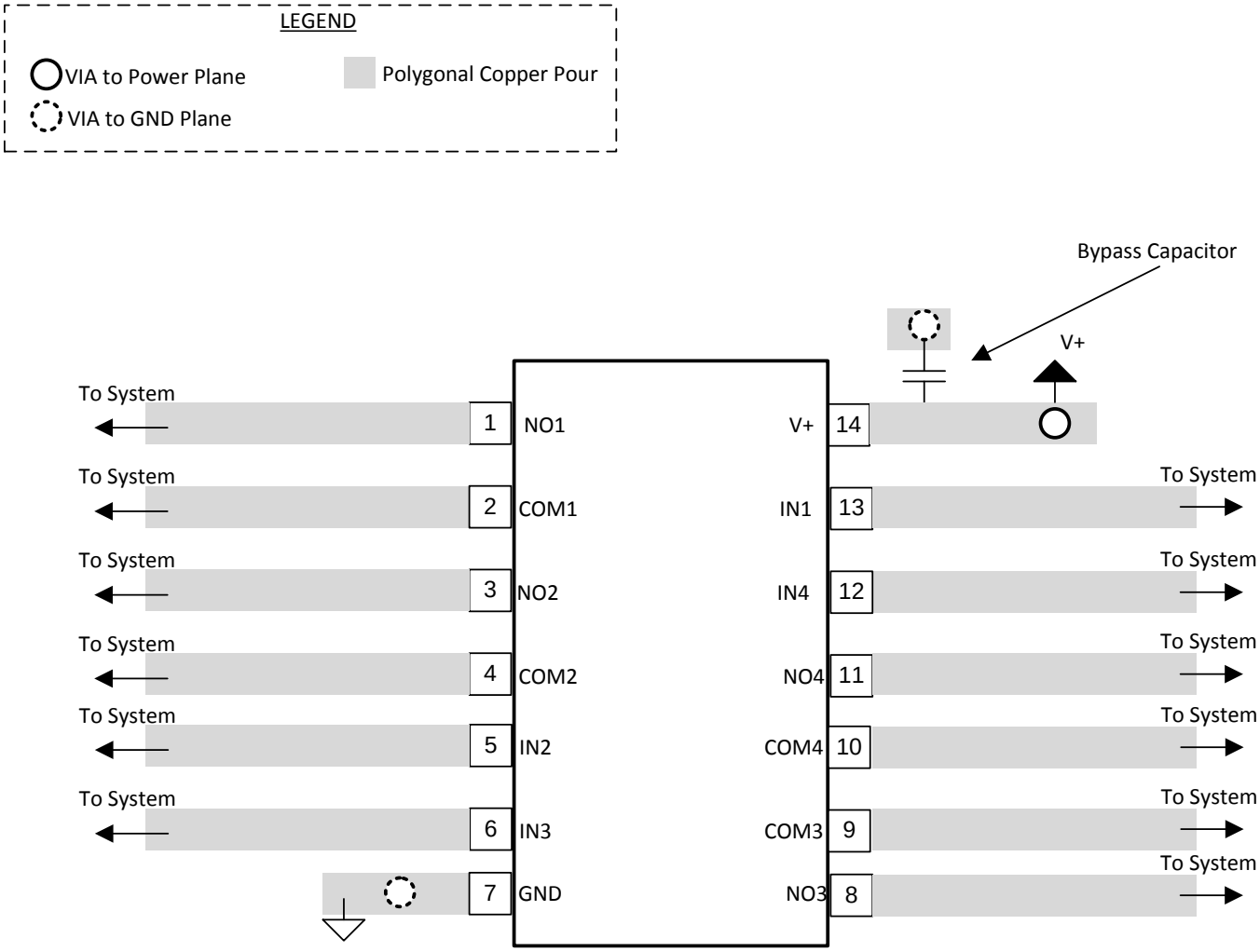


Figure 11. Layout Schematic

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TS12A44513	Click here	Click here	Click here	Click here	Click here
TS12A44514	Click here	Click here	Click here	Click here	Click here
TS12A44515	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS12A44513DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS12A44513	Samples
TS12A44513PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD4513	Samples
TS12A44514DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS12A44514	Samples
TS12A44514PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD4514	Samples
TS12A44515DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS12A44515	Samples
TS12A44515PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD4515	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

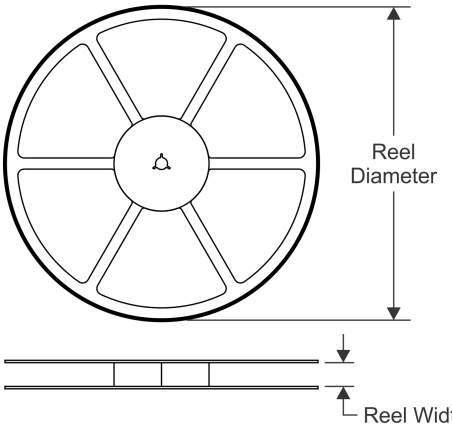
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

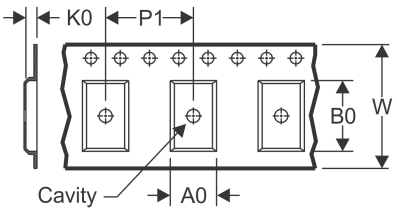
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

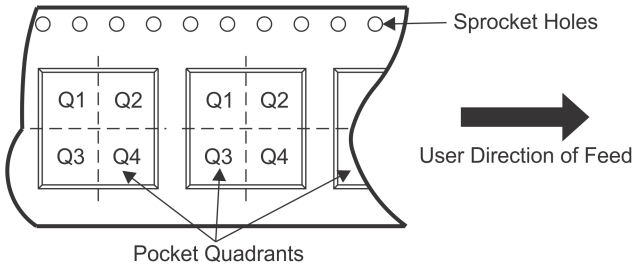


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

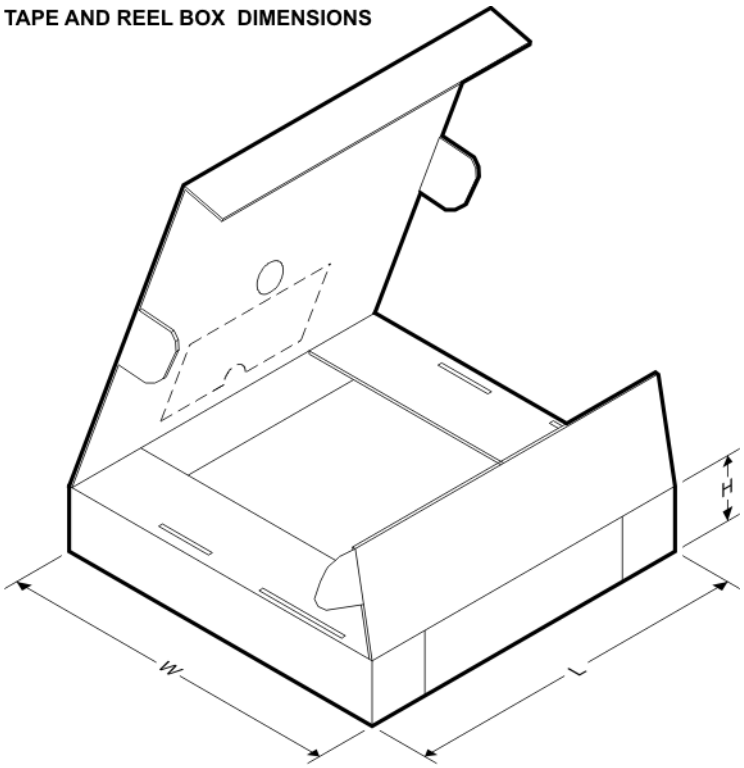
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS12A44513DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TS12A44513PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS12A44514DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TS12A44514PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS12A44515DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TS12A44515PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

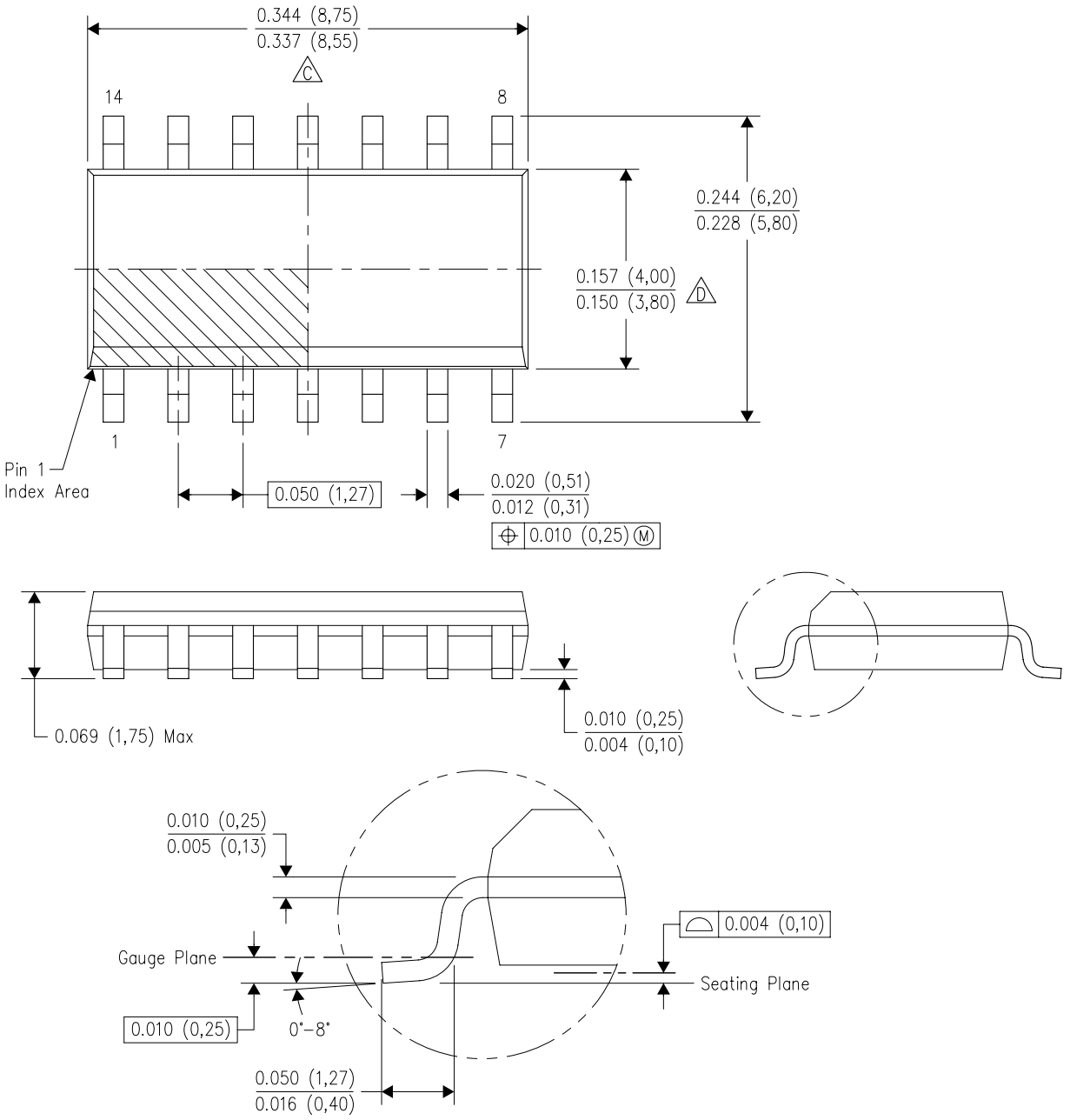
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS12A44513DR	SOIC	D	14	2500	367.0	367.0	38.0
TS12A44513PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TS12A44514DR	SOIC	D	14	2500	367.0	367.0	38.0
TS12A44514PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TS12A44515DR	SOIC	D	14	2500	367.0	367.0	38.0
TS12A44515PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

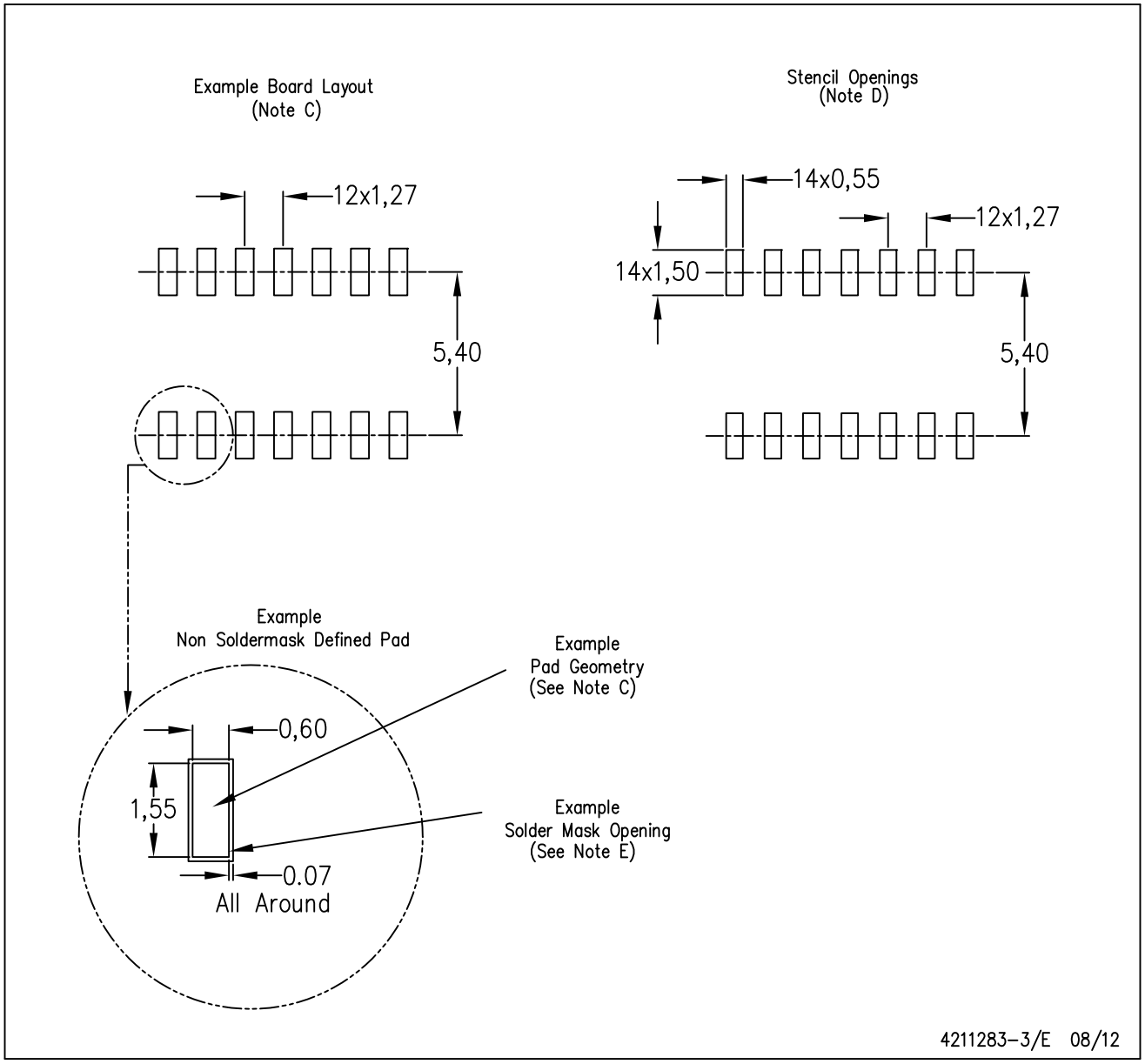
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

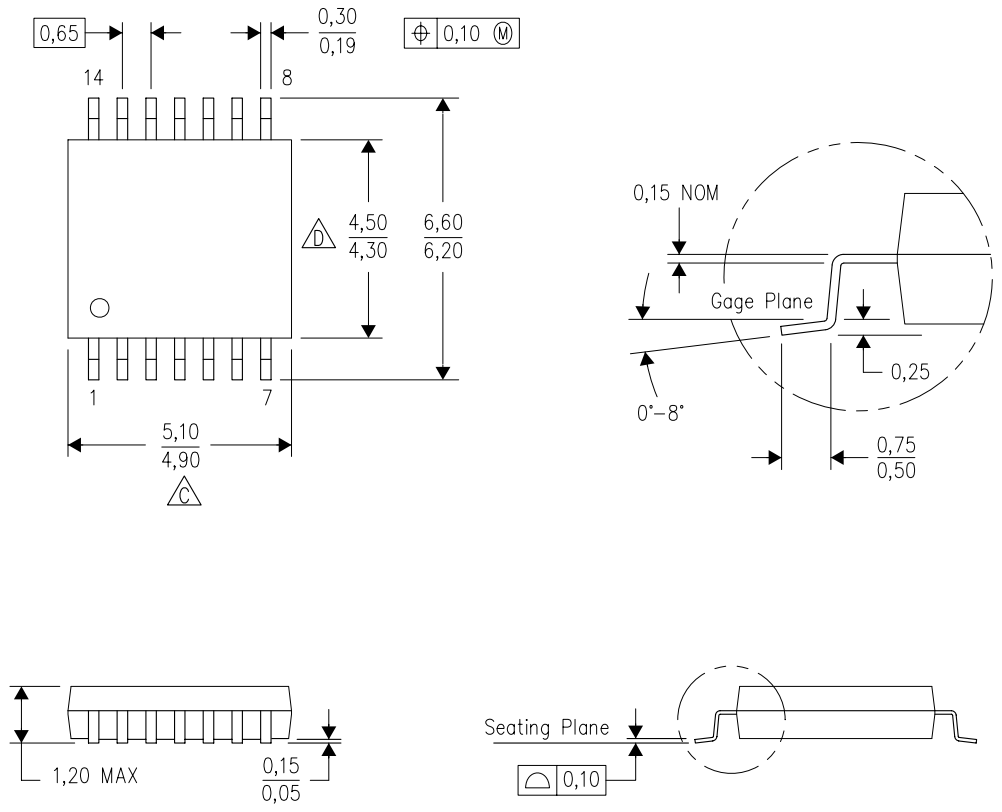
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

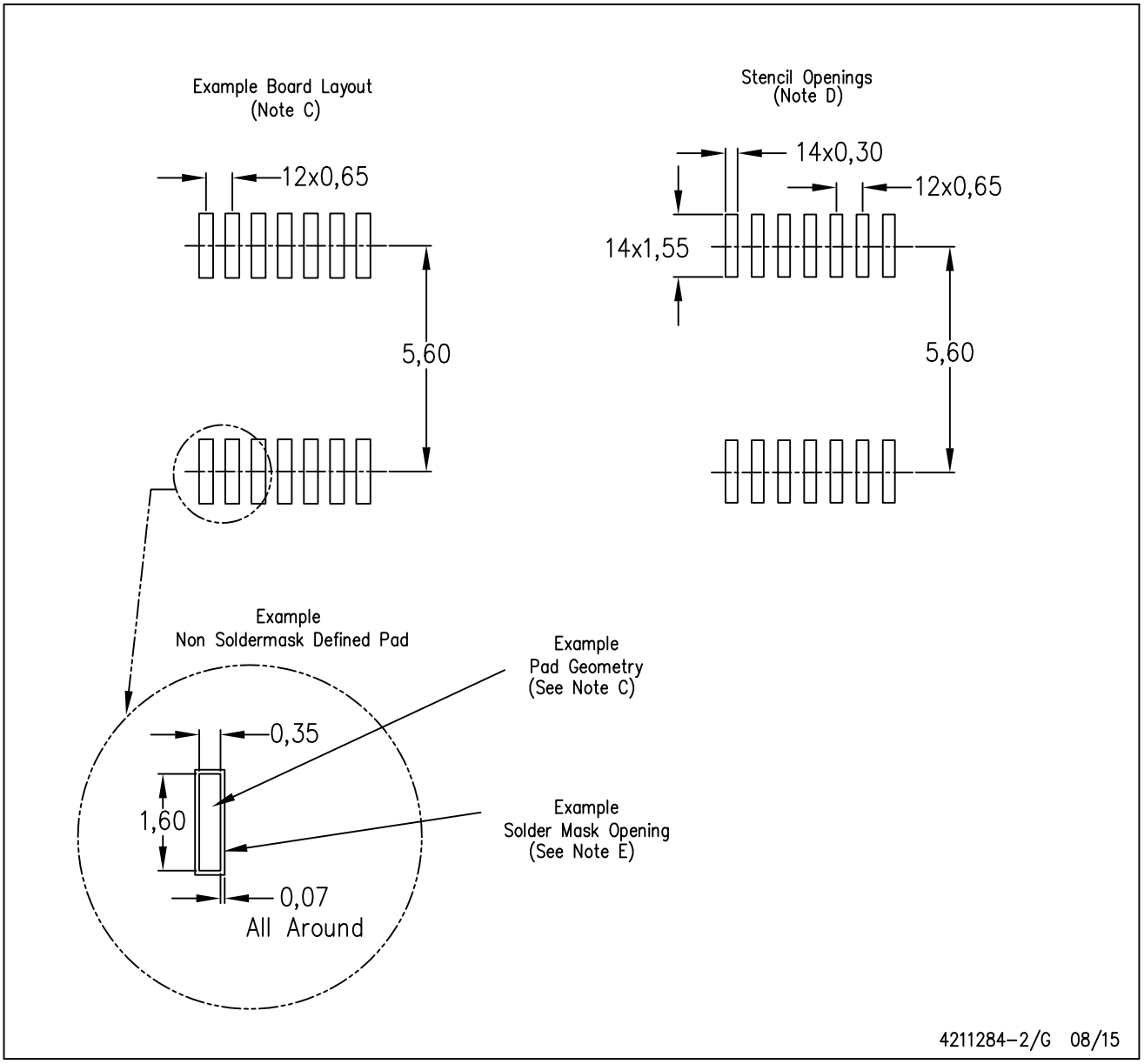
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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