



**THE DATASHEET OF  
DG508ADJ+**



# Monolithic CMOS Analog Multiplexers

## General Description

Maxim's DG508A and DG509A are monolithic CMOS analog multiplexers (muxes): the DG508A is a single 8-channel (1-of-8) mux, and the DG509A is a differential 4-channel (2-of-8) mux.

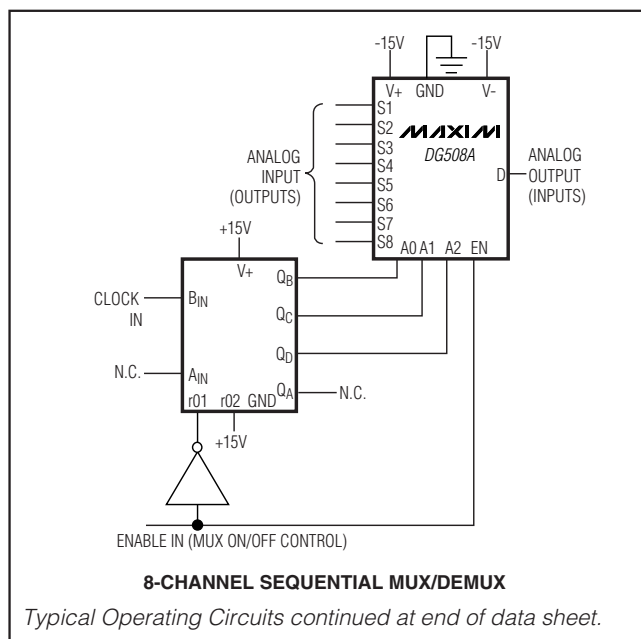
Both devices guarantee break-before-make switching. Maxim guarantees these muxes will not latch up if the power supplies are turned off with the input signals still present. Maxim also guarantees continuous operation when these devices are powered by supplies ranging from  $\pm 4.5\text{V}$  to  $\pm 18\text{V}$ .

The DG508A/DG509A are plug-in upgrades for the industry-standard DG508A/DG509A, respectively. Maxim's parts have faster enable switching times and significantly lower leakage currents. The DG508A/DG509A also consume significantly lower power, making them ideal for portable equipment.

## Applications

Control Systems  
Data Logging Systems  
Aircraft Heads-Up Displays  
Data-Acquisition Systems  
Signal Routing

## Typical Operating Circuits



## Features

- ◆ Improved Second Source
- ◆ Operate from  $\pm 4.5\text{V}$  to  $\pm 18\text{V}$  Supplies
- ◆ Symmetrical, Bidirectional Operation
- ◆ Logic and Enable Inputs, TTL and CMOS Compatible
- ◆ Latchup-Proof Construction
- ◆ Monolithic, Low-Power CMOS Design

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DG508ACJ	0°C to +70°C	16 Plastic DIP
DG508ACWE	0°C to +70°C	16 Wide SO
DG508AC/D	0°C to +70°C	Dice*
DG508ABK	-20°C to +85°C	16 CERDIP
DG508ADJ	-40°C to +85°C	16 Plastic DIP
DG508ADY	-40°C to +85°C	16 Narrow SO
DG508AEWE	-40°C to +85°C	16 Wide SO
DG508AAK	-55°C to +125°C	16 CERDIP
DG508AMY/PR	-55°C to +125°C	16 Narrow SO
DG509ACJ	0°C to +70°C	16 Plastic DIP
DG509ACWE	0°C to +70°C	16 Wide SO
DG509AC/D	0°C to +70°C	Dice*
DG509ABK	-20°C to +85°C	16 CERDIP
DG509ADJ	-40°C to +85°C	16 Plastic DIP
DG509ADY	-40°C to +85°C	16 Narrow SO
DG509AEWE	-40°C to +85°C	16 Wide SO
DG509AAK	-55°C to +125°C	16 CERDIP
DG509AMY/PR	-55°C to +125°C	16 Narrow SO

Devices are available in a lead(Pb)-free/RoHS-compliant package (except CERDIP). Specify lead-free by adding a plus (+) to the part number when ordering.

\*Contact factory for dice specifications.

# Monolithic CMOS Analog Multiplexers

## ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ .....	+44V
GND .....	+25V
Digital Inputs, V <sub>S</sub> and V <sub>D</sub> (Note 1) .....	-2V to (V+ + 2V) or 20mA, whichever occurs first

Current (any terminal, except S or D) .....

Continuous Current, S or D .....	30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) ..	40mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
Plastic DIP (derate 10.53mW/°C above +70°C) .....	842mW
Narrow SO (derate 8.70mW/°C above +70°C) .....	696mW
Wide SO (derate 9.52mW/°C above +70°C) .....	762mW
CERDIP (derate 10.00mW/°C above +70°C) .....	800mW

Operating Temperature Ranges:

DG50_ACJ/CWE .....	0°C to +70°C
DG50_ABK .....	-20°C to +85°C
DG50_ADJ/DY/EWE .....	-40°C to +85°C
DG50_AAK/MY .....	-55°C to +125°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C
Soldering Temperature (reflow)	
PDIP, Wide SO, Narrow SO, CERDIP containing lead(Pb) ..	+240°C
PDIP, Wide SO, Narrow SO lead(Pb)-free .....	+260°C

**Note 1:** Signals on S<sub>-</sub> or D<sub>-</sub> exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V<sub>GND</sub> = 0V, T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	DG508AA/M DG509AA/M			DG508AD/E/B/C DG509AD/E/B/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>SWITCH</b>									
Analog Signal	V <sub>ANALOG</sub>		-15		+15	-15		+15	V
Drain-Source On-Resistance	R <sub>DS(ON)</sub>	Sequence each switch on, V <sub>A_L</sub> = 0.8V, V <sub>A_H</sub> = 2.4V (Note 4)	V <sub>D</sub> = 10V, I <sub>S</sub> = -200μA		170	400	170	450	Ω
			V <sub>D</sub> = -10V, I <sub>S</sub> = 200μA		130	400	130	450	
Greatest Change in Drain-Source On-Resistance Between Channels	ΔR <sub>DS(ON)</sub>	$\Delta R_{DS(ON)} = \left( \frac{R_{DS(ON) \max} - R_{DS(ON) \min}}{R_{DS(ON)}} \right)$ -10V ≥ V <sub>S</sub> ≥ 10V			6		6		%
Source Off-Leakage Current	I <sub>S(OFF)</sub>	V <sub>EN</sub> = 0V	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V		0.002	0.5	0.002	1	nA
			V <sub>S</sub> = -10V, V <sub>D</sub> = 10V		-0.5	-0.005	-1	-0.005	
Drain Off-Leakage Current	DG508A	V <sub>EN</sub> = 0V	V <sub>D</sub> = 10V, V <sub>S</sub> = -10V		0.01	2	0.01	5	nA
			V <sub>D</sub> = -10V, V <sub>S</sub> = 10V		-2	-0.015	-5	-0.015	
	DG509A		V <sub>D</sub> = 10V, V <sub>S</sub> = -10V		0.005	2	0.005	5	
			V <sub>D</sub> = -10V, V <sub>S</sub> = 10V		-2	-0.008	-5	-0.008	
Drain On-Leakage Current	DG508A	Sequence each switch on, V <sub>A_L</sub> = 0.8V V <sub>A_H</sub> = 2.4V (Note 2)	V <sub>S(all)</sub> = V <sub>D</sub> = 10V		0.015	2	0.015	5	nA
			V <sub>S(all)</sub> = V <sub>D</sub> = -10V		-2	-0.03	-5	-0.03	
	DG509A		V <sub>S(all)</sub> = V <sub>D</sub> = 10V		0.007	2	0.007	5	
			V <sub>S(all)</sub> = V <sub>D</sub> = -10V		-2	-0.015	-5	-0.015	

# Monolithic CMOS Analog Multiplexers

**DG508A/DG509A**

## ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, VGND = 0V, TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	DG508AA/M DG509AA/M			DG508AD/E/B/C DG509AD/E/B/C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
<b>LOGIC INPUT</b>										
Logic Input Current, Input Voltage High	IAH	VA_ = 2.4V		-10	-		10	-0.002	μA	
		VA_ = 15V			0.006	10		0.006		10
Logic Input Current, Input Voltage Low	IAL	All VA_ = 0V	VEN = 2.4V		-10	-		10	-0.002	μA
			VEN = 0V		-10	-		-10	-0.002	
<b>DYNAMIC</b>										
Multiplexer Switching	ttransition	Figure 1		0.6	1.0		0.6	1.0	μs	
Break-Before-Make Interval	tOPEN	Figure 3		0.2			0.2		μs	
Enable Turn-On Time	tON(EN)	Figure 2		0.4	1.0		0.4	1.5	μs	
Enable Turn-Off Time	tOFF(EN)	Figure 2		0.2	0.7		0.2	1.0	μs	
Off-Isolation	OIRR	VEN = 0V, RL = 1kΩ, CL = 15pF, VS = 7VRMS f = 500kHz (Note 3)		68			68		dB	
Source Off-Capacitance	CS(OFF)	VS = 0V, VEN = 0V, f = 140kHz		5			5		pF	
Drain Off- Capacitance	IDG508A	CD(OFF)	VS = 0V, VEN = 0V, f = 140kHz		25		25		pF	
	DGS09A				12		12			
<b>SUPPLY</b>										
Positive Supply Current	I+	VEN = 2.4V, all VA_ = 0V or 2.4V		0.02	0.2		0.02	0.2	mA	
Negative Supply Current	I-	VEN = 2.4V, all VA_ = 0V or 2.4V		-0.1	-0.01		-0.1	-0.01	mA	
Positive Supply Current in Standby	I+	VEN = 0V, all VA_ = 0V or 2.4V		0.02	0.2		0.02	0.2	mA	
Negative Supply Current in Standby	I-	VEN = 0V, all VA_ = 0V or 2.4V		-0.1	-0.01		-0.1	-0.01	mA	
Power-Supply Range for Continuous Operation	V-, V+	(Notes 4, 5)		±4.5		±18.0	±4.5		±18.0	V

# Monolithic CMOS Analog Multiplexers

## ELECTRICAL CHARACTERISTICS

(V<sub>+</sub> = 15V, V<sub>GND</sub> = 0V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	DG508AA/M DG509AA/M			DG508AD/E/B/C DG509AD/E/B/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>SWITCH</b>									
Analog Signal Range	V <sub>ANALOG</sub>		-15	+15		-15	+15		V
Drain-Source On-Resistance	R <sub>DS(ON)</sub>	Sequence each switch on, V <sub>A_L</sub> = 0.8V, V <sub>A_H</sub> = 2.4V	V <sub>D</sub> = 10V, I <sub>S</sub> = -200μA		500		550		Ω
			V <sub>D</sub> = -10V, I <sub>S</sub> = 200μA		500		550		
Source Off-Leakage Current	I <sub>S(OFF)</sub>	V <sub>EN</sub> = 0V	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V		+50		+50		nA
			V <sub>S</sub> = -10V, V <sub>D</sub> = -10V		-50		-50		
Drain Off-Leakage Current	DG508A DG509A	I <sub>D(OFF)</sub>	V <sub>EN</sub> = 0V	V <sub>D</sub> = 10V, V <sub>S</sub> = -10V		+200		+100	nA
				V <sub>D</sub> = -10V, V <sub>S</sub> = -10V		-200		-200	
				V <sub>D</sub> = 10V, V <sub>S</sub> = -10V		+200		+100	
				V <sub>D</sub> = -10V, V <sub>S</sub> = -10V		-100		-100	
Drain On-Leakage Current	DG508A DG509A	I <sub>D(ON)</sub>	Sequence each switch on, V <sub>A_L</sub> = 0.8V, V <sub>A_H</sub> = 2.4V (Note 2)	V <sub>S(all)</sub> = V <sub>D</sub> = 10V		+200		+100	nA
				V <sub>S(all)</sub> = V <sub>D</sub> = -10V		-200		-100	
				V <sub>S(all)</sub> = V <sub>D</sub> = 10V		+100		+100	
				V <sub>S(all)</sub> = V <sub>D</sub> = -10V		-100		-100	
<b>LOGIC INPUT</b>									
Logic Input Current, Input Voltage High	I <sub>AH</sub>	V <sub>A_</sub> = 2.4V		-30		-30		μA	
		V <sub>A_</sub> = 15V		+30		+30			
Logic Input Current, Input Voltage Low	I <sub>AL</sub>	All V <sub>A_</sub> = 0V	V <sub>EN</sub> = 2.4V		-30		-30	μA	
			V <sub>EN</sub> = 0V		-30		-30		

**Note 2:** I<sub>D(ON)</sub> is leakage from driver into on switch.

**Note 3:** Off-isolation = 20log  $\frac{|V_S|}{|V_D|}$

V<sub>S</sub> = input to off switch,  
V<sub>D</sub> = output due to V<sub>S</sub>.

**Note 4:** Electrical characteristics (such as on-resistance) change when power supplies other than ±15V are used.

**Note 5:** For designs requiring single 5V or dual ±5V operation, refer to Maxim's improved MAX338 and MAX339. Minimum operating voltage for DG508ADY/MY and DG509ADY/MY is ±9V.

# Monolithic CMOS Analog Multiplexers

**DG508A/DG509A**

## Pin Configurations



## Pin Descriptions

PIN		NAME	FUNCTION
DG508A DIP/SO	DG509A DIP/SO		
1, 15, 16	—	A0, A2, A1	Address Input
—	1, 16	A0, A1	Address Input
2	2	EN	Enable
3	3	V-	Negative-Supply Voltage Input
4-7	—	S1-S4	Analog Inputs, Bidirectional
—	4-7	S1A-S4A	Analog Inputs, Bidirectional
8	—	D	Analog Outputs, Bidirectional
—	8, 9	DA, DB	Analog Outputs, Bidirectional
9-12	—	S8-S5	Analog Inputs, Bidirectional
—	10-13	S4B-S1B	Analog Inputs, Bidirectional
13	14	V+	Positive-Supply Voltage Input
14	15	GND	Ground

## Functional Diagrams



# Monolithic CMOS Analog Multiplexers

## DG508A/DG509A

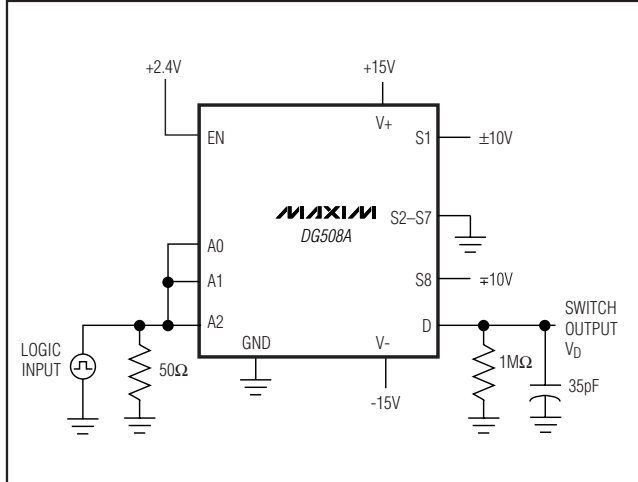


Figure 1a. Switching-Time Test Circuit

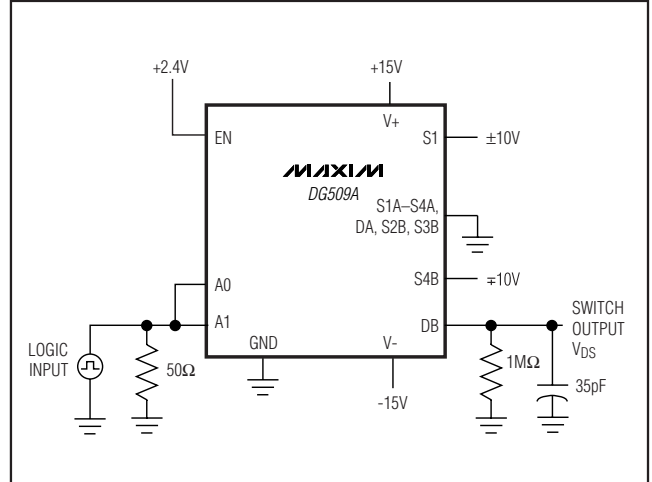


Figure 1b. Switching-Time Test Circuit



Figure 2a. DG508A Enable-Time Test Circuit



Figure 2b. DG509A Enable-Time Test Circuit

# Monolithic CMOS Analog Multiplexers

**DG508A/DG509A**

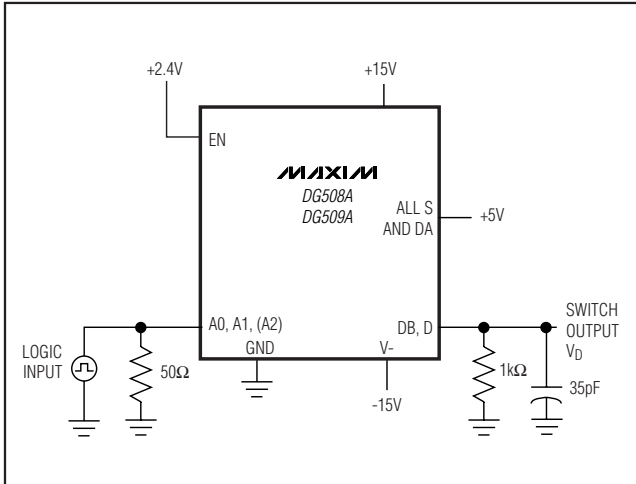


Figure 3. Break-Before-Make Test Circuit

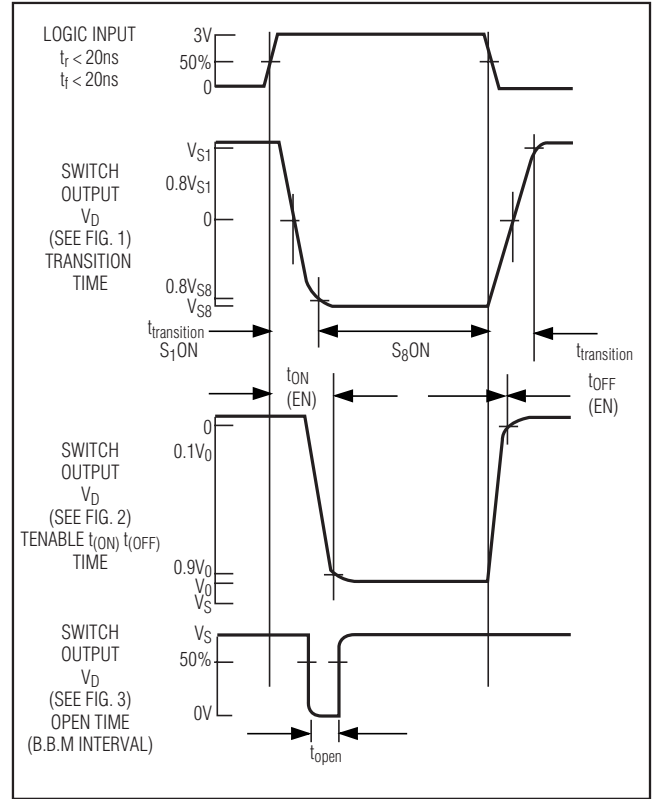


Figure 4. Timing Diagram for Figures 1, 2, and 3

**Table 1a. DG508A Truth Table**

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't care.

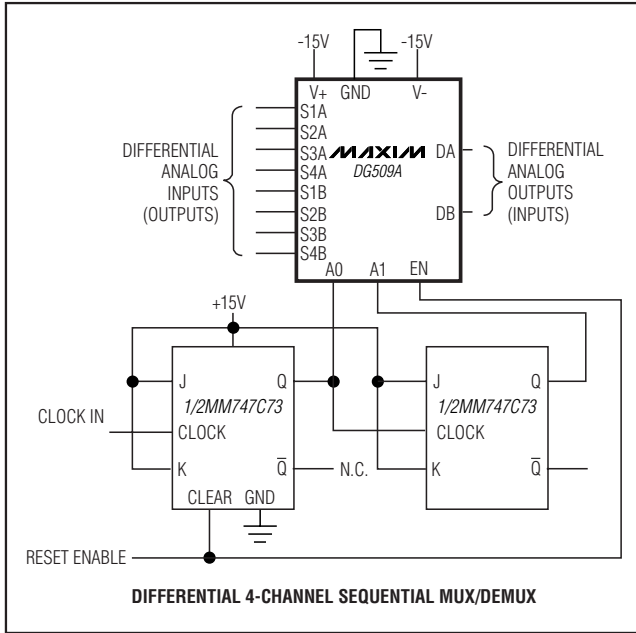
**Table 1b. DG509A Truth Table**

A1	A0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't care.

# Monolithic CMOS Analog Multiplexers

## Typical Operating Circuits (continued)



## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 Plastic DIP	P16-1	<a href="#">21-0043</a>
16 Wide SO	W16-2	<a href="#">21-0042</a>
16 Narrow SO	S16-5	<a href="#">21-0041</a>
16 CERDIP	J16-3	<a href="#">21-0045</a>

# Monolithic CMOS Analog Multiplexers

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	5/10	Updated the "Drain-Source On-Resistance" parameter for both the $T_A = +25^\circ\text{C}$ and $T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$ conditions.	2, 4
		Deleted the QFN package from the <i>Ordering Information</i> , <i>Absolute Maximum Ratings</i> , <i>Pin Configurations</i> , <i>Pin Descriptions</i> , and <i>Package Information</i> sections.	1, 2, 5, 8
		Added the DG508AMY/PR and DG509AMY/PR parts to the <i>Ordering Information</i> table.	1

DG508A/DG509A

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