THE DATASHEET OF

LE87251NQCT

Le87251

Worldwide ADSL2+ Dual Channel Line Driver BD870 Series

Data Sheet

June 2009

Document Number 129739

Features

- Fixed Voltage Gain Of 13
- 450 mA Peak Output Drive Capability
- ±5 V to ±12 V Dual Supplies Or 10 V to 24 V Single Supply
- 44 V_{p-p} Differential Output Into a 100 Ω Load
- 40.5 V_{p-p} Differential Output Into a 60 Ω Load
- Low-power Disable Mode For Each Driver
- 4 mA Per Amplifier Quiescent Supply Current
- -75 dBc THD With 1 MHz Signal Into a 60 Ω load
- 16-pin (4 mm x 4 mm) QFN Package
- RoHS Compliant

Applications

- Dual Port Full Rate ADSL2+ Line Drivers
- HDSL Line Drivers

Description

The Le87251 is a dual channel differential amplifier designed to drive full rate ADSL2+ signals with very low power dissipation. The Le87251 contains two pairs of wide band amplifiers designed with Zarlink's HV30 Bipolar SOI process for low power consumption in DSL systems. The amplifiers have an internal fixed gain, which helps to eliminate external feedback and gain setting resistors.

The drivers achieve better than -75 dB MTPR while driving a 1 MHz, 16Vp_p signal into a 60 Ω load. The amplifiers are enabled by forcing the ENAB/ENCD pins to ground. Leaving the ENAB/ENCD pins floating or forcing them high will disable the two amplifiers. The ENAB and ENCD pins are pulled up to an internal 2.5 V through on-chip 50 kΩ resistors.

Le87251 device is one of the most cost-effective and high performance line drivers for xDSL2+ applications.

Ordering Information

Le87251NQC16 pin QFN Green Pkg.Tray
Le87251NQCT16 pin QFN Green Pkg.Tape & Reel

The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.

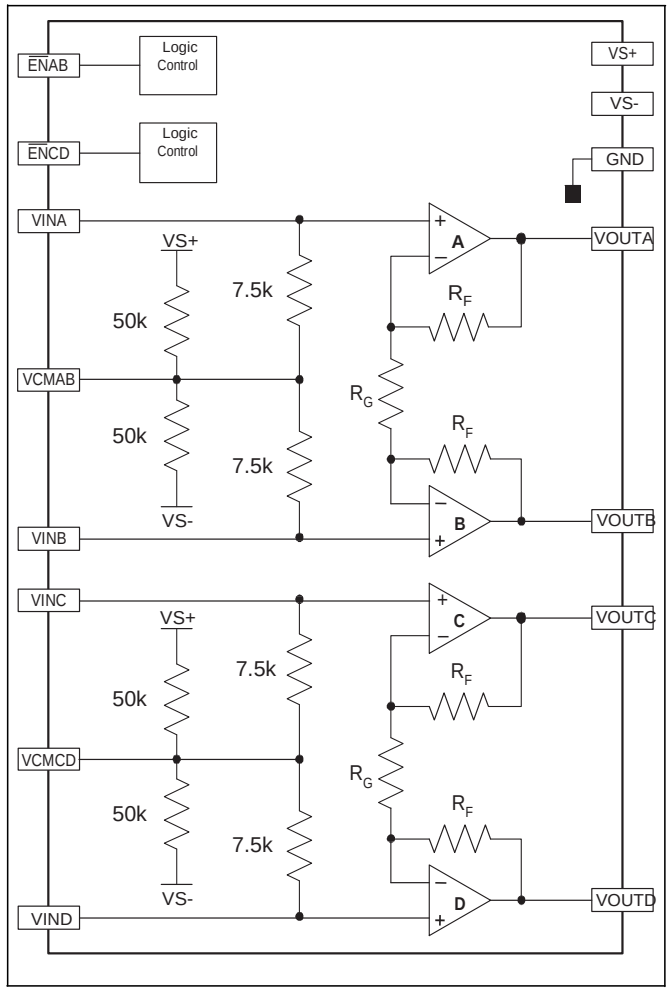

Figure 1 - Block Diagram

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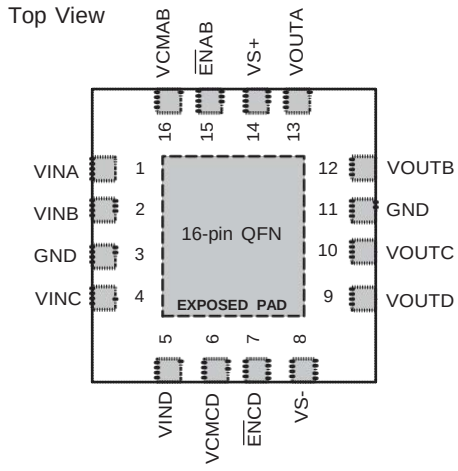
1.0 Pin Diagram



Notes:

1. Pin 1 is marked for orientation.
2. The Le87251 device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through thermal vias, for proper heat dissipation.

1.1 Pin Description

Pin Name	Type	Description	Note
ENAB	Input	DSL channel #1 enable/disable control pin	Reference Circuit 1
ENCD	Input	DSL channel #2 enable/disable control pin	Reference Circuit 1
VINA	Input	Amplifier A non-inverting input	Reference Circuit 2
VINB	Input	Amplifier B non-inverting input	Reference Circuit 2
VINC	Input	Amplifier C non-inverting input	Reference Circuit 2
VIND	Input	Amplifier D non-inverting input	Reference Circuit 2
VCMAB	Input	Bias voltage for amplifier A and B	
VCMCD	Input	Bias voltage for amplifier C and D	
VS+	Power	Positive power supply	
VS-	Power	Negative power supply	
GND	Ground	Ground connection	
VOUTA	Output	Amplifier A output	Reference Circuit 2
VOUTB	Output	Amplifier B output	Reference Circuit 2
VOUTC	Output	Amplifier C output	Reference Circuit 2
VOUTD	Output	Amplifier D output	Reference Circuit 2

Note 1: Amplifiers A and B comprise DSL channel #1. $\overline{\text{ENAB}}$ allows enable/disable control for DSL channel #1.

Note 2: Amplifiers C and D comprise DSL channel #2. $\overline{\text{ENCD}}$ allows enable/disable control for DSL channel #2.

Note 3: Reference circuits 1 and 2 are shown in Figure 2.

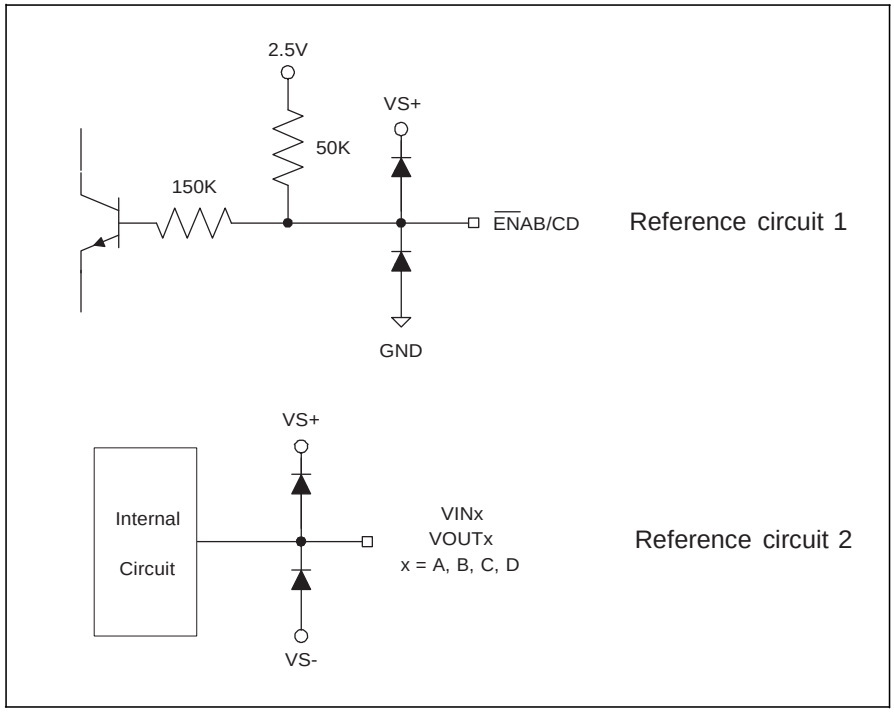


Figure 2 - Reference Circuit

2.0 Applications

The Le87251 integrates two sets of high-power line driver amplifiers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with signals up to 10 MHz with low signal distortion. The driver can put out 20.5 dBm power level onto the telephone line and can drive 450 mA current, which exceeds the level required when using a transformer with 1:2 ratio.

2.1 Typical Application Circuit

A typical application interface circuit (one channel) is shown in Figure 3.

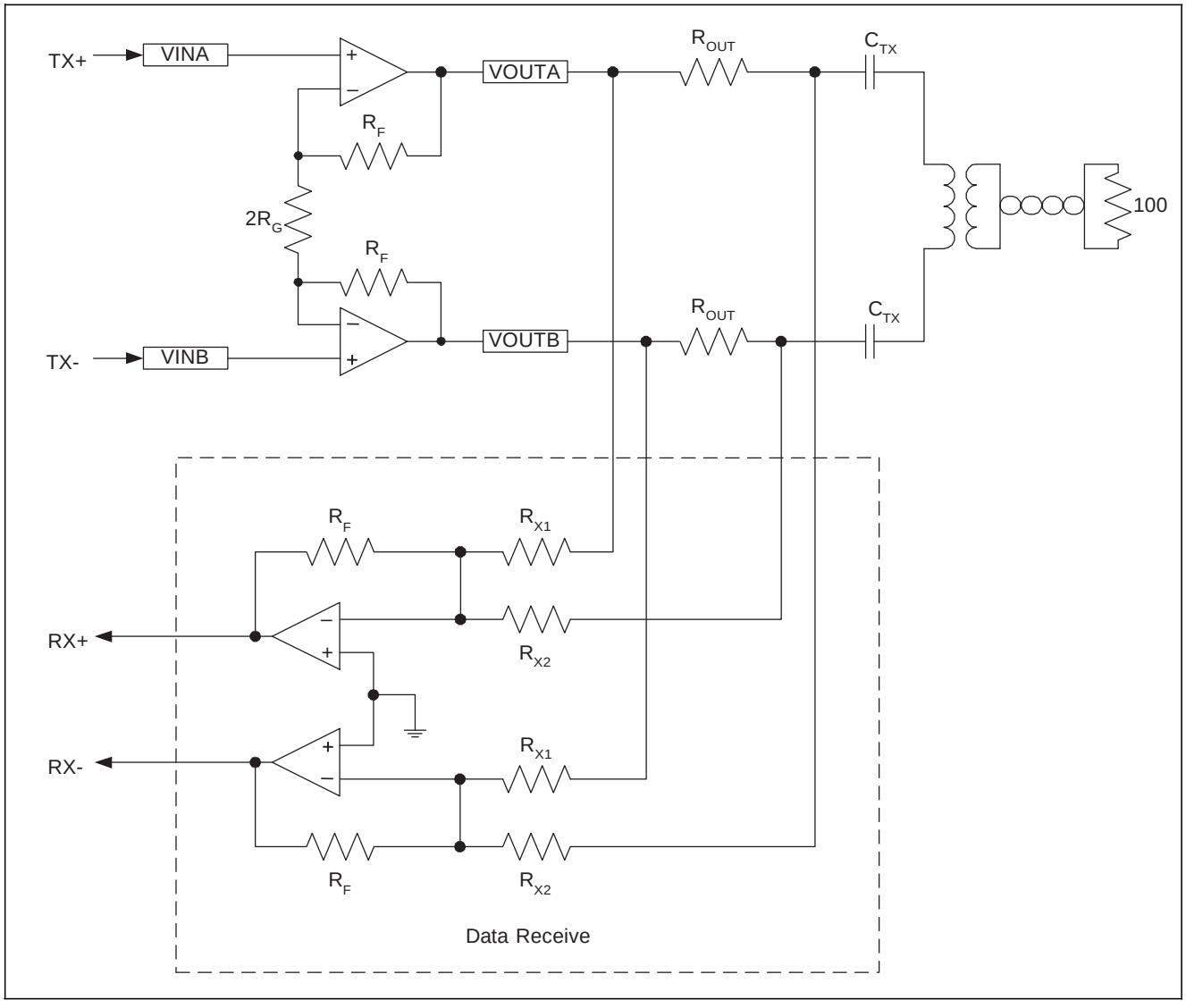


Figure 3 - Typical Application Interface Circuit

As shown in Figure 3 the amplifiers have identical positive gain connections with common-mode rejection. Any DC input errors are duplicated and create common-mode rather than differential line errors.

2.1.1 Component Values for Typical Application

Item	Quantity	Type	Value	Tolerance	Rating
R_{OUT}	2	SMT	49.9 Ω	1%	1/16 W
C_{TX}	2	X7R	0.22 µF	10%	50V

Table 1 - Parts List for Typical Application Circuit

2.1.2 Input Considerations

The driving source impedance should be less than 100 nH to avoid any ringing or oscillation. This inductance is equivalent to about 4" of unshielded wiring, or 6" of unterminated transmission line. Normal high-frequency construction obviates any such problem.

2.1.3 Output Driving Considerations

While the drive amplifiers can output in excess of 450 mA peak, the internal metallization is not designed to carry more than 100 mA of steady DC current and there is no current limit mechanism. The device can safely drive sinusoidal currents of 2 x 100 mArms, or 200 mArms. This current is more than that required to drive line impedance to large output levels, but output short circuits can not be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is not recommended.

The amplifiers are sensitive to capacitive loading. More than 100pF may cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

When in power down mode, several volts of differential voltage may appear across the line driver outputs. If a DC current path exists between the two outputs, a large DC current can flow from the positive supply rail to the negative supply rail through the outputs. To avoid DC current flow, the most effective solution is to place DC blocking capacitors in series at the output, as shown in the typical application circuit.

2.1.4 Power Supplies and Component Placement

The power supplies should be well bypassed close to the Le87251 device. A 2.2 µF tantalum capacitor and a 0.1 µF ceramic capacitor for each supply is recommended. The ground terminal of the positive and negative bypass capacitors should be connected to each other directly and then returned to circuit ground to prevent ground current loops.

The Le87251 can also be powered from a single positive voltage supply. When operating in this mode, the VS+ pin is connected to the positive supply. The VS- pin is connected to GND.

2.1.5 Stability

The Le87251 features improved frequency compensation for all applications, allowing stable operation at very low power levels and eliminating any need for external “snubber” circuit. Differential circuits, such as ADSL line driver applications, can be especially prone to common-mode oscillation. The Le87251 is specifically compensated to eliminate this type of instability and allows for reliable operation even at very low power levels.

2.2 Cable Termination Technique

There are various techniques available. Figure 4 shows a passive termination technique. Figure 5 shows an active termination technique. A quick comparison of the reduction in voltage and power requirements for the driver with passive or active termination is shown in Table 2.

The output impedance and the voltage gain of the circuit in Figure 5 are shown in the following equations.

$$Z_{OUT} = K \bullet R_{BM}$$

$$\frac{V_O}{V_{IN}} = \frac{RD(P2)}{2(RD(G) - RD(P1))}$$

where

Z_{OUT} is the output impedance.

$$K = \frac{1}{1 - \frac{RD(P1)}{RD(G)}}$$

And the resistor dividers are defined as following

$$RD(P1) = \frac{RP1}{RP1 + RP2}$$

$$RD(P2) = \frac{RP2}{RP1 + RP2}$$

$$RD(G) = \frac{RG}{RG + RF}$$

And V_O/V_{IN} represents the voltage gain.

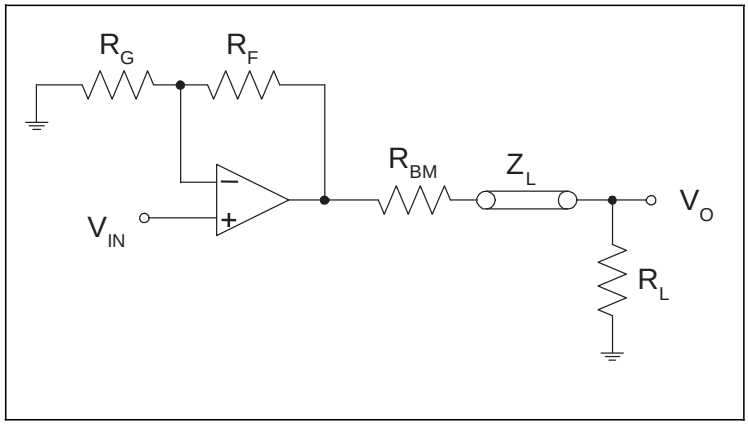


Figure 4 - Passive Termination Technique

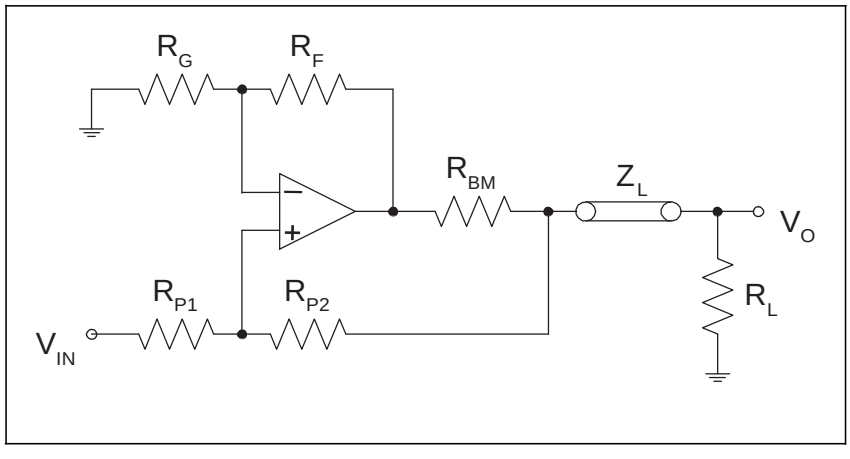


Figure 5 - Active Termination Technique

Passive Termination	Active Termination
16.5 V_{P-P} into a 100 Ω line	16.5 V_{P-P} into a 100 Ω line
$V_{OUT\ DRIVER} = V_{RBM} + V_{RLOAD}$	$V_{OUT\ DRIVER} = V_{RBM} + V_{RLOAD}$
RBM = R_{LOAD}	RBM = $R_{LOAD}/5$
$V_{RBM} = V_{RLOAD}$	$V_{RBM} = V_{RLOAD}/5$
$V_{OUT\ DRIVER}$ = 33.52 V	$V_{OUT\ DRIVER}$ = 20.11 V
V_{SUPPLY} = 37.52 V	V_{SUPPLY} = 24.11 V
I_{OUT} = 31.6 mA	I_{OUT} = 31.6 mA
$P_{OUT\ DRIVER} = V_{SUPPLY} * I_{OUT}$ = 1.185 W (plus quiescent power)	$P_{OUT\ DRIVER} = V_{SUPPLY} * I_{OUT}$ = 0.714 W (plus quiescent power)

Table 2 - Passive and Active Termination Comparison

2.3 Line Driver Protection

High voltage transients such as lightning can appear on the telephone lines. Transient protection devices should be used to absorb the transient energy and clamp the transient voltages. However, large transient voltages can still couple to the primary side of the transformer. As shown in Reference Circuit 2, the outputs of the Le87251 incorporate on-chip circuitry that clamps the output voltage to no more than a diode drop beyond either rail. No external diodes immediately at the output of the amplifiers are required. As shown in Figure 6, the series output termination resistors limit the current going into the line driver and internal clamps, thus these termination resistors should be specified at 0.5 W. The actual protection scheme may vary depending on the type of data transformer used and the line protection components used in the front of the data transformer.

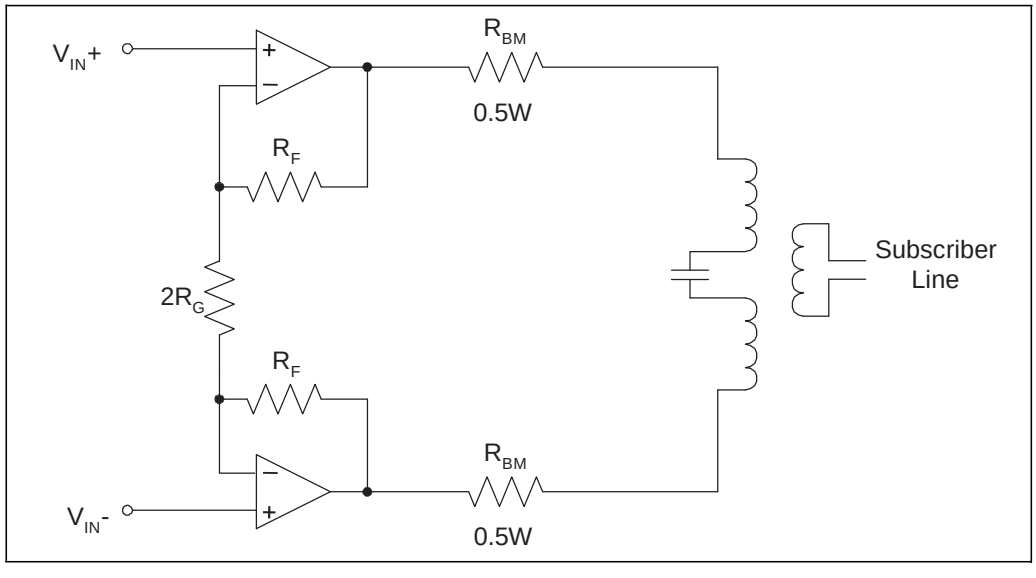


Figure 6 - Line Driver Protection

A large DC voltage can develop between the line driver outputs during system turn-on when the AFE has not been reset or when the line driver is disabled. Figure 6 shows an AC coupling capacitor between the two line driver outputs. This AC coupling capacitor prevents large DC current from flowing from one output of the line driver to another.

3.0 Absolute Maximum Ratings

Stresses above the values listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	$-65 \leq T_A \leq +150°C$
Operating Ambient Temperature	$-40 \leq T_A \leq +85°C$
Operating Junction Temperature (See Notes 1 and 2)	$-40 \leq T_A \leq +150°C$
VS+ to VS- Supply Voltage	−0.3 V to 30 V
VS+ with respect to GND	−0.3 V to 30 V
VS- with respect to GND	−30 V to +0.3 V
Driver inputs VINA/B/C/D	VS- to VS+
Control inputs $\overline{\text{ENAB}}$/$\overline{\text{ENCD}}$ with respect to GND	−0.3 V to 6 V
Maximum current on any input	10 mA
Maximum current at amplifier output (DC continuous)	100 mA
ESD Immunity (Human Body Model)	JESD22 Class 2 compliant
ESD Immunity (Charge Device Model)	JESD22 Class IV compliant

Note: Continuous operation above 145°C junction temperature may degrade device reliability.

3.1 Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.Please refer to the *QFN Package* application note, available from http://www.zarlink.com, for layout and heat sinking guidelines.

3.2 Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 Table 4-2 for recommended peak soldering temperature and Table 5-2 for the recommended solder reflow temperature profile.

4.0 Operating Ranges

Zarlink guarantees the performance of this device over commercial (0°C to 70°C) and industrial (−40°C to 85°C) temperature ranges by conducting electrical characterization over each range and by conducting a single insertion production test coupled with periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Ambient temperature	-40°C to +85°C
VS+ with respect to GND	+12 V ± 5%
VS- with respect to GND	-12 V ± 5%
Single battery operation, VS+ with respect to GND (VS- to GND)	+24V ± 5%

5.0 Device Specifications

Typical Conditions: VS = ±12V, RL = 65Ω, unless otherwise specified, T_A = 25°C.

Min/Max Parameters: T_A = −40 to +85°C

Amplifiers are tested separately.

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Supply Current Characteristics						
IS+ (Full IS)	Positive Supply Current per Amplifier	All outputs at 0V, $\overline{ENAB}$ = $\overline{ENCD}$ = 0V	3.75	4.0	5.3	mA
IS- (Full IS)	Negative Supply Current per Amplifier	All outputs at 0V, $\overline{ENAB}$ = $\overline{ENCD}$ = 0V	-5.1	-3.8	-3.0	mA
IS+ (power down)	Positive Supply Current per Amplifier	All outputs at 0V, $\overline{ENAB}$ = $\overline{ENCD}$ = 5V		0.2	0.4	mA
IS- (power down)	Negative Supply Current per Amplifier	All outputs at 0V, $\overline{ENAB}$ = $\overline{ENCD}$ = 5V	-0.3	0.1		mA
IGND	GND Supply Current per Amplifier	All outputs at 0V		0.25		mA
Control Input (C0 and C1) Characteristics						
VIH	Input High Voltage	ENAB and ENCD inputs	1.6			V
VIL	Input Low Voltage	ENAB and ENCD inputs			0.8	V
IIH	Input High Current	ENAB = ENCD = 5V	5	20	40	µA
IIL	Input Low Current	ENAB = ENCD = 0V	-85	-50	-30	µA
Amplifier Input (VINx+ and VINx-) Characteristics						
VOS	Input Offset Voltage		-10	0	10	mV
ΔVOS	VOS mismatch		-5	0	5	mV
IB	Input Bias Current		-15		14	µA
ΔIB	IB Mismatch		-25	0	25	µA
VCM	Driver common mode voltage	pins VCMAB/CD floating, reference to VS-	0.475	0.5	0.525	|VS+| + |VS-|
ROL	Transimpedance[1]			5		MΩ

Table 3 - Electrical Specifications

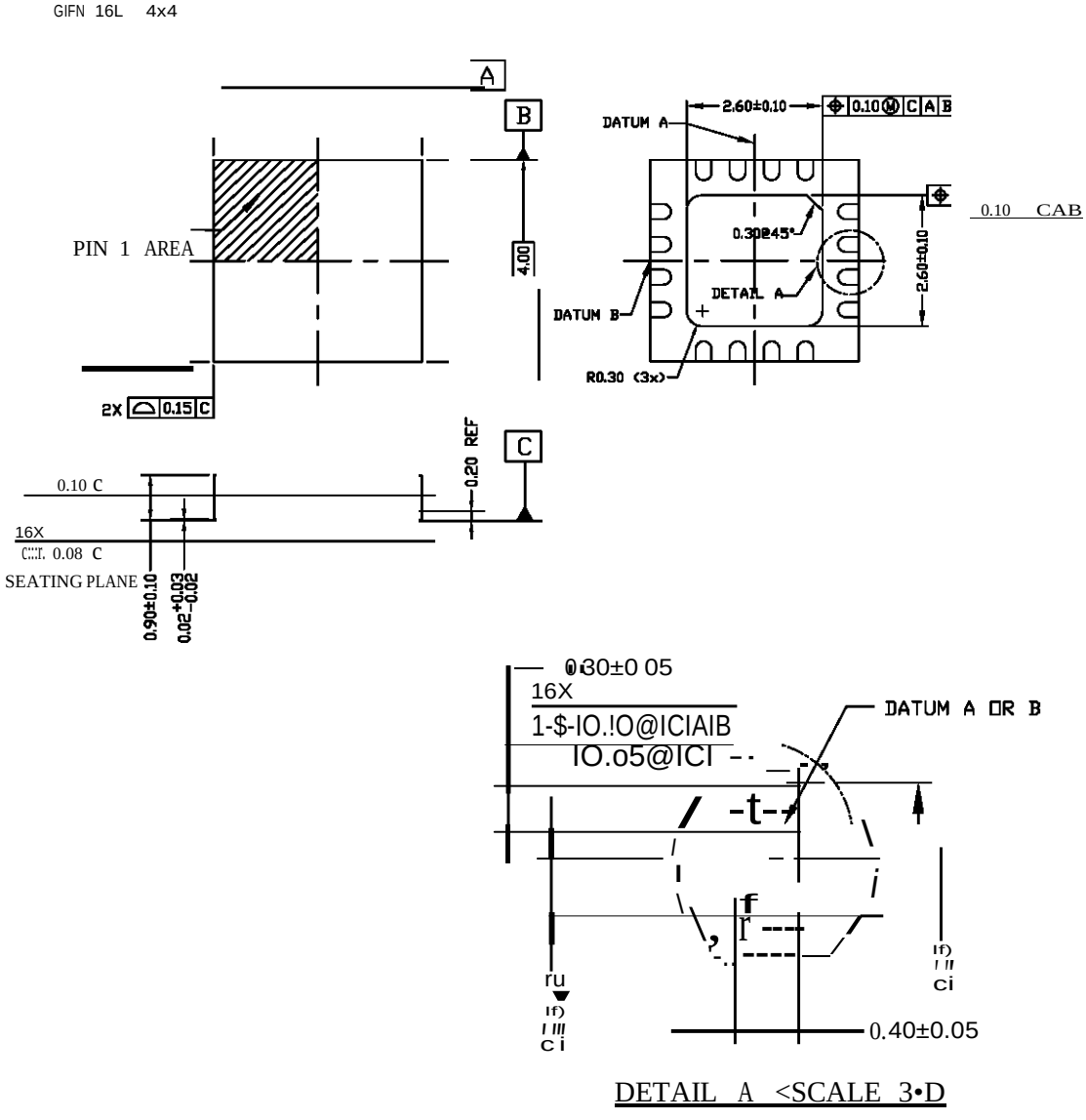
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
eN	Input Noise Voltage[1]			3.5		nV/ $\sqrt{Hz}$
iN	Input Noise Current[1]			13		pA/ $\sqrt{Hz}$
Amplifier Output (VOUT) Characteristics						
VOUT	Loaded Output Swing (RL Single-ended to GND)	RL = 100 Ω	±10.3	±11.1		V
		RL = 30 Ω (+)	10.1	10.7		V
		RL = 30 Ω (–)		-10.5	-10.1	V
IOUT	Output Current[1]	VOUT = 0.6 V, RL = 1 Ω		600		mA
Amplifier Dynamic Characteristics						
THD	Total Harmonic Distortion	f = 1 MHz, RL = 50 Ω, VOUT = 16 Vpp		-75		dBc
MTPR	Multi-Tone Power Ratio	26 kHz to 1.1 MHz, RL = 100 Ω, PLINE =20.4 dBm		-70		dBc
SR	Slew rate (single-ended)[1]	VOUT from -8 V to +8 V measured at ±4 V	200	400		V/µs
AV	Voltage Gain	VOUT = 16 Vpp, RL = 100 Ω	12.9	13.0	13.1	V/V

Note 1: This parameter is not tested in production. It is guaranteed by design and device characterization.

Table 3 - Electrical Specifications

6.0 Physical Dimensions

6.1 16-Pin QFN



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NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
ALL. DIMENSIONS ARE IN MIWMETERS " IN DEGREES

7.0 Revision History

7.1 Version 1 to Version 2

- Document is changed from “Preliminary Data Sheet” to “Data Sheet”.
- Added a note in Table 3 on page 10 and 11.

7.2 Version 2 to Version 3

- Updated the Absolute Maximum Rating table on page 9.

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