THE DATASHEET OF

SN74S00PSR

TEXAS INSTRUMENTS

SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00

SDLS025D – DECEMBER 1983 – REVISED MAY 2017

SNx400, SNx4LS00, and SNx4S00 Quadruple 2-Input Positive-NAND Gates

1 Features

- Package Options Include:
  - Plastic Small-Outline (D, NS, PS)
  - Shrink Small-Outline (DB)
  - Ceramic Flat (W)
  - Ceramic Chip Carriers (FK)
  - Standard Plastic (N)
  - Ceramic (J)
- Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package
- Inputs Are TTL Compliant; V_{IH} = 2 V and V_{IL} = 0.8 V
- Inputs Can Accept 3.3-V or 2.5-V Logic Inputs
- SN5400, SN54LS00, and SN54S00 are Characterized For Operation Over the Full Military Temperature Range of –55ºC to 125ºC

2 Applications

- AV Receivers
- Portable Audio Docks
- Blu-Ray Players
- Home Theater
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)

3 Description

The SNx4xx00 devices contain four independent, 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LS00DB	SSOP (14)	6.20 mm × 5.30 mm
SN7400D, SN74LS00D, SN74S00D	SOIC (14)	8.65 mm × 3.91 mm
SN74LS00NSR	PDIP (14)	19.30 × 6.35 mm
SNJ5400J, SNJ54LS00J, SNJ54S00J	CDIP (14)	19.56 mm × 6.67 mm
SNJ5400W, SNJ54LS00W, SNJ54S00W	CFP (14)	9.21 mm × 5.97 mm
SN54LS00FK, SN54S00FK	LCCC (20)	8.89 mm × 8.89 mm
SN7400NS, SN74LS00NS, SN74S00NS	SO (14)	10.30 mm × 5.30 mm
SN7400PS, SN74LS00PS	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Gate (Positive Logic)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2016) to Revision D **Page**

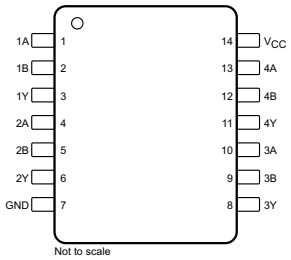
- Changed *Typical Application* Diagram see *Application and Implementation* section ... 1

Changes from Revision B (October 2003) to Revision C **Page**

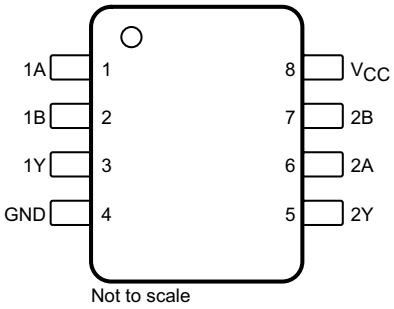
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed *Ordering Information* table to *Device Comparison Table*; see *Package Option Addendum* at the end of the data sheet ... 1
- Changed Package thermal impedance, $R_{\theta JA}$, values in *Thermal Information* table From: 86°C/W To: 90.9°C/W (D), From: 96°C/W To: 102.8°C/W (DB), From: 80°C/W To: 54.8°C/W (N), and From: 76°C/W To: 89.7°C/W (NS) ... 6

5 Pin Configuration and Functions

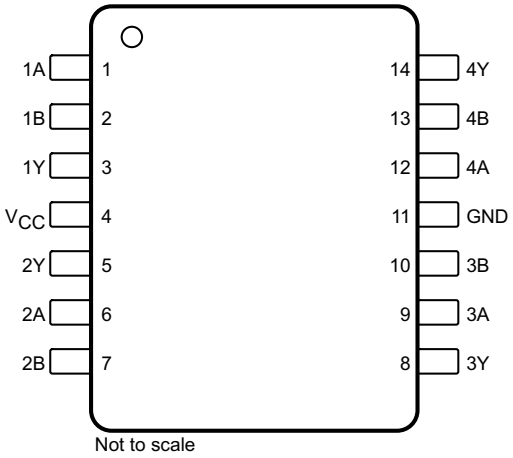
SN5400 J, SN54xx00 J and W, SN74x00 D, N, and NS, or SN74LS00 D, DB, N, and NS Packages
14-Pin CDIP, CFP, SOIC, PDIP, SO, or SSOP
Top View



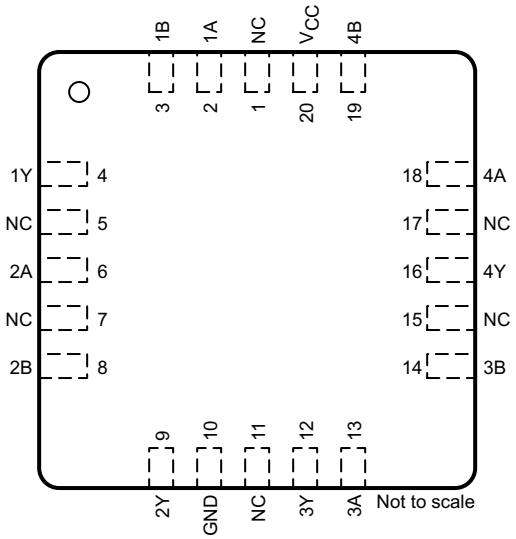
SN5400 W Package
14-Pin CFP
Top View



SN74xx00 PS Package
18-Pin SO
Top View



SN54xx00 FK Package
20-Pin LCCC
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
1A	1	1	1	2	I	Gate 1 input
1B	2	2	2	3	I	Gate 1 input
1Y	3	3	3	4	O	Gate 1 output
2A	4	6	6	6	I	Gate 2 input
2B	5	7	7	8	I	Gate 2 input
2Y	6	5	5	9	O	Gate 2 output
3A	10	—	9	13	I	Gate 3 input
3B	9	—	10	14	I	Gate 3 input

Pin Functions (continued)

PIN					I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
3Y	8	—	8	12	O	Gate 3 output
4A	13	—	12	18	I	Gate 4 input
4B	12	—	13	19	I	Gate 4 input
4Y	11	—	14	16	O	Gate 4 output
GND	7	4	11	10	—	Ground
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No connect
V_{CC}	14	8	4	20	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)			7	V
Input voltage	SNx400 and SNxS400		5.5	V
	SNx4LS00		7	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

6.2 ESD Ratings: SN74LS00

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance. ESD Tested on SN74LS00N package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN54xx00	4.5	5	5.5	V
		SN74xx00	4.75	5	5.25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage	SNx400, SN7LS400, and SNx4S00			0.8	V
		SN54LS00			0.7	
I_{OH}	High-level output current	SN5400, SN54LS00, and SN74LS00			–0.4	mA
		SNx4S00			–1	
I_{OL}	Low-level output current	SNx400			16	mA
		SN5LS400			4	
		SN7LS400			8	
		SNx4S00			20	

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	SN54xx00	–55		125	°C
		SN74xx00	0		70	

6.4 Thermal Information

THERMAL METRIC[1][2]		SN74LS00				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.9	102.8	54.8	89.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	53.3	42.1	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48	53.4	34.8	50.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.6	16.5	26.9	16.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.8	52.9	34.7	49.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics: SNx400

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN and I_I = –12 mA				–1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, and I_{OH} = –0.4 mA		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, and I_{OL} = 16 mA			0.2	0.4	V
I_I	V_{CC} = MAX and V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = MAX and V_I = 2.4 V				40	µA
I_{IL}	V_{CC} = MAX and V_I = 0.4 V				–1.6	mA
I_{OS}	V_{CC} = MAX	SN5400	–20		–55	mA
		SN7400	–18		–55	
I_{CCH}	V_{CC} = MAX and V_I = 0 V			4	8	mA
I_{CCL}	V_{CC} = MAX and V_I = 4.5 V			12	22	mA

6.6 Electrical Characteristics: SNx4LS00

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN and I_I = –18 mA				–1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, and I_{OH} = –0.4 mA		2.5	3.4		V
V_{OL}	V_{CC} = MIN and V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4	V
		I_{OL} = 8 mA (SN74LS00)		0.35	0.5	
I_I	V_{CC} = MAX and V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = MAX and V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = MAX and V_I = 0.4 V				–0.4	mA
I_{OS}	V_{CC} = MAX		–20		–100	mA
I_{CCH}	V_{CC} = MAX and V_I = 0 V			0.8	1.6	mA
I_{CCL}	V_{CC} = MAX and V_I = 4.5 V			2.4	4.4	mA

6.7 Electrical Characteristics: SNx4S00

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN and I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, and I_{OH} = –1 mA	2.5	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, and I_{OL} = 20 mA			0.5	V
I_I	V_{CC} = MAX and V_I = 5.5 V			1	mA
I_{IH}	V_{CC} = MAX and V_I = 2.7 V			50	µA
I_{IL}	V_{CC} = MAX and V_I = 0.5 V			–2	mA

Electrical Characteristics: SNx4S00 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OS}	V_{CC} = MAX	–40		–100	mA
I_{CCH}	V_{CC} = MAX and V_I = 0 V		10	16	mA
I_{CCL}	V_{CC} = MAX and V_I = 4.5 V		20	36	mA

6.8 Switching Characteristics: SNx400

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted). See Figure 2.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω and C_L = 15 pF		11	22	ns
t_{PHL}					7	15	

6.9 Switching Characteristics: SNx4LS00

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted). See Figure 2.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ and C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

6.10 Switching Characteristics: SNx4S00

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted). See Figure 2.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω and C_L = 15 pF		3	4.5	ns
			R_L = 280 Ω and C_L = 50 pF		4.5		
t_{PHL}	A or B	Y	R_L = 280 Ω and C_L = 15 pF		3	5	
			R_L = 280 Ω and C_L = 50 pF		5		

6.11 Typical Characteristics

C_L = 15 pF

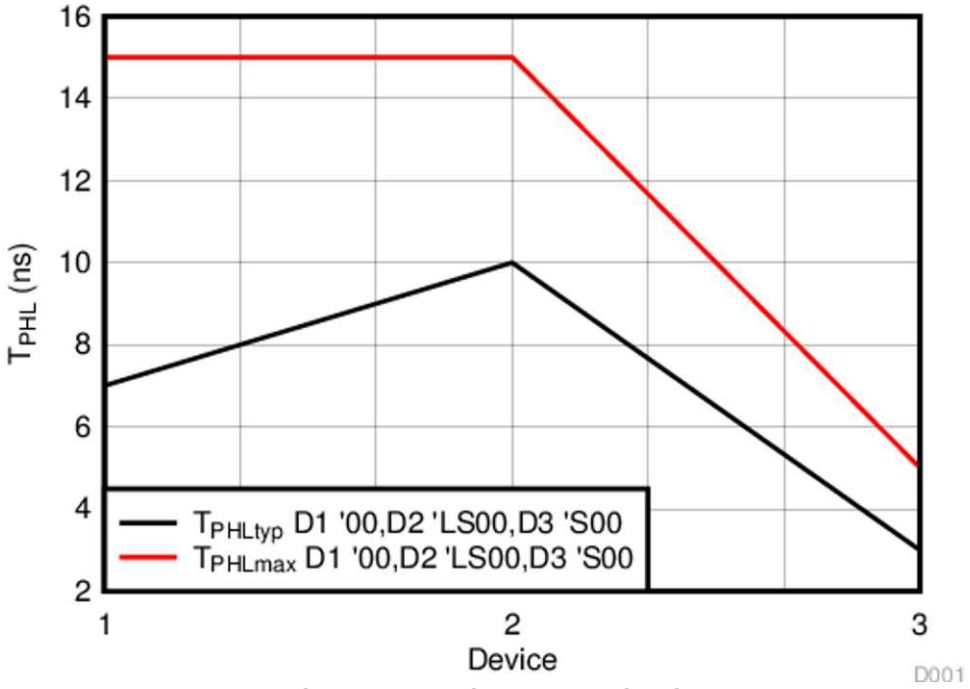
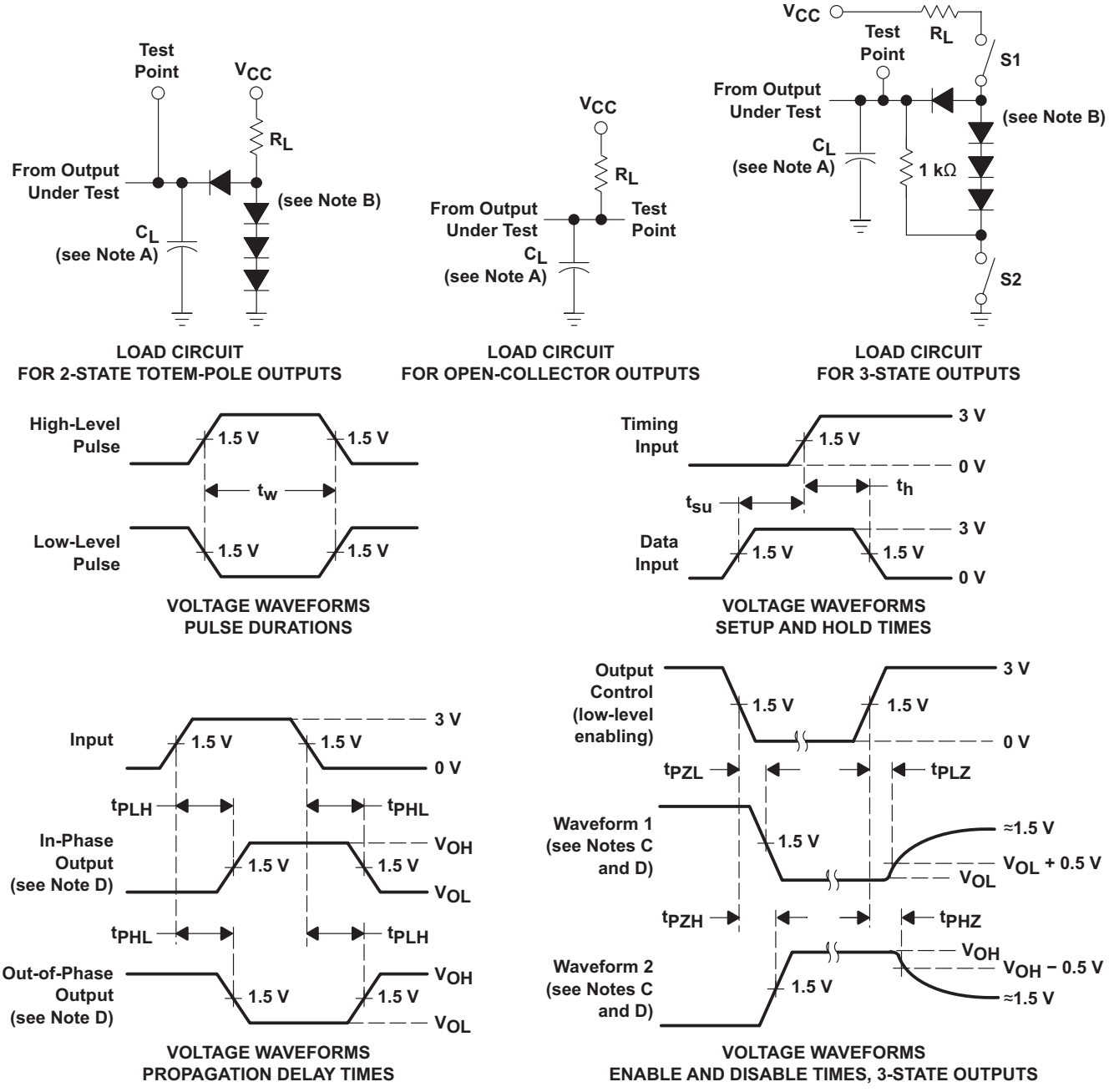


Figure 1. T_{PHL} (Across Devices)

7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Width



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\,\Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4xx00 devices are quadruple, 2-input NAND gates which perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

8.2 Functional Block Diagram

8.3 Feature Description

The operating voltage of SN74xx00 is from 4.75-V to 5.25-V V_{CC}. The operating voltage of SN54xx00 is from 4.5-V to 5.5-V V_{CC}. The SN54xx00 devices are rated from –55°C to 125°C whereas SN74xx00 device are rated from 0°C to 70°C.

8.4 Device Functional Modes

Table 1 lists the functions of the devices.

Table 1. Functional Table (Each Gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4xx00 devices are quadruple, 2-input NAND gate. A typical application of NAND gate can be as an error indicator as shown in Figure 3. If either of the sensor has an error, the error flag is high to indicate system error.

9.2 Typical Application

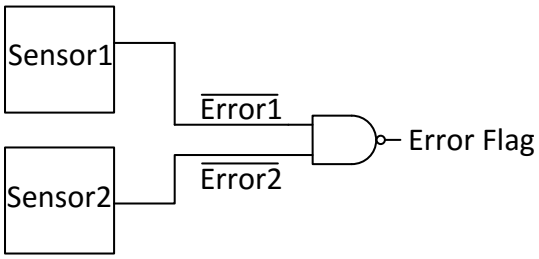


Figure 3. Typical Application Diagram

9.2.1 Design Requirements

These devices use BJT technology and have unbalanced output drive with I_{OL} and I_{OH} specified as per the *Recommended Operating Conditions*.

9.2.2 Detailed Design Procedure

- Recommended Input Conditions:
  - The inputs are TTL compliant.
  - Because the base-emitter junction at the inputs breaks down, no voltage greater than 5.5 V must be applied to the inputs.
  - Specified high and low levels: See V_{IH} and V_{IL} in *Recommended Operating Conditions*.
- Recommended Output Conditions:
  - No more than one output must be shorted at a time as per the *Electrical Characteristics: SNx400* for thermal stability and reliability.
  - For high-current applications, consider thermal characteristics of the package listed in *Thermal Information*.

Typical Application (continued)

9.2.3 Application Curve

C_L = 15 pF

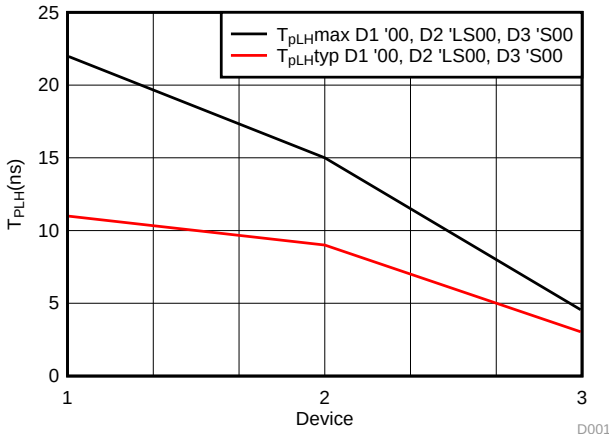


Figure 4. T_{PLH} (Across Devices)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions* for each of the SNx4LS00, SNx4S00, and SNx400 devices.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple V_{CC} pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic, devices inputs must never float.

Devices with multiple-emitter inputs (SN74 and SN74S series) need special care. Because no voltage greater than 5.5 V must be applied to the inputs (if exceeded, the base-emitter junction at the inputs breaks down), the inputs of these devices must be connected to the supply voltage, V_{CC}, through series resistor, R_S (see Figure 5). This resistor must be dimensioned such that the current flowing into the gate or gates, which results from overvoltage, does not exceed 1 mA. However, because the high-level input current of the circuits connected to the gate flows through this resistor, the resistor must be dimensioned so that the voltage drop across it still allows the required high level. Equation 1 and Equation 2 are for dimensioning resistor, R_S, and several inputs can be connected to a high level through a single resistor if the following conditions are met.

$$R_{S(min)} \frac{V_{CCP} \ 5.5 \ V}{1 \, mA} \quad (1)$$

$$R_{S(max)} \frac{V_{CC(min)} \ 2.4 \ V}{n \ I_{IH}} \quad (2)$$

where

- n = number of inputs connected
- I_{IH} = high input current (typical 40 µA)
- $V_{CC(min)}$ = minimum supply voltage, V_{CC}
- V_{CCP} = maximum peak voltage of the supply voltage, V_{CC} (about 7 V)

11.2 Layout Example

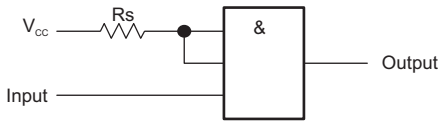


Figure 5. Series Resistor Connected to Unused Inputs of Multiple-Emitter Transistors

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Designing With Logic (SDYA009)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN5400	Click here	Click here	Click here	Click here	Click here
SN54LS00	Click here	Click here	Click here	Click here	Click here
SN54S00	Click here	Click here	Click here	Click here	Click here
SN7400	Click here	Click here	Click here	Click here	Click here
SN74LS00	Click here	Click here	Click here	Click here	Click here
SN74S00	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/00104BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00104BCA	Samples
JM38510/00104BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00104BDA	Samples
JM38510/07001BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07001BCA	Samples
JM38510/07001BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07001BDA	Samples
JM38510/30001B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30001B2A	Samples
JM38510/30001BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30001BCA	Samples
JM38510/30001BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30001BDA	Samples
JM38510/30001SCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30001S CA	Samples
JM38510/30001SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30001S DA	Samples
M38510/00104BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00104BCA	Samples
M38510/00104BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00104BDA	Samples
M38510/07001BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07001BCA	Samples
M38510/07001BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07001BDA	Samples
M38510/30001B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30001B2A	Samples
M38510/30001BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30001BCA	Samples
M38510/30001BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30001BDA	Samples
M38510/30001SCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30001S CA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/30001SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30001S DA	Samples
SN5400J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5400J	Samples
SN54LS00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS00J	Samples
SN54S00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S00J	Samples
SN7400D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7400	Samples
SN7400DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7400	Samples
SN7400N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7400N	Samples
SN7400NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7400N	Samples
SN74LS00D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples
SN74LS00DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples
SN74LS00DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples
SN74LS00DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples
SN74LS00DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples
SN74LS00N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS00N	Samples
SN74LS00NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS00N	Samples
SN74LS00NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS00	Samples
SN74LS00NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS00	Samples
SN74LS00PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS00PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples
SN74S00D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S00	
SN74S00DE4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S00	
SN74S00N	NRND	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S00N	
SNJ5400J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5400J	Samples
SNJ5400W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5400W	Samples
SNJ54LS00FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS00FK	Samples
SNJ54LS00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS00J	Samples
SNJ54LS00W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS00W	Samples
SNJ54S00FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 00FK	Samples
SNJ54S00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S00J	Samples
SNJ54S00W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S00W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN5400, SN54LS00, SN54LS00-SP, SN54S00, SN7400, SN74LS00, SN74S00 :

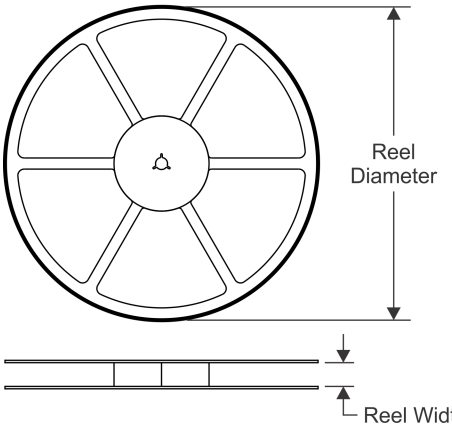
- Catalog: SN7400, SN74LS00, SN54LS00, SN74S00
- Military: SN5400, SN54LS00, SN54S00
- Space: SN54LS00-SP

NOTE: Qualified Version Definitions:

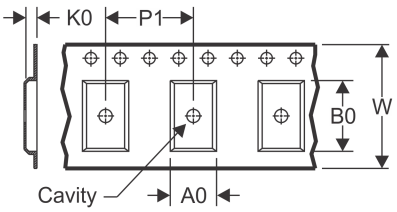
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

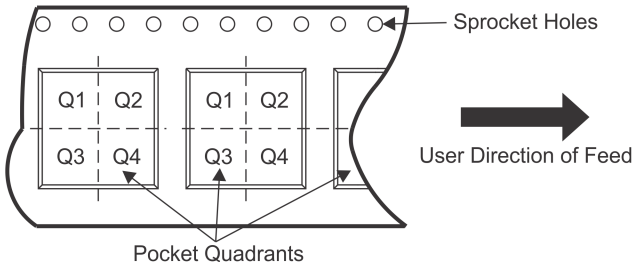


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

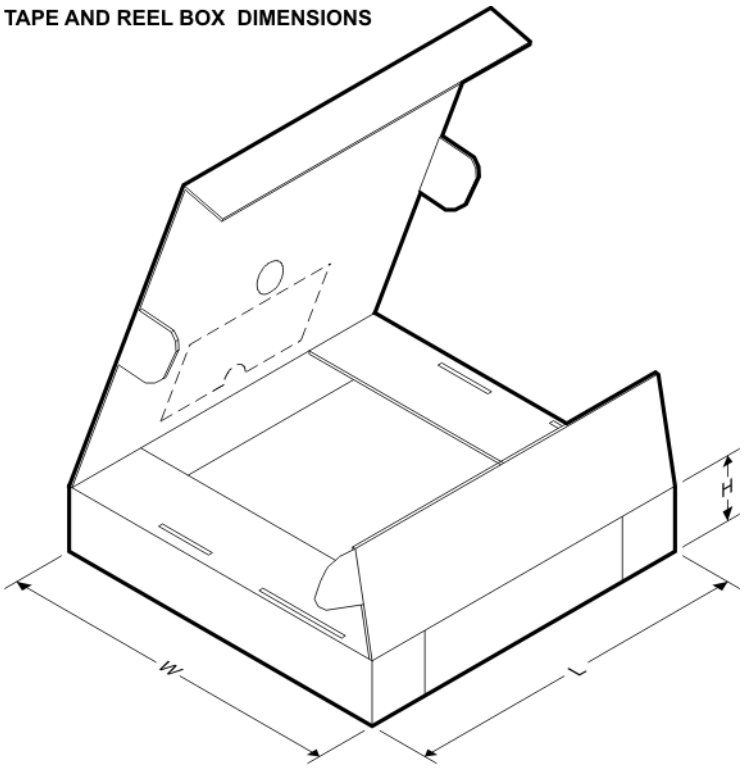
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS00DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS00NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

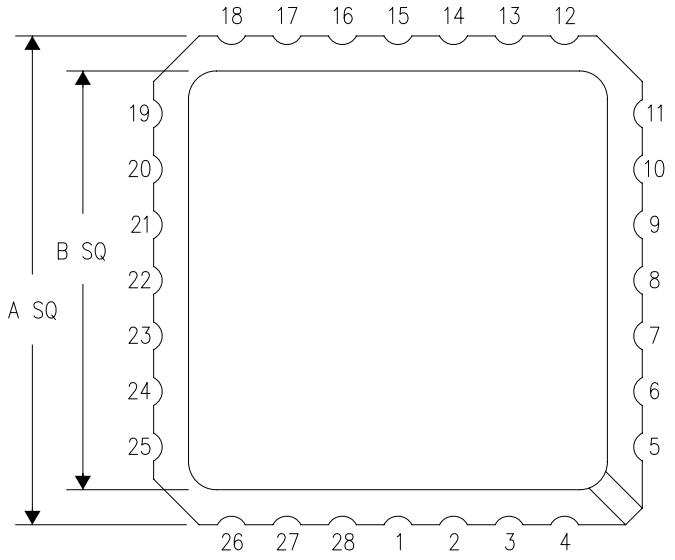


*All dimensions are nominal

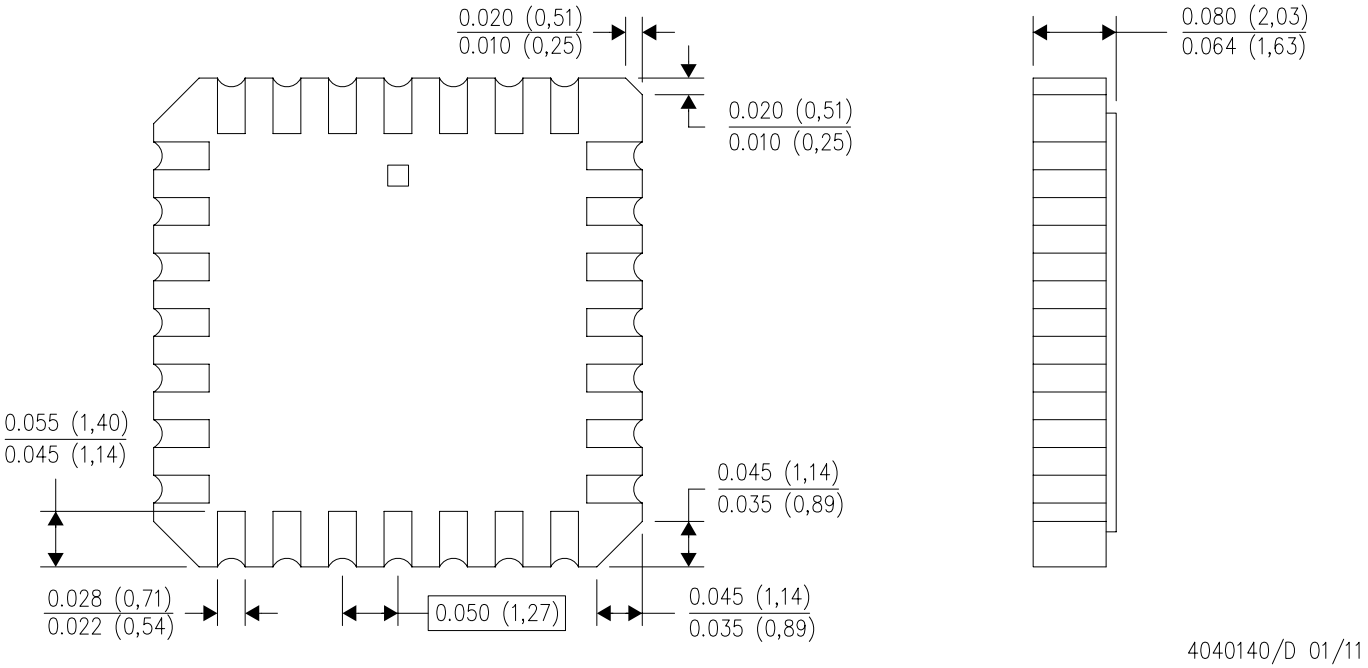
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS00DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS00NSR	SO	NS	14	2000	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



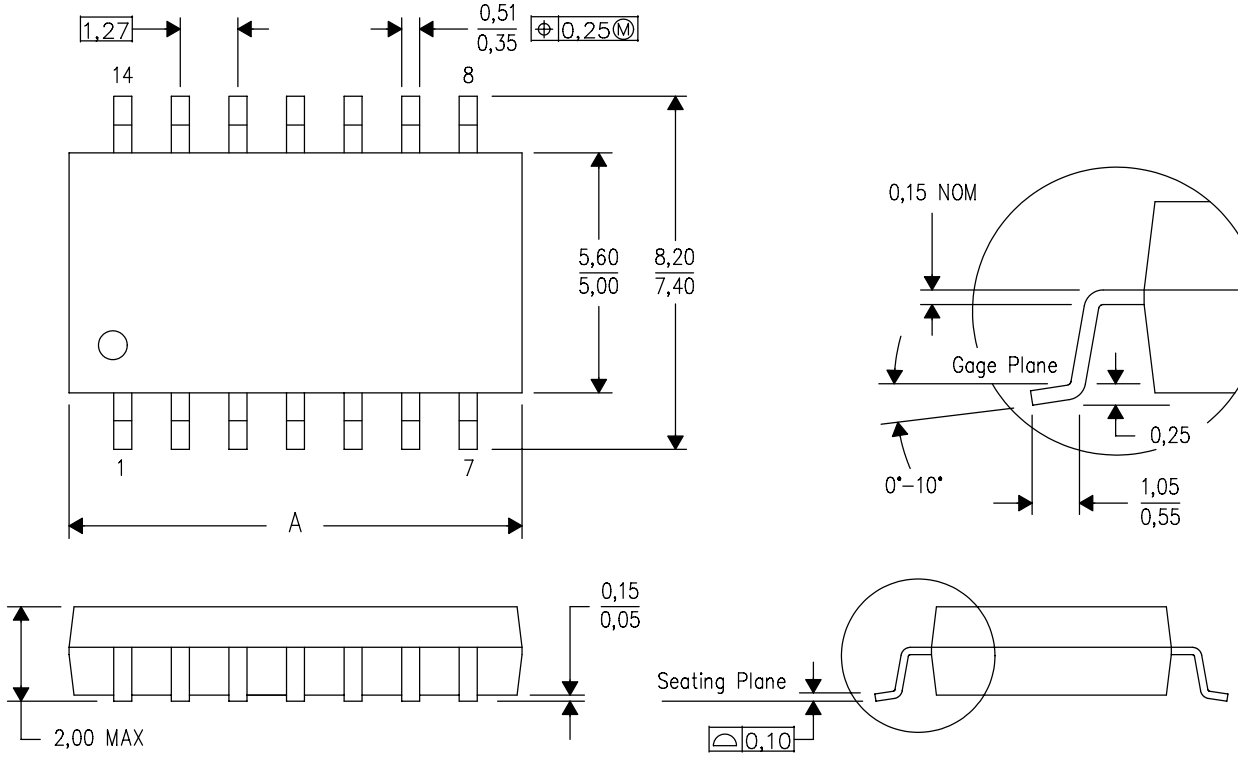
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

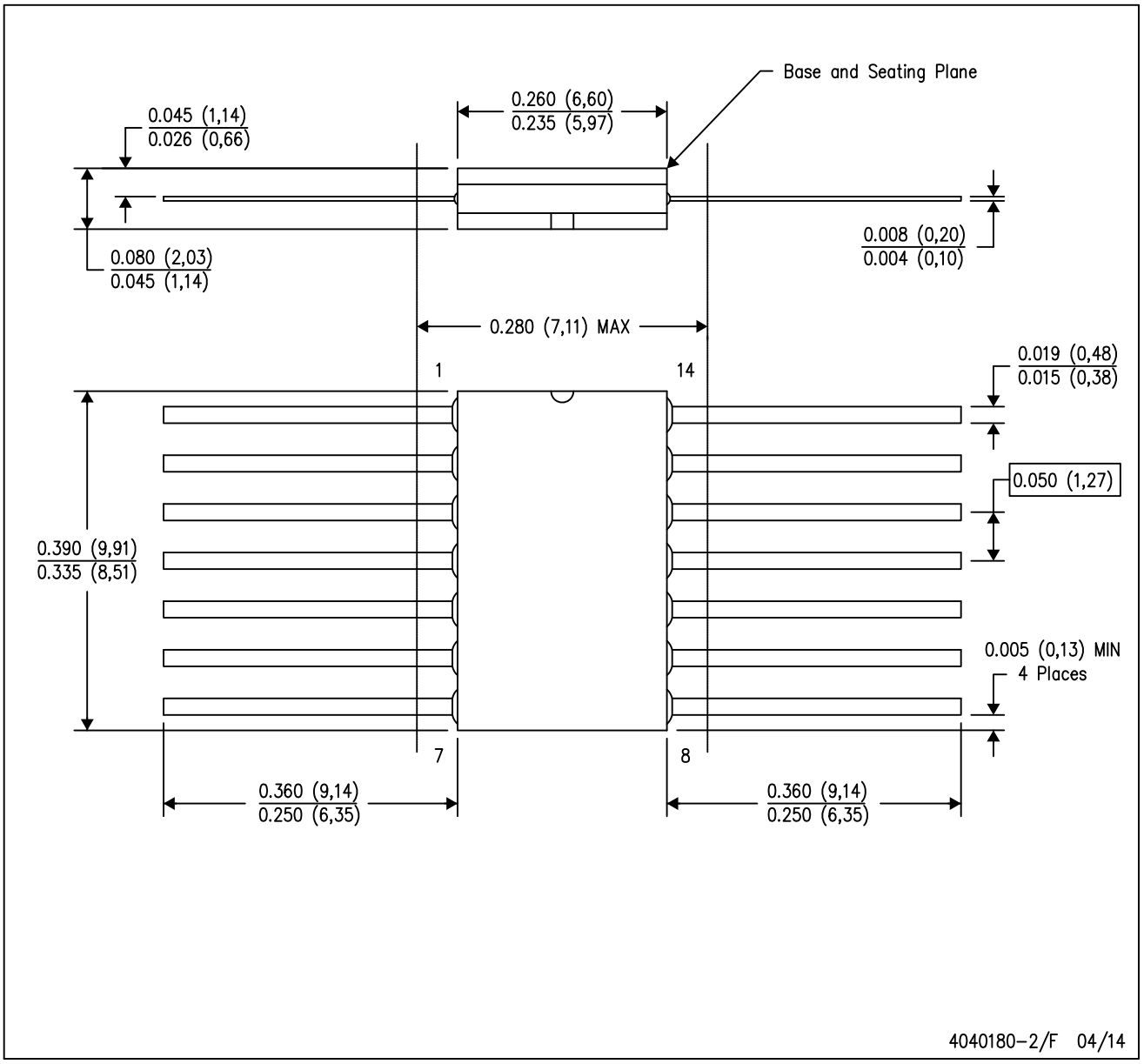


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

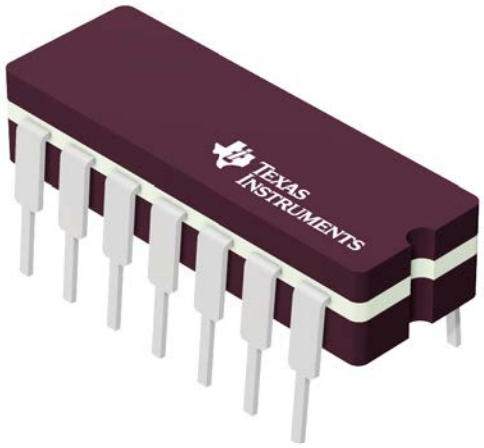


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

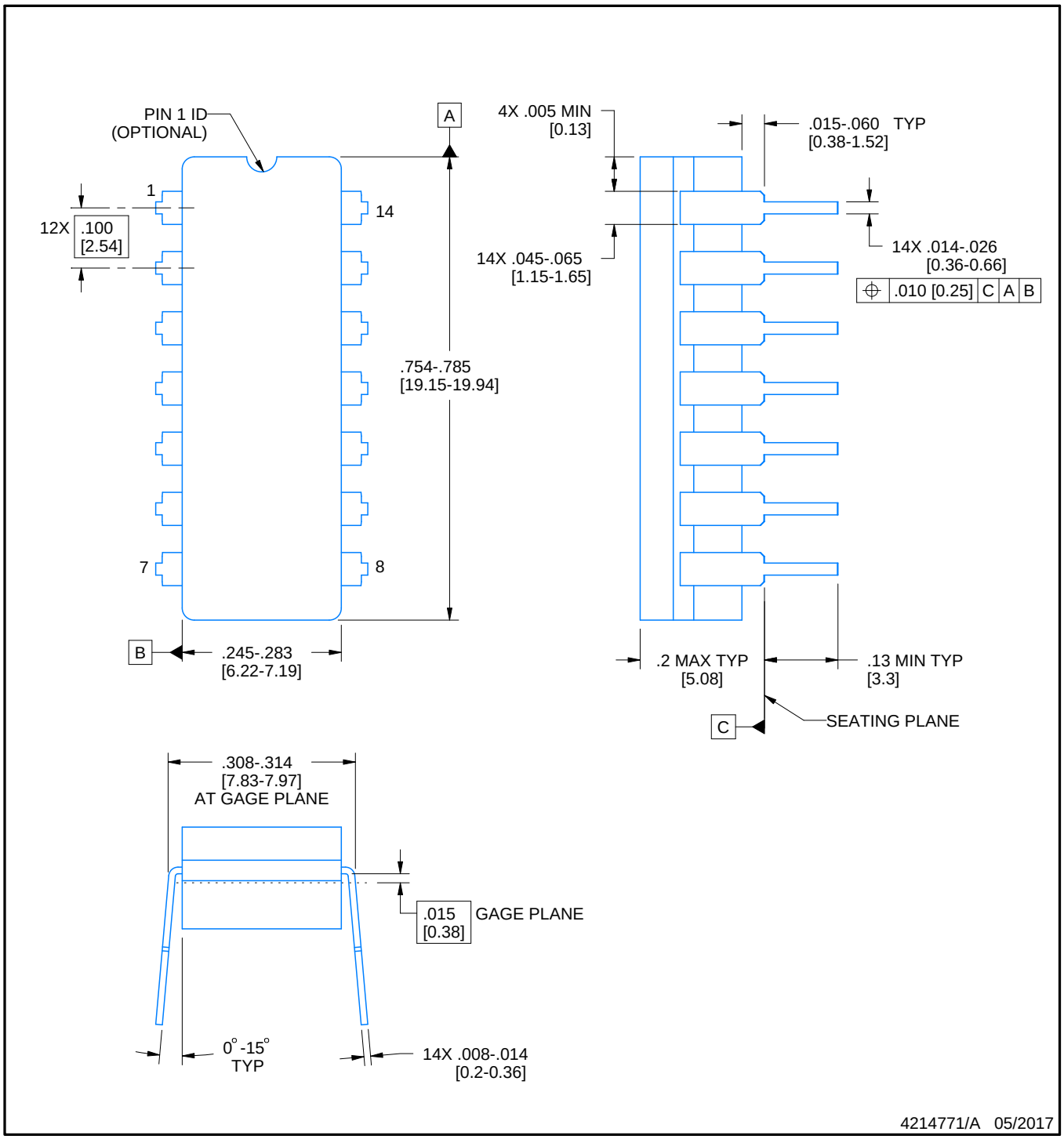
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

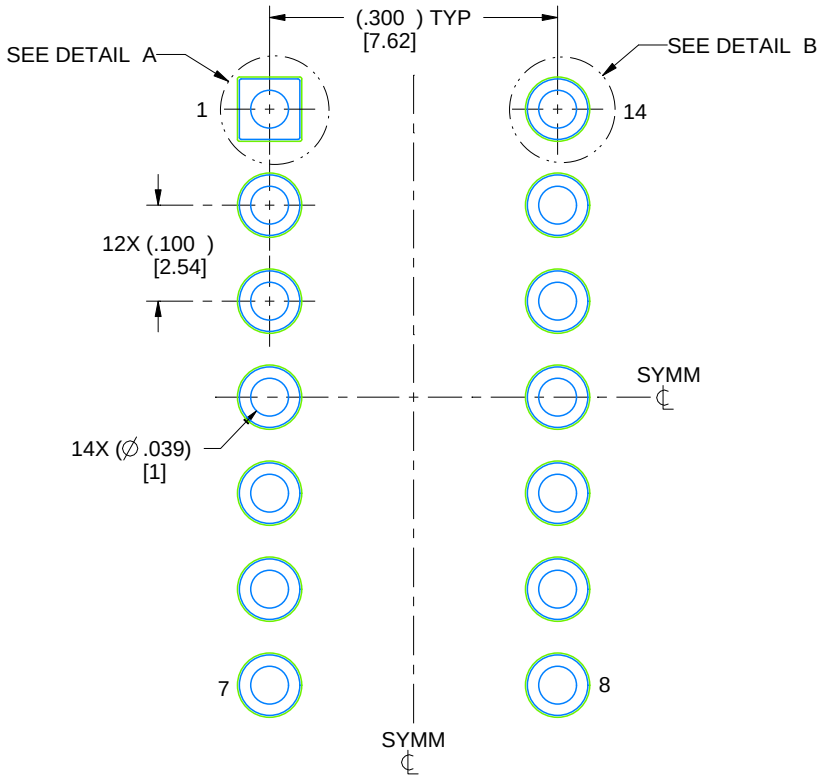
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

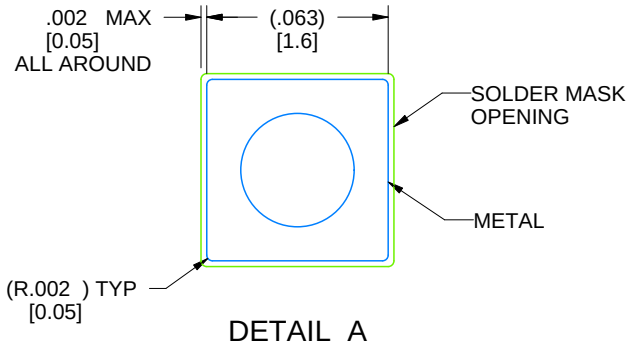
J0014A

CDIP - 5.08 mm max height

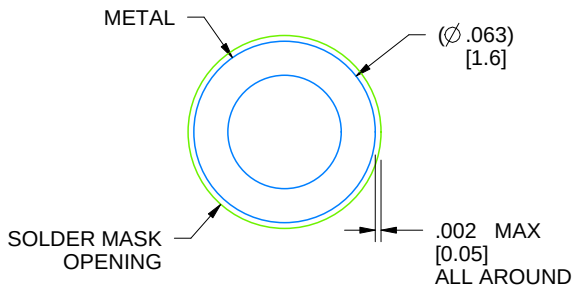
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



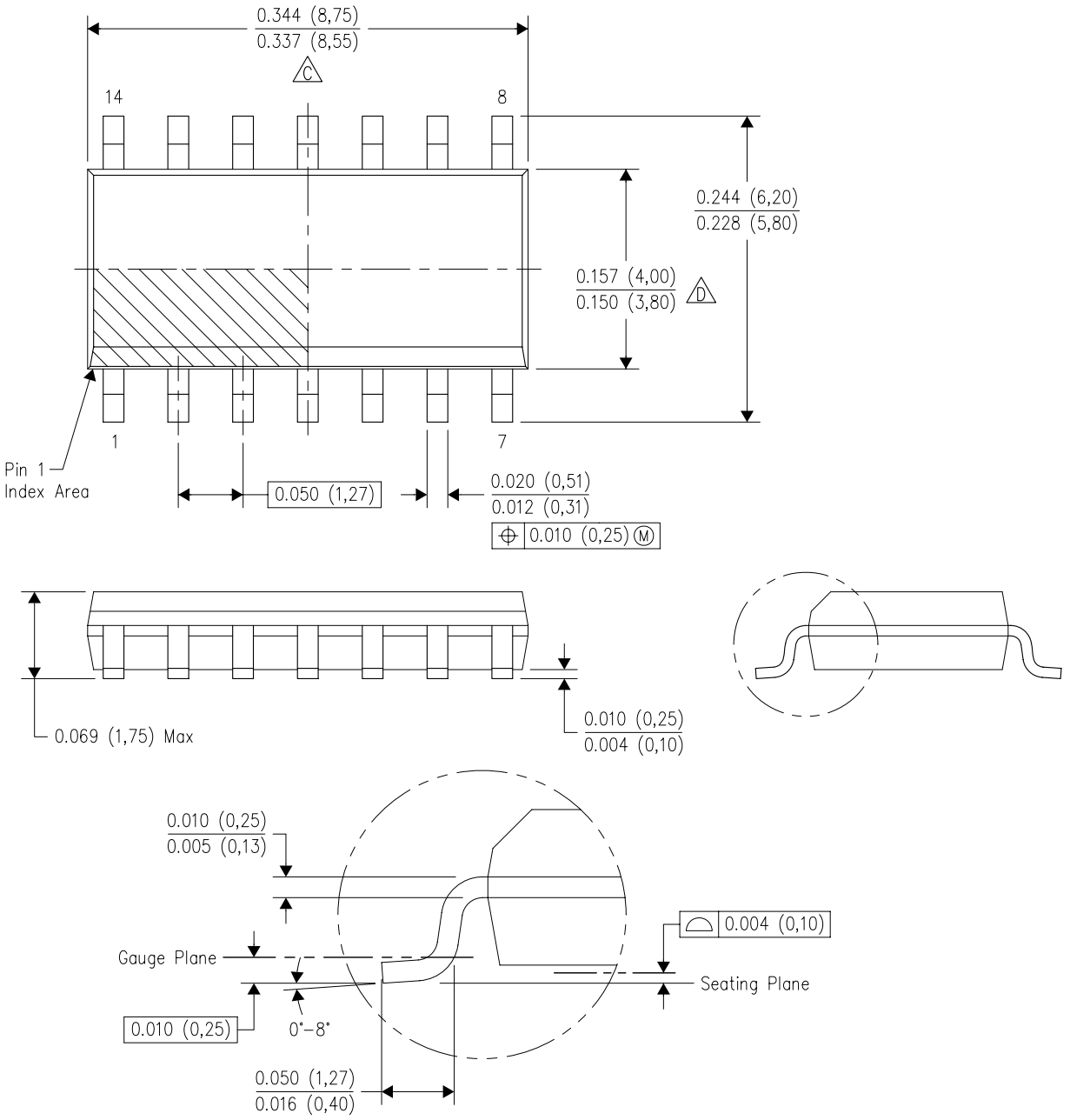
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

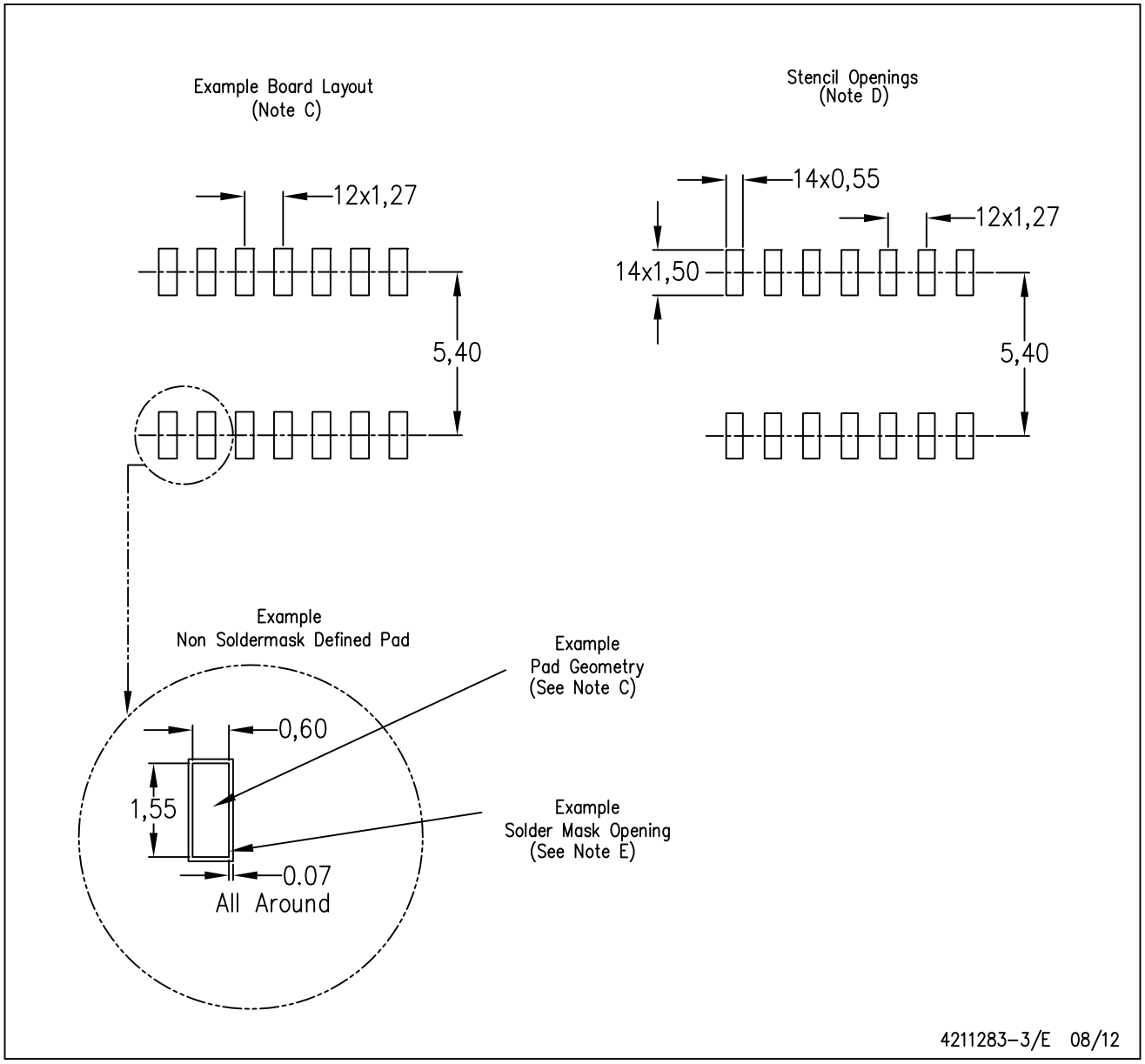
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

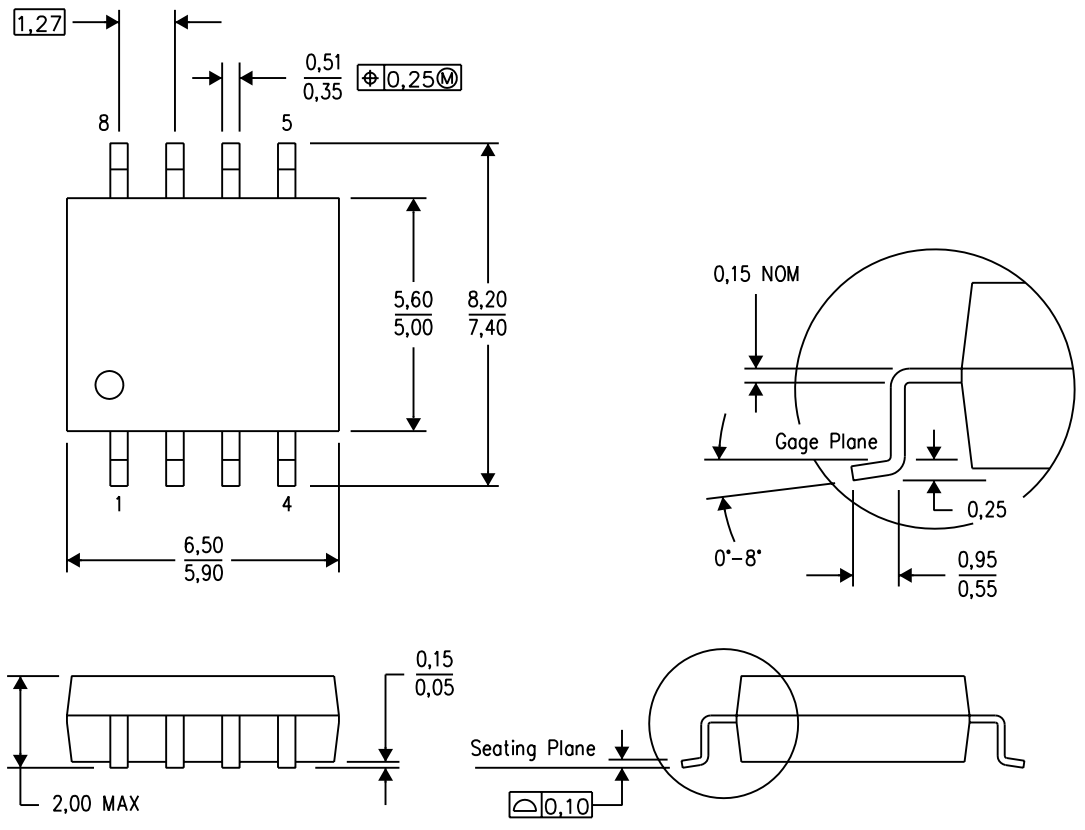
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

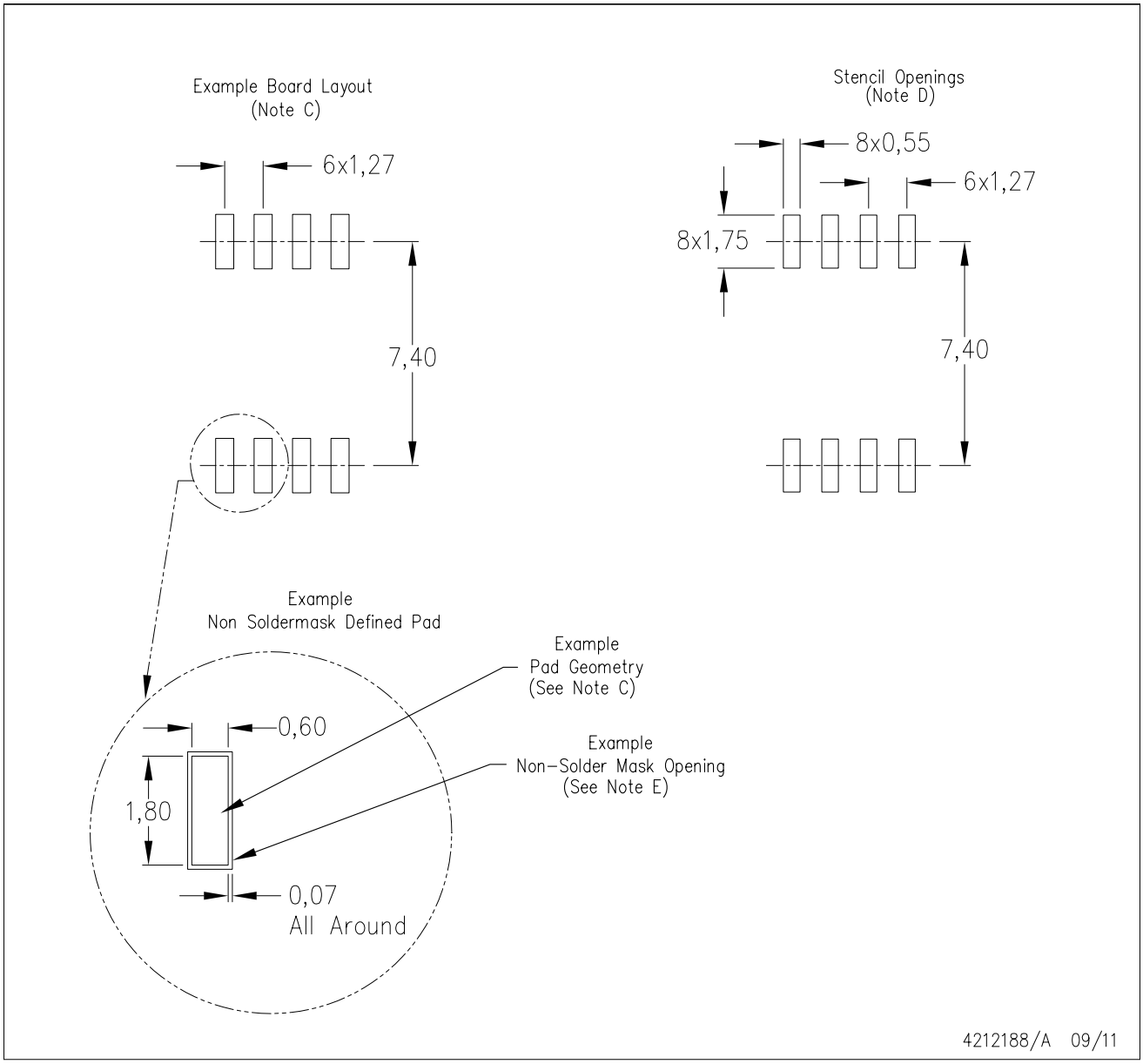
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE

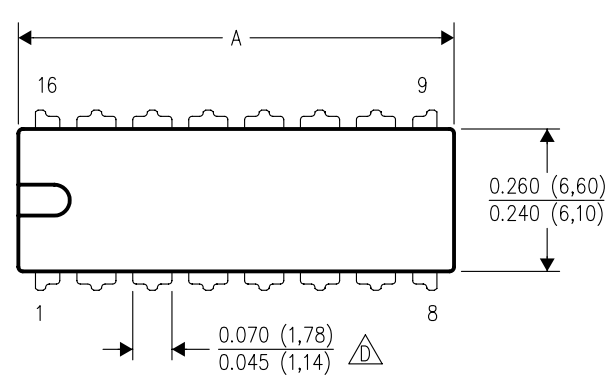


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

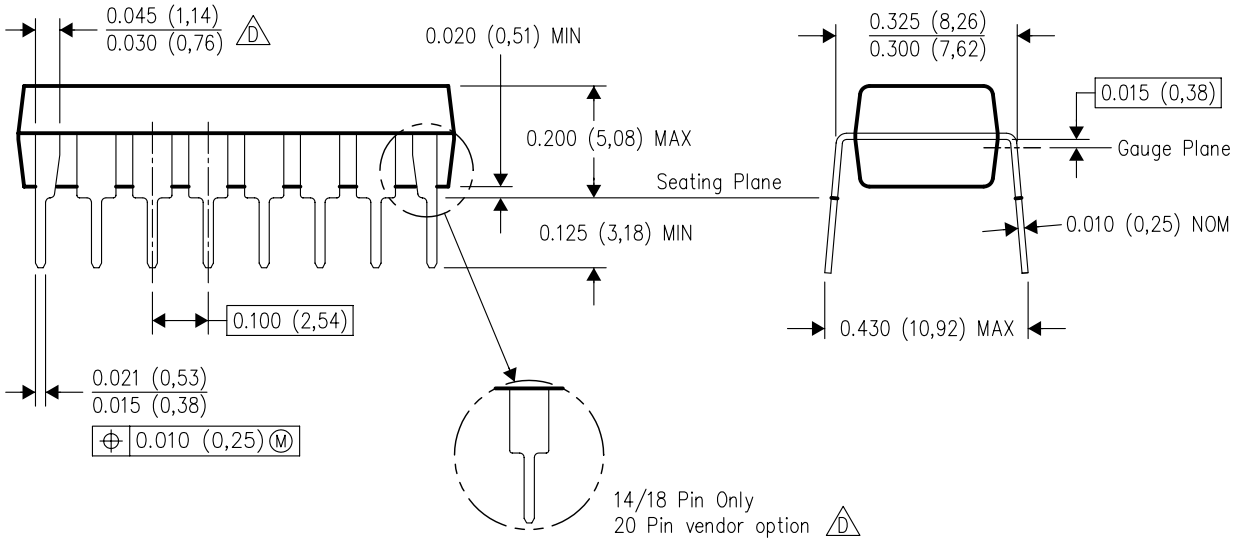
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



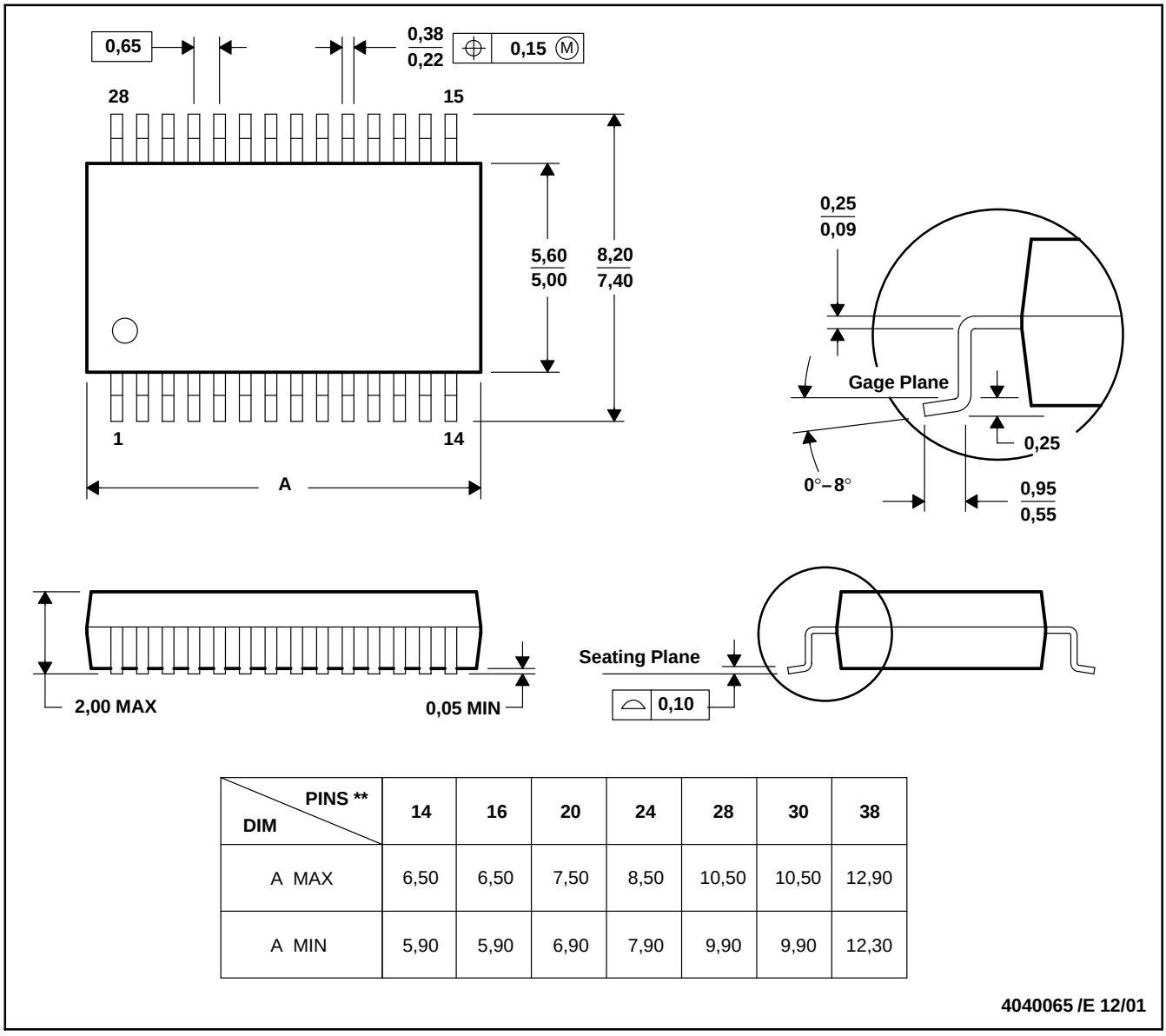
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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