THE DATASHEET OF

CAB4AZNRR

CAB4A - DDR4 Register
32-Bit 1:2 Command/Address/Control Buffer and 1:4 Differential Clock Buffer

Check for Samples: CAB4A

FEATURES

- **DDR4RCD01 JEDEC Compliant**
- **DDR4 RDIMM and LRDIMM up to DDR4-2400**
- **32 Bits 1-to-2 Register Outputs**
- **1-to-4 Differential Clock Buffer**
- **1.2V Operation**
- **PLL with Internal Feedback**
- **Configurable Driver Strength**
- **Scalable Weak Driver**
- **Programmable Latency**
- **Output Driver Calibration**
- **Address Mirroring and Inversion**
- **DDR4 Full-Parity Operation**
- **On-Chip Programmable V_{REF} Generation**
- **CA Bus Training Mode**
- **I^2C™ Interface Support**
- **Up to 16-Logical Ranks Support for 3DS RDIMMs and LRDIMMs**
- **Up to 4 Physical Ranks Support for RDIMMs and LRDIMMs**

DESCRIPTION

The CAB4 is 32-bit 1:2 Command/Address/Control Buffer and 1:4 differential Clock Buffer designed for operation on DDR4 registered DIMMs with a 1.2 V VDD mode.

All inputs are pseudo-differential using external or internal voltage reference. All outputs are full swing CMOS drivers optimized to drive 15 to 50 Ω effective terminated traces in DDR4 RDIMM, LRDIMM and 3D-Stacked DIMM applications. The clock outputs, command/address outputs, control outputs, data buffer control outputs can be enabled in groups, and independently driven with different strengths to compensate for different DIMM net topologies. The DDR4 Register operates from a differential clock (CK_t and CK_c). Inputs are registered at the crossing of CK_t going HIGH, and CK_c going LOW. The input signals could be either re-driven to the outputs if one of the input signals DCS[n:0]_n is driven LOW or it could be used to access device internal control registers when certain input conditions are met.

The device is characterized in the operating temperature range from -40°C to 95°C.

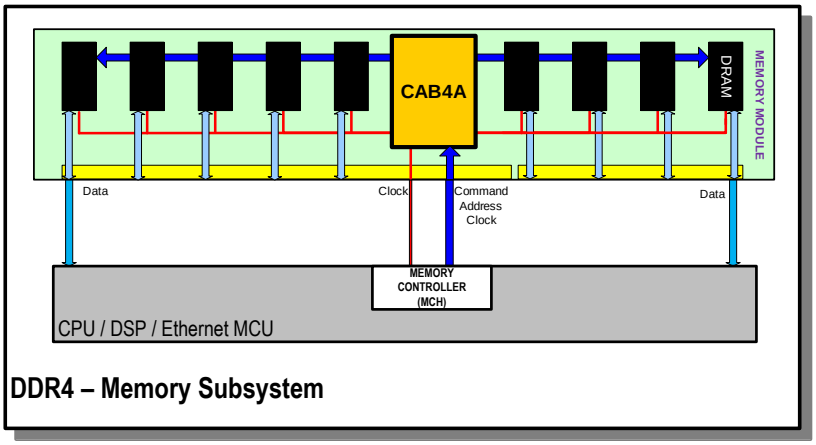


Figure 1. DDR4 - RDIMM Memory Subsystem

FUNCTIONAL BLOCK DIAGRAM

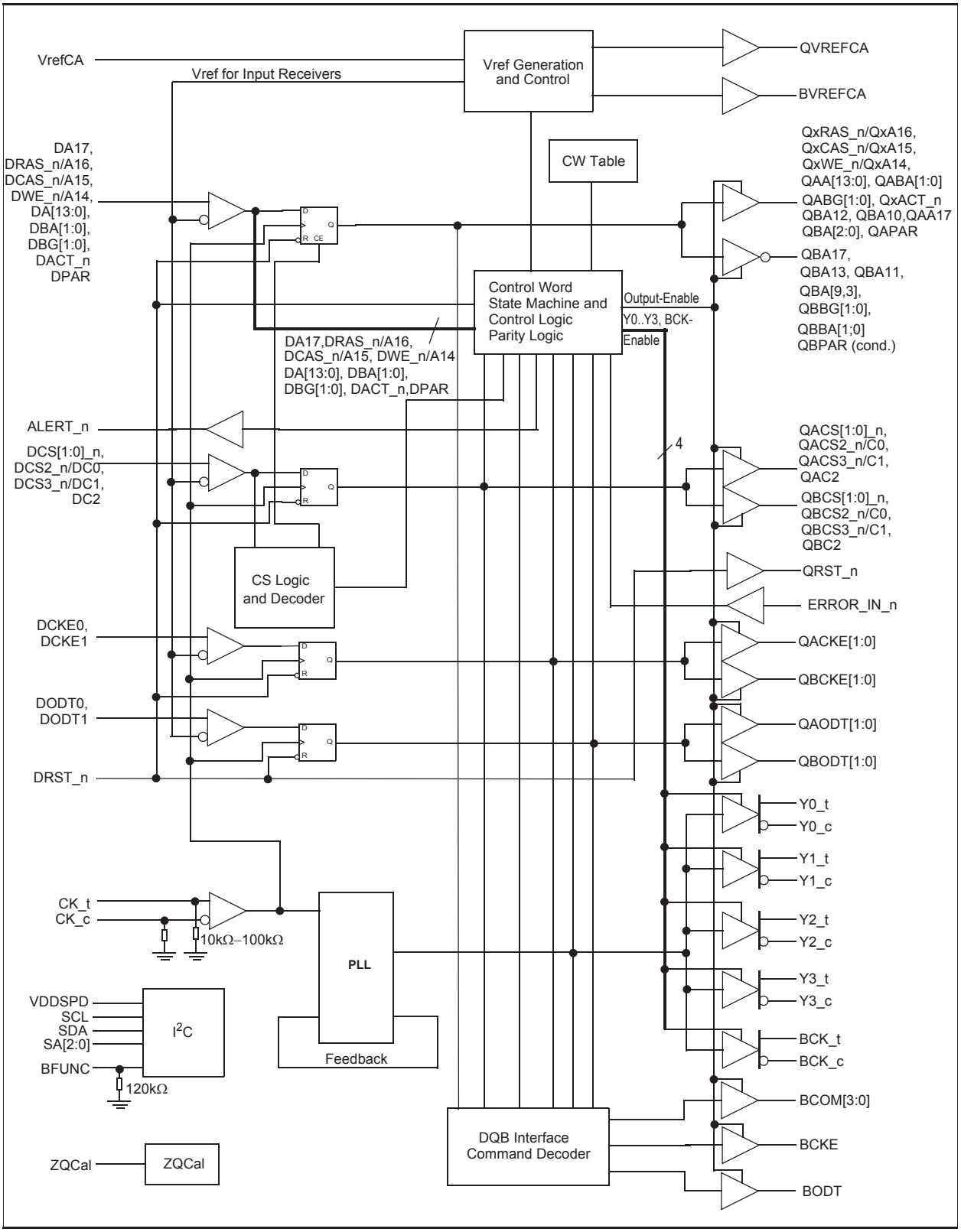


Table 1. TERMINAL FUNCTIONS

SIGNAL		TYPE	DESCRIPTION
GROUP	NAME		
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] VREF based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n		DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1		DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be LOW when a valid address/command is present which should be re-driven. Some of these have alternative functions: • DCS2_n ↔ DC0 • DCS3_n ↔ DC1
	DC2		DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] VREF based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals • DA14 ↔ DWE_n • DA15 ↔ DCAS_n • DA16 ↔ DRAS_n
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n		
	DACT_n		DRAM corresponding register DACT_n signal.
Clock inputs	CK_t, CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10 kΩ ~ 100 kΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS[2] VREF based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error Input	ERROR_IN_n	CMOS input	DRAM address parity and CRC Alert is connected to this input pin, which in turn is buffered and re-driven to the ALERT_n output of the register. Requires external pull-up resistor.[3]
Data buffer control and communication outputs	BODT	CMOS[3]	Data buffer on-die termination signal.
	BCKE		Data buffer clock enable signal for PLL power management.
	BCOM[3:0]		Register communication bus for data buffer programming and control access.
	BCK_t, BCK_c	CMOS differential	Differential clock output pair to the data buffer
	BVREFCA	VDD/2Reference Voltage	Output reference voltage for data buffer control bus receivers.

(1) These receivers use VREFCA as the switching point reference.
(2) These receivers use VREFCA as the switching point reference.
(3) CMOS: These outputs with rail to rail signal swing and programmable impedance are optimized for memory applications to drive DRAM inputs over a terminated transmission line.
Error_In_n: Internal Pull-up resistor can be turned on.

Table 1. TERMINAL FUNCTIONS (continued)

SIGNAL		TYPE	DESCRIPTION
GROUP	NAME		
Output Control Bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n		Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1		Register output Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be LOW when a valid address/command is present which should be re-driven. Some of these have alternative functions (Chip ID): • QxCS2_n ↔ QxC0 • QxCS2_n ↔ QxC0
	QAC2, QBC2		Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1		Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n		Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: • QxA14 ↔ QxWE_n • QxA15 ↔ QxCAS_n • QxA16 ↔ QxRAS_n
	QAACT-n, QBACT_n		Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVREFCA	VDD/2 Reference voltage	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS differential	Re-driven clocks
Reset output	QRST_n	CMOS	Re-driven reset. This is not an asynchronous output.
Parity outputs	QAPAR, QBPAR		Re-driven parity (4)
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I^2C pins	SDA SCL SA[2:0] BFUNC VDDSPD	Open drain I/O CMOS input CMOS input CMOS input Power input	I^2C Data I^2C Clock I^2C Address signals Reserved (5) I^2C power input

(4) I^2C inputs: These inputs are 2.5V inputs, except BFUNC which is a 1.2V input.
(5) BFUNC has an internal pull-down resistor of 120 kΩ to V.

Table 1. TERMINAL FUNCTIONS (continued)

SIGNAL		TYPE	DESCRIPTION
GROUP	NAME		
Miscellaneous pins	VREFCA	VCC/2Reference voltage	Input reference voltage for the CMOS inputs.
	VDD	Power input	Power supply voltage
	VSS	Ground input	Ground
	AVDD	Analog power	Analog supply voltage
	PVDD	Clock power	Clock logic and clock output driver power supply.
	PVSS	Clock ground	Clock logic and clock output driver ground.
	ZQCAL	Reference	Needs a calibration resistor of 240Ω ±1% to VSS.
	NU	Mechanical ball	Do not connect on PCB.
	RFU[3:0]	I/O	Reserved; must be left floating on DIMM and in DDR4 register.

REVISION HISTORY

Change document to production data.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAB4AZNRR	ACTIVE	NFBGA	ZNR	253	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 95	CAB4A6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

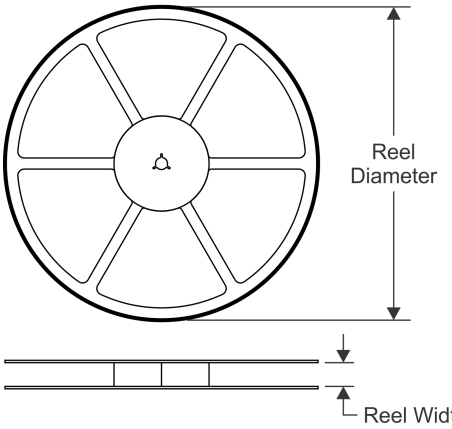
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

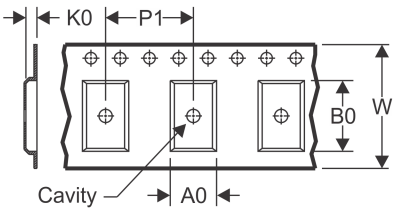
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

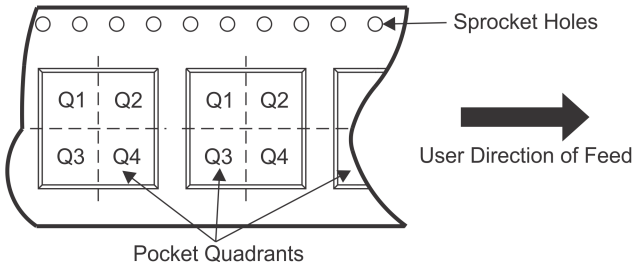


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

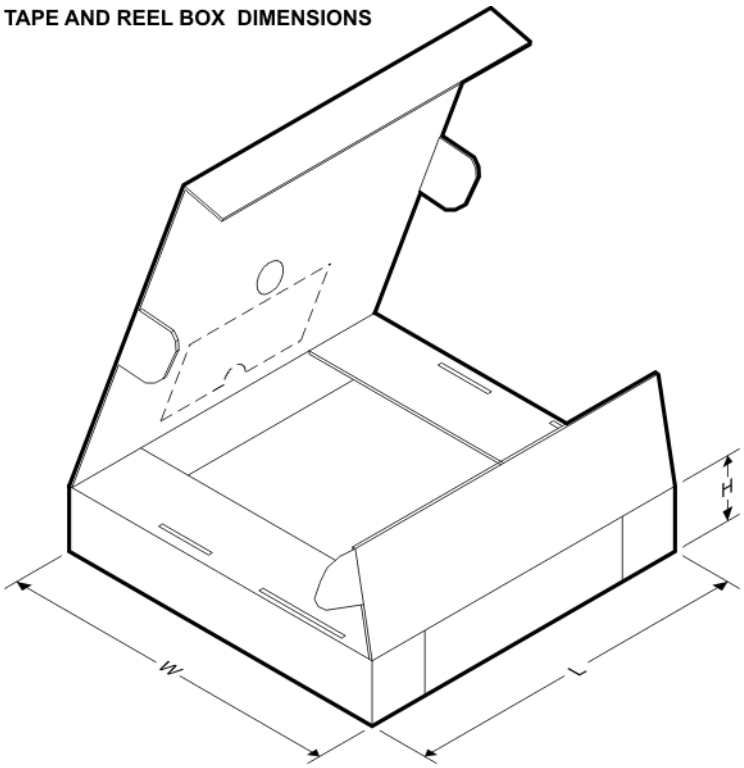
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAB4AZNRR	NFBGA	ZNR	253	2000	330.0	24.4	8.3	13.8	1.8	12.0	24.0	Q1

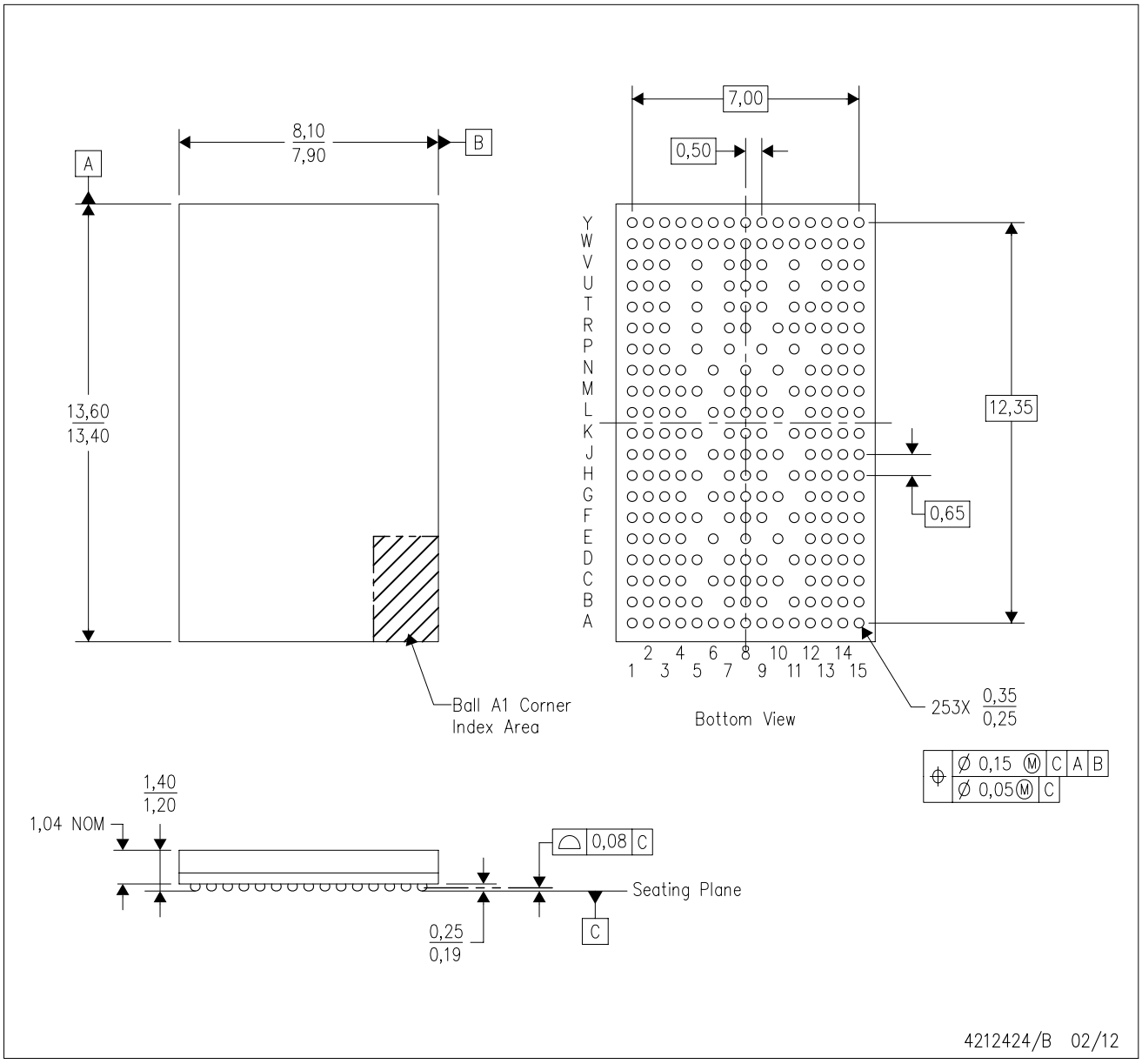
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAB4AZNRR	NFBGA	ZNR	253	2000	336.6	336.6	31.8

ZNR (R–PBGA–N253) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

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