THE DATASHEET OF

XR18W750IL48-F

www.win-source.net 0086-755-83957316

GENERAL DESCRIPTION

The XR18W750 is a Wireless UART Controller with a two-wire I²C interface to the XR18W753 RF transceiver to complete Exar's Wireless UART chipset solution. The XR18W750 supports both the parallel and serial interfaces to any host system thus providing flexibility for system designers to select their interface option.

The XR18W750 includes an embedded 8051 microprocessor which provides the power to process the protocol framing for data transmission and to handle error processing. Internally, the XR18W750 has a 32KB system memory for loading the firmware from an external EEPROM and for data processing. The XR18W750 also includes a 128-bit AES engine for data encoding and decoding.

The XR18W750 is available in a 48-pin QFN package.

APPLICATIONS

- Industrial Automation
- Factory Automation
- Point of Sales Systems
- Industrial Servers
- Data Collection Terminals

FEATURES

- 2.25 to 3.63 Volt Operation
- 5 Volt Tolerant Inputs
- 8051 Microcontroller
- 32KB System Memory
- 128-bit AES Engine
- I²C Bus Master Interface to RF Transceivers
- Optional UART interface to RF Transceiver
- Selectable Serial or Parallel Mode Interface
- Enhanced UART
  - 16550 Compatible Register Set
  - Parallel mode data rate from 1200 bps to 230.4 Kbps
  - Serial mode data rate from 1200 bps to 921.6Kbps
  - Transmit and Receive FIFOs of 64 bytes
  - Programmable TX and RX FIFO Trigger Levels
  - Transmit and Receive FIFO Level Counters
  - Automatic Hardware (RTS/CTS) Flow Control
  - Selectable Auto RTS Flow Control Hysteresis
  - Full modem interface
- Device Identification and Revision
- 48-pin QFN package

FIGURE 1. XR18W750 BLOCK DIAGRAM

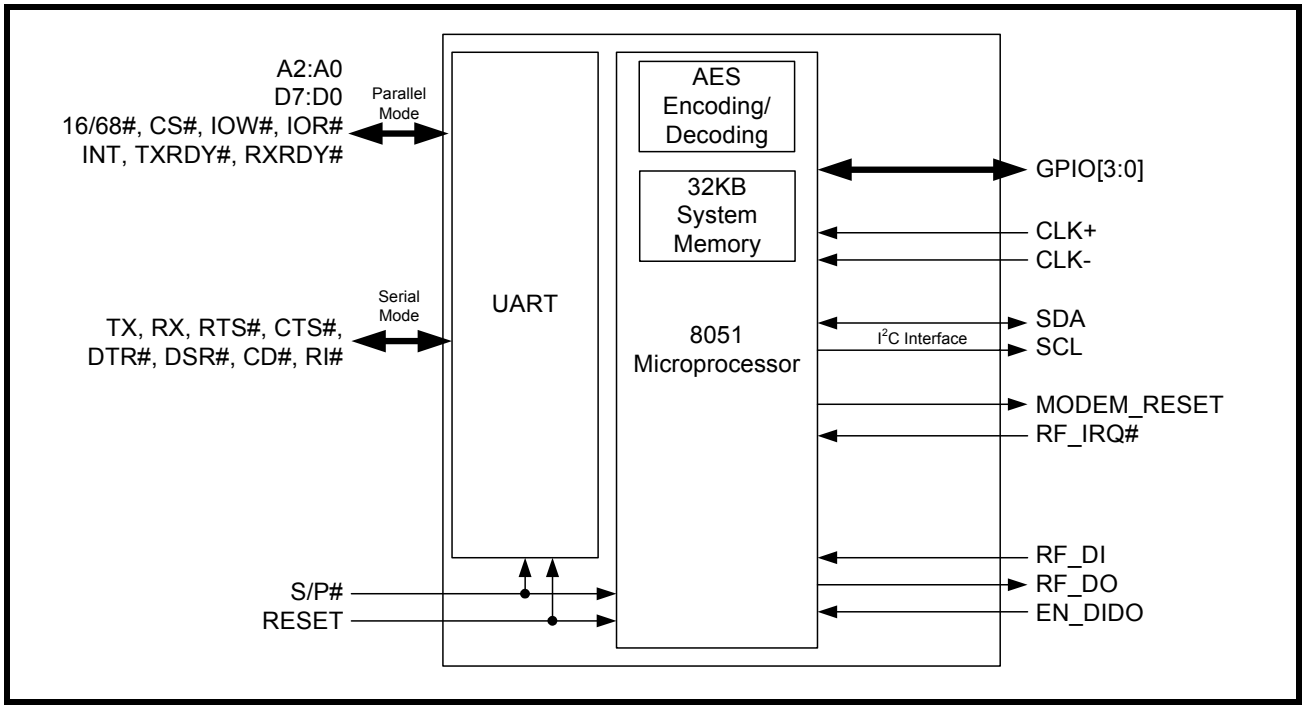
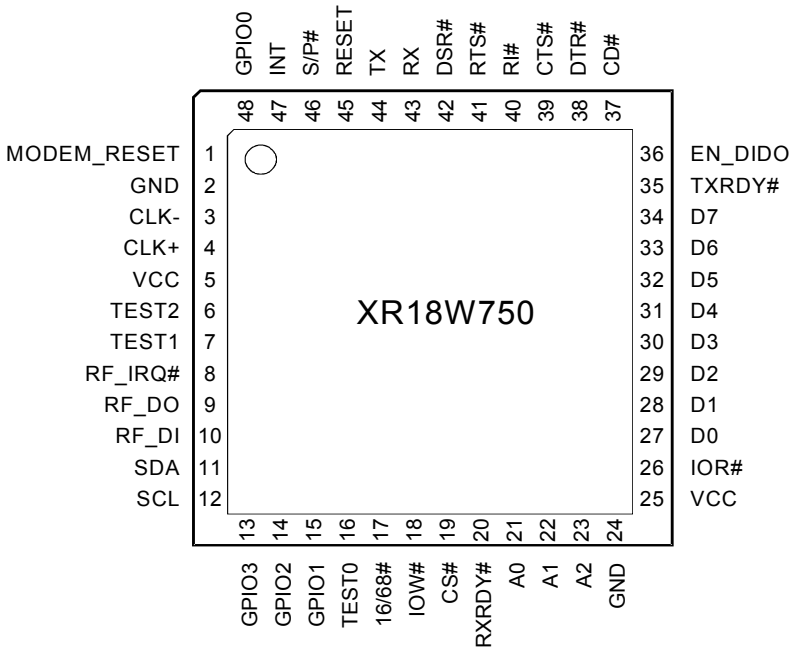


FIGURE 2. PIN OUT ASSIGNMENT



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR18W750IL48	48-Lead QFN	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Description

NAME	48-QFN PIN #	TYPE	DESCRIPTION
PARALLEL MODE INTERFACE SIGNALS			
A2 A1 A0	23 22 21	I	Address data lines [2:0]. These 3 address lines select one of the internal registers in the UART during a data bus transaction. The internal UART registers are not accessed by the 8051 microprocessor in the parallel mode.
D7 D6 D5 D4 D3 D2 D1 D0	34 33 32 31 30 29 28 27	I/O	Data bus lines [7:0] (bidirectional).
IOR# (VCC)	26	I	When 16/68# pin is HIGH, the Intel bus interface is selected and this input becomes read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge. When 16/68# pin is LOW, the Motorola bus interface is selected and this input is not used and should be connected to VCC.
IOW# (R/W#)	18	I	When 16/68# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines. When 16/68# pin is LOW, the Motorola bus interface is selected and this input becomes read (HIGH) and write (LOW) signal.
CS#	19	I	Chip select (active low) signal.
INT (IRQ#)	47	O	When 16/68# pin is HIGH for Intel bus interface, this output is an active high interrupt output. Upon power-up, this output is in three-state mode. The output state is controlled by the user through the software setting of MCR[3]. The INT output is enabled when MCR[3] is set to a logic 1. See MCR[3]. When 16/68# pin is LOW for Motorola bus interface, this output becomes an active low, open drain interrupt output. An external pull-up resistor is required for proper operation.
TXRDY#	35	O	UART Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit. See **Table 3**. If it is not used, leave it unconnected.
RXRDY#	20	O	UART Receiver Ready (active low). This output provides the RX FIFO/RHR status for receive. See **Table 3**. If it is not used, leave it unconnected.
SERIAL MODE INTERFACE SIGNALS			
TX	44	O	UART Transmit Data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be HIGH during reset or idle (no data). If this pin is not used, leave it unconnected.
RX	43	I	UART Receive Data. Normal receive data input must idle HIGH. If this pin is not used, tie it to VCC or pull it high via a 100k ohm resistor.

Pin Description

NAME	48-QFN PIN #	TYPE	DESCRIPTION
RTS#	41	O	UART Request-to-Send (active low) or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1], FCTR[1:0], EMSR[5:4] and IER[6].
CTS#	39	I	UART Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. This input should be connected to VCC when not used.
DTR#	38	O	UART Data-Terminal-Ready (active low) or general purpose output. If it is not used, leave it unconnected.
DSR#	42	I	UART Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CD#	37	I	UART Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RI#	40	I	UART Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RF TRANSCEIVER INTERFACE SIGNALS			
MODEM_RESET	1	O	Reset output to the RF transceiver.
RF_IRQ#	8	I	Interrupt input from RF transceiver.
SDA	11	I/O	I^2C Serial Data Line.
SCL	12	I/O	I^2C Serial Clock Line. The I^2C clock frequency can be up to 400 KHz.
RF_DO	9	O	Data out to RF transceiver.
RF_DI	10	I	Data in from RF transceiver.
EN_DIDO	36	I	Enable RF_DI and RF_DO (active high) for sending data to and from RF transceiver. If I^2C bus is used for this purpose, this input should be connected to GND.
ANCILLARY SIGNALS			
S/P#	46	I	Serial or Parallel Mode select. If this pin is HIGH, then the serial interface will be enabled. If this pin is LOW, then the parallel mode will be enabled.
16/68#	17	I	Intel or Motorola Bus Select. When 16/68# pin is HIGH, 16 or Intel Mode, the device will operate in the Intel bus type of interface. When 16/68# pin is LOW, 68 or Motorola mode, the device will operate in the Motorola bus type of interface.
RESET (RESET#)	45	I	When 16/68# pin is HIGH for Intel bus interface, this input becomes RESET (active high). When 16/68# pin is LOW for Motorola bus interface, this input becomes RESET# (active low). A 40 ns minimum active pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held HIGH, the receiver input will be ignored and outputs are reset during reset period (see **Table 15**).

Pin Description

NAME	48-QFN PIN #	TYPE	DESCRIPTION
CLK- CLK+	3 4	I I	16 MHz differential clock input or CMOS clock input. Use both signals for differential clock. Connect CLK- to VCC to enable the CMOS/TTL clock mode. The external CMOS/TTL clock should be connected to CLK+.
GPIO[3:0]	13, 14, 15, 48	I/O	General Purpose I/O.
TEST2 TEST1 TEST0	6 7 16	I I I	Factor Test Modes (active high). For normal operation, connect these inputs to GND.
VCC	5, 25	Pwr	2.97V to 3.63V power supply.
GND	2, 24	Pwr	Power supply common, ground.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The XR18W750 is a Digital Baseband with a two-wire I²C interface to the XR18W753 RF transceiver to complete Exar's Wireless UART chipset solution. An external I²C EEPROM is required to store Exar's proprietary firmware and Wireless UART chipset parameters.

The XR18W750 is functionally, as well as architecturally, divided into the following blocks and modules:

- 8051 Microprocessor
- Enhanced UART
- AES Engine
- I²C Interface

1.1 8051 Microprocessor

The embedded 8051 microprocessor is compatible with the industry standard 803x/805x microprocessors using a standard 8051 instruction set. The embedded 8051 microprocessor has a high-speed architecture that takes four clocks per instruction cycle, eliminates wasted bus cycles and improves instruction execution time on average by 2.5X over the standard 8051. The embedded 8051 microprocessor has a 32KB system memory for loading the firmware from an external I²C EEPROM and for data processing. The firmware is loaded from the external I²C EEPROM upon power on or reset. A 16MHz clock is required for correct operation of the 8051 microprocessor. (This same 16MHz clock is also used by the enhanced UART in the XR18W750.) For the firmware for communicating with the XR18W753 RF Transceiver, send an e-mail to uarttechsupport@exar.com.

1.2 Enhanced UART

A CPU or serial port can communicate with the XR18W750 via the enhanced 64 byte FIFO UART. The XR18W750 can communicate with an external CPU when the parallel mode is enabled (S/P# connected to GND) or it can communicate directly with another serial port when the serial mode is enabled (S/P# connected to VCC). The enhanced UART has a register set that is compatible to the industry standard 16550, but with additional features such as Auto RTS/CTS Hardware Flow Control, Programmable TX and RX FIFO Trigger Levels, and a Programmable Fractional Baud Rate Generator.

1.2.1 Parallel Mode

When the parallel mode is enabled, an external CPU can communicate with the enhanced UART via either the Intel bus (CS#, IOR#, IOW#, INT) or Motorola bus (CS#, R/W#, IRQ#) interface. Any data that is written to the TX FIFO of the enhance UART will be transmitted serially to UART of the 8051 microprocessor, where it is processed and sent via the I²C interface to the RF Transceiver.

1.2.2 Serial Mode

When the serial mode is enabled, an external serial port can communicate with the enhanced UART via RS-232, RS-422, or RS-485. The data that is received in the RX FIFO of the enhanced UART will be read out via the parallel bus by the 8051 microprocessor, where it is processed and appropriate actions are taken. There are two modes of operation in the serial mode: Command Mode and Data Mode. In the command mode, the enhanced UART can be configured via AT commands.

1.3 AES Engine

The internal 128-bit AES engine guarantees that the data is transmitted securely from one Wireless UART chipset to another Wireless UART chipset with the same AES security key. This prevents other wireless devices on the same frequency to listen in on the Wireless UART chipset unless it knows the 128-bit AES security key.

1.4 I²C Interface

The I²C interface on the XR18W750 operates in the I²C master mode. The I²C interface is a two-wire serial interface consisting of a serial data line (SDA) and serial clock line (SCL). The maximum I²C clock frequency is 400 kHz. The XR18W750 loads the firmware from the EEPROM and can communicate with an RF Transceiver like the XR18W753 via the I²C interface.

1.4.1 XR18W753 RF Transceiver

The XR18W753 is an RF Transceiver with frequency ranges of 868MHz - 954MHz and a data rate of 250kbps. All of the Physical Layer Management Entity (PLME) registers to configure and control the XR18W753 can be accessed via the I^2C interface. See the XR18W753 datasheet for complete details.

1.4.2 External EEPROM

An external I^2C EEPROM is required to store the firmware for the 8051 microprocessor and the parameters of the Wireless UART chipset. The I^2C EEPROM must have at least 32KB of memory.

1.4.2.1 EEPROM Parameters

The table below describes all of the parameters that are stored in the external I^2C EEPROM.

TABLE 1: EEPROM PARAMATERS

PARAMETER	BYTES	DESCRIPTION
Source ID	4	These bytes are sent in the packet preamble to identify who is sending the packet in P2P mode.
Destination ID	4	These bytes are sent in the packet preamble to identify who is to receive the packet in the P2P mode.
Baud Rate	4	These 4 bytes store the default baud rate that the UART will be initialized to during the next power-up.
Communication Mode	1	This parameter selects the communication mode: P2P, P2M, Broadcast.
Channel Number (Frequency)	1	This byte stores the default or last used channel frequency of the XR18W753 RF Transceiver.
Number of Retries	1	This byte stores the number of times to re-transmit a packet when an ACK is not received in P2P mode before giving up.
Group ID	1	These bytes are compared by the recipient when a broadcast packet has been received.
Power Level	1	This byte stores the default power level for the XR18W753.
XR18W753 address	1	This byte stores the I^2C address of the XR18W753.
Autobaud Detect	1	This byte selects whether the device has the Autobaud Detect feature enabled upon power-up.
Power-up Mode	1	This byte selects whether the device powers up in the command or the data mode.
AES Security Key	16	This parameter is used for as the encoding/decoding key in the AES Engine.

2.0 COMMUNICATION MODES

2.1 Point-to-Point

Point-to-point communication is similar to two UARTs communicating via RS-232 or RS-422. The differences being that the communication is now wireless and half-duplex. Each time a wireless data packet is transmitted, the Wireless UART chipset waits until an ACK is received. If an ACK has not been received, the Wireless UART chipset will re-transmit the packet. The Wireless UART chipset will attempt to re-transmit the packet until the specified number of retries has been reached.

In this communication mode, the packet will only be received and an ACK will be sent if the two Wireless UART chipsets are configured for the same frequency, with matching AES security keys and the Destination ID of the packet matches the Source ID of the Wireless UART chipset.

2.2 Point-to-Multipoint (Group Mode)

Point-to-multipoint communication, also known as Group mode, is when one master station transmits a packet to all Wireless UART chipsets with the same Group ID. All Wireless UART chipsets with the same Group ID will receive the message. No ACK will be sent by the receiving stations and no ACK is expected by the master station. The Source and Destination ID is not checked in this communication mode.

2.3 Broadcast

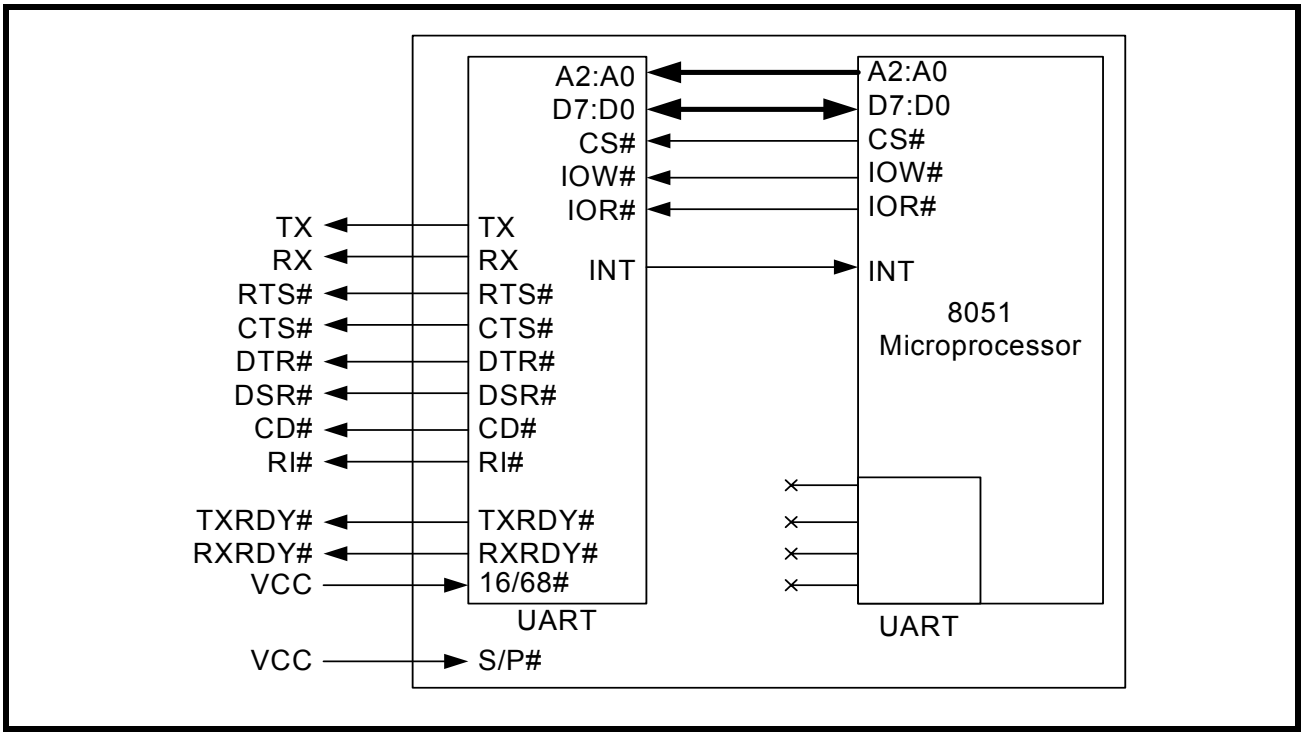
The broadcast mode is when one master station transmits a packet and is received by all Wireless UART chipsets that are on the same channel frequency and that have the same AES security key. In this case, the Source ID, Destination ID and Group ID are not checked. No ACK will be sent by the receiving stations and no ACK is expected by the master station.

3.0 ENHANCED UART DESCRIPTION

3.1 Serial Mode Interface

In the serial mode, the enhanced UART is controlled by the 8051 processor. The enhanced UART can communicate with another serial port via RS-232, RS-485, or RS-422. A typical connection for the serial mode of operation is shown below.

FIGURE 3. XR18W750 TYPICAL CONNECTIONS (SERIAL MODE)



In the serial mode, the external serial port will need to communicate with the UART via AT commands.

3.1.1 Auto Baud Rate Detect

Upon power-up, the XR18W750 can automatically detect any baud rate from 1200 bps to 230.4Kbps in the parallel mode or from 1200 bps to 921.6Kbps in the serial mode. The only requirement is that the carriage return character (0x0D) is sent twice to the enhanced UART. After that the enhanced UART will be configured for the correct baud rate.

3.1.2 AT Commands

The AT Commands supported are given in the table below.

TABLE 2: AT COMMANDS

SYNTAX	DESCRIPTION	EXAMPLE
ATI3	Displays the firmware version.	ATI3<Enter>
AT+PPM=[x]	0 = Enable Point-to-Point Mode (P2P) 1 = Enable Point-To-Multipoint Mode (P2M) 2 = Enable Broadcast Mode	AT+PPM=0<Enter>
AT+SID=[xxxxxxxx]	Source address. The range is 0x1 to 0xFFFFFFFD. 0xFFFFFFFE and 0xFFFFFFFF are reserved.	AT+SID = 38437452<Enter> // Source Address = 0x38437452
AT+DID	Destination address. The range is 0x1 to 0xFFFFFFFD. 0xFFFFFFFE and 0xFFFFFFFF are reserved.	AT+DID=23437<Enter> // Destination address = 0x23437
AT+BDR=[xxxxxx]	Change baud rate to 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400 bps.	AT+BDR=19200<Enter>
AT+GID=[xxx]	Group ID. The valid range is 0x1 to 0xFE.	AT+GID=10<Enter> //Set group ID = 10
AT+CHN=[xx]	Sets the RF channel number for the device. See the XR18W753 for the valid channel range.	AT+CHN=2<Enter> //Set channel number = 2
AT+NRE=[x]	Number of Retries. The range is 0x1 to 0xA.	AT+NRE=3<Enter> //Set the number of retries to 3
AT+PWR=[x]	Power level of RF transmitter. The range is 0x1 to 0x8	AT+PWR=1 //Set the power level = -3dbm
AT&V	Display the current values of the source address, destination address, baud rate, channel number, etc.	AT&V<Enter>
ATO	Switch from command mode to data mode.	ATO<Enter>
+++	Switch from data mode to command mode. The time between each "+" should be between 250ms and 1 sec.	+++

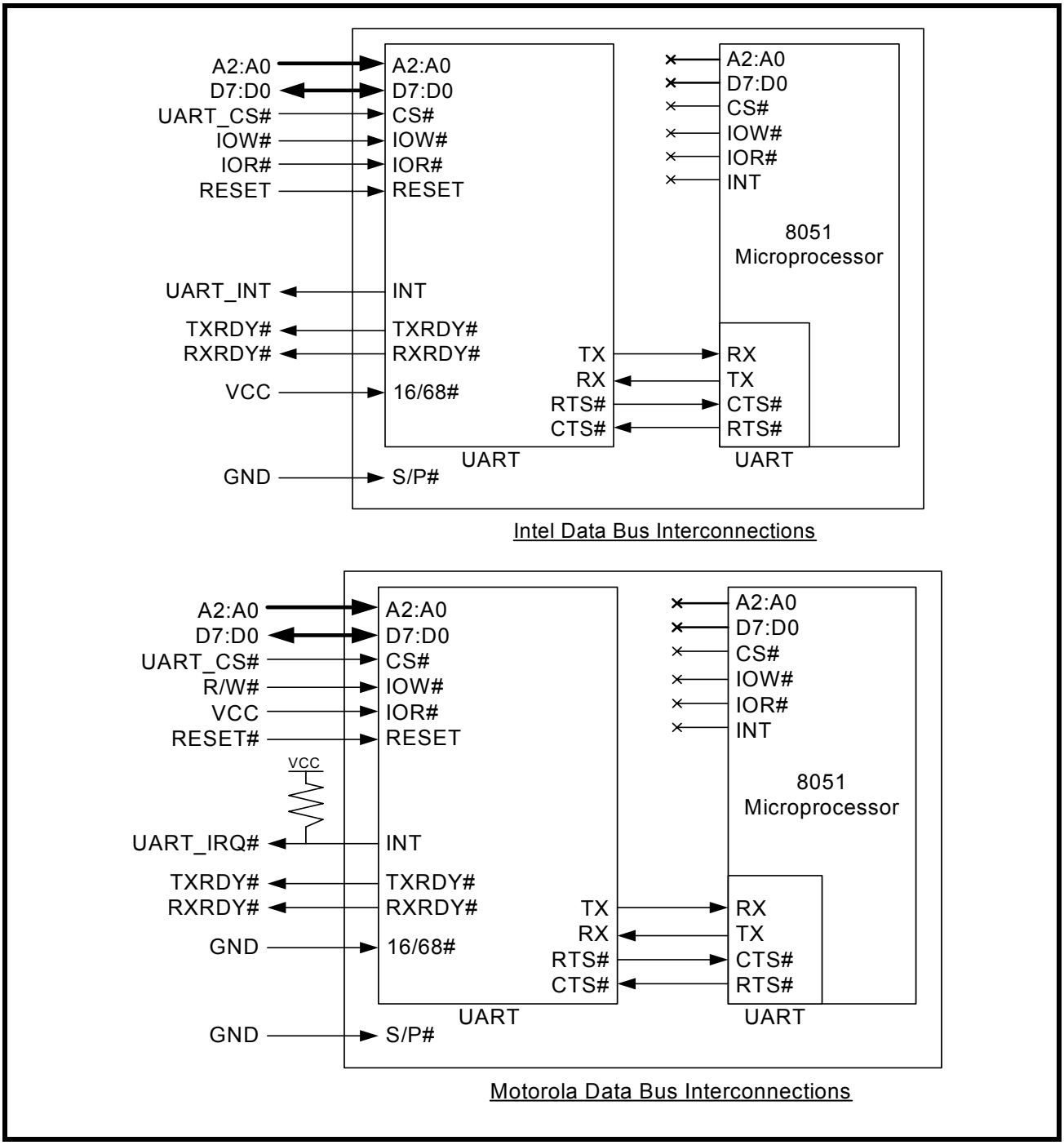
AT+KEY=
[xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx]
	Sets a key for the AES engine	AT+KEY=0001020304050607
		08090A0B0C0D0E0F<Enter>
		//Set the AES key to the specified
		//value

AT+I2C=[xx]	Change the I^2C address of the RF Transceiver.	AT+I2C=60<Enter> // Change I^2C address to 0x60
AT+MOD=[x]	0 = Power-up in command mode 1 = Power-up in data mode	AT+MOD=1<Enter>
AT+ABD=[x]	0 = Autobaud detect disabled at next power-up 1 = Autobaud detect enabled at next power-up	AT+ABD=1<Enter>

3.2 Parallel Mode (CPU) Interface

In the parallel mode, the CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The XR18W750 data interface supports both the Intel and Motorola compatible types of CPUs and is compatible to the industry standard 16C550 UART. Each bus cycle is asynchronous using CS#, IOR# and IOW#, or CS# and R/W# inputs. A typical data bus interconnection for Intel and Motorola mode is shown in Figure 4.

FIGURE 4. XR18W750 TYPICAL INTEL/MOTOROLA DATA BUS INTERCONNECTIONS (PARALLEL MODE)



3.3 Device Reset

The RESET input resets the internal registers and the serial interface outputs to their default state (see Table 15). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

3.4 Device Identification and Revision

The XR18W750 has the same Device ID as the XR16L275x and XR16V275x. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x0A and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

3.5 Internal Registers

The enhanced UART has a set of registers for control, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible Scratchpad Register (SPR).

Beyond the general 16C550 features and capabilities, the XR18W750 offers enhanced feature registers (EMSR, FLVL, EFR, FCTR, TRG, FC) that provide automatic RTS and CTS hardware flow control, FIFO trigger level control, and FIFO level counters. All the register functions are discussed in full detail later in **"Section 4.0, UART INTERNAL REGISTERS" on page 18**.

3.6 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document doesn't mean "direct memory access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# and TXRDY# output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the enhanced UART is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. In this mode, the enhanced UART sets the TXRDY# pin when the transmit FIFO becomes full, and sets the RXRDY# pin when the receive FIFO becomes empty. The following table shows their behavior. Also see Figures 16 through 21.

TABLE 3: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
RXRDY#	LOW = 1 byte. HIGH = no data.	LOW = at least 1 byte in FIFO. HIGH = FIFO empty.	HIGH to LOW transition when FIFO reaches the trigger level, or time-out occurs. LOW to HIGH transition when FIFO empties.
TXRDY#	LOW = THR empty. HIGH = byte in THR.	LOW = FIFO empty. HIGH = at least 1 byte in FIFO.	LOW = FIFO has at least 1 empty location. HIGH = FIFO is full.

3.7 INT (IRQ#) Output

The INT interrupt output changes according to the operating mode and enhanced features setup. Table 4 and 5 summarize the operating behavior for the transmitter and receiver. When operating in the Motorola bus mode, the IRQ# output is the opposite polarity of the INT output. Also see Figures 16 through 21.

TABLE 4: INT PIN OPERATION FOR TRANSMITTER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin	LOW = a byte in THR HIGH = THR empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or FIFO empty

TABLE 5: INT PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin	LOW = no data HIGH = 1 byte	LOW = FIFO below trigger level HIGH = FIFO above trigger level

3.8 Programmable Baud Rate Generator

The enhanced UART has a programmable Baud Rate Generator (BRG) for the transmitter and receiver. The divisor values for the specific data rates are given in the table below.

TABLE 6: UART DATA RATES

Data Rate	DIVISOR FOR 16x Clock (Decimal)	DLM VALUE (HEX)	DLL VALUE (HEX)
300	3333.333	0D	05
600	1666.667	06	82
2400	416.667	01	A0
4800	208.333	00	D0
9600	104.167	00	68
19200	52.083	00	34
38400	26.042	00	1A
57600	17.361	00	11
115200	8.681	00	8
230400	4	00	4

3.9 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

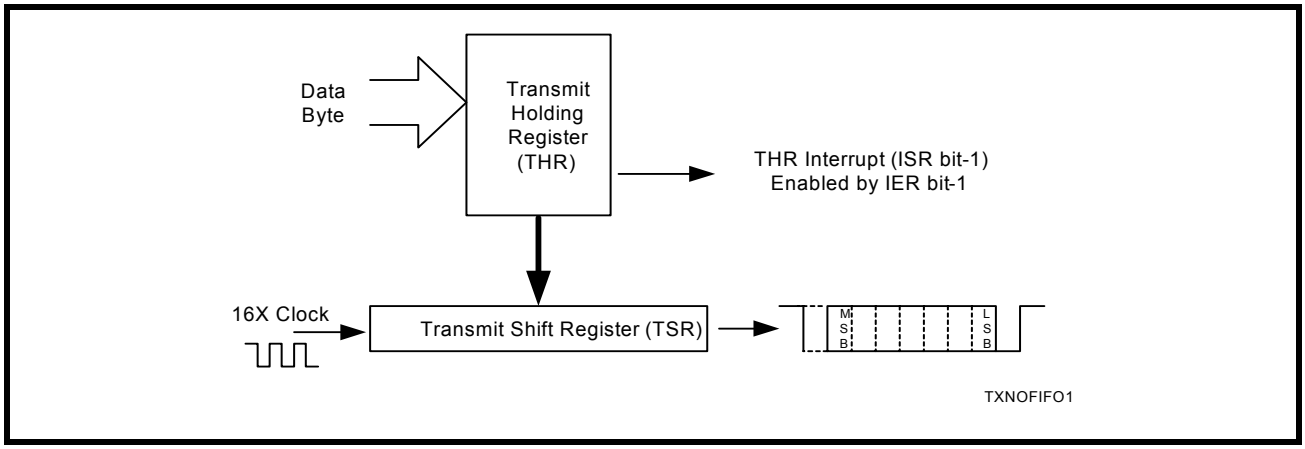
3.9.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

3.9.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

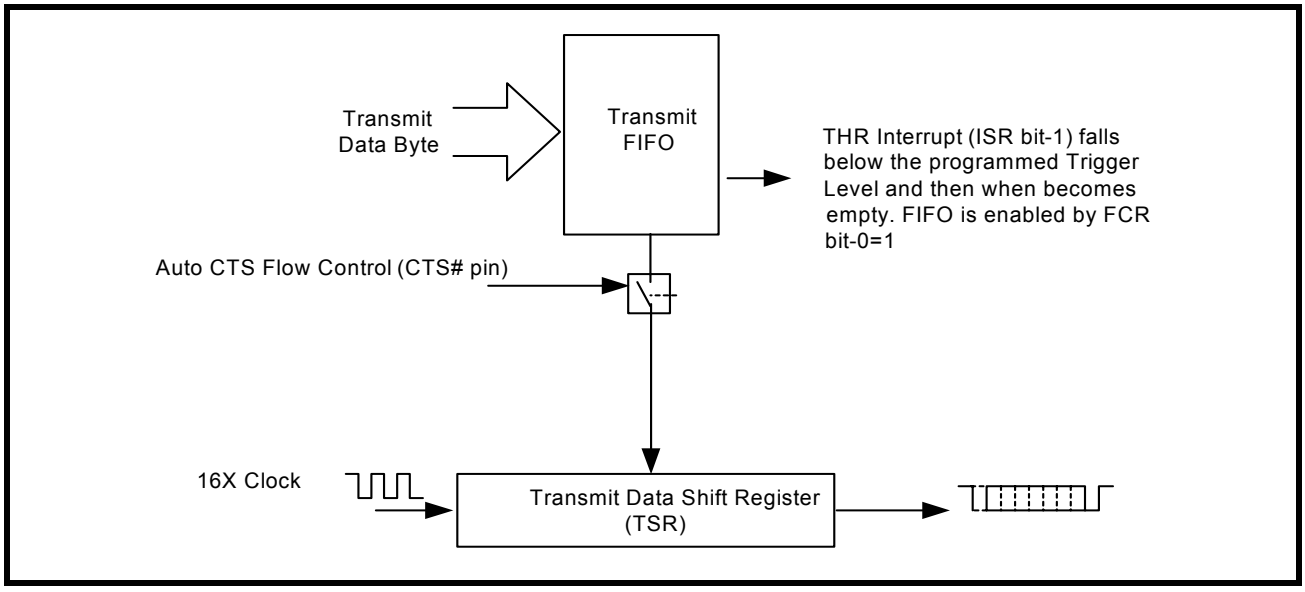
FIGURE 5. TRANSMITTER OPERATION IN NON-FIFO MODE



3.9.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 6. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



3.10 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

3.10.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 7. RECEIVER OPERATION IN NON-FIFO MODE

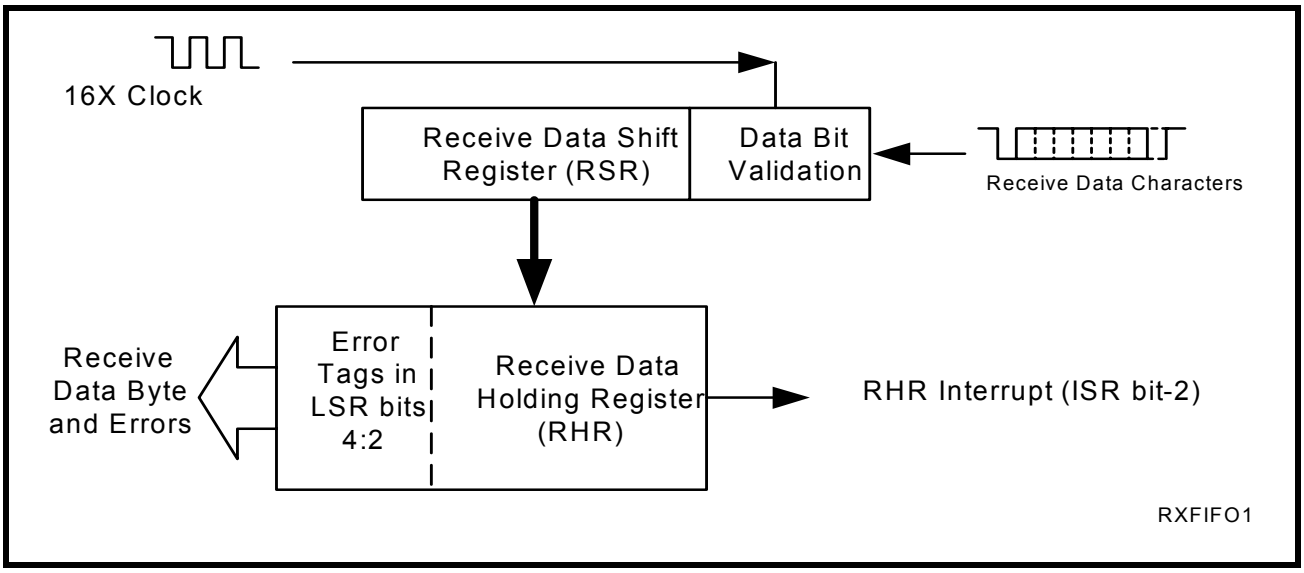
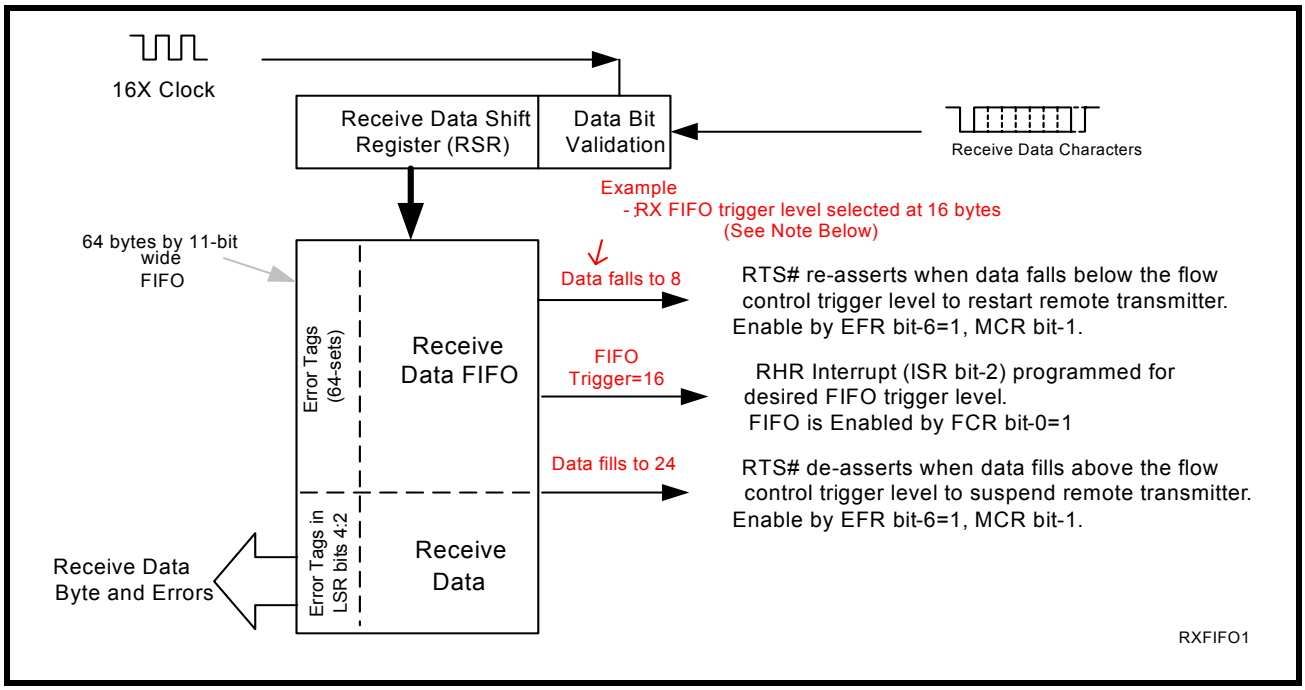


FIGURE 8. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



NOTE: *Table-B selected as Trigger Table for* **Figure 8** *(***Table 10***).*

3.11 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see **Figure 9**):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

3.12 Auto RTS Hysteresis

With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed RX trigger level. The RTS# pin will not be forced HIGH (RTS off) until the receive FIFO reaches the upper limit of the hysteresis level. The RTS# pin will return LOW after the RX FIFO is unloaded to the lower limit of the hysteresis level. Under the above described conditions, the enhanced UART will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted LOW (RTS On). **Table 13** shows the complete details for the Auto RTS# Hysteresis levels. Please note that this table is for programmable trigger levels only (Table D). The hysteresis values for Tables A-C are the next higher and next lower trigger levels in the corresponding table.

3.13 Auto CTS Flow Control

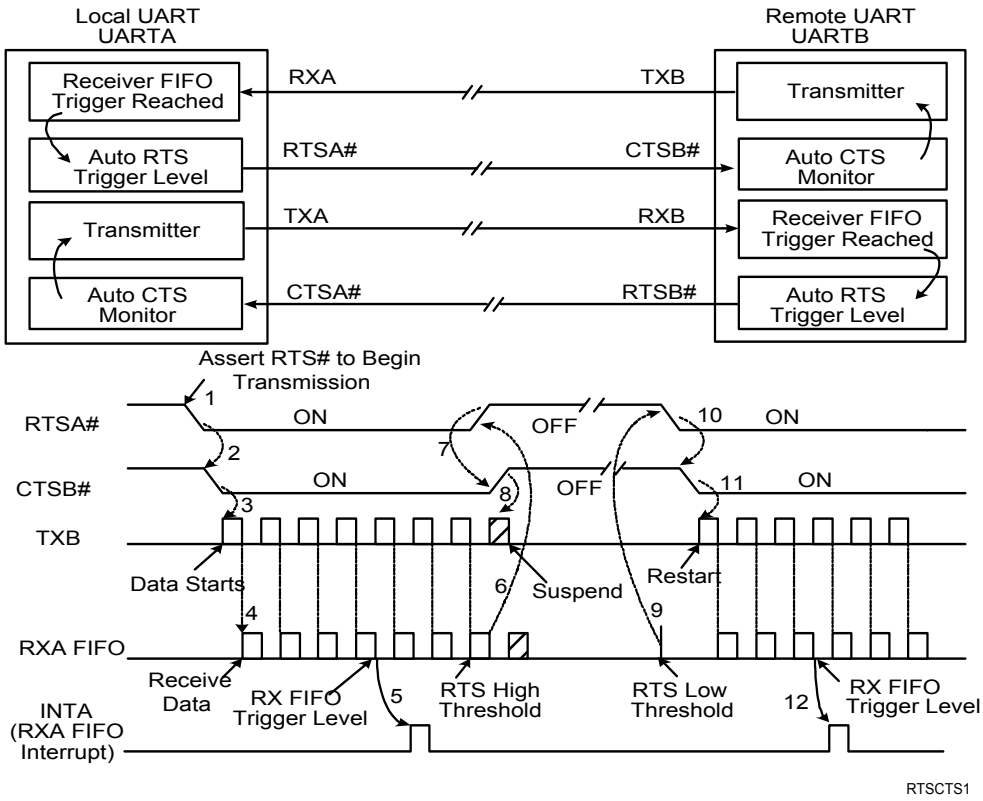
Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 9**):

- Enable auto CTS flow control using EFR bit-7.

If using the Auto CTS interrupt:

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (HIGH): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (LOW), indicating more data may be sent.

FIGURE 9. AUTO RTS AND CTS FLOW CONTROL OPERATION

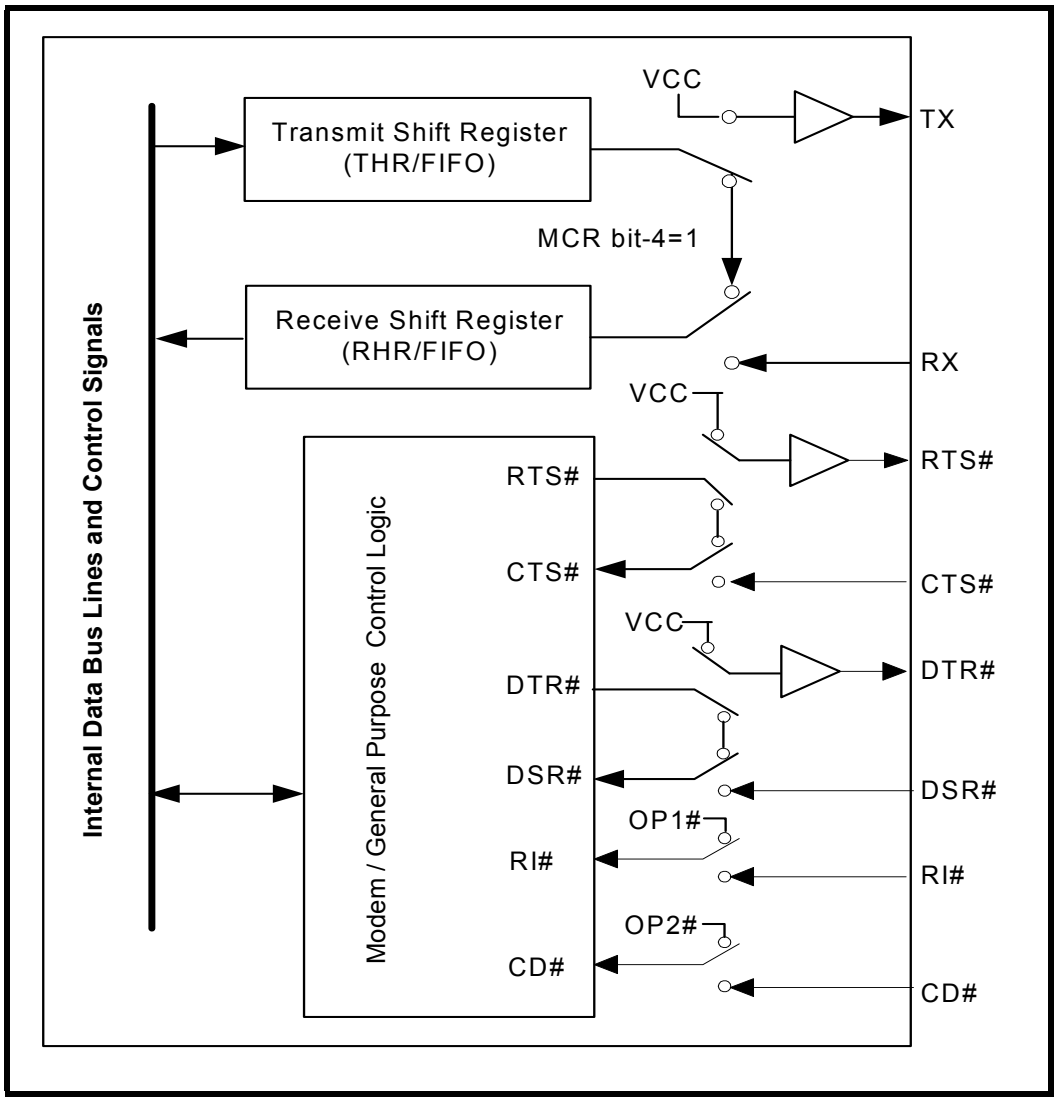


The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

3.14 Internal Loopback

The enhanced UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 10 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX, RTS# and DTR# pins are held while the CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input pin must be held HIGH during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal. Also, Auto RTS/CTS flow control is not supported during internal loopback.

FIGURE 10. INTERNAL LOOPBACK



4.0 UART INTERNAL REGISTERS

The internal registers of the UART are selected by address lines A2-A0 in the parallel mode. In the serial mode, the UART registers are not accessible via these address lines. The 8051 microprocessor does not access the enhanced UART in the parallel mode. The complete register set is shown on Table 7 and Table 8.

TABLE 7: UART INTERNAL REGISTERS

ADDRESS A2 A1 A0	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor LSB	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Divisor MSB	Read/Write	
0 0 0	DREV - Device Revision Code	Read-only	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DVID - Device Identification Code	Read-only	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR ≠ 0xBF
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR ≠ 0xBF
1 0 1	LSR - Line Status Register	Read-only	
1 1 0	MSR - Modem Status Register	Read-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR ≠ 0xBF, FCTR[6] = 0
1 1 1	FLVL - RX/TX FIFO Level Counter Register	Read-only	LCR ≠ 0xBF, FCTR[6] = 1
1 1 1	EMSR - Enhanced Mode Select Register	Write-only	
ENHANCED REGISTERS			
0 0 0	TRG - RX/TX FIFO Trigger Level Register FC - RX/TX FIFO Level Counter Register	Write-only Read-only	LCR = 0xBF
0 0 1	FCTR - Feature Control Register	Read/Write	
0 1 0	EFR - Enhanced Function Register	Read/Write	
1 X X	Rsrvd	Read/Write	

.

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2 A1 A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/	0	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	LCR[7]=0
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	LCR ≠ 0xBF
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Par-ity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/	0/	0/	Internal Lopback Enable	OP2#/INT Output Enable	Rsrvd (OP1#)	RTS# Output Control	DTR# Output Control	
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Over-run Error	RX Data Ready	LCR ≠ 0xBF
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR ≠ 0xBF FCTR[6]=0
1 1 1	EMSR	WR	Rsrvd (1)	LSR Error Inter-rupt. Imd/Dly#	Auto RTS Hyst. bit-3	Auto RTS Hyst. bit-2	Rsrvd	Rsrvd	Rx/Tx FIFO Count	Rx/Tx FIFO Count	LCR ≠ 0xBF FCTR[6]=1
1 1 1	FLVL	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2 A1 A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR≠0xBF DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	0	1	0	1	0	
Enhanced Registers											
0 0 0	TRG	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
0 0 0	FC	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	FCTR	RD/WR	RX/TX Mode	SCPAD Swap	Trig Table Bit-1	Trig Table Bit-0	Rsrvd	Rsrvd	Auto RTS Hyst Bit-1	Auto RTS Hyst Bit-0	
0 1 0	EFR	RD/WR	Auto CTS Enable	Auto RTS Enable	Rsrvd	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5]	Rsrvd	Rsrvd	Rsrvd	Rsrvd	
1 X X	Rsrvd	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

5.0 INTERNAL REGISTER DESCRIPTIONS

5.1 Receive Holding Register (RHR) - Read- Only

SEE"RECEIVER" ON PAGE 14.

5.2 Transmit Holding Register (THR) - Write-Only

SEE"TRANSMITTER" ON PAGE 12.

5.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

5.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

5.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt when the character with errors is read out of the FIFO (default). Instead, LSR bits 2-4 can be programmed to generate an interrupt immediately, by setting EMSR bit-6 to a logic 1.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Reserved

This bit is reserved and should remain at a logic 0.

IER[5]: Reserved

For normal operation, this bit should be '0'.

IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from low to high.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from low to high.

5.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 9, shows the data values (bit 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

5.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty.
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- CTS# is when its transmitter toggles the input pin (from LOW to HIGH) during auto CTS flow control.
- RTS# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS flow control.

5.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- RTS# and CTS# flow control interrupts are cleared by a read to the MSR register.

TABLE 9: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)
7	1	0	0	0	0	0	CTS#, RTS# change of state
-	0	0	0	0	0	1	None (default) or Wake-up Indicator

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Interrupt Source Table 9).

ISR[4]: Reserved

ISR[5]: RTS#/CTS# Interrupt Status

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-5 indicates that the CTS# or RTS# has been de-asserted.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

5.5 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a ‘1’.

- Logic 0 = No receive FIFO reset (default)
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

Controls the behavior of the TXRDY# and RXRDY# pins. See DMA operation section for details.

- Logic 0 = Normal Operation (default).
- Logic 1 = DMA Mode.

FCR[5:4]: Transmit FIFO Trigger Select

(logic 0 = default, TX trigger level = 1)

These 2 bits set the trigger level for the transmit FIFO. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. **Table 10** below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1)

The FCTR Bits 5-4 are associated with these 2 bits. These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. **Table 10** shows the complete selections. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

TABLE 10: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION

TRIGGER TABLE	FCTR BIT-5	FCTR BIT-4	FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL	COMPATIBILITY
Table-A	0	0			0	0		1 (default)	16C550, 16C2550, 16C2552, 16C554, 16C580
			0	0			1 (default)		
			0	1			4		
			1	0			8		
			1	1			14		
Table-B	0	1			0	0		16	16C650A
					0	1		8	
					1	0		24	
					1	1		30	
			0	0			8		
			0	1			16		
			1	0			24		
			1	1			28		

TABLE 10: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION

TRIGGER TABLE	FCTR BIT-5	FCTR BIT-4	FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL	COMPATIBILITY
Table-C	1	0			0	0		8	16C654
					0	1		16	
					1	0		32	
					1	1		56	
			0	0			8		
			0	1			16		
			1	0			56		
			1	1			60		
Table-D	1	1	X	X	X	X	Programmable via TRG register. FCTR[7] = 0.	Programmable via TRG register. FCTR[7] = 1.	16x275x, 16C285x, 16C850, 16C854, 16C864

5.6 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 11 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR bit-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

TABLE 11: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, "1"
1	1	1	Forced parity to space, "0"

LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a "space", LOW state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a "space", LOW, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL and DLM) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

5.7 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force DTR# output HIGH (default).
- Logic 1 = Force DTR# output LOW.

MCR[1]: RTS# Output

The RTS# pin is a modem control output and may be used for automatic hardware flow control by enabled by EFR bit-6. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# HIGH (default).
- Logic 1 = Force RTS# LOW.

MCR[2]: Reserved

OP1# is not available as an output pin on the enhanced UART. But it is available for use during Internal Loopback Mode. In the Loopback Mode, this bit is used to write the state of the modem RI# interface signal.

MCR[3]: OP2# Output / INT Output Enable

This bit enables or disables the operation of INT, interrupt output. If INT output is not used, OP2# can be used as a general purpose output. Also, if 16/68# pin selects Motorola bus interface mode, this bit must be set to logic 0.

- Logic 0 = INT (A-B) outputs disabled (three state mode) and OP2# output set HIGH(default).
- Logic 1 = INT (A-B) outputs enabled (active mode) and OP2# output set LOW.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and **Figure 10**.

MCR[7:5]: Reserved

For normal operation, these register bits should be ’0’.

5.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Error Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[2]: Receive Data Parity Error Tag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Tag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[4]: Receive Break Error Tag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was LOW for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to a logic 1 whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in any of the bytes in the RX FIFO.

5.9 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface input signals. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used for general purpose inputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a LOW to HIGH, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A HIGH on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a LOW will resume data transmission. Normally MSR bit-4 bit is the complement of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

Normally this bit is the complement of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

Normally this bit is the complement of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

Normally this bit is the complement of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

5.10 Scratch Pad Register (SPR) - Read/Write

This is a 8-bit general purpose register for the user to store temporary data.

5.11 Enhanced Mode Select Register (EMSR)

This register replaces SPR (during a Write) and is accessible only when FCTR[6] = 1.

EMSR[1:0]: Receive/Transmit FIFO Level Count (Write-Only)

When Scratchpad Swap (FCTR[6]) is asserted, EMSR bits 1-0 controls what mode the FIFO Level Counter is operating in.

TABLE 12: SCRATCHPAD SWAP SELECTION

FCTR[6]	EMSR[1]	EMSR[0]	Scratchpad is
0	X	X	Scratchpad
1	X	0	RX FIFO Level Counter Mode
1	0	1	TX FIFO Level Counter Mode
1	1	1	Alternate RX/TX FIFO Counter Mode

During Alternate RX/TX FIFO Level Counter Mode, the first value read after EMSR bits 1-0 have been asserted will always be the RX FIFO Level Counter. The second value read will correspond with the TX FIFO Level Counter. The next value will be the RX FIFO Level Counter again, then the TX FIFO Level Counter and so on and so forth.

EMSR[3:2]: Reserved

For normal operation, these bits should be ’0’.

EMSR[5:4]: Extended RTS Hysteresis

TABLE 13: AUTO RTS HYSTERESIS

EMSR BIT-5	EMSR BIT-4	FCTR BIT-1	FCTR BIT-0	RTS# HYSTERESIS (CHARACTERS)
0	0	0	0	0
0	0	0	1	±4
0	0	1	0	±6
0	0	1	1	±8
0	1	0	0	±8
0	1	0	1	±16
0	1	1	0	±24
0	1	1	1	±32
1	0	0	0	±40
1	0	0	1	±44
1	0	1	0	±48
1	0	1	1	±52
1	1	0	0	±12
1	1	0	1	±20
1	1	1	0	±28
1	1	1	1	±36

EMSR[6]: LSR Interrupt Mode

- Logic 0 = LSR Interrupt Delayed (for 16C550 compatibility, default). LSR bits 2, 3, and 4 will generate an interrupt when the character with the error is in the RHR.
- Logic 1 = LSR Interrupt Immediate. LSR bits 2, 3, and 4 will generate an interrupt as soon as the character is received into the FIFO.

EMSR[7]: Reserved

For normal operation, this bit should be '1'.

5.12 FIFO Level Register (FLVL) - Read-Only

The FIFO Level Register replaces the Scratchpad Register (during a Read) when FCTR[6] = 1. Note that this is not identical to the FIFO Data Count Register which can be accessed when LCR = 0xBF.

FLVL[7:0]: FIFO Level Register

This register provides the FIFO counter level for the RX FIFO or the TX FIFO or both depending on EMSR[1:0]. See Table 12 for details.

5.13 Baud Rate Generator Registers (DLL and DLM) - Read/Write

These registers make-up the value of the baud rate divisor. SEE"PROGRAMMABLE BAUD RATE GENERATOR" ON PAGE 12.

5.14 Device Identification Register (DVID) - Read Only

This register contains the device ID (0x0A). Prior to reading this register, DLL and DLM should be set to 0x00.

5.15 Device Revision Register (DREV) - Read Only

This register contains the device revision information. For example, 0x01 means revision A. Prior to reading this register, DLL and DLM should be set to 0x00.

5.16 Trigger Level Register (TRG) - Write-Only

User Programmable Transmit/Receive Trigger Level Register. If both the TX and RX trigger levels are used, the TX trigger levels must be set before the RX trigger levels.

TRG[7:0]: Trigger Level Register

These bits are used to program desired trigger levels when trigger Table-D is selected. FCTR bit-7 selects between programming the RX Trigger Level (a logic 0) and the TX Trigger Level (a logic 1).

5.17 RX/TX FIFO Level Count Register (FC) - Read-Only

This register is accessible when LCR = 0xBF. Note that this register is not identical to the FIFO Level Count Register which is located in the general register set when FCTR bit-6 = 1 (Scratchpad Register Swap). It is suggested to read the FIFO Level Count Register at the Scratchpad Register location when FCTR bit-6 = 1. See Table 12.

FC[7:0]: RX/TX FIFO Level Count

Receive/Transmit FIFO Level Count. Number of characters in Receiver FIFO (FCTR[7] = 0) or Transmitter FIFO (FCTR[7] = 1) can be read via this register. Reading this register is not recommended when transmitting or receiving data.

5.18 Feature Control Register (FCTR) - Read/Write

FCTR[1:0]: RTS Hysteresis

User selectable RTS# hysteresis levels for hardware flow control application. After reset, these bits are set to "0" to select the next trigger level for hardware flow control. See Table 13 for more details.

FCTR[3:2]: Reserved

For normal operation, these bits should be ’0’.

FCTR[5:4]: Transmit/Receive Trigger Table Select

See Table 10 for more details.

TABLE 14: TRIGGER TABLE SELECT

FCTR BIT-5	FCTR BIT-4	TABLE
0	0	Table-A (TX/RX)
0	1	Table-B (TX/RX)
1	0	Table-C (TX/RX)
1	1	Table-D (TX/RX)

FCTR[6]: Scratchpad Swap

- Logic 0 = Scratch Pad register is selected as general read and write register. ST16C550 compatible mode.
- Logic 1 = FIFO Level Count register (Read-Only), Enhanced Mode Select Register (Write-Only). Number of characters in transmit or receive FIFO can be read via scratch pad register when this bit is set. Enhanced Mode Select Register is selected when it is written into.

FCTR[7]: Programmable Trigger Register Select

If using both programmable TX and RX trigger levels, TX trigger levels must be set before RX trigger levels.

- Logic 0 = Registers TRG and FC selected for RX.
- Logic 1 = Registers TRG and FC selected for TX.

5.19 Enhanced Feature Register (EFR)

EFR[3:0]: Reserved

For normal operation, these bits should be ’0’.

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 (MCR bits 7-5 should remain at their default values of ’0’). After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to a logic 0 to be compatible with ST16C550 mode (default).
- Logic 1 = Enables the above-mentioned register bits to be modified by the user.

EFR[5]: Reserved

For normal operation, this bit should be ’0’.

EFR[6]: Auto RTS Flow Control Enable

RTS# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS de-asserts HIGH at the next upper trigger level or hysteresis level. RTS# will return LOW when FIFO data falls below the next lower trigger level. The RTS# output must be asserted (LOW) before the auto RTS can take effect. RTS# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS flow control is disabled (default).
- Logic 1 = Enable Automatic RTS flow control.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS Flow Control.

- Logic 0 = Automatic CTS flow control is disabled (default).
- Logic 1 = Enable Automatic CTS flow control. Data transmission stops when CTS# input de-asserts HIGH. Data transmission resumes when CTS# returns LOW.

TABLE 15: UART RESET CONDITIONS

REGISTERS	RESET STATE
DLM, DLL	DLM = 0x00 and DLL = 0x01. Only resets to these values during a power up. They do not reset when the Reset Pin is asserted.
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = Logic 0 Bits 7-4 = Logic levels of the inputs inverted
SPR	Bits 7-0 = 0xFF
EMSR	Bits 7-0 = 0x80
FLVL	Bits 7-0 = 0x00
EFR	Bits 7-0 = 0x00
FCTR	Bits 7-0 = 0x00
I/O SIGNALS	**RESET STATE**
TX	HIGH
RTS#	HIGH
DTR#	HIGH
RXRDY#	HIGH
TXRDY#	LOW
INT (IRQ#)	Three-State Condition (16 mode) HIGH (68 mode)

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	4 Volts
Voltage at Any Pin	GND-0.3V to 4V
Operating Temperature	-40^{o} to +85^{o}C
Storage Temperature	-65^{o} to +150^{o}C
Package Dissipation	500 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (48-QFN)	theta-ja =28^{o}C/W, theta-jc = 10.5^{o}C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

TA=0^{o} TO 70^{o}C (-40^{o} TO +85^{o}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.25V TO 3.6V

SYMBOL	PARAMETER	LIMITS 2.5V MIN	LIMITS 2.5V MAX	LIMITS 3.3V MIN	LIMITS 3.3V MAX	UNITS	CONDITIONS
V_{ILCKC}	CMOS/TTL Clock Input Low Level	-0.3	0.4	-0.3	0.6	V	
V_{IHCKC}	CMOS/TTL Clock Input High Level	2.0	VCC	2.4	VCC	V	
V_{ILCKD} V_{IHCKD}	Differential Clock Input Amplitude	200		200		mV	
V_{IL}	Input Low Voltage	-0.3	0.5	-0.3	0.7	V	
V_{IH}	Input High Voltage	1.8	5.5	2.0	5.5	V	
V_{OL}	Output Low Voltage		 0.4		0.4	V V	I_{OL} = 4 mA I_{OL} = 2 mA
V_{OH}	Output High Voltage	 1.8		2.0		V V	I_{OH} = -1 mA I_{OH} = -400 uA
I_{IL}	Input Low Leakage Current		±10		±10	uA	
I_{IH}	Input High Leakage Current		±10		±10	uA	
C_{IN}	Input Pin Capacitance		5		5	pF	
I_{CC}	Power Supply Current		50		60	mA	

AC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC=2.25 - 3.63V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 2.5V ± 10%		LIMITS 3.3V ± 10%		UNIT
		MIN	MAX	MIN	MAX	
ECLK	External Clock (CMOS/TTL or Differential)	16		16		MHz
T_{AS}	Address Setup Time (16 mode)	0		0		ns
T_{AH}	Address Hold Time (16 mode)	0		0		ns
T_{CS}	Chip Select Width (16 mode)	50		40		ns
T_{RD}	IOR# Strobe Width (16 mode)	50		40		ns
T_{DY}	Read Cycle Delay (16 mode)	50		40		ns
T_{RDV}	Data Access Time (16 mode)		45		35	ns
T_{DD}	Data Disable Time (16 mode)		25		25	ns
T_{WR}	IOW# Strobe Width (16 mode)	50		40		ns
T_{DY}	Write Cycle Delay (16 mode)	50		40		ns
T_{DS}	Data Setup Time (16 mode)	10		10		ns
T_{DH}	Data Hold Time (16 mode)	5		5		ns
T_{ADS}	Address Setup (68 Mode)	0		0		ns
T_{ADH}	Address Hold (68 Mode)	0		0		ns
T_{RWS}	R/W# Setup to CS# (68 Mode)	0		0		ns
T_{RDA}	Read Data Access (68 mode)		45		35	ns
T_{RDH}	Read Data Disable (68 mode)		25		25	ns
T_{WDS}	Write Data Setup (68 mode)	10		10		ns
T_{WDH}	Write Data Hold (68 Mode)	5		5		ns
T_{RWH}	CS# De-asserted to R/W# De-asserted (68 Mode)	5		5		ns
T_{CSL}	CS# Width (68 Mode)	50		40		ns
T_{CSD}	CS# Cycle Delay (68 Mode)	50		40		ns
T_{WDO}	Delay From IOW# To Output		50		50	ns
T_{MOD}	Delay To Set Interrupt From MODEM Input		50		50	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		50		50	ns
T_{SSI}	Delay From Stop To Set Interrupt		1		1	Bclk
T_{RRI}	Delay From IOR# To Reset Interrupt		45		45	ns
T_{SI}	Delay From Stop To Interrupt		45		45	ns

AC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC=2.25 - 3.63V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 2.5V ± 10%		LIMITS 3.3V ± 10%		UNIT
		MIN	MAX	MIN	MAX	
T_{INT}	Delay From Initial INT Reset To Transmit Start	8	24	8	24	Bclk
T_{WRI}	Delay From IOW# To Reset Interrupt		45		45	ns
T_{SSR}	Delay From Stop To Set RXRDY#		1		1	Bclk
T_{RR}	Delay From IOR# To Reset RXRDY#		45		45	ns
T_{WT}	Delay From IOW# To Set TXRDY#		45		45	ns
T_{SRT}	Delay From Center of Start To Reset TXRDY#		8		8	Bclk
T_{RST}	Reset Pulse Width	40		40		ns
Bclk	Baud Clock	16X of data rate				Hz

FIGURE 11. MODEM INPUT/OUTPUT TIMING

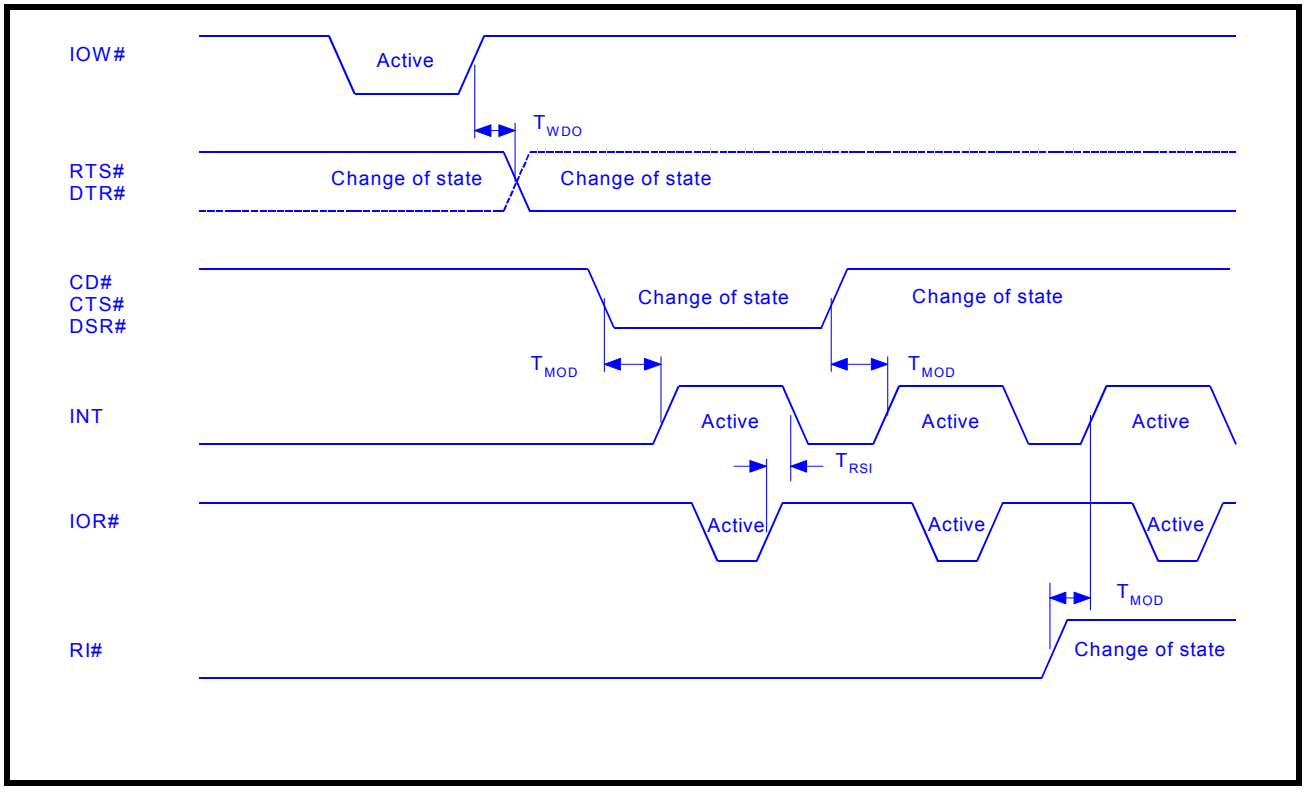


FIGURE 12. 16 MODE (INTEL) DATA BUS READ TIMING - PARALLEL MODE

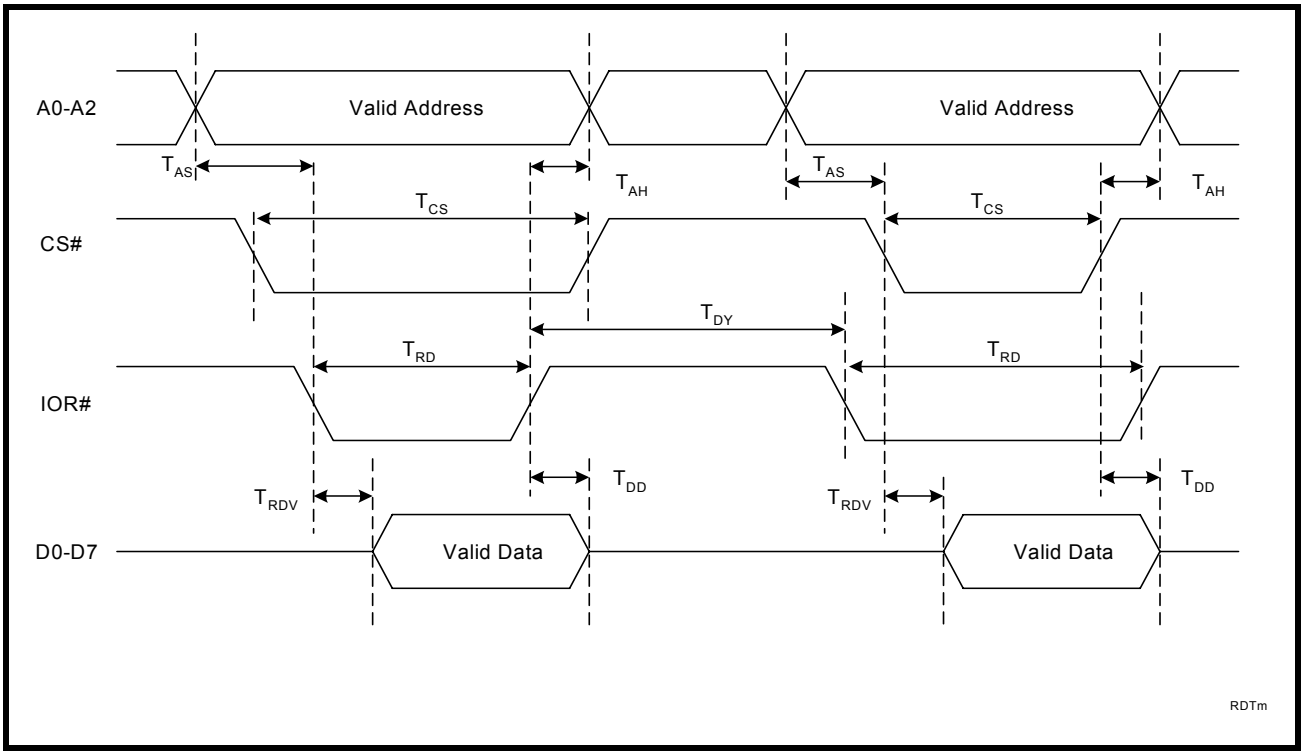


FIGURE 13. 16 MODE (INTEL) DATA BUS WRITE TIMING - PARALLEL MODE

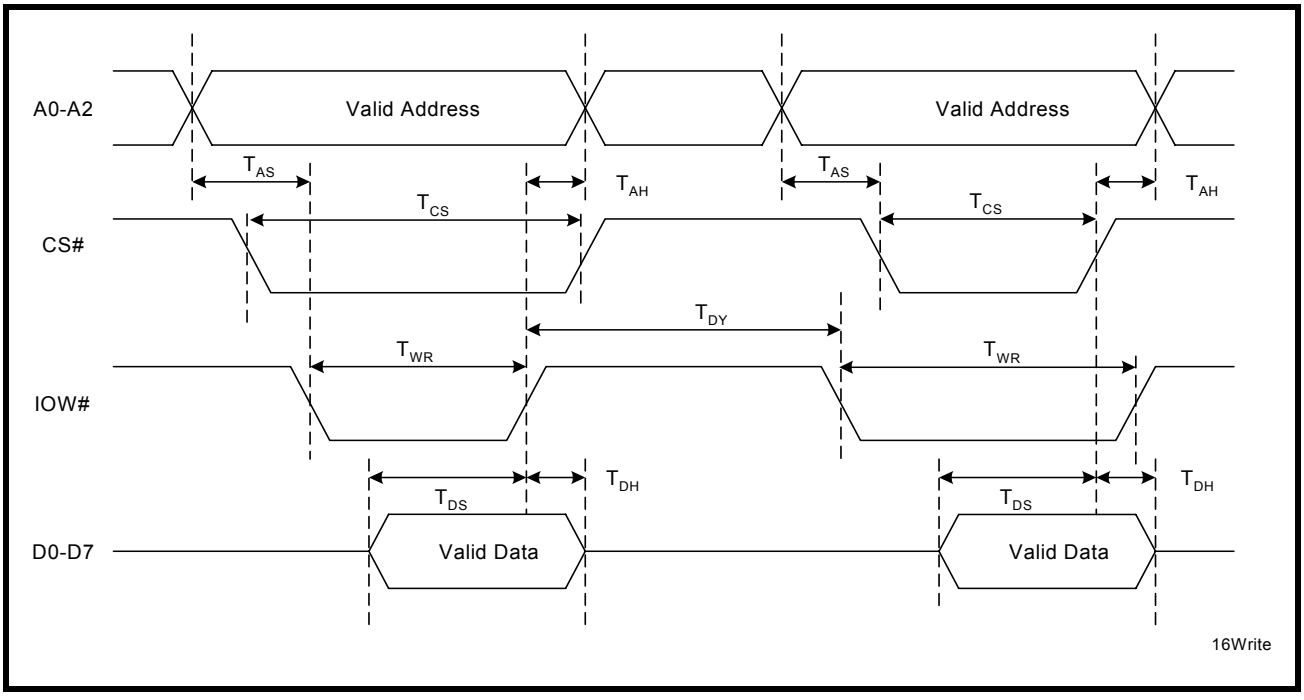


FIGURE 14. 68 MODE (MOTOROLA) DATA BUS READ TIMING - PARALLEL MODE

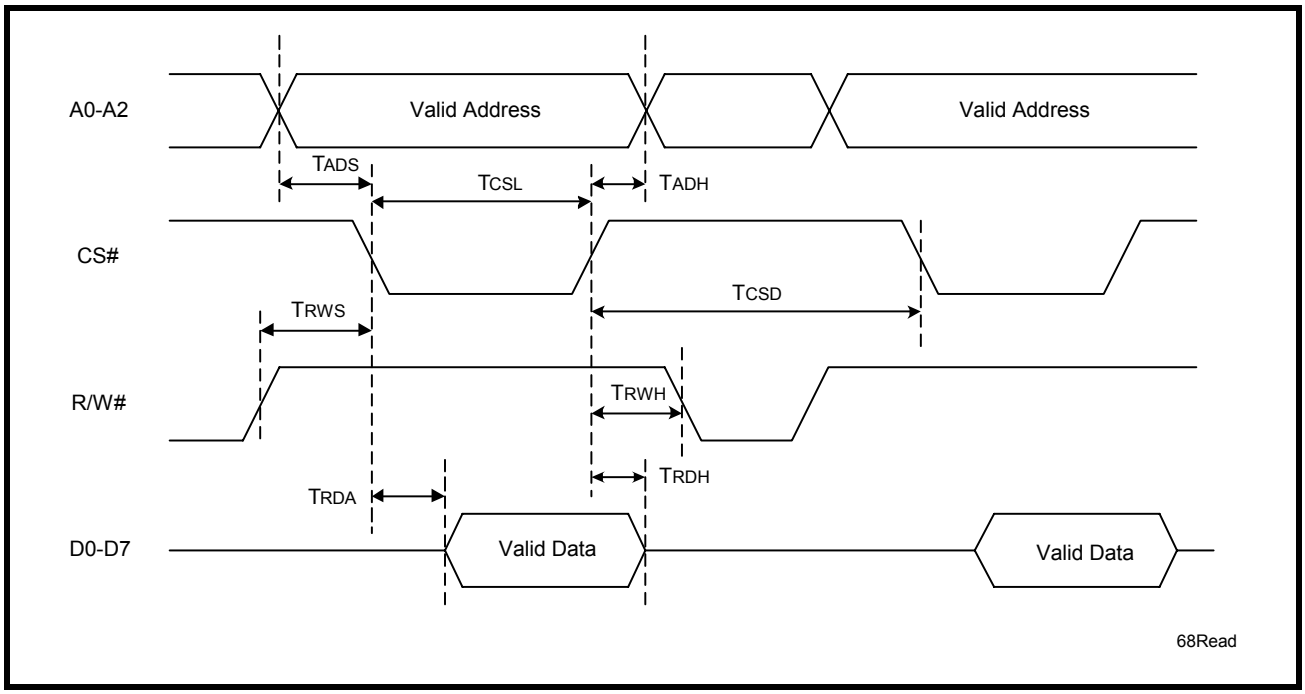


FIGURE 15. 68 MODE (MOTOROLA) DATA BUS WRITE TIMING - PARALLEL MODE

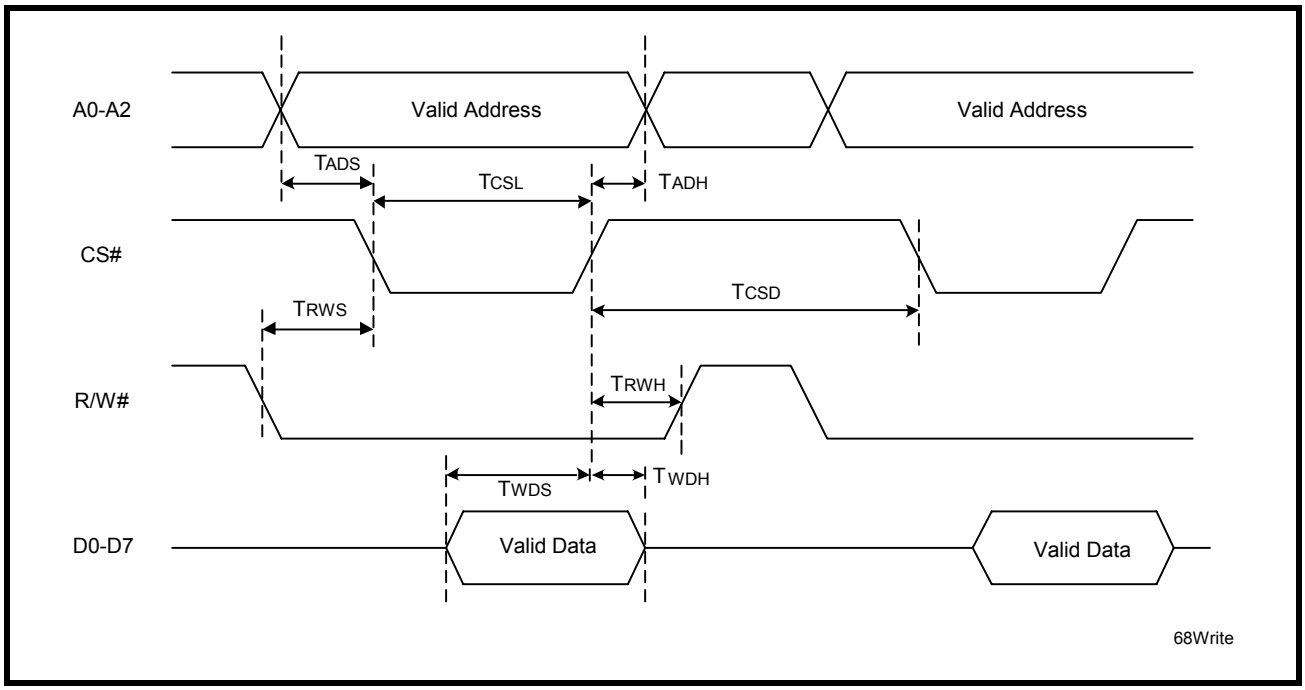


FIGURE 16. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE] - PARALLEL MODE

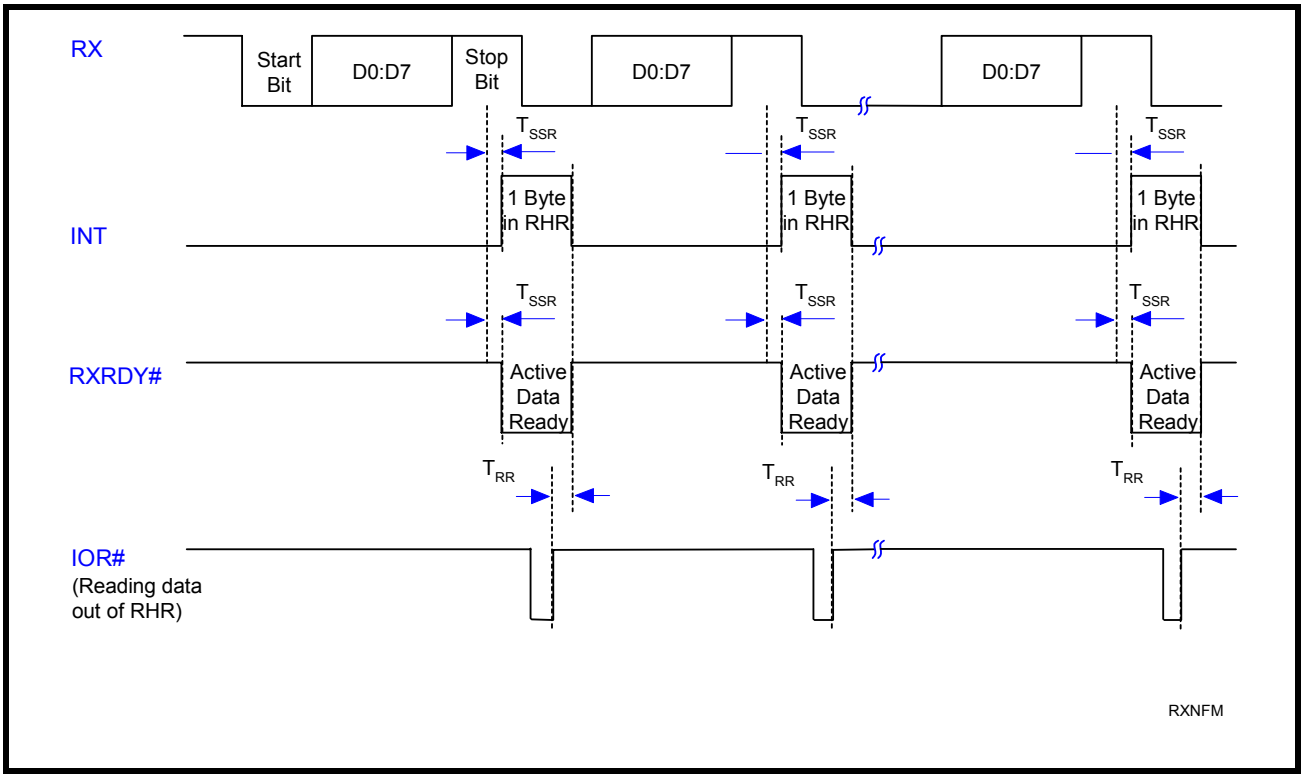


FIGURE 17. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE] - PARALLEL MODE

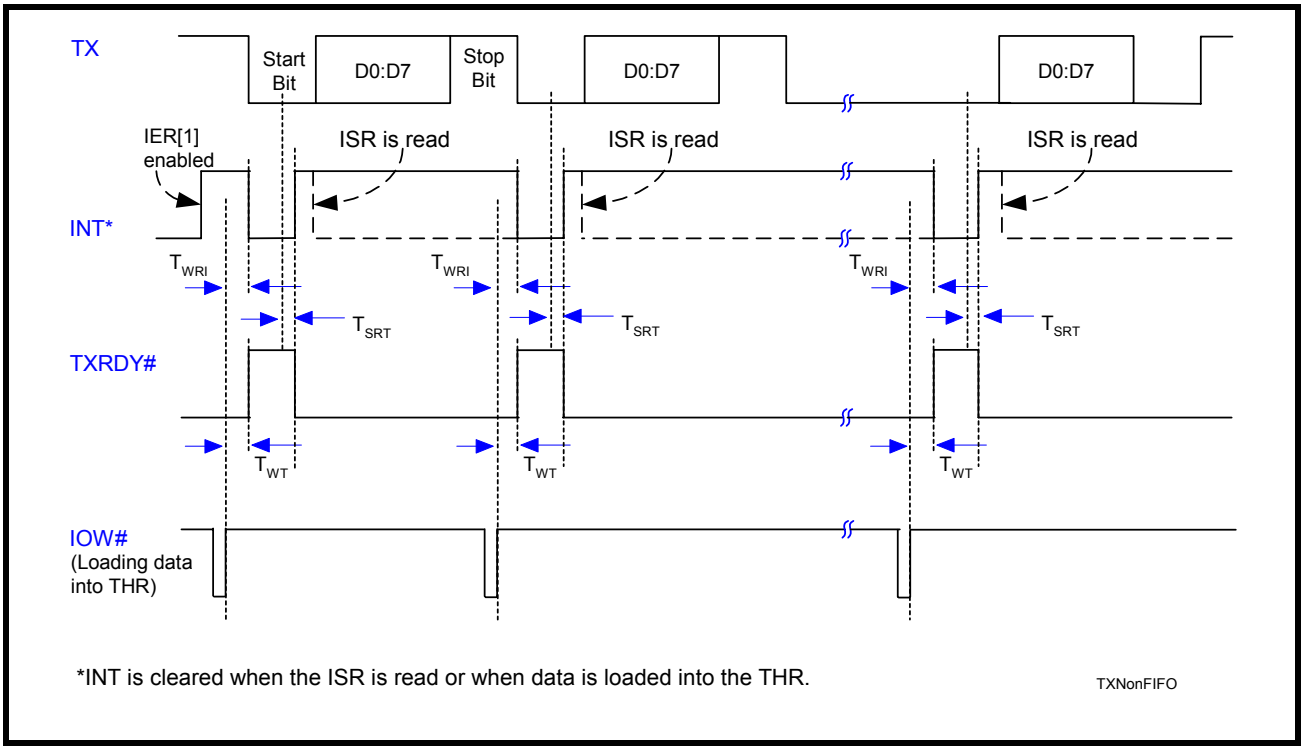


FIGURE 18. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED] - PARALLEL MODE

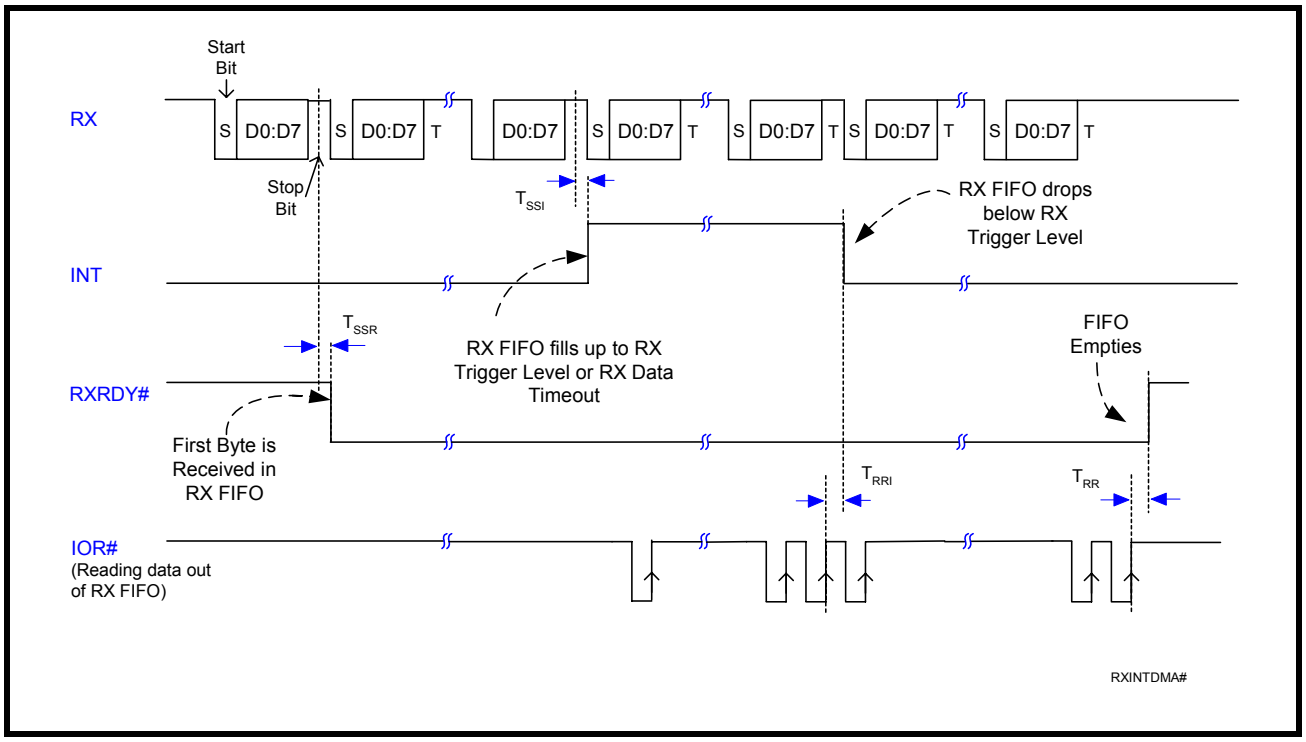


FIGURE 19. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED] - PARALLEL MODE

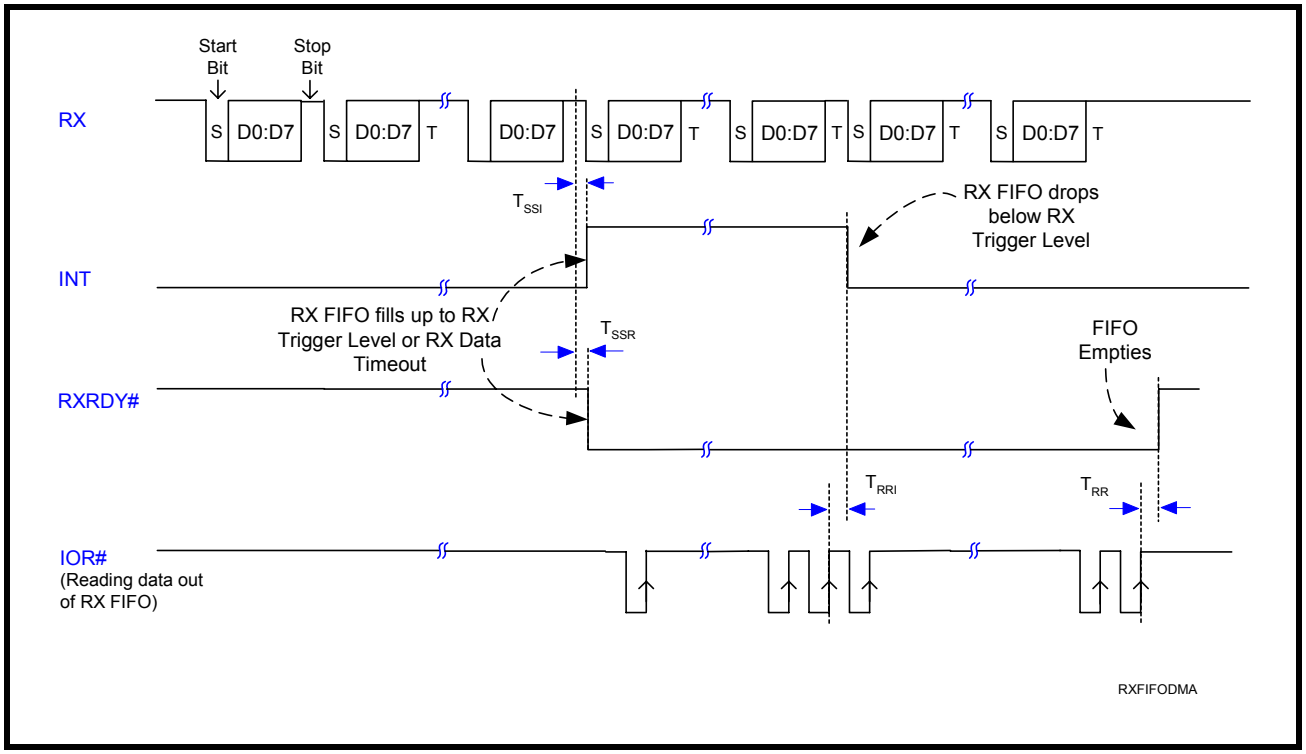


FIGURE 20. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED]

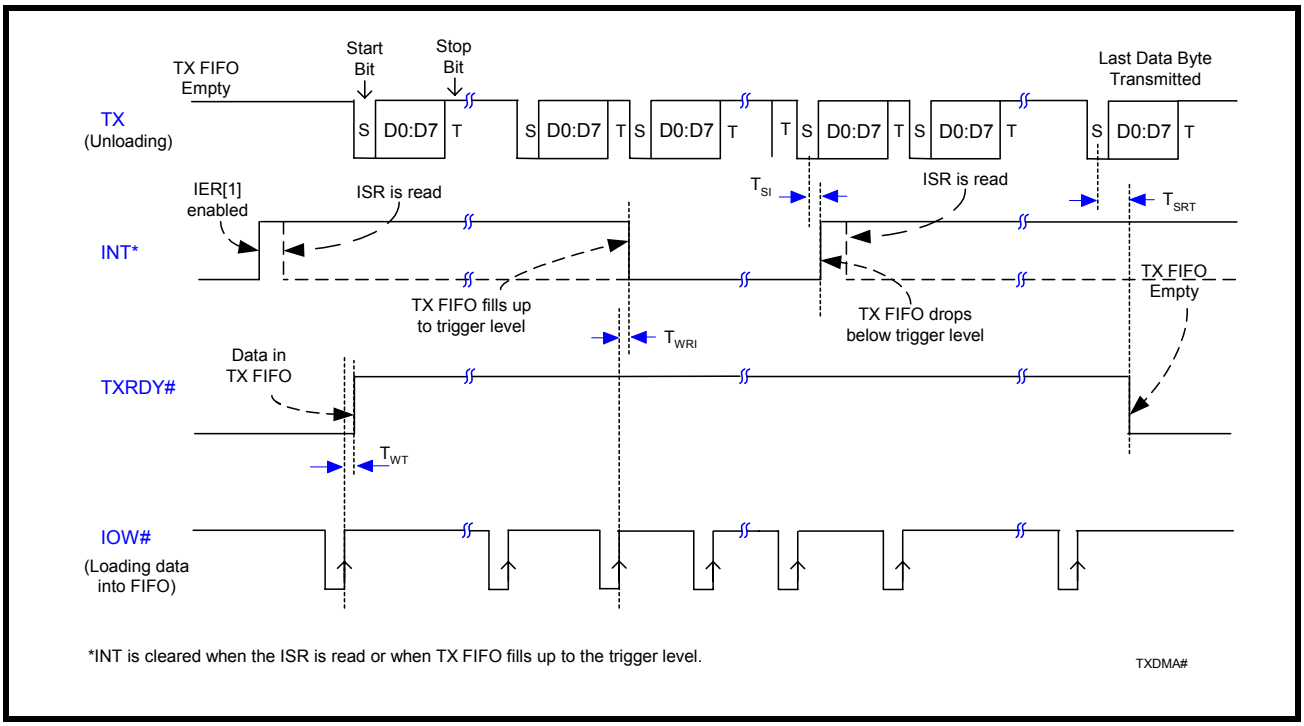
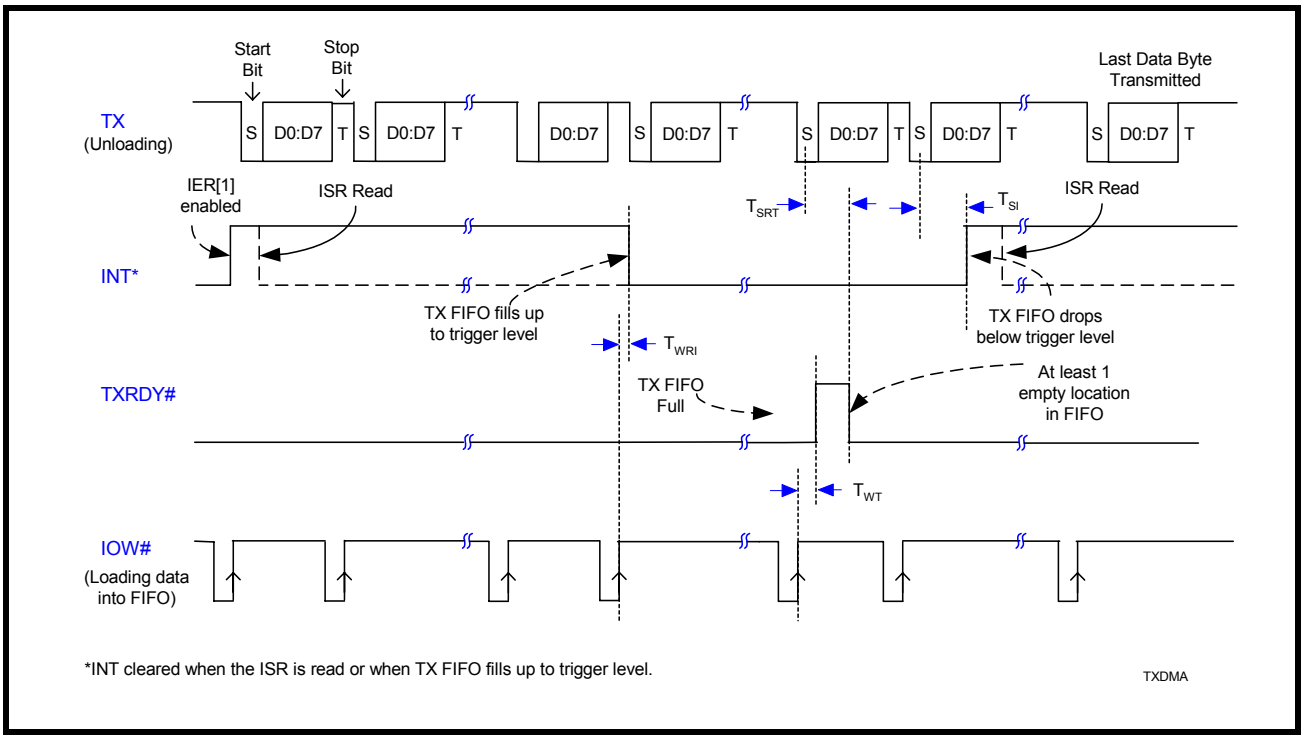
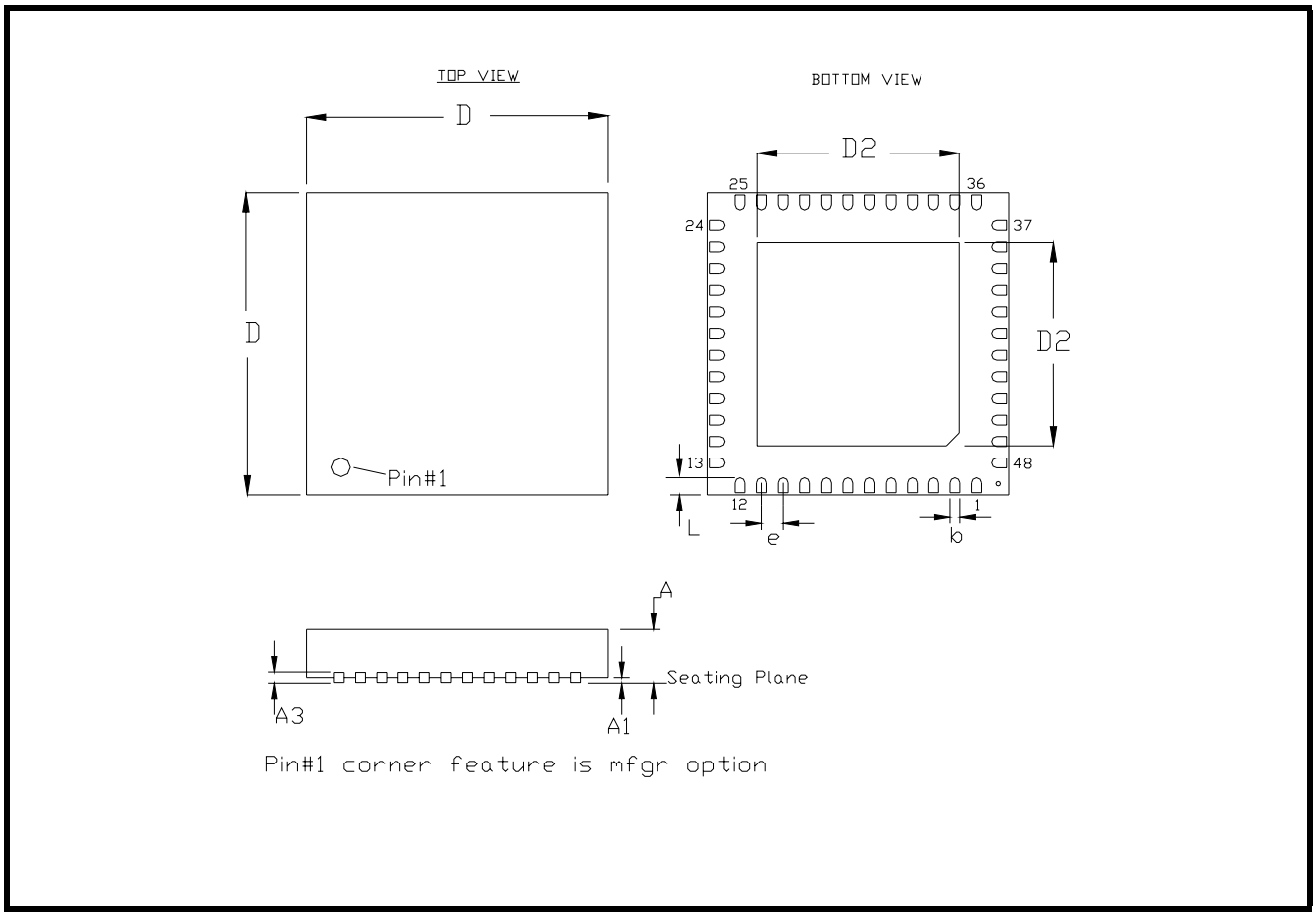


FIGURE 21. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED] - PARALLEL MODE



PACKAGE DIMENSIONS (48 PIN QFN - 7 X 7 X 0.9 mm)



Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A3	0.006	0.010	0.15	0.25
D	0.270	0.281	6.85	7.15
D2	0.201	0.209	5.10	5.30
b	0.007	0.012	0.18	0.30
e	0.0197 BSC		0.50 BSC	
L	0.012	0.020	0.30	0.50

REVISION HISTORY

DATE	REVISION	DESCRIPTION
February 2007	P1.0.0	Preliminary Datasheet.
March 2008	1.0.0	Final Datasheet.

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