TDA3683

Multiple voltage regulator with switch and ignition buffer

Rev. 02 — 7 October 2005 Product data sheet

1. General description

- The TDA3683 is a multiple output voltage regulator with a power switch and an ignition buffer. Several protections and diagnostic options are incorporated in this design.
- The TDA3683 is primarily developed to cover the complete power supply requirements in car radio applications.
- The standby regulators (regulators 1, 2 and 3) are especially designed to supply digital circuitry that has to be permanently connected e.g. Controller Area Network (CAN) bus, Digital Signal Processor (DSP) core and the microcontroller. In combination with the reset delay capacitor (pin RDC1 or pin RDC2/3) and the reset function (pin RST1 or pin RST2/3), a proper start-up sequence for a microcontroller is guaranteed. The storage capacitor (pin STC) makes the standby regulator outputs insensitive for short battery drops (e.g. during engine start-up).
- The switched regulators (regulators 4, 5, 6 and 7) are intended to be used as supply for the tuner, logic, sound processor and CD / tape control.
- The power switch (pin PSW) can be used for switching the electrically powered antenna, display unit and CD / tape drives.
- The ignition buffer is intended to produce a clean logic output signal when a polluted ignition key signal is used as input.

2. Features

- Three enable pin controlled standby regulators:
  - REG1: 5 V / 600 mA controlled by the EN1 input
  - REG2: 3.3 V / 200 mA controlled by the EN2/3 input
  - REG3: 1.9 V / 150 mA controlled by the EN2/3 input
- Four mode pin controlled switched regulators:
  - REG4: 8.5 V / 350 mA
  - REG5: 5 V / 1.8 A
  - REG6: 3.3 V / 1.2 A
  - REG7: 2.4 V to 10 V / 2 A adjustable using external resistor divider
- One mode pin controlled power switch; 2.2 A continuous and 3 A surge, with delayed lower current limit so as to be less sensitive to inrush currents
- One independent ignition buffer (inverted output, open-collector) with good input protection against high transients
- A storage capacitor is included to provide back-up supply for the standby regulators in the event of loss of battery supply

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- A hold output (3-state) which can be used to communicate to a microcontroller in the event of an internal or external fault condition, such as:
  - Low supply indication in Standby mode
  - One or more switched regulators (except REG7) out of regulation
  - Power switch output short-circuited to ground
  - Load dump, thermal pre-warning and thermal shutdown
- Reset outputs (push-pull output stage) can be used to call a microcontroller in a smooth way (adjustable delay) at the first power-up
- Two supply pins that can withstand load dump pulses and negative supply voltages; the second supply pin (connected to REG5 and REG6) can be supplied from a separate external voltage (e.g. DC-to-DC downconverter) to reduce power dissipation
- All regulator and power switch outputs are short-circuit proof to ground and supply lines; the dissipation is limited in this condition since all regulators (except REG3) and power switch have a foldback current protection incorporated
- The TDA3683 has three modes of operation:
  - Sleep: all outputs disabled (very low quiescent current)
  - Standby: one or more standby regulators enabled (low quiescent current)
  - On: all outputs enabled
- The standby regulators (including the reset function) and the ignition buffer also function during load dump and thermal shutdown; the switched regulators and power switch will be disabled during these conditions
- Hysteresis is incorporated on internal switching levels
- The TDA3683 is protected against Electrostatic Discharge (ESD) on all pins
- DBS23 package with low thermal resistance and flexible leads.

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{P1}	supply voltage 1	operating	9	14.4	18	V
		reverse polarity; non-operating	-	-	18	V
		regulators 1, 2 and 3 on	4.0	14.4	50	V
		jump start; t ≤ 10 minutes	-	-	30	V
		load dump protection; t ≤ 50 ms; $t_r \geq 2.5$ ms	-	-	50	V
V_{P2}	supply voltage 2	operating	6.5	14.4	18	V
		reverse polarity; non-operating	-	-	18	V
		regulators 1, 2 and 3 on	0	-	50	V
		jump start; t ≤ 10 minutes	-	-	30	V
		load dump protection; t ≤ 50 ms; $t_r \geq 2.5$ ms	-	-	50	V
$I_{q(tot)}$	total quiescent supply current	V_{EN1}, $V_{EN2/3}$ and V_{MODE} < 0.8 V	-	5	30	µA
		V_{MODE} and V_{IGNIN} < 0.8 V; V_{EN1} and $V_{EN2/3}$ > 2.4 V	-	300	450	µA
T_j	junction temperature	operating	–40	-	+150	°C

Table 1: Quick reference data *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage regulator; V_P = 14.4 V						
$V_{o(REG1)}$	regulator 1 output voltage	1 mA ≤ I_{REG1} ≤ 600 mA	4.75	5.0	5.25	V
$V_{o(REG2)}$	regulator 2 output voltage	1 mA ≤ I_{REG2} ≤ 200 mA	3.15	3.3	3.45	V
$V_{o(REG3)}$	regulator 3 output voltage	1 mA ≤ I_{REG3} ≤ 150 mA	1.72	1.9	2.0	V
$V_{o(REG4)}$	regulator 4 output voltage	1 mA ≤ I_{REG4} ≤ 350 mA	8.1	8.5	8.9	V
$V_{o(REG5)}$	regulator 5 output voltage	1 mA ≤ I_{REG5} ≤ 1800 mA	4.75	5.0	5.25	V
$V_{o(REG6)}$	regulator 6 output voltage	1 mA ≤ I_{REG6} ≤ 1200 mA	3.15	3.3	3.45	V
$V_{o(REG7)}$	output voltage of regulator 7	1 mA ≤ I_{REG7} ≤ 2000 mA	V_o – 5 %	2.4 to 10	V_o + 5 %	V
Power switch						
$V_{drop(PSW)}$	drop-out voltage	I_{PSW} = 1 A; V_{P1} = V_{P2} = 13.5 V	-	0.45	0.65	V
		I_{PSW} = 2.2 A; V_{P1} = V_{P2} = 13.5 V	-	1.0	1.8	V
$I_{M(PSW)}$	peak current	V_{P1} = V_{P2} < 17 V	3	-	-	A

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA3683J	DBS23P	plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm)	SOT411-1
TDA3683SD	RDBS23P	plastic rectangular DIL-bent-SIL (reverse bent) power package; 23 leads (row spacing 2.54 mm)	SOT889-1

5. Block diagram

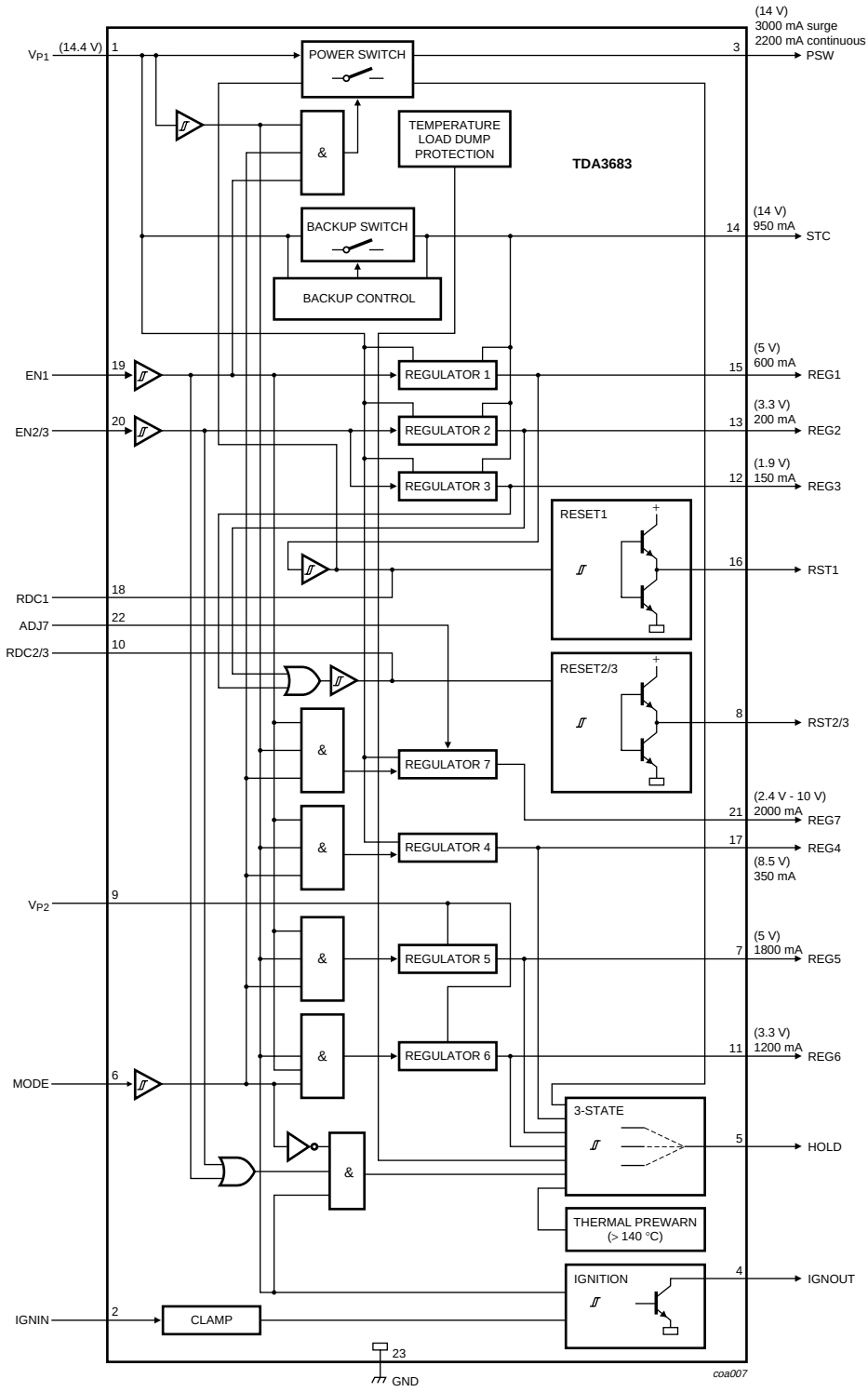


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

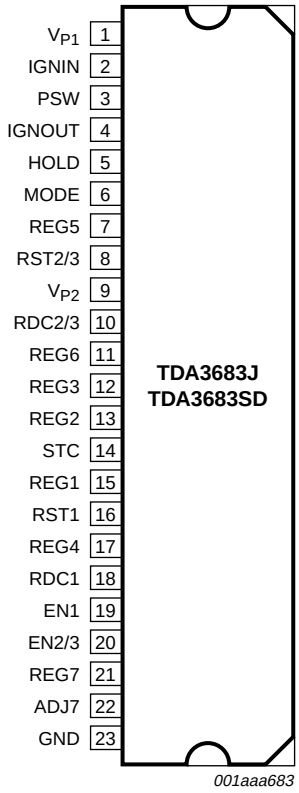


Fig 2. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
V_{P1}	1	supply voltage 1
IGNIN	2	ignition input
PSW	3	power switch output
IGNOUT	4	ignition output
HOLD	5	hold output
MODE	6	enable input for regulators 4, 5, 6, 7 and power switch
REG5	7	regulator 5 output
RST2/3	8	reset output for regulators 2 and 3
V_{P2}	9	supply voltage 2 (for regulators 5 and 6)
RDC2/3	10	reset delay capacitor for regulators 2 and 3
REG6	11	regulator 6 output
REG3	12	regulator 3 output

Table 3: Pin description *...continued*

Symbol	Pin	Description
REG2	13	regulator 2 output
STC	14	storage capacitor (backup) output
REG1	15	regulator 1 output
RST1	16	reset output for regulator 1
REG4	17	regulator 4 output
RDC1	18	reset delay capacitor for regulator 1
EN1	19	enable input for regulator 1
EN2/3	20	enable input for regulators 2 and 3
REG7	21	regulator 7 output
ADJ7	22	regulator 7 adjust input
GND	23	ground / substrate [1]

[1] The heat tab is internally connected to pin GND.

7. Functional description

The TDA3683 is a multiple output voltage regulator with a power switch and ignition buffer. The device is primarily intended for use in car radio applications. An overall functional description of the building blocks is given in the following sections.

7.1 Standby regulators

The standby regulators (pins REG1, REG2 and REG3) are used for digital circuitry that has to be permanently connected to a supply voltage (e.g. CAN bus DSP core or microcontroller). REG1 is controlled by its own active HIGH enable input (EN1). REG2 and REG3 have a combined enable input (EN2/3) with similar logic properties. Permanent voltage tracking will exist between REG2 and REG3 during power-up and power-down. All standby regulators have a low quiescent current and will not be switched off during thermal shutdown and load dump conditions. The outputs are protected against overload and short-circuit conditions by a current limit / foldback protection.

7.2 Switched regulators

The switched regulators (pins REG4, REG5, REG6 and REG7) are activated by the active HIGH mode input. The regulators are protected against overload and short-circuit conditions by a current limit / foldback protection. They will be switched off during thermal shutdown and load dump conditions. The output voltage of REG7 can be adjusted (2.4 V to 10 V) by using two external resistors connected between the regulator output, the feedback input and ground; see Figure 10. REG7 has a built-in flyback clamp for use in case of inductive loads.

7.3 Power switch

The power switch (pin PSW) is activated by the MODE input. It is switched off during thermal shutdown and load dump conditions. The power switch output voltage is internally clamped at 16 V to protect connected application circuitry (e.g. display and CD / tape drives). The power switch has three different output current modes, depending on its output voltage, the reset capacitor (RDC1) and the junction temperature (i.e. high current, low current and foldback protection); see Figure 7. In the event of an overload the power switch can maintain the maximum output current for a limited period of time (determined by the integration time of the reset delay capacitor) before it drops back to the lower output current capability. This functionality is implemented to prevent, in case of loads such as light bulbs, relays or electrical motors, the power switch from folding back on momentary high inrush currents. In the event of junction temperatures above 150 °C, the power switch will drop back to the lower output current capability.The power switch has a built-in flyback clamp for use in case of inductive loads.

7.4 Enable and mode inputs

The enable inputs (pins EN1 and EN2/3) are used to switch on or switch off the standby regulators. The mode input (MODE) is used to enable the switched regulators and the power switch. When all of these inputs are LOW the circuit is in Sleep mode and only the enable detection circuit and the supply overvoltage protection circuit are active. In Sleep mode the device draws a very small quiescent current from the supply. When at least one of the enable inputs is activated the circuit will operate in Standby mode. When the mode input is activated the on condition will be established; before the MODE pin can be activated at least one of the standby regulators must be activated. The enable and mode inputs are 3.3 V and 5 V CMOS logic compatible. A detailed description of the enable and mode pin dependencies is given in Table 4.

Table 4: Enable and mode pin dependencies

Pin			Description
EN1	EN2/3	MODE	
0	0	0	standby regulators, switched regulators, power switch and ignition buffer disabled
0	0	1	standby regulators, switched regulators, power switch and ignition buffer disabled
0	1	0	standby regulators 2 and 3 and ignition buffer enabled; standby regulator 1, switched regulators and power switch disabled
0	1	1	standby regulators 2 and 3, switched regulators and ignition buffer enabled; standby regulator 1 and power switch disabled
1	0	0	standby regulator 1 and ignition buffer enabled; standby regulators 2 and 3, switched regulators and power switch disabled
1	0	1	standby regulator 1, switched regulators, power switch and ignition buffer enabled; standby regulators 2 and 3 disabled
1	1	0	standby regulators and ignition buffer enabled; switched regulators and power switch disabled
1	1	1	standby regulators, ignition buffer, switched regulators and power switch enabled

7.5 Storage capacitor

The storage capacitor (pin STC) is used as a back-up supply for the standby regulators when the battery (pins V_{P1} / V_{P2}) can no longer provide the supply. This situation may occur for cold weather engine starts. The rising and falling storage capacitor voltage threshold levels determine if the standby regulators can be switched on.

The storage capacitor pin is not intended to be used as an output (e.g. supply switch). No external load should be connected to this pin.

7.6 Reset delay capacitors

The reset delay capacitors (pins RDC1 and RDC2/3) are used to delay the reset pulse (RST1 and RST2/3) starting from the time the associated standby regulator output voltage comes within its regulated voltage range i.e. crosses the rising reset threshold level. An internal current source is used to charge the reset delay capacitor. The reset output will be released (output goes HIGH) when the voltage on the reset delay capacitor crosses the rising threshold level.

If the associated standby regulator voltage drops out of its regulated voltage range (drops below its falling reset threshold level) the reset delay capacitor will be discharged with a relatively high sink current. The reset output will be activated (output goes LOW) when the reset delay capacitor crosses the falling threshold level. This feature is included to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of the relevant standby regulators during a start-up sequence. It should be noted that RDC1 is also used as a time constant for the delayed current protection of the power switch.

7.7 Reset outputs

The reset function depends on the reset delay capacitor voltage and includes hysteresis to avoid oscillation at the threshold level. The reset outputs are push-pull for sourcing or sinking current. The output voltage can be switched between the ground level and the output voltage of the relevant standby regulator. An external reset delay capacitor can be added if a timed reset pulse is required (C_{RDC1} or $C_{RDC2/3}$).

Standby regulator 1 has an independent reset function (pins RST1 and RDC1). Standby regulators 2 and 3 have combined circuitry (pins RST2/3 and RDC2/3). The reset trigger signals from both regulators are connected using an OR function to the reset output buffer thus ensuring that both regulators can generate a reset when appropriate. The RST1 output is linked to standby regulator 1 (5 V) and, therefore, generates a 5 V HIGH-level output voltage. The RST2/3 output is linked to regulator 2 (3.3 V) and, therefore, generates a 3.3 V HIGH-level output voltage.

7.8 Hold output

The hold output (pin HOLD) is a combined output for the thermal pre-warning signal and all other diagnostic signals. To distinguish between these signals, the HOLD output is designed as an active HIGH 3-state output buffer. When a no failure condition is present the output is LOW. When a thermal pre-warning signal is generated (e.g. to shut down other circuits in the radio before the regulator itself shuts down) the signal rises to its MID

level. In all other warning situations, the HOLD output rises to its HIGH level. In order to generate standard CMOS logic compliant signals an external decoding circuit has to be implemented; see Figure 9.

The HOLD output will be active HIGH when:

- The output voltage of one or more switched regulators is out of regulation (except REG7), due to overload or supply voltage drops
- The power switch operates in the Foldback mode
- In Standby or On mode the thermal shutdown is activated
- In Standby or On mode the load dump protection is activated
- In Standby mode a low battery voltage occurs (V_{P1}) indicating that it is not possible to pull REG4 into regulation when switching it on.

It should be noted that there is intentionally no out-of-regulation detection for REG7 since it can be adjusted to maximum 10 V and would, in that event, activate the HOLD signal very early.

The HOLD function includes hysteresis in order to avoid oscillations when the hold threshold level is crossed. A schematic diagram of the HOLD function is illustrated in Figure 3.

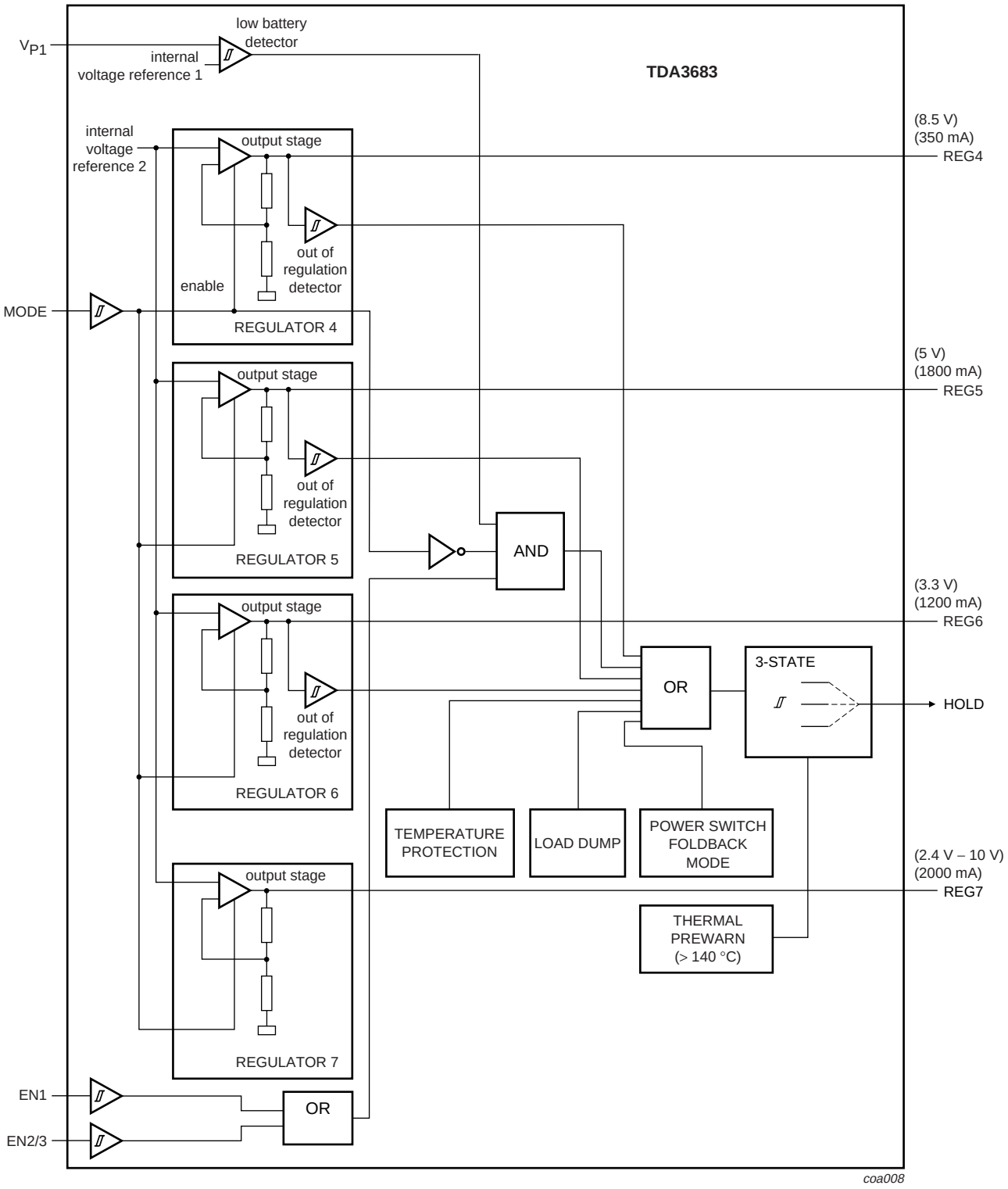


Fig 3. Schematic diagram of the HOLD function

7.9 Ignition buffer

The ignition buffer (pins IGNIN and IGNOUT) is an independent inverting open-collector output buffer circuit that can be used to sense the start line of the ignition key in a car. The start line will only be pulled-up to the battery voltage in the event of an engine crank resulting in a LOW at the inverting output of the ignition buffer. This output signal can be used to immediately mute an audio amplifier during the engine crank.

To guarantee a reliable LOW output signal, even in extreme cold weather crank conditions (the battery voltage may momentarily drop down to 3 V) a low supply latch function is implemented.

To make the ignition buffer input robust, for possible extreme transients present on the battery line, an input RC filter is strongly advised. A blocking diode is also recommended to prevent substrate injection in case of negative voltage spikes at the input.

7.10 Supply voltage inputs

The supply voltage inputs (pins V_{P1} and V_{P2}) are intended to be connected to the battery. Both inputs are protected against load dump transients and reverse battery connections. The second supply pin (V_{P2}) is internally connected to the high current/ low output voltage switched regulators (REG5 and REG6) and can be connected to an external DC-to-DC downconverter for reduced power dissipation and increased power supply efficiency.

Power must be applied to pin V_{P1} to ensure that the circuits are functional, since the band gaps for the switched and standby regulators are connected to this supply pin.

Rising and falling supply voltage threshold levels determine if the switched regulators and power switch can be switched on.

The timing diagrams for various regulator functions are illustrated in Figure 4 and Figure 5.

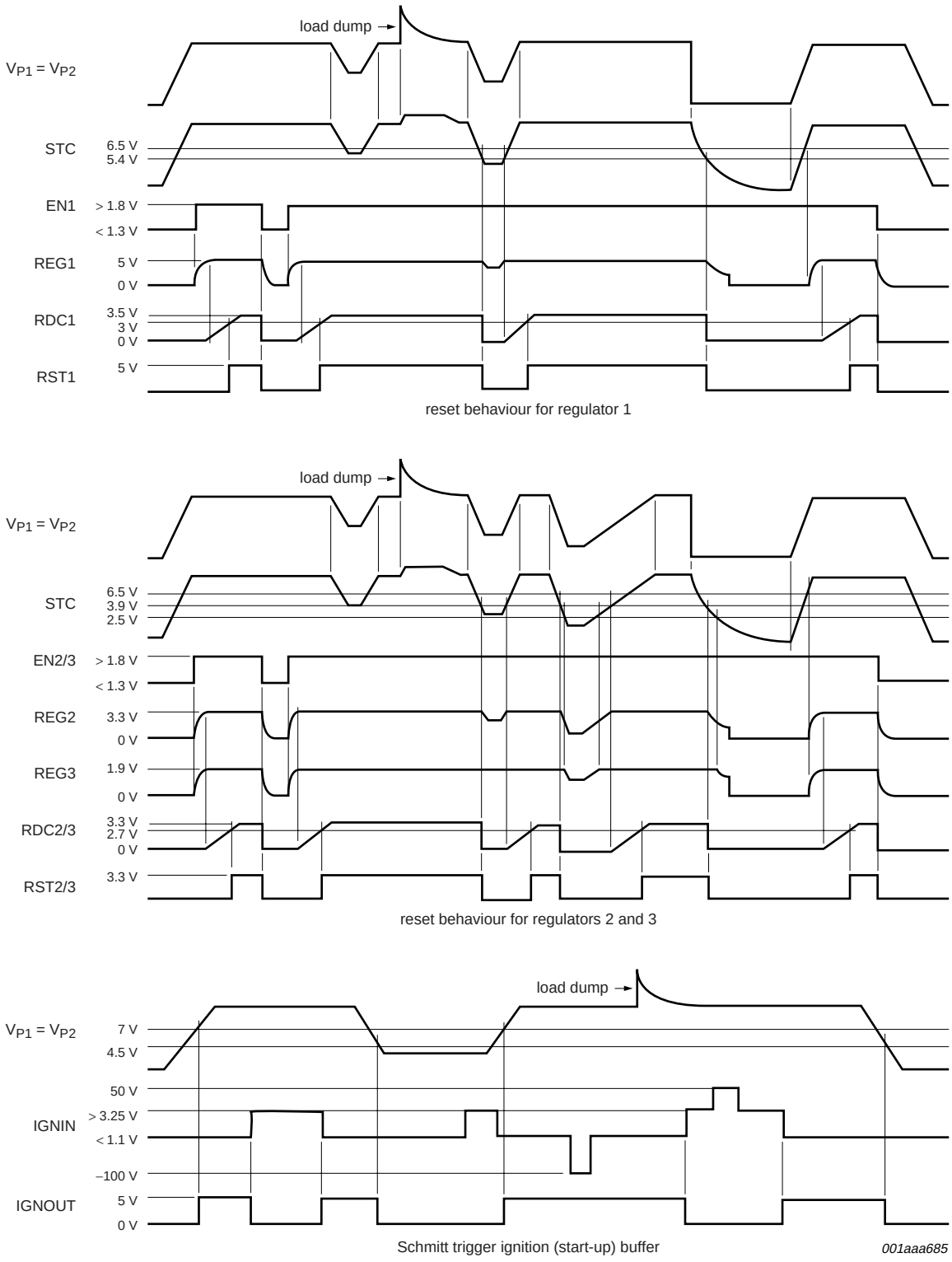


Fig 4. Timing diagram of the reset outputs for REG1, REG2 and REG3 and ignition Schmitt trigger

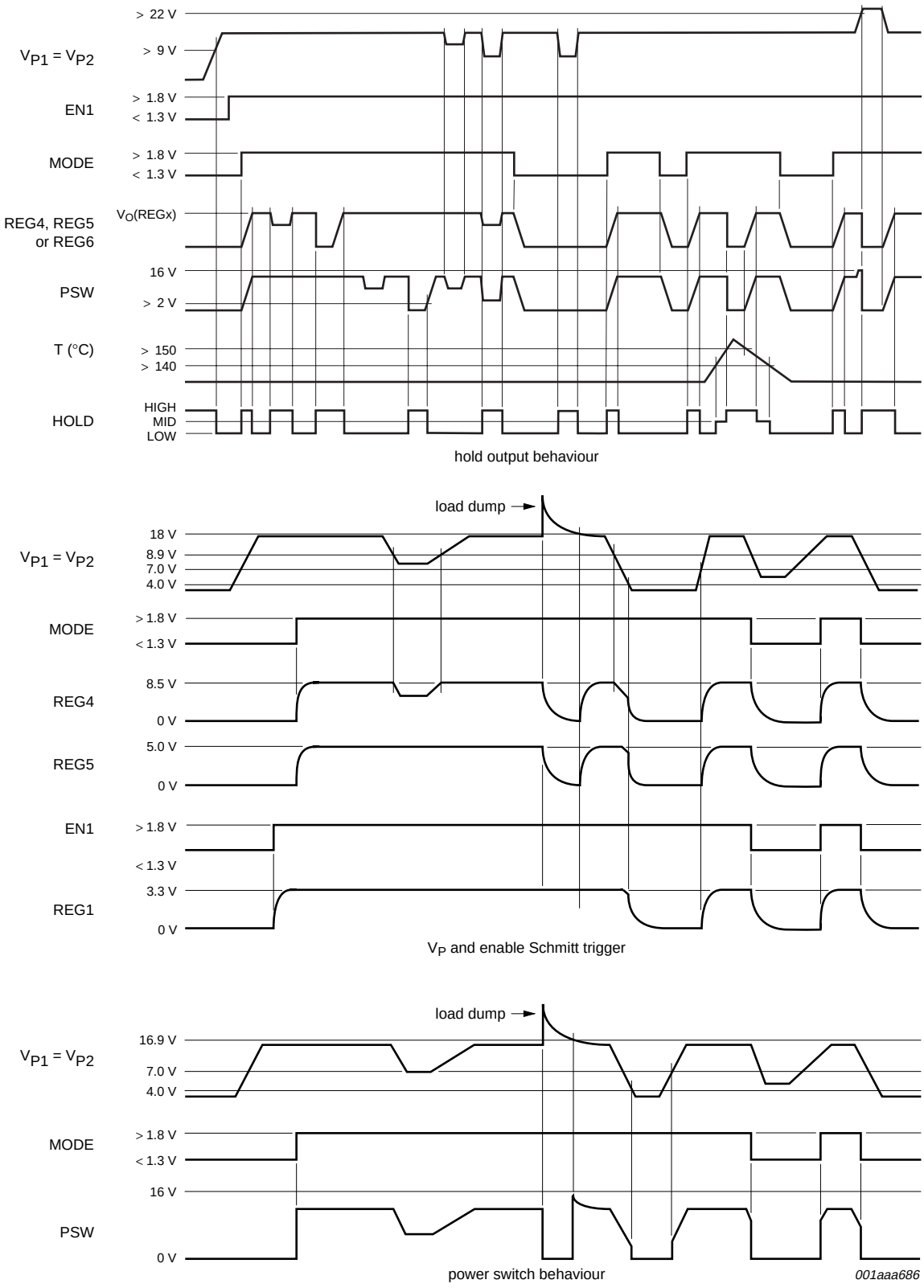


Fig 5. Timing diagram of the HOLD output, V_P and Schmitt trigger and power switch

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{P1}	supply voltage 1	operating	-	18	V
		reverse polarity; non-operating	-	18	V
		jump start; t ≤ 10 minutes	-	30	V
		load dump protection; t ≤ 50 ms; t_r ≥ 2.5 ms	-	50	V
V_{P2}	supply voltage 2	operating	-	18	V
		reverse polarity; non-operating	-	18	V
		jump start; t ≤ 10 minutes	-	30	V
		load dump protection; t ≤ 50 ms; t_r ≥ 2.5 ms	-	50	V
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
T_j	junction temperature	operating	–40	+150	°C

9. Thermal characteristics

Table 6: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

10. Characteristics

Table 7: Characteristics

V_{P1} = V_{P2} = 14.4 V; T_{amb} = 25 °C; R_L = ∞ Ω; measured in test circuits of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{P1}	supply voltage 1	operating		9	14.4	18	V
		regulators 1, 2 and 3 on	[1]	4.0	14.4	50	V
		jump start; t ≤ 10 minutes		-	-	30	V
		load dump protection; t ≤ 50 ms; t_r ≥ 2.5 ms		-	-	50	V
V_{P2}	supply voltage 2	operating		6.5	14.4	18	V
		regulators 1, 2 and 3 on		0	-	50	V
		jump start; t ≤ 10 minutes		-	-	30	V
		load dump protection; t ≤ 50 ms; t_r ≥ 2.5 ms		-	-	50	V
$V_{bat(loaddump)}$	battery overvoltage shutdown	V_{P1} and/or V_{P2}		18	20	22	V

Table 7: Characteristics *...continued*

V_{P1} = V_{P2} = 14.4 V; T_{amb} = 25 °C; R_L = ∞ Ω; measured in test circuits of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{q(tot)}$	total quiescent supply current	V_{EN1}, $V_{EN2/3}$ and V_{MODE} < 0.8 V		-	5	30	µA
		V_{MODE} and V_{IGNIN} < 0.8 V; V_{EN1} and $V_{EN2/3}$ > 2.4 V		-	300	450	µA
		V_{MODE} and V_{IGNIN} < 0.8 V; V_{EN1} > 2.4 V; $V_{EN2/3}$ < 0.8 V		-	150	250	µA
		V_{MODE} and V_{IGNIN} < 0.8 V; V_{EN1} < 0.8 V; $V_{EN2/3}$ > 2.4 V		-	225	325	µA
Schmitt trigger for power supply (regulators 4, 5, 6, 7 and power switch)							
$V_{th(r)}$	rising threshold voltage	V_{P1} and V_{P2} rising		6.5	7.0	7.5	V
$V_{th(f)}$	falling threshold voltage	V_{P1} and V_{P2} falling		4.0	4.5	5.0	V
V_{hys}	hysteresis voltage			-	2.5	-	V
Schmitt trigger for enable (EN1, EN2/3) and MODE inputs							
$V_{th(r)}$	rising threshold voltage			1.4	1.8	2.4	V
$V_{th(f)}$	falling threshold voltage			0.9	1.3	1.9	V
V_{hys}	hysteresis voltage	I_{REGx} = I_{PSW} = 1 mA		-	0.5	-	V
I_{LI}	input leakage current	$V_{ENx/MODE}$ = 5 V		1	5	20	µA
Reset trigger level of regulator 1							
$V_{th(r)}$	rising threshold voltage	V_{P1} and V_{P2} rising; I_{REG1} = 50 mA	[2]	4.43	V_{REG1} – 0.15	V_{REG1} – 0.1	V
$V_{th(f)}$	falling threshold voltage	V_{P1} and V_{P2} falling; I_{REG1} = 50 mA	[2]	4.4	V_{REG1} – 0.25	V_{REG1} – 0.13	V
Reset trigger level of regulator 2							
$V_{th(r)}$	rising threshold voltage	V_{P1} and V_{P2} rising; I_{REG2} = 50 mA	[2]	3.03	V_{REG2} – 0.15	V_{REG2} – 0.1	V
$V_{th(f)}$	falling threshold voltage	V_{P1} and V_{P2} falling; I_{REG2} = 50 mA	[2]	3.0	V_{REG2} – 0.25	V_{REG2} – 0.13	V
Reset trigger level of regulator 3							
$V_{th(r)}$	rising threshold voltage	V_{P1} and V_{P2} rising; I_{REG3} = 50 mA	[2]	1.75	V_{REG3} – 0.10	V_{REG3} – 0.08	V
$V_{th(f)}$	falling threshold voltage	V_{P1} and V_{P2} falling; I_{REG3} = 50 mA	[2]	1.72	V_{REG3} – 0.15	V_{REG3} – 0.10	V
Schmitt triggers for HOLD output							
$V_{th(r)(REG4)}$	rising threshold voltage of regulator 4	V_{P1} and V_{P2} rising	[2]	-	V_{REG4} – 0.15	V_{REG4} – 0.075	V
$V_{th(f)(REG4)}$	falling threshold voltage of regulator 4	V_{P1} and V_{P2} falling	[2]	7.9	V_{REG4} – 0.35	-	V
$V_{hys(REG4)}$	hysteresis voltage due to regulator 4			-	0.2	-	V
$V_{th(r)(REG5)}$	rising threshold voltage of regulator 5	V_{P1} and V_{P2} rising	[2]	-	V_{REG5} – 0.15	V_{REG5} – 0.075	V
$V_{th(f)(REG5)}$	falling threshold voltage of regulator 5	V_{P1} and V_{P2} falling	[2]	4.3	V_{REG5} – 0.35	-	V

Table 7: Characteristics *...continued*

$V_{P1} = V_{P2} = 14.4$ V; $T_{amb} = 25$ °C; $R_L = \infty$ Ω; measured in test circuits of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{hys(REG5)}$	hysteresis voltage due to regulator 5			-	0.2	-	V
$V_{th(r)(REG6)}$	rising threshold voltage of regulator 6	V_{P1} and V_{P2} rising	[2]	-	$V_{REG6} - 0.15$	$V_{REG6} - 0.075$	V
$V_{th(f)(REG6)}$	falling threshold voltage of regulator 6	V_{P1} and V_{P2} falling	[2]	2.7	$V_{REG6} - 0.3$	-	V
$V_{hys(REG6)}$	hysteresis voltage due to regulator 6			-	0.15	-	V
$V_{th(r)(VP)}$	rising threshold voltage of supply voltage	V_{P1} and V_{P2} rising; $V_{MODE} < 0.8$ V; V_{EN1} or $V_{EN2/3} > 2.4$ V		7.8	8.4	9	V
$V_{th(f)(VP)}$	falling threshold voltage of supply voltage	V_{P1} and V_{P2} falling; $V_{MODE} < 0.8$ V; V_{EN1} or $V_{EN2/3} > 2.4$ V		7.7	8.1	8.5	V
$V_{hys(VP)}$	hysteresis voltage of supply voltage			-	0.3	-	V
Hold buffer							
$V_{o(HOLD)(L)}$	LOW-level HOLD output			0	0.1	0.6	V
$I_{sink(L)}$	LOW-level sink current	$V_{HOLD} \leq 0.6$ V		0.5	-	-	mA
$V_{o(HOLD)(H)}$	HIGH-level HOLD output			6.0	7.0	8.0	V
$I_{source(H)}$	HIGH-level source current	$V_{HOLD} = 3.3$ V		1	2	-	mA
$V_{o(HOLD)(M)}$	MID-level HOLD output			1.8	2.15	2.5	V
$I_{source(M)}$	MID-level source current	$V_{HOLD} = 1.5$ V		1	2	-	mA
t_r	rise time	$C_L = 50$ pF		-	7	50	µs
t_f	fall time	$C_L = 50$ pF		-	1	50	µs
Reset and Reset delay 1							
$I_{sink(L)}$	LOW-level sink current	$V_{RST1} \leq 0.8$ V; $V_{RDC1} < 1.0$ V		2	-	-	mA
$I_{source(H)}$	HIGH-level source current	$V_{RST1} = 4.5$ V; $V_{RDC1} > 3.5$ V		240	400	900	µA
t_r	rise time	$C_L = 50$ pF		-	7	50	µs
t_f	fall time	$C_L = 50$ pF		-	1	50	µs
I_{ch}	charge current	$V_{RDC1} = 0$ V; $V_{EN1} > 2.4$ V		2	4	8	µA
I_{dch}	discharge current	$V_{RDC1} = 3$ V; $V_{P1} = V_{P2} = 4.3$ V		1.0	1.6	-	mA
$V_{th(r)(RDC1)}$	reset delay capacitor 1 rising voltage threshold		[3]	2.5	3.0	3.5	V
$V_{th(f)(RDC1)}$	reset delay capacitor 1 falling voltage threshold		[3]	1.0	1.2	1.4	V
$t_{d(RST1)}$	delay time reset signal	$C_{RDC1} = 47$ nF	[4]	20	35	70	ms

Table 7: Characteristics *...continued*

$V_{P1} = V_{P2} = 14.4$ V; $T_{amb} = 25$ °C; $R_L = \infty$ Ω; measured in test circuits of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(PSW)}$	delay time power switch foldback protection	C_{RDC1} = 47 nF	[5]	8	17.5	40	ms
$V_{OH(RST1)}$	HIGH-level output voltage on pin RST1	I_{RST1} = 0 A		4.5	5	5.25	V
$V_{OL(RST1)}$	LOW-level output voltage on pin RST1	I_{RST1} = 0 A		0	0.2	0.8	V
Reset and reset delay 2/3							
$I_{sink(L)}$	LOW-level sink current	$V_{RST2/3} \leq 0.6$ V; $V_{RDC2/3} < 1.0$ V		2	-	-	mA
$I_{source(H)}$	HIGH-level source current	$V_{RST2/3} = 2.7$ V; $V_{RDC2/3} > 3.2$ V		240	400	900	µA
t_r	rise time	C_L = 50 pF		-	7	50	µs
t_f	fall time	C_L = 50 pF		-	1	50	µs
I_{ch}	charge current	$V_{RDC2/3} = 0$ V; $V_{EN2/3} > 2.4$ V		2	4	8	µA
I_{dch}	discharge current	$V_{RDC2/3} = 2.7$ V; $V_{P1} = V_{P2} = 3$ V		1.0	1.6	-	mA
$V_{th(r)(RDC2/3)}$	reset delay capacitor 2/3 rising voltage threshold		[6]	2.2	2.7	3.2	V
$V_{th(f)(RDC2/3)}$	reset delay capacitor 2/3 falling voltage threshold		[6]	1.0	1.2	1.4	V
$V_{OH(RST2/3)}$	HIGH-level output voltage on pin RST2/3	$I_{RST2/3}$ = 0 A		3.0	3.3	3.45	V
$V_{OL(RST2/3)}$	LOW-level output voltage on pin RST2/3	$I_{RST2/3}$ = 0 A		0	0.2	0.6	V
$t_{d(RST2/3)}$	delay time reset signal	$C_{RDC2/3}$ = 47 nF	[4]	20	35	70	ms
Regulator 1 (I_{REG1} = 5 mA; unless otherwise specified)							
$V_{o(REG1)}$	output voltage	1 mA ≤ I_{REG1} ≤ 600 mA		4.75	5.0	5.25	V
		7 V ≤ $V_{P1/2}$ ≤ 18 V		4.75	5.0	5.25	V
		18 V ≤ $V_{P1/2}$ ≤ 50 V		4.75	5.0	5.25	V
ΔV	line regulation	7 V ≤ $V_{P1/2}$ ≤ 18 V		-	2	100	mV
ΔV_L	load regulation	1 mA ≤ I_{REG1} ≤ 300 mA		-	20	50	mV
		1 mA ≤ I_{REG1} ≤ 600 mA		-	-	100	mV
PSRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)		40	45	-	dB
$V_{drop(REG1)}$	drop-out voltage	I_{REG1} = 300 mA; $V_{P1} = V_{P2}$ = 4.75 V	[7]	-	0.4	0.6	V
		I_{REG1} = 600 mA; $V_{P1} = V_{P2}$ = 5.75 V	[7]	-	0.8	1.2	V
		I_{REG1} = 300 mA; V_{STC} = 4.75 V	[8]	-	0.2	0.5	V
		I_{REG1} = 600 mA; V_{STC} = 5.75 V	[8]	-	0.8	1.0	V

Table 7: Characteristics *...continued*

$V_{P1} = V_{P2} = 14.4$ V; $T_{amb} = 25$ °C; $R_L = \infty$ Ω; measured in test circuits of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{m(REG1)}$	current limit	$V_{REG1} > 4.5$ V	[9]	640	1400	2500	mA
$I_{st(REG1)}$	start-up current	$V_{REG1} \leq 1.5$ V		120	-	-	mA
$I_{sc(REG1)}$	short-circuit current	$R_L \leq 0.5$ Ω	[10]	160	250	-	mA
Regulator 2 (I_{REG2} = 5 mA; unless otherwise specified)							
$V_{o(REG2)}$	output voltage	1 mA ≤ I_{REG2} ≤ 200 mA		3.15	3.3	3.45	V
		7 V ≤ $V_{P1/2}$ ≤ 18 V		3.15	3.3	3.45	V
		18 V ≤ $V_{P1/2}$ ≤ 50 V		3.15	3.3	3.45	V
ΔV	line regulation	7 V ≤ $V_{P1/2}$ ≤ 18 V		-	2	50	mV
ΔV_L	load regulation	1 mA ≤ I_{REG2} ≤ 100 mA		-	20	50	mV
		1 mA ≤ I_{REG2} ≤ 200 mA		-	-	100	mV
PSRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)		45	50	-	dB
$V_{drop(REG2)}$	drop-out voltage	I_{REG2} = 200 mA; $V_{P1} = V_{P2}$ = 4.0 V	[7]	-	0.75	0.85	V
		I_{REG2} = 200 mA; V_{STC} = 4.0 V	[8]	-	0.75	0.85	V
$I_{m(REG2)}$	current limit	$V_{REG2} > 3$ V	[9]	225	800	1500	mA
$I_{sc(REG2)}$	short-circuit current	$R_L \leq 0.5$ Ω	[10]	75	200	-	mA
Regulator 3 (I_{REG3} = 5 mA; unless otherwise specified)							
$V_{o(REG3)}$	output voltage	1 mA ≤ I_{REG3} ≤ 150 mA		1.72	1.9	2.0	V
		4.0 V ≤ $V_{P1/2}$ ≤ 18 V		1.72	1.9	2.0	V
		18 V ≤ $V_{P1/2}$ ≤ 50 V		1.72	1.9	2.0	V
ΔV	line regulation	7 V ≤ $V_{P1/2}$ ≤ 18 V		-	2	50	mV
ΔV_L	load regulation	1 mA ≤ I_{REG3} ≤ 50 mA		-	20	50	mV
		1 mA ≤ I_{REG3} ≤ 150 mA		-	-	100	mV
PSRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)		50	55	-	dB
$V_{drop(REG3)}$	drop-out voltage	I_{REG3} = 150 mA; $V_{P1} = V_{P2}$ = 4.0 V	[7]	-	2.20	2.28	V
		I_{REG3} = 150 mA; V_{STC} = 4.0 V	[8]	-	2.20	2.28	V
$I_{m(REG3)}$	current limit	$V_{REG3} > 1.6$ V	[9]	160	600	1000	mA
$I_{sc(REG3)}$	short-circuit current	$R_L \leq 0.5$ Ω	[10]	160	200	-	mA
$V_{o(REG2)}$ - $V_{o(REG3)}$	output voltage tracking REG3 to REG2	0 ≤ $V_{P1/2}$ ≤ 18 V		-	-	2.8	V
Regulator 4 (I_{REG4} = 5 mA; unless otherwise specified)							
$V_{o(off)}$	output voltage off			-	1	400	mV
$V_{o(REG4)}$	output voltage	1 mA ≤ I_{REG4} ≤ 350 mA		8.1	8.5	8.9	V
		9.5 V ≤ $V_{P1/2}$ ≤ 18 V		8.1	8.5	8.9	V
ΔV	line regulation	9.5 V ≤ $V_{P1/2}$ ≤ 18 V		-	2	50	mV
ΔV_L	load regulation	1 mA ≤ I_{REG4} ≤ 350 mA		-	20	85	mV

Table 7: Characteristics *...continued*

$V_{P1} = V_{P2} = 14.4$ V; $T_{amb} = 25$ °C; $R_L = \infty$ Ω; measured in test circuits of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PSRR	supply voltage ripple rejection	$f_i = 3$ kHz; $V_i = 2$ V (p-p)		60	70	-	dB
$V_{drop(REG4)}$	drop-out voltage	$I_{REG4} = 350$ mA; $V_{P1} = V_{P2} = 8.55$ V	[7]	-	0.4	0.7	V
$I_{m(REG4)}$	current limit	$V_{REG4} > 7$ V	[9]	400	1300	2000	mA
$I_{sc(REG4)}$	short-circuit current	$R_L \leq 0.5$ Ω	[10]	125	200	-	mA
Regulator 5 (I_{REG5} = 5 mA; unless otherwise specified)							
$V_{o(off)}$	output voltage off			-	1	400	mV
$V_{o(REG5)}$	output voltage	1 mA ≤ I_{REG5} ≤ 1800 mA		4.75	5.0	5.25	V
		7 V ≤ $V_{P1/2}$ ≤ 18 V		4.75	5.0	5.25	V
ΔV	line regulation	7 V ≤ V_{P2} ≤ 18 V		-	2	50	mV
ΔV_L	load regulation	1 mA ≤ I_{REG5} ≤ 1800 mA		-	20	150	mV
PSRR	supply voltage ripple rejection	$f_i = 3$ kHz; $V_i = 2$ V (p-p)		60	70	-	dB
$V_{drop(REG5)}$	drop-out voltage	$I_{REG5} = 1800$ mA; $V_{P2} = 6$ V	[7]	-	1	1.5	V
$I_{m(REG5)}$	current limit	$V_{REG5} > 4.5$ V	[9]	2.0	4.5	6.25	A
$I_{sc(REG5)}$	short-circuit current	$R_L \leq 0.5$ Ω	[10]	1.0	1.2	-	A
Regulator 6 (I_{REG6} = 5 mA; unless otherwise specified)							
$V_{o(off)}$	output voltage off			-	1	400	mV
$V_{o(REG6)}$	output voltage	1 mA ≤ I_{REG6} ≤ 1200 mA		3.15	3.3	3.45	V
		7 V ≤ $V_{P1/2}$ ≤ 18 V		3.15	3.3	3.45	V
ΔV	line regulation	5 V ≤ V_{P2} ≤ 18 V; $V_{P1} = 7$ V		-	2	50	mV
ΔV_L	load regulation	1 mA ≤ I_{REG6} ≤ 1200 mA; $T_{amb} > 0$ °C		-	20	50	mV
		1 mA ≤ I_{REG6} ≤ 1200 mA; $T_{amb} \leq 0$ °C		-	35	70	mV
PSRR	supply voltage ripple rejection	$f_i = 3$ kHz; $V_i = 2$ V (p-p)		60	75	-	dB
$V_{drop(REG6)}$	drop-out voltage	$I_{REG6} = 1200$ mA ; $V_{P2} = 5$ V	[7]	-	1.7	2.2	V
$I_{m(REG6)}$	current limit	$V_{REG6} > 3.0$ V	[9]	1.3	2.9	4.0	A
$I_{sc(REG6)}$	short-circuit current	$R_L \leq 0.5$ Ω	[10]	0.8	0.9	-	A
Regulator 7 (I_{REG7} = 5 mA; unless otherwise specified)							
$V_{o(off)}$	output voltage off			-	1	400	mV
$V_{o(REG7)}$	output voltage	1 mA ≤ I_{REG7} ≤ 2000 mA		V_o – 5 %	2.4 to 10	V_o + 5 %	V
		11 V ≤ $V_{P1/2}$ ≤ 18 V		V_o – 5 %	2.4 to 10	V_o + 5 %	V
ΔV	line regulation	11 V ≤ $V_{P1/2}$ ≤ 18 V		-	2	50	mV
ΔV_L	load regulation	1 mA ≤ I_{REG7} ≤ 2000 mA		-	20	150	mV
PSRR	supply voltage ripple rejection	$f_i = 3$ kHz; $V_i = 2$ V (p-p)		45	50	-	dB

Table 7: Characteristics *...continued*

$V_{P1} = V_{P2} = 14.4$ V; $T_{amb} = 25$ °C; $R_L = \infty$ Ω; measured in test circuits of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{drop(REG7)}$	drop-out voltage	I_{REG7} = 1000 mA; V_o = 10 V; $V_{P1} = V_{P2}$ = 10.75 V	[7]	-	1.0	1.25	V
		I_{REG7} = 2000 mA; V_o = 10 V; $V_{P1} = V_{P2}$ = 10.75 V	[7]	-	1.25	1.5	V
		I_{REG7} = 1000 mA; V_o = 5 V; $V_{P1} = V_{P2}$ = 5.75 V	[7]	-	1.0	1.25	V
		I_{REG7} = 2000 mA; V_o = 5 V; $V_{P1} = V_{P2}$ = 5.75 V	[7]	-	1.25	1.5	V
		I_{REG7} = 1000 mA; V_o = 2.4 V; $V_{P1} = V_{P2}$ = 5 V	[7]	-	2.6	3.1	V
		I_{REG7} = 2000 mA; V_o = 2.4 V; $V_{P1} = V_{P2}$ = 5 V	[7]	-	2.6	3.4	V
$I_{m(REG7)}$	current limit	V_{REG7} > 8.0 V at V_o = 10 V or V_{REG7} > 1.9 V at V_o = 2.4 V	[9]	2.1	3.7	5.5	A
$I_{sc(REG7)}$	short-circuit current	$R_L \leq 0.5$ Ω	[10]	1.35	1.8	-	A
$V_{fb(REG7)}$	flyback voltage	I_{REG7} = –1000 mA		-	V_{P1} + 3	22	V
Power switch							
$V_{drop(PSW)}$	drop-out voltage	I_{PSW} = 1 A; $V_{P1} = V_{P2}$ = 13.5 V	[11]	-	0.45	0.65	V
		I_{PSW} = 2.2 A; $V_{P1} = V_{P2}$ = 13.5 V	[11]	-	1.0	1.8	V
$I_{DC(PSW)}$	continuous current	$V_{P1} = V_{P2}$ = 16 V; V_{PSW} = 13.5 V		2.2	4.3	6.0	A
$V_{clamp(PSW)}$	clamping voltage	$V_{P1} = V_{P2} \geq 17$ V; 1 mA < I_{PSW} < 2.2 A		13.5	15.0	16.0	V
$I_{M(PSW)}$	peak current	$V_{P1} = V_{P2}$ < 17 V	[5]	3	-	-	A
$V_{fb(PSW)}$	flyback voltage	I_{PSW} = –1000 mA		-	V_{P1} + 3	22	V
$I_{sc(PSW)}$	short-circuit current	V_{P1} = 14.4 V; V_{PSW} < 1.0 V		0.75	1.0	-	A
Storage capacitor switch							
$I_{DC(STC)}$	continuous current	V_{STC} > 5 V		0.95	1.0	-	A
$V_{clamp(STC)}$	clamping voltage	$V_{P1} = V_{P2} \geq 16.7$ V; I_{STC} = 100 mA		-	-	16	V
$I_{r(STC)}$	reverse current	$V_{P1} = V_{P2}$ = 0 V; V_{STC} = 12.4 V		-	-	100	µA
$V_{th(STC)}$	regulator enable threshold voltage	V_{EN1} or $V_{EN2/3}$ > 2.4 V	[12]	5.5	6.5	7.5	V
Schmitt trigger for enable input of ignition							
$V_{th(r)}$	rising threshold voltage of ignition input	V_{EN1} or $V_{EN2/3}$ > 2.4 V		2.75	3.25	3.75	V
$V_{th(f)}$	falling threshold voltage of ignition input	V_{EN1} or $V_{EN2/3}$ > 2.4 V		0.8	1.1	1.3	V
V_{hys}	hysteresis voltage	V_{EN1} or $V_{EN2/3}$ > 2.4 V		1.5	-	-	V
I_{LI}	input leakage current	V_{IGNIN} = 5 V		-	-	1.0	µA
$I_{I(clamp)}$	input clamping current	V_{IGNIN} > 50 V		-	-	50	mA

Table 7: Characteristics *...continued*

V_{P1} = V_{P2} = 14.4 V; T_{amb} = 25 °C; R_L = ∞ Ω; measured in test circuits of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH(clamp)}$	HIGH-level input clamping voltage	V_{IGNIN} = 50 V	V_P	-	50	V
$V_{IL(clamp)}$	LOW-level input clamping voltage	V_{IGNIN} = –100 V	–0.6	-	0	V
Schmitt trigger for power supply of ignition						
$V_{th(r)}$	rising threshold voltage		6.5	7.0	7.5	V
$V_{th(f)}$	falling threshold voltage	V_{IGNOUT} = LOW; V_{IGNIN} > 1.2 V	4.0	4.5	5.0	V
Ignition buffer						
V_{OL}	LOW-level output voltage	I_{IGNOUT} = 0 mA	0	0.2	0.8	V
V_{OH}	HIGH-level output voltage	I_{IGNOUT} = 0 mA	4.5	5.0	5.25	V
$I_{o(sink)(L)}$	LOW-level output sink current	V_{IGNOUT} ≤ 0.8 V	0.6	0.8	-	mA
I_{LO}	output leakage current	V_{IGNOUT} = 5 V; V_{IGNIN} = 0 V	-	-	1.0	µA
Temperature protection						
$T_{j(sd)}$	junction temperature for shutdown		150	160	170	°C
$T_{j(HOLD)}$	junction temperature for HOLD thermal pre-warning		140	150	160	°C
ΔT_j	delta junction temperature pre-warning / shutdown		10	-	-	°C

[1] Minimum operating voltage, only if V_{P1} has first exceeded 6.5 V.

[2] The voltage of the regulators 1, 2, 3, 4 and 7 drops as a result of decreasing V_{P1} voltage. The output voltage of regulators 5 and 6 drops as a result of decreasing V_{P2} voltage.

[3] Pin RST1 goes HIGH when $V_{th(r)(RDC1)}$ is reached and goes LOW when reaching $V_{th(f)(RDC1)}$.

[4] The delay time depends on the value of C_{RDC1} or $C_{RDC2/3}$: $t_d = \frac{C}{I_{ch}} \times V_{C(th)} = C \times (750 \times 10^3)[s]$

[5] The delay time depends on the value of C_{RDC1}: $t_{d\_high\ current} = \frac{C}{I_{ch}} \times V_{C(th)} = C \times (375 \times 10^3)[s]$

[6] Pin RST2/3 goes HIGH when $V_{th(r)(RDC2/3)}$ is reached and goes LOW when reaching $V_{th(f)(RDC2/3)}$.

[7] The drop-out voltage of regulators 1,2,3,4 and 7 is measured between V_{P1} and REG1, REG2, REG3, REG4 or REG7, the drop-out voltage of regulators 5 and 6 is measured between V_{P2} and REG5 or REG6.

[8] The drop-out voltage is measured between pins STC and REG1, REG2 and REG3.

[9] At current limit, $I_{m(REGn)}$ is held constant; see Figure 6.

[10] The foldback current protection limits the dissipated power at short circuit; see Figure 6.

[11] The drop-out voltage of the power switch is measured between pins V_{P1} and PSW; see Figure 7.

[12] Standby regulators are enabled when the increasing storage capacitor voltage reaches this threshold voltage at first power-up.

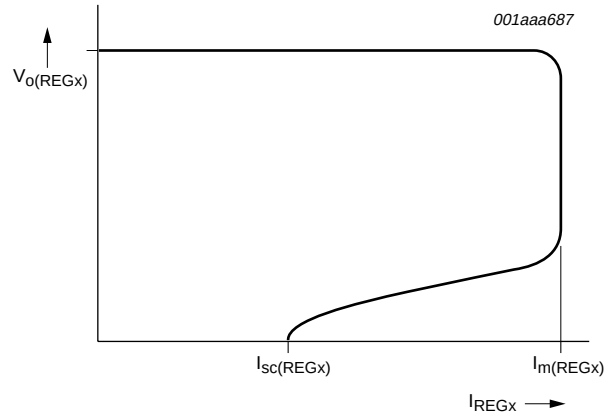


Fig 6. Typical foldback current protection curve for all regulators (except REG3)

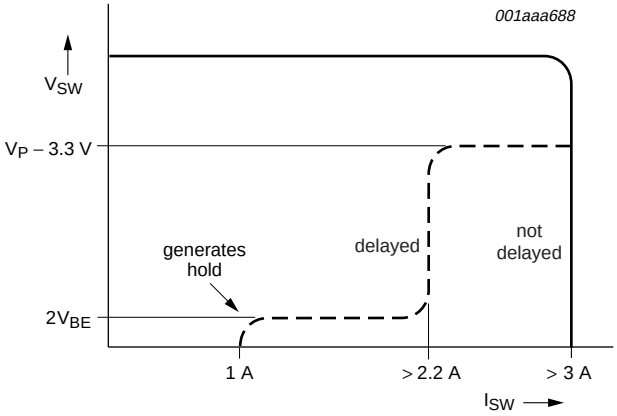


Fig 7. Current protection of the power switch

11. Application information

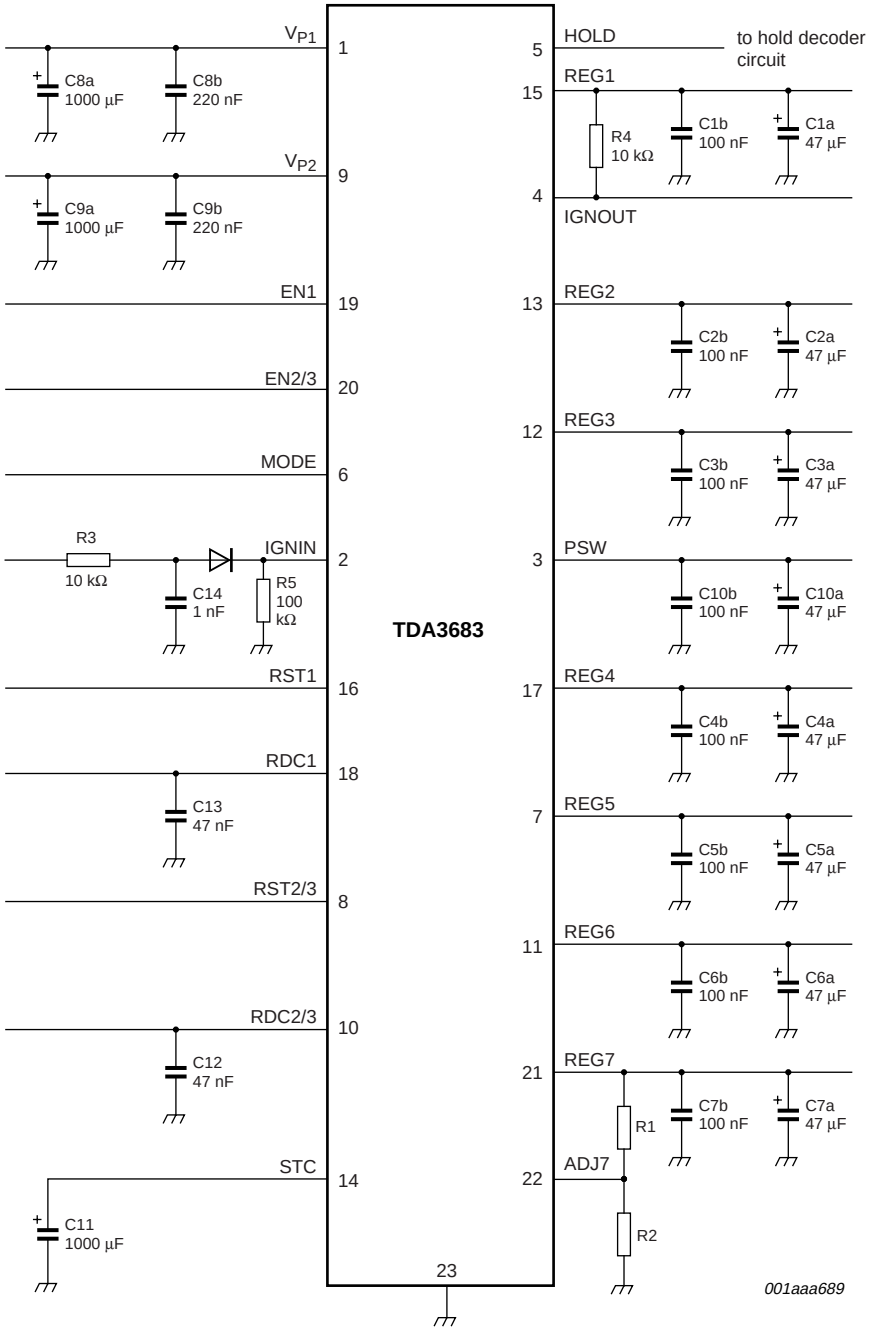
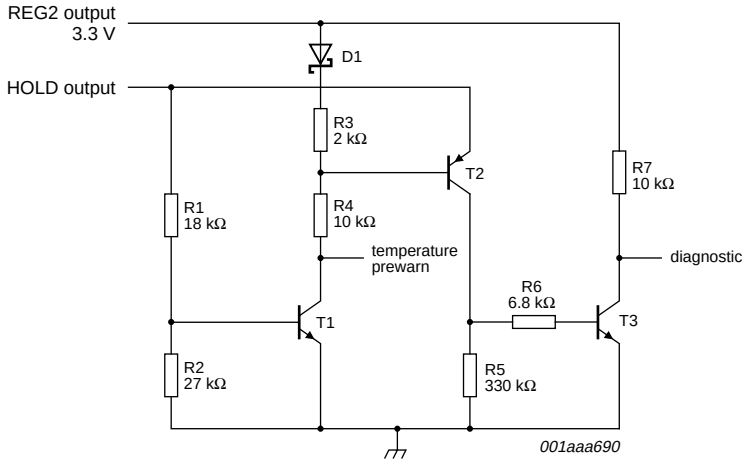


Fig 8. Test and application circuit



R1 to R7: Standard E12 series resistor, 5 % tolerance

T1, T3: Standard small signal NPN transistor

T2: Standard small signal PNP transistor

D1: Low forward voltage (Schottky) diode

Fig 9. Hold decoder circuit

11.1 Application notes

- A ceramic capacitor of 220 nF must be connected to both supply pins to guarantee stability over the ambient temperature range. For improved noise performance it is also recommended to connect a standard electrolytic capacitor of 2200 µF close to the supply pins.
- A ceramic capacitor of 220 nF must be connected to the storage capacitor pin when the back-up function is not used to guarantee stability over the ambient temperature range. There are basically no restrictions for the maximum value of the storage capacitor, but the required value depends on the actual output currents of the three standby regulators and the length of time that their outputs must be maintained after the supply voltage collapsed ($V_{P1} = V_{P2} = 0$ V).
- A standard electrolytic capacitor of 10 µF, or more, must be connected to the output of the power switch to guarantee stability over the ambient temperature range. A ceramic capacitor of 100 nF can be added in parallel with the electrolytic capacitor to provide improved HF performance.
- An electrolytic capacitor of 10 µF, or more, must be connected to each regulator output to guarantee stability over the ambient temperature range. There are restrictions concerning the maximum ESR of the electrolytic capacitors that are used; see Table 8. Usually the nominal value of electrolytic capacitors increases and the ESR decreases with temperature so the worst case condition for stability (i.e. minimum capacitance and maximum ESR) exists at low temperatures. Depending on the specified temperature range of the radio set, some of the regulator outputs may need low ESR type electrolytic or tantalum capacitors. A ceramic capacitor of 100 nF can be added in parallel with the electrolytic or tantalum capacitor to provide improved HF performance. However, in the case of the standby regulators (REG1 to REG3) these additional ceramic capacitors should preferably not be connected very close to the device pins to avoid stability issues.

- The output voltage of regulator 7 can be adjusted between 2.4 V and 10 V using two external resistors (R1 and R2); see Figure 10. The following equation can be used for global calculations to determine the output voltage at a given value of R1 and R2:

$$V_{REG7} = 1.2 \times \left(1 + \frac{R1}{R2}\right)$$

To meet an overall accuracy of 5 % the external resistors should have a 1 % tolerance and the total resistance of the external resistors should have a value maximum 2 kΩ.

In the event that no external resistors are used the output voltage will be determined only by the internal feedback resistors. The output voltage will be as follows: V_o = 10 V (±5 %).

Table 8: ESR restrictions

Output of regulator	Maximum ESR
Regulator 1	3 Ω
Regulator 2	3 Ω
Regulator 3	6 Ω
Regulator 4	20 Ω
Regulator 5	6 Ω
Regulator 6	14 Ω
Regulator 7	10 Ω

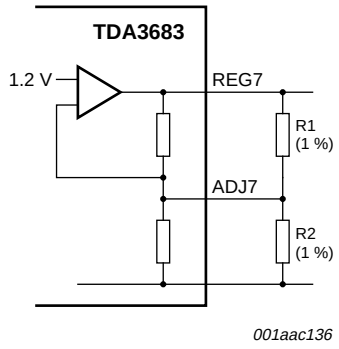
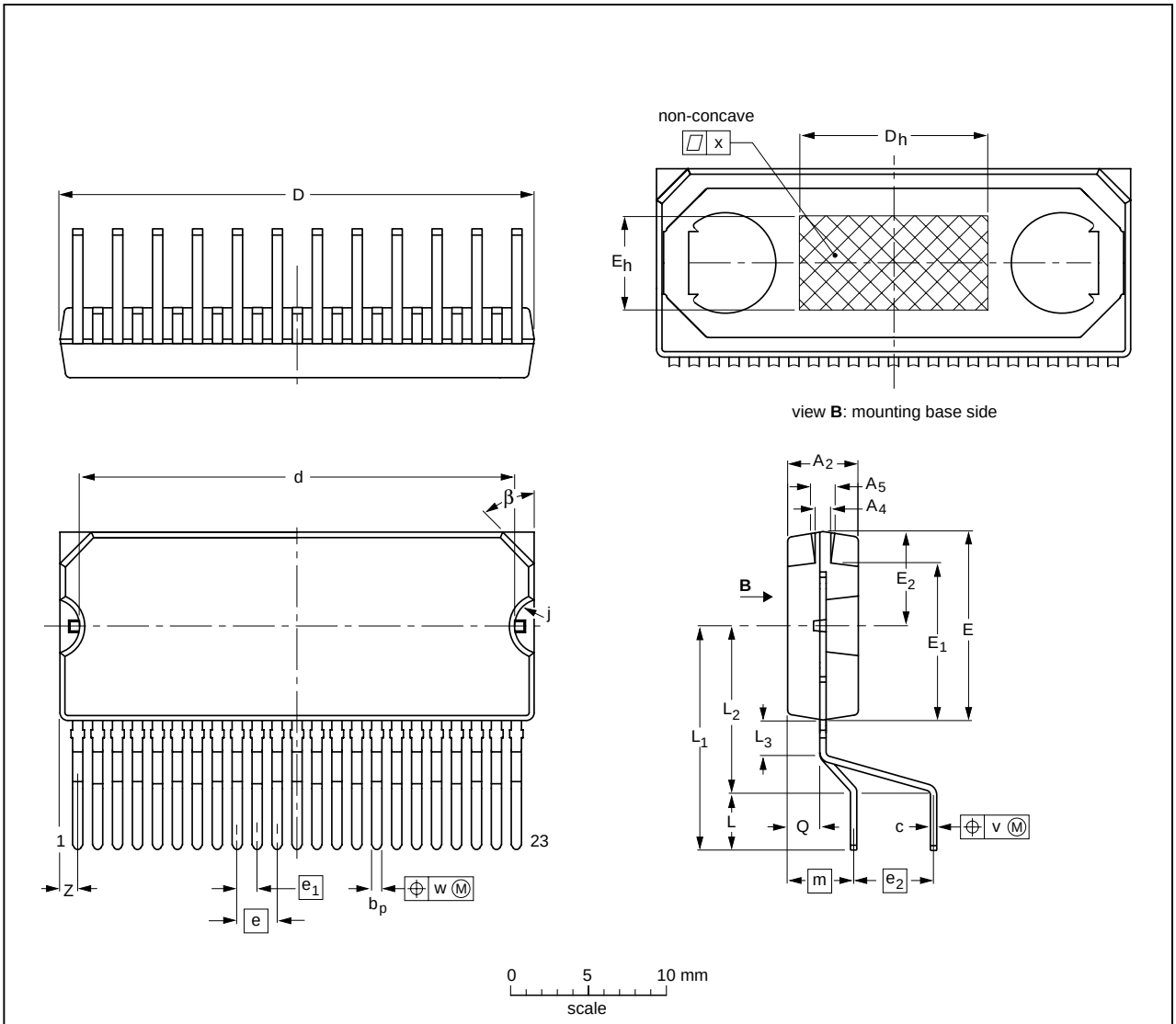


Fig 10. Application diagram for REG7

12. Package outline

DBS23P: plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm) **SOT411-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2	A_4	A_5	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	E_1	E_2	j	L	L_1	L_2	L_3	m	Q	v	w	x	β	$Z^{(1)}$
mm	4.6 4.3	1.15 0.85	1.65 1.35	0.75 0.60	0.55 0.35	30.4 29.9	28.0 27.5	12	12.2 11.8	2.54	1.27	5.08	6	10.15 9.85	6.2 5.8	1.85 1.65	3.6 2.8	14 13	10.7 9.9	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	45°	1.43 0.78

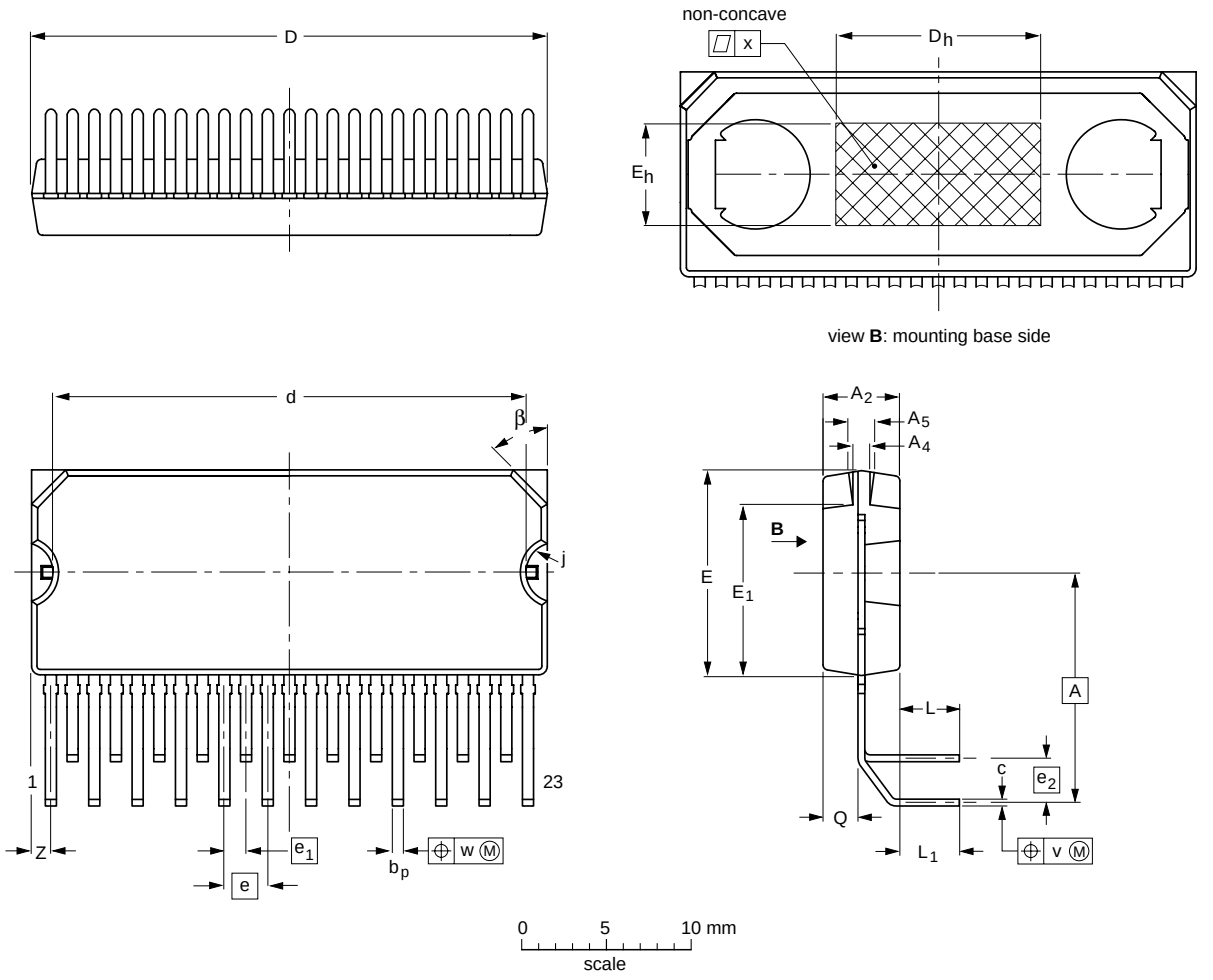
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT411-1						~~98-02-20~~ 02-04-24

Fig 11. Package outline SOT411-1 (DBS23P)

RDBS23P: plastic rectangular-DIL-bent-SIL (reverse bent) power package; 23 leads (row spacing 2.54 mm) **SOT889-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	A_4	A_5	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	E_1	j	L	L_1	Q	v	w	x	β	$Z^{(1)}$
mm	13.5	4.6 4.3	1.15 0.85	1.65 1.35	0.75 0.60	0.55 0.35	30.4 29.9	28.0 27.5	12	12.2 11.8	2.54	1.27	2.54	6	10.15 9.85	1.85 1.65	3.75 3.15	3.75 3.15	2.1 1.8	0.6	0.25	0.03	45°	1.43 0.78

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT889-1						~~05-02-15~~ 05-03-24

Fig 12. Package outline SOT889-1 (RDBS23P)

13. Soldering

13.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

13.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

13.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

13.4 Package related soldering information

Table 9: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	-	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable [1]
PMFP [2]	-	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TDA3683_2	20051007	Product data sheet	-	-	TDA3683J_1
Modifications:	• Replaced through the document TDA3683J with TDA3683 • Section 4 “Ordering information”: Added TDA3683SD (SOT889-1 package) • Section 7.5 “Storage capacitor”: Added last paragraph • Section 10 “Characteristics” – Added on page 15 two values to $I_{q(tot)}$ – Changed on page 16 symbols $V_{th(r)(RST1)}$ and $V_{th(f)(RST1)}$ to $V_{th(r)(RDC1)}$ and $V_{th(f)(RDC1)}$ with adapted parameter description – Added on page 16 parameters $V_{OH(RST1)}$ and $V_{OL(RST1)}$ – Changed on page 17 symbols $V_{th(r)(RST2/3)}$ and $V_{th(f)(RST2/3)}$ to $V_{th(r)(RDC2/3)}$ and $V_{th(f)(RDC2/3)}$ with adapted parameter description – Added on page 17 parameters $V_{OH(RST2/3)}$ and $V_{OL(RST2/3)}$ – Changed on page 18 to 20 the values of $I_{m(REG1)}$ to $I_{m(REG7)}$ and $I_{DC(PSW)}$ • Figure 9: Added a figure note with component specifications • Section 12 “Package outline”: Added SOT889-1 drawing				
TDA3683J_1	20041213	Preliminary data sheet	-	9397 750 13057	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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20. Contents

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