THE DATASHEET OF

LTC3577EUFF-1#PBF

Highly Integrated 6-Channel Portable PMIC

FEATURES

- **Full Featured Li-Ion/Polymer Charger/PowerPath™ Controller with Instant-On Operation**
- **Triple Adjustable High Efficiency Step-Down Switching Regulators (800mA, 500mA, 500mA I_{OUT})**
- **6µA Battery Drain Current in Hard Reset**
- **Bat-Track™ Control for External HV Buck DC/DCs**
- **I^2C Adjustable SW Slew Rates for EMI Reduction**
- **High Temperature Battery Voltage Reduction Improves Safety and Reliability**
- Overvoltage Protection for USB (V_{BUS})/Wall Inputs Provides Protection to 30V
- Integrated 40V Series LED Backlight Driver with 60dB Brightness Control and Gradation via I^2C
- 1.5A Maximum Charge Current with Thermal Limiting
- Battery Float Voltage: 4.2V (LTC3577)
  4.1V (LTC3577-1)
- Pushbutton On/Off Control with System Reset
- Dual 150mA Current Limited LDOs
- Small 4mm × 7mm 44-Pin QFN Package

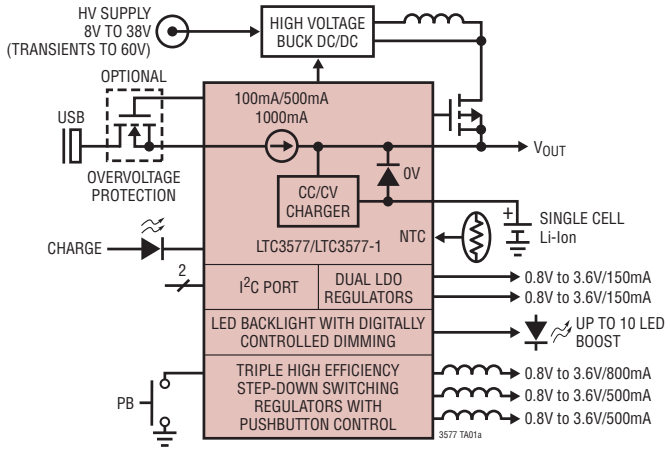
APPLICATIONS

- PNDs, DMB/DVB-H; Digital/Satellite Radio; Media Players
- Portable Industrial/Medical Products
- Universal Remotes, Photo Viewers
- Other USB-Based Handheld Products

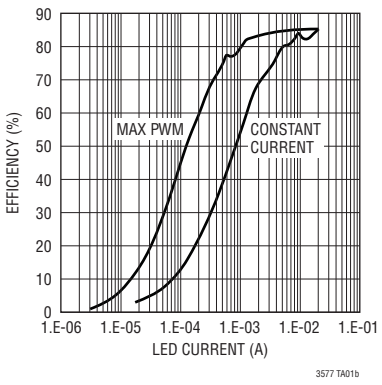
DESCRIPTION

The LTC®3577 is a highly integrated power management IC for single cell Li-Ion/Polymer battery applications. It includes a PowerPath manager with automatic load prioritization, a battery charger, an ideal diode, input overvoltage protection and numerous other internal protection features. The LTC3577 is designed to accurately charge from current limited supplies such as USB by automatically reducing charge current such that the sum of the load current and the charge current does not exceed the programmed input current limit (100mA or 500mA modes). The LTC3577 reduces the battery voltage at elevated temperatures to improve safety and reliability. Efficient high current charging from supplies up to 38V is available using the on-chip Bat-Track controller. The LTC3577 also includes a pushbutton input to control the three synchronous step-down switching regulators and system reset. The onboard LED backlight boost circuitry can drive up to 10 series LEDs and includes versatile digital dimming via I^2C input. The I^2C input also controls two 150mA LDOs as well as other operating modes and status read back. The LTC3577 is available in a low profile 4mm × 7mm × 0.75mm 44-pin QFN package.

TYPICAL APPLICATION



LED Driver Efficiency (10 LEDs)



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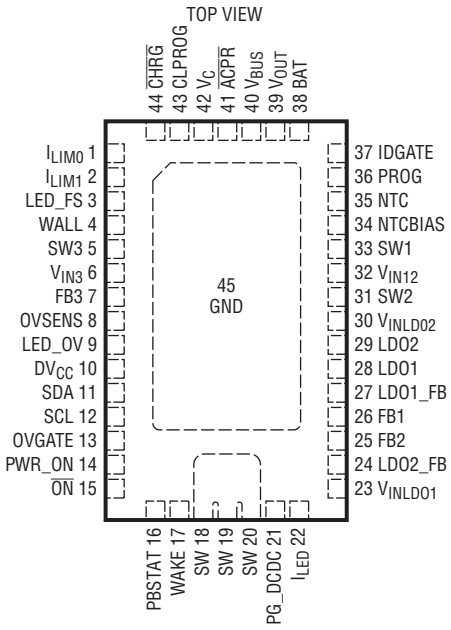
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V_{SW} ..... –0.3V to 45V
V_{BUS}, V_{OUT}, V_{IN12}, V_{IN3}, V_{INLDO1}, V_{INLDO2}, WALL
t < 1ms and Duty Cycle < 1% ..... –0.3V to 7V
Steady State ..... –0.3V to 6V
$\overline{CHRG}$, BAT, LED_FS, LED_OV, PWR_ON, WAKE, PBSTAT, PG_DCDC, FB1, FB2, FB3, LDO1, LDO1_FB, LDO2, LDO2_FB, DV_{CC}, SCL, SDA ..... –0.3V to 6V
NTC, PROG, CLPROG, $\overline{ON}$, I_{LIM0}, I_{LIM1}
(Note 4) ..... –0.3V to V_{CC} + 0.3V
I_{VBUS}, I_{VOUT}, I_{BAT}, Continuous (Note 16) 2A
I_{SW3}, Continuous (Note 16) 850mA
I_{SW2}, I_{SW1}, Continuous (Note 16) 600mA
I_{LDO1}, I_{LDO2}, Continuous (Note 16) 200mA
$I_{\overline{CHRG}}$, $I_{\overline{ACPR}}$, I_{WAKE}, I_{PBSTAT}, I_{PG_DCDC} 75mA
I_{OVSENS} 10mA
I_{CLPROG}, I_{PROG}, I_{LED_FS}, I_{LED_OV} 2mA
Junction Temperature ..... 110°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UFF PACKAGE
44-LEAD (7mm × 4mm) PLASTIC QFN

T_{JMAX} = 110°C, θ_{JA} = 45°C/W
EXPOSED PAD (PIN 45) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3577EUFF#PBF	LTC3577EUFF#TRPBF	3577	44-Lead (4mm × 7mm) Plastic QFN	–40°C to 85°C
LTC3577EUFF-1#PBF	LTC3577EUFF-1#TRPBF	35771	44-Lead (4mm × 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

Power Manager. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, V_{BAT} = 3.8V, I_{LIM0} = I_{LIM1} = WALL = 0V, V_{INLDO1} = V_{INLDO2} = V_{IN12} = V_{IN3} = V_{OUT}, R_{PROG} = 2k, R_{CLPROG} = 2.1k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply							
V_{BUS}	Input Supply Voltage			4.35		5.5	V
$I_{BUS(LIM)}$	Total Input Current (Note 5)	I_{LIM0} = 0V, I_{LIM1} = 0V (1x Mode) I_{LIM0} = 5V, I_{LIM1} = 5V (5x Mode) I_{LIM0} = 5V, I_{LIM1} = 0V (10x Mode)	● ● ●	80 450 900	90 475 950	100 500 1000	mA mA mA
I_{BUSQ}	Input Quiescent Current, POFF State	1x, 5x, 10x Modes I_{LIM0} = 0V, I_{LIM1} = 5V (Suspend Mode)			0.42 0.042	 0.1	mA mA
h_{CLPROG}	Ratio of Measured V_{BUS} Current to CLPROG Program Current				1000		mA/mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	1x Mode 5x Mode 10x Mode			0.2 1.0 2.0		V V V
V_{UVLO}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.5	3.8 3.7	3.9 	V V
V_{DUVLO}	V_{BUS} to V_{OUT} Differential Undervoltage Lockout	Rising Threshold Falling Threshold			50 –50	100 	mV mV
R_{ON_ILIM}	Input Current Limit Power FET On-Resistance (Between V_{BUS} and V_{OUT})				200		mΩ
Battery Charger							
V_{FLOAT}	V_{BAT} Regulated Output Voltage	LTC3577 LTC3577, 0 ≤ T_A ≤ 85°C LTC3577-1 LTC3577-1, 0 ≤ T_A ≤ 85°C		4.179 4.165 4.079 4.065	4.200 4.200 4.100 4.100	4.221 4.235 4.121 4.135	V V V V
I_{CHG}	Constant-Current Mode Charge Current	R_{PROG} = 1k, Input Current Limit = 2A R_{PROG} = 2k, Input Current Limit = 1A R_{PROG} = 5k, Input Current Limit = 0.4A	● ● ●	950 465 180	1000 500 200	1050 535 220	mA mA mA
I_{BATQ_HR}	Battery Drain Current, Hard Reset	V_{BUS} = 0V, I_{OUT} = 0µA			7	15	µA
I_{BATQ_OFF}	Battery Drain Current, POFF State	V_{BAT} = 4.3V, Charger Time Out V_{BUS} = 0V			6 40	27 100	µA µA
I_{BATQ_ON}	Battery Drain Current, PON State LDOs, and LED Backlight Disabled	V_{BUS} = 0V, I_{OUT} = 0µA, No Load on Supplies, Burst Mode Operation (Note 10)			90	160	µA
$V_{PROG,CHG}$	PROG Pin Servo Voltage	V_{BAT} > V_{TRKL}			1.000		V
$V_{PROG,TRKL}$	PROG Pin Servo Voltage in Trickle Charge	V_{BAT} < V_{TRKL}			0.100		V
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1000		mA/mA
I_{TRKL}	Trickle Charge Current	V_{BAT} < V_{TRKL}		40	50	60	mA
V_{TRKL}	Trickle Charge Rising Threshold Trickle Charge Falling Threshold	V_{BAT} Rising V_{BAT} Falling		 2.5	2.85 2.75	3.0 	V V
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–100	–125	mV
t_{TERM}	Safety Timer Termination Period	Timer Starts When V_{BAT} = V_{FLOAT} – 50mV		3.2	4	4.8	Hour
t_{BADBAT}	Bad Battery Termination Time	V_{BAT} < V_{TRKL}		0.4	0.5	0.6	Hour
$h_{C/10}$	End-of-Charge Indication Current Ratio	(Note 6)		0.085	0.1	0.11	mA/mA
R_{ON_CHG}	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)				200		mΩ
T_{LIM}	Junction Temperature in Constant Temperature Mode				110		°C

ELECTRICAL CHARACTERISTICS

Power Manager. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, V_{BAT} = 3.8V, I_{LIM0} = I_{LIM1} = WALL = 0V, V_{INLDO1} = V_{INLDO2} = V_{IN12} = V_{IN3} = V_{OUT}, R_{PROG} = 2k, R_{CLPROG} = 2.1k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NTC, Battery Discharge Protection							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising NTC Voltage Hysteresis		75	76 1.3	77	$\%V_{NTCBIAS}$ $\%V_{NTCBIAS}$
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling NTC Voltage Hysteresis		34	35 1.3	36	$\%V_{NTCBIAS}$ $\%V_{NTCBIAS}$
V_{2HOT}	NTC Discharge Threshold Voltage	Falling NTC Voltage Hysteresis		24.5	25.5 50	26.5	$\%V_{NTCBIAS}$ mV
I_{NTC}	NTC Leakage Current	V_{NTC} = V_{BUS} = 5V		–50		50	nA
$I_{BAT2HOT}$	BAT Discharge Current	V_{BAT} = 4.1V, NTC < V_{TOO_HOT}			180		mA
$V_{BAT2HOT}$	BAT Discharge Threshold	I_{BAT} < 0.1mA, NTC < V_{TOO_HOT}			3.9		V
Ideal Diode							
V_{FWD}	Forward Voltage Detection	I_{OUT} = 10mA		5	15	25	mV
$R_{DROPOUT}$	Diode On-Resistance, Dropout	I_{OUT} = 200mA			200		mΩ
I_{MAX}	Diode Current Limit	(Note 7)			3.6		A
Overvoltage Protection							
$V_{OVCUTOFF}$	Overvoltage Protection Threshold	Rising Threshold, R_{OVSENS} = 6.2k		6.10	6.35	6.70	V
V_{OVGATE}	OVGATE Output Voltage	Input Below $V_{OVCUTOFF}$ Input Above $V_{OVCUTOFF}$			1.88 • V_{OVSENS} 0	12	V V
$I_{OVSENSQ}$	OVSENS Quiescent Current	V_{OVSENS} = 5V			40		µA
t_{RISE}	OVGATE Time to Reach Regulation	C_{OVGATE} = 1nF			2.5		ms
Wall Adapter							
$V_{\overline{ACPR}}$	$\overline{ACPR}$ Pin Output High Voltage $\overline{ACPR}$ Pin Output Low Voltage	$I_{\overline{ACPR}}$ = 0.1mA $I_{\overline{ACPR}}$ = 1mA		V_{OUT} – 0.3	V_{OUT} 0	 0.3	V V
V_W	Absolute Wall Input Threshold Voltage	V_{WALL} Rising V_{WALL} Falling		 3.1	4.3 3.2	4.45	V V
ΔV_W	Differential Wall Input Threshold Voltage	V_{WALL} – V_{BAT} Falling V_{WALL} – V_{BAT} Rising		0	25 75	 100	mV mV
I_{QWALL}	Wall Operating Quiescent Current	I_{WALL} + I_{VOUT}, I_{BAT} = 0mA, WALL = V_{OUT} = 5V			440		µA
Logic (I_{LIM0}, I_{LIM1} and $\overline{CHRG}$)							
V_{IL}	Input Low Voltage	I_{LIM0}, I_{LIM1}				0.4	V
V_{IH}	Input High Voltage	I_{LIM0}, I_{LIM1}		1.2			V
I_{PD}	Static Pull-Down Current	I_{LIM0}, I_{LIM1}; V_{PIN} = 1V			2		µA
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 10mA			0.15	0.4	V
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Input Current	V_{BAT} = 4.5V, $V_{\overline{CHRG}}$ = 5V			0	1	µA

ELECTRICAL CHARACTERISTICS

I²C Interface. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. DV_{CC} = 3.3V, V_{OUT} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DV_{CC}	Input Supply Voltage			1.6		5.5	V
I_{DVCC}	DV_{CC} Supply Current	SCL = 400kHz SCL = SDA = 0kHz			1 0.4		µA µA
$V_{DVCC,UVLO}$	DV_{CC} UVLO				1.0		V
V_{IH}	Input HIGH Voltage				50	70	$\%DV_{CC}$
V_{IL}	Input LOW Voltage			30	50		$\%DV_{CC}$
I_{IH}	Input HIGH Leakage Current	SDA = SCL = DV_{CC} = 5.5V		–1		1	µA
I_{IL}	Input LOW Leakage Current	SDA = SCL = 0V, DV_{CC} = 5.5V		–1		1	µA
V_{OL}	SDA Output LOW Voltage	I_{SDA} = 3mA				0.4	V
Timing Characteristics (Note 8) (All Values are Referenced to V_{IH} and V_{IL})							
f_{SCL}	SCL Clock Frequency					400	kHz
t_{LOW}	LOW Period of the SCL Clock			1.3			µs
t_{HIGH}	HIGH Period of the SCL Clock			0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition			0.6			µs
$t_{SU,STA}$	Setup Time for a Repeated Start Condition			0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time			0.6			µs
$t_{HD,DATO}$	Output Data Hold Time			0		900	ns
$t_{HD,DATI}$	Input Data Hold Time			0			ns
$t_{SU,DAT}$	Data Setup Time			100			ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns

Step-Down Switching Regulators. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = V_{IN12} = V_{IN3} = 3.8V, all regulators enabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Down Switching Regulators (Buck1, Buck2 and Buck3)							
V_{IN12}, V_{IN3}	Input Supply Voltage	(Note 9)	●	2.7		5.5	V
V_{OUT} UVLO	V_{OUT} Falling V_{OUT} Rising	V_{IN12} and V_{IN3} Connected to V_{OUT} Through Low Impedance. Switching Regulators are Disabled Below V_{OUT} UVLO		2.5	2.7 2.8	 2.9	V V
f_{OSC}	Oscillator Frequency			1.91	2.25	2.59	MHz
800mA Step-Down Switching Regulator 3 (Buck3 – Pushbutton Enabled, Third in Sequence)							
I_{VIN3Q}	Pulse-Skipping Mode Input Current	(Note 10)			100		µA
	Burst Mode Operation Input Current	(Note 10)			17		µA
	Shutdown Input Current				0.01		µA
I_{LIM3}	Peak PMOS Current Limit	(Note 7)		1000	1400	1700	mA
V_{FB3}	Feedback Voltage	Pulse-Skipping Mode Burst Mode Operation	● ●	0.78 0.78	0.8 0.8	0.82 0.824	V V
I_{FB3}	FB3 Input Current	(Note 10)		–0.05		0.05	µA
D3	Max Duty Cycle	FB3 = 0V		100			%
R_{P3}	$R_{DS(ON)}$ of PMOS				0.3		Ω
R_{N3}	$R_{DS(ON)}$ of NMOS				0.4		Ω

ELECTRICAL CHARACTERISTICS

Step-Down Switching Regulators. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = V_{IN12} = V_{IN3} = 3.8V, all regulators enabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{SW3_PD}	SW3 Pull-Down in Shutdown	POFF State			10		kΩ
500mA Step-Down Switching Regulator 2 (Buck2 – Pushbutton Enabled, Second in Sequence)							
I_{VIN12Q}	Pulse-Skipping Mode Input Current	(Note 10)			100		µA
	Burst Mode Operation Input Current	(Note 10)			17		µA
	Shutdown Input Current				0.01		µA
I_{LIM2}	Peak PMOS Current Limit	(Note 7)		650	900	1200	mA
V_{FB2}	Feedback Voltage	Pulse-Skipping Mode Burst Mode Operation	● ●	0.78 0.78	0.8 0.8	0.82 0.824	V V
I_{FB2}	FB2 Input Current	(Note 10)		–0.05		0.05	µA
D2	Max Duty Cycle	FB2 = 0V		100			%
R_{P2}	$R_{DS(ON)}$ of PMOS	I_{SW2} = 100mA			0.6		Ω
R_{N2}	$R_{DS(ON)}$ of NMOS	I_{SW2} = –100mA			0.6		Ω
R_{SW2_PD}	SW2 Pull-Down in Shutdown	POFF State			10		kΩ
500mA Step-Down Switching Regulator 1 (Buck1 – Pushbutton Enabled, First in Sequence)							
I_{VIN12Q}	Pulse-Skipping Mode Input Current	(Note 10)			100		µA
	Burst Mode Operation Input Current	(Note 10)			17		µA
	Shutdown Input Current				0.01		µA
I_{LIM1}	Peak PMOS Current Limit	(Note 7)		650	900	1200	mA
V_{FB1}	Feedback Voltage	Pulse-Skipping Mode Burst Mode Operation	● ●	0.78 0.78	0.8 0.8	0.82 0.824	V V
I_{FB1}	FB1 Input Current	(Note 10)		–0.05		0.05	µA
D1	Max Duty Cycle	FB1 = 0V		100			%
R_{P1}	$R_{DS(ON)}$ of PMOS	I_{SW1} = 100mA			0.6		Ω
R_{N1}	$R_{DS(ON)}$ of NMOS	I_{SW1} = –100mA			0.6		Ω
R_{SW1_PD}	SW1 Pull-Down in Shutdown	POFF State			10		kΩ

LDO Regulators. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{INLDO1} = V_{INLDO2} = V_{OUT} = V_{BAT} = 3.8V, LDO1 and LDO2 enabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Regulator 1 (LDO1 – Enabled via I^2C)							
V_{INLDO1}	Input Voltage Range	$V_{INLDO1} \le V_{OUT}$ + 0.3V	●	1.65		5.5	V
V_{OUT_UVLO}	V_{OUT} Falling V_{OUT} Rising	LDO1 is Disabled Below V_{OUT} UVLO		2.5	2.7 2.8	 2.9	V V
I_{QLDO1_VO} I_{QLDO1_VI}	LDO1 V_{OUT} Quiescent Current LDO1 V_{INLDO1} Quiescent Current	LDO1 Enabled, PON State, I_{LDO1} = 0mA LDO1 Enabled, PON State, I_{LDO1} = 0mA			18 0.1	30 2	µA µA
$I_{VINLDO1}$	Shutdown Current	LDO1 Disabled, PON or POFF State			0.01	1	µA
V_{LDO1_FB}	LDO1_FB Regulated Feedback Voltage	I_{LDO1} = 1mA	●	0.78	0.8	0.82	V
	LDO1_FB Line Regulation (Note 11)	I_{LDO1} = 1mA, V_{IN} = 1.65V to 5.5V			0.4		mV/V
	LDO1_FB Load Regulation (Note 11)	I_{LDO1} = 1mA to 150mA			5		µV/mA
I_{LDO1_FB}	LDO1_FB Input Current	LDO1_FB = 0.8V		–50		50	nA
I_{LDO1_OC}	Available Output Current		●	150			mA

ELECTRICAL CHARACTERISTICS

LDO Regulators. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{INLDO1} = V_{INLDO2} = V_{OUT} = V_{BAT} = 3.8V, LDO1 and LDO2 enabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LDO1_SC}	Short-Circuit Output Current				270		mA
V_{DROP1}	Dropout Voltage (Note 12)	I_{LDO1} = 150mA, V_{INLDO1} = 3.6V I_{LDO1} = 150mA, V_{INLDO1} = 2.5V I_{LDO1} = 75mA, V_{INLDO1} = 1.8V			160 200 170	260 320 280	mV mV mV
R_{LDO1_PD}	Output Pull-Down Resistance in Shutdown	LDO1 Disabled			10		kΩ
LDO Regulator 2 (LDO2 – Enabled via I²C)							
V_{INLDO2}	Input Voltage Range	$V_{INLDO2} \le V_{OUT}$ + 0.3V	●	1.65		5.5	V
V_{OUT_UVLO}	V_{OUT} Falling V_{OUT} Rising	LDO2 is Disabled Below V_{OUT} UVLO		2.5	2.7 2.8	 2.9	V V
I_{QLDO2_VO} I_{QLDO2_VI}	LDO2 V_{OUT} Quiescent Current LDO2 V_{INLDO2} Quiescent Current	LDO2 Enabled, PON State, I_{LDO2} = 0mA LDO2 Enabled, PON State, I_{LDO2} = 0mA			18 0.1	30 2	µA µA
$I_{VINLDO2}$	Shutdown Current	LDO2 Disabled, PON or POFF State			0.01	1	µA
V_{LDO2_FB}	LDO2_FB Regulated Output Voltage	I_{LDO2} = 1mA	●	0.78	0.8	0.82	V
	LDO2_FB Line Regulation (Note 11)	I_{LDO2} = 1mA, V_{IN} = 1.65V to 5.5V			0.4		mV/V
	LDO2_FB Load Regulation (Note 11)	I_{LDO2} = 1mA to 150mA			5		µV/mA
I_{LDO2_FB}	LDO2_FB Input Current	LDO2_FB = 0.8V		–50		50	nA
I_{LDO2_OC}	Available Output Current		●	150			mA
I_{LDO2_SC}	Short-Circuit Output Current				270		mA
V_{DROP2}	Dropout Voltage (Note 12)	I_{LDO2} = 150mA, V_{INLDO2} = 3.6V I_{LDO2} = 150mA, V_{INLDO2} = 2.5V I_{LDO1} = 75mA, V_{INLDO1} = 1.8V			160 200 170	260 320 280	mV mV mV
R_{LDO2_PD}	Output Pull-Down Resistance in Shutdown	LDO2 Disabled			14		kΩ

LED Boost Switching Regulator. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN3} = V_{OUT} = 3.8V, R_{OV} = 10M, R_{LED_FS} = 20k, boost regulator disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN3}, V_{OUT}	Operating Supply Range	(Note 9)	●	2.7		5.5	V
I_{VOUT_LED}	Operating Quiescent Current Shutdown Quiescent Current	(Notes 10, 14)			560 0.01		µA µA
V_{LED_OV}	LED_OV Overvoltage Threshold	LED_OV Rising LED_OV Falling		 0.6	1.0 0.85	1.25	V V
I_{LIM}	Peak NMOS Switch Current			800	1000	1200	mA
I_{LED_FS}	I_{LED} Pin Full-Scale Operating Current			18	20	22	mA
I_{LED_DIM}	I_{LED} Pin Full-Scale Dimming Range	64 Steps			60		dB
R_{NSWON}	$R_{DS(ON)}$ of NMOS Switch				240		mΩ
I_{NSWOFF}	NMOS Switch-Off Leakage Current	V_{SW} = 5.5V			0.01	1	µA
f_{OSC}	Oscillator Frequency			0.95	1.125	1.3	MHz
V_{LED_FS}	LED_FS Pin Voltage		●	780	800	820	mV
I_{LED_OV}	LED_OV Pin Current	R_{LED_FS} = 20k	●	3.8	4	4.2	µA
D_{BOOST}	Maximum Duty Cycle	I_{LED} = 0			97		%
$V_{BOOSTFB}$	Boost Mode I_{LED} Feedback Voltage		●	775	800	825	mV

ELECTRICAL CHARACTERISTICS

Pushbutton Controller. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Pushbutton Pin ($\overline{ON}$)							
V_{OUT}	Pushbutton Operating Supply Range	(Note 9)	●	2.7		5.5	V
V_{OUT} UVLO	V_{OUT} Falling V_{OUT} Rising	Pushbutton is Disabled Below V_{OUT} UVLO		2.5	2.7 2.8	2.9	V V
$V_{\overline{ON}\_TH}$	$\overline{ON}$ Threshold Rising $\overline{ON}$ Threshold Falling			0.4	0.8 0.7	1.2	V V
$I_{\overline{ON}}$	$\overline{ON}$ Input Current	$V_{\overline{ON}} = V_{OUT}$ $V_{\overline{ON}} = 0V$		–1 –4	–9	1 –14	µA µA
Power-On Input Pin (PWR_ON)							
V_{PWR_ON}	PWR_ON Threshold Rising PWR_ON Threshold Falling			0.4	0.8 0.7	1.2	V V
I_{PWR_ON}	PWR_ON Input Current	V_{PWR_ON} = 3V		–1		1	µA
Status Output Pins (PBSTAT, WAKE, PG_DCDC)							
I_{PBSTAT}	PBSTAT Output High Leakage Current	V_{PBSTAT} = 3V		–1		1	µA
V_{PBSTAT}	PBSTAT Output Low Voltage	I_{PBSTAT} = 3mA			0.1	0.4	V
I_{WAKE}	Wake Output High Leakage Current	V_{WAKE} = 3V		–1		1	µA
V_{WAKE}	Wake Low Output Voltage	I_{WAKE} = 3mA			0.1	0.4	V
I_{PG_DCDC}	PG_DCDC Output High Leakage Current	V_{PG_DCDC} = 3V		–1		1	µA
V_{PG_DCDC}	PG_DCDC Output Low Voltage	I_{PG_DCDC} = 3mA			0.1	0.4	V
V_{THPG_DCDC}	PG_DCDC Threshold Voltage	(Note 13)			–8		%
Pushbutton Timing Parameters							
$t_{ON\_PBSTAT1}$	$\overline{ON}$ Low Time to PBSTAT Low	WAKE High			50		ms
$t_{ON\_PBSTAT2}$	$\overline{ON}$ High to PBSTAT High	PBSTAT Low > t_{PBSTAT_PW}			900		µs
t_{ON_WAKE}	$\overline{ON}$ Low Time to WAKE High	WAKE Low > t_{PWR_ONBK2}			400		ms
t_{ON_HR}	$\overline{ON}$ Low to Hard Reset	Hard Reset = All Supplies Disabled		4.2	5	5.8	Seconds
t_{PBSTAT_PW}	PBSTAT Minimum Pulse Width			40	50	60	ms
t_{WAKE_EXTP}	WAKE High from USB or Wall Present	WAKE Low > t_{PWR_ONBK2}			100		ms
t_{WAKE_DCDC}	WAKE High to Buck1 Enable	WAKE Low > t_{PWR_ONBK2}			5		µs
t_{PWR_ONH}	PWR_ON High to WAKE High	WAKE Low > t_{PWR_ONBK2}			50		ms
t_{PWR_ONL}	PWR_ON Low to WAKE Low	WAKE High > t_{PWR_ONBK1}			50		ms
t_{PWR_ONBK1}	PWR_ON Power-Up Blanking	WAKE Rising Until PWR_ON Low Recognized			5		Seconds
t_{PWR_ONBK2}	PWR_ON Power-Down Blanking	WAKE Falling Until PWR_ON High Recognized			1		Seconds
t_{PG_DCDCH}	Bucks in Regulation to PG_DCDC High	All Bucks Within PG_DCDC Threshold Voltage			230		ms
t_{PG_DCDCL}	Bucks Disabled to PG_DCDC Low	All Bucks Disabled			44		µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3577E/LTC3577E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 110°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 4: V_{CC} is the greater of V_{BUS}, V_{OUT} or BAT.

Note 5: Total input current is the sum of quiescent current, I_{BUSQ}, and measured current given by $V_{CLPROG}/R_{CLPROG} \bullet (h_{CLPROG} + 1)$.

Note 6: $h_{C/10}$ is expressed as a fraction of measured full charge current with indicated PROG resistor.

Note 7: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the specified maximum pin current rating may result in device degradation or failure.

Note 8: The serial port is tested at rated operating frequency. Timing parameters are tested and/or guaranteed by design.

Note 9: V_{OUT} not in UVLO.

Note 10: FB high, not switching.

Note 11: Measured with the LDO running unity gain with output tied to feedback pin.

Note 12: Dropout voltage is the minimum input to output voltage differential needed for an LDO to maintain regulation at a specified output current. When an LDO is in dropout, its output voltage will be equal to $V_{IN} – V_{DROP}$.

Note 13: PG_DCDC threshold is expressed as a percentage difference from the Buck1-3 regulation voltages. The threshold is measured from Buck1-3 output rising.

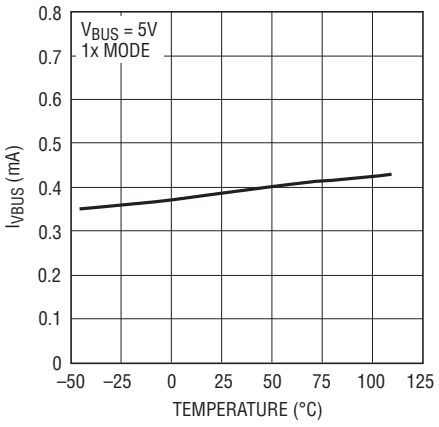
Note 14: I_{VOUT_LED} is the sum of V_{OUT} and V_{IN3} current due to LED driver.

Note 15: The I_{BATQ} specifications represent the total battery load assuming V_{INLDO1}, V_{INLDO2}, V_{IN12} and V_{IN3} are tied directly to V_{OUT}.

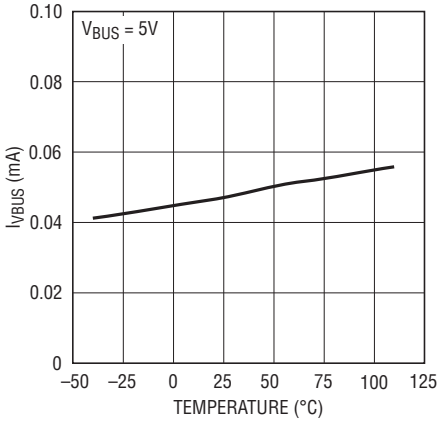
Note 16: Long-term current density rating for the part.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

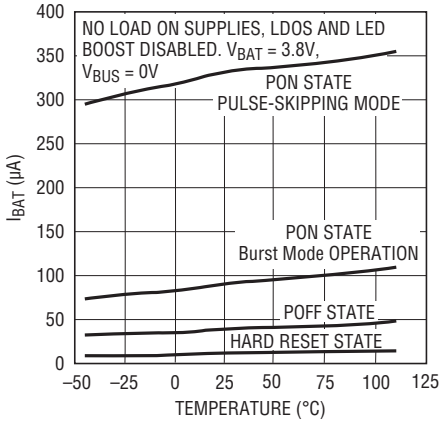
Input Supply Current vs Temperature



Input Supply Current vs Temperature (Suspend Mode)

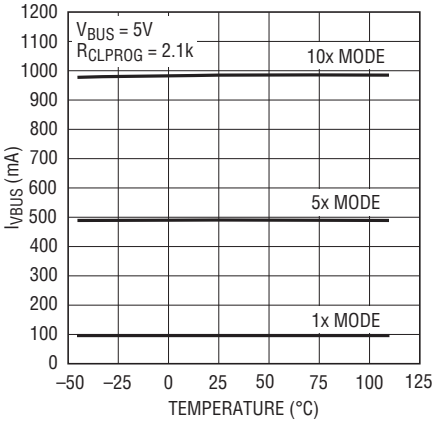


Battery Drain Current vs Temperature



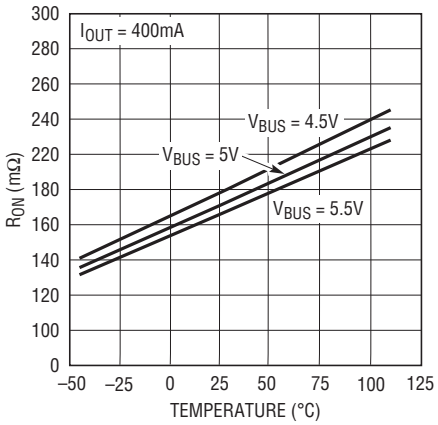
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

Input Current Limit vs Temperature



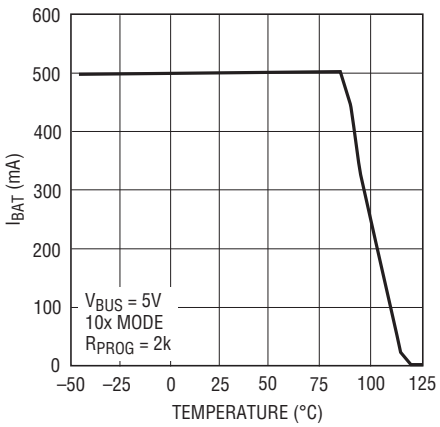
3577 G04

Input R_{ON} vs Temperature



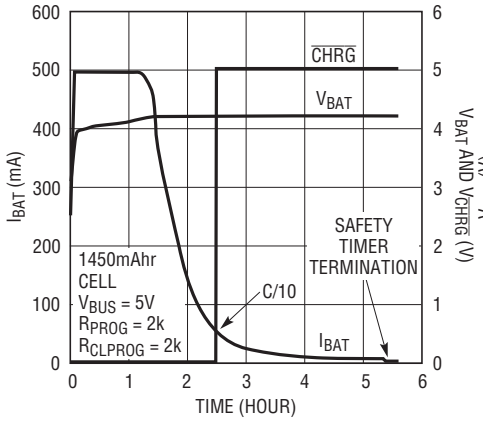
3577 G05

Charge Current vs Temperature (Thermal Regulation)



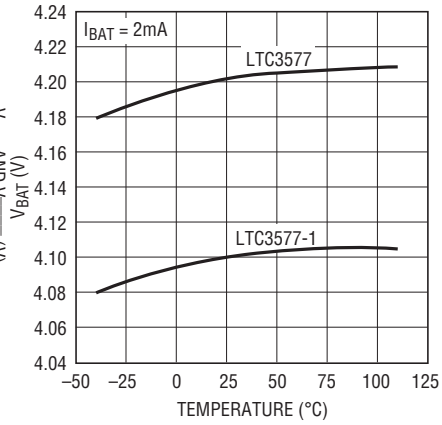
3577 G06

Battery Current and Voltage vs Time



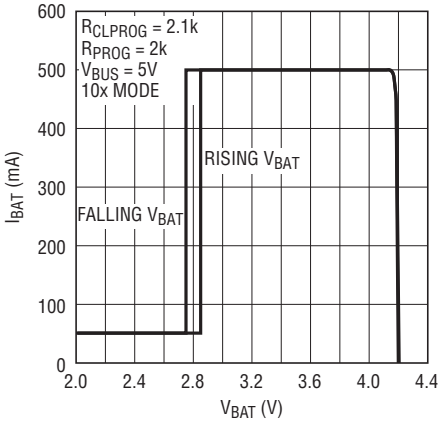
3577 G07

Battery Regulation (Float) Voltage vs Temperature



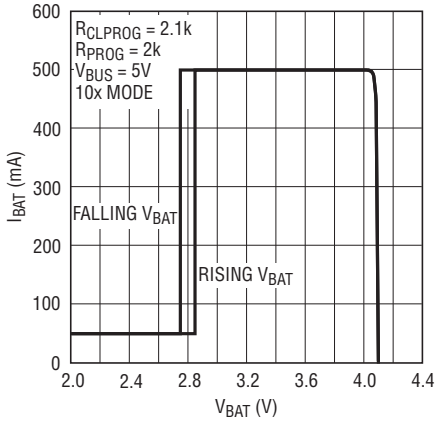
3577 G08

LTC3577 I_{BAT} vs V_{BAT}



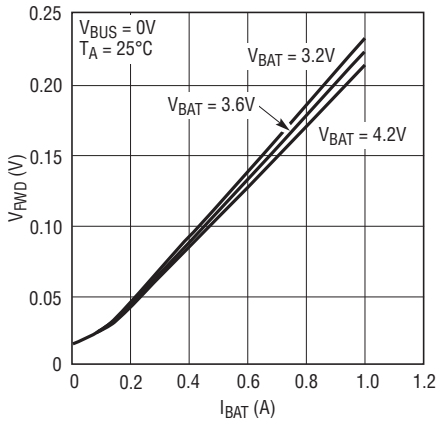
3577 G09

LTC3577-1 I_{BAT} vs V_{BAT}



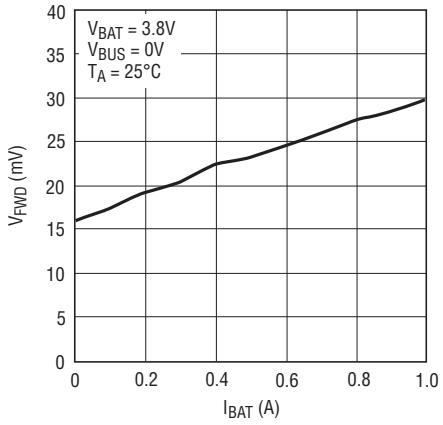
3577 G10

Forward Voltage vs Ideal Diode Current (No External FET)



3577 G11

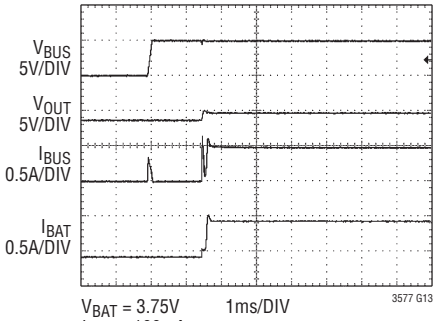
Forward Voltage vs Ideal Diode Current (with Si2333DS External FET)



3577 G12

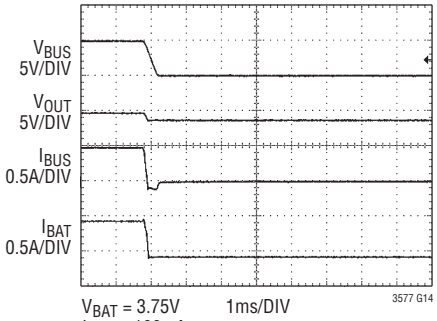
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

Input Connect Waveform



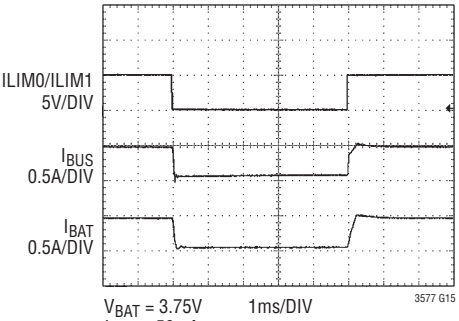
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{CLPROG} = 2k
R_{PROG} = 2k

Input Disconnect Waveform



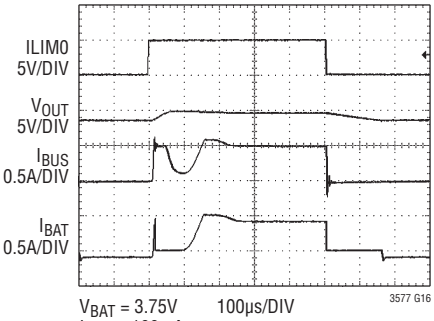
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{CLPROG} = 2k
R_{PROG} = 2k

Switching from 1x to 5x Mode



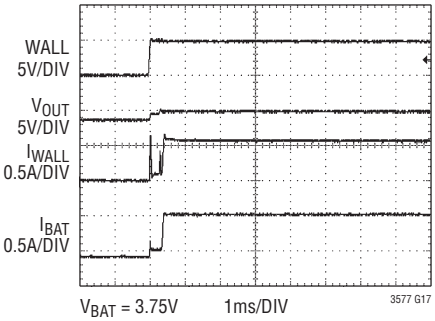
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 50mA
R_{CLPROG} = 2k
R_{PROG} = 2k

Switching from Suspend Mode to 5x Mode



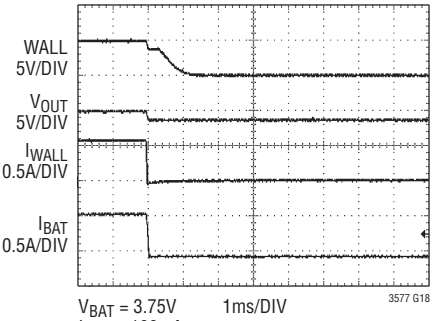
V_{BAT} = 3.75V 100µs/DIV
I_{OUT} = 100mA
R_{CLPROG} = 2k
R_{PROG} = 2k
ILIM1 = 5V

WALL Connect Waveform



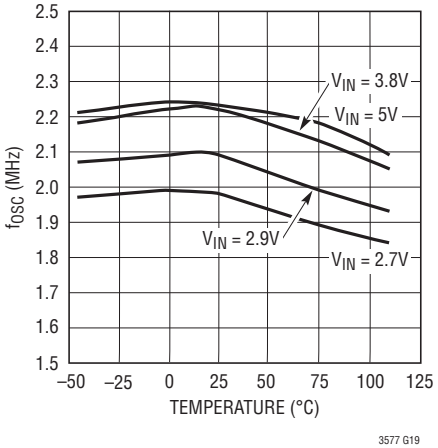
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{PROG} = 2k

WALL Disconnect Waveform

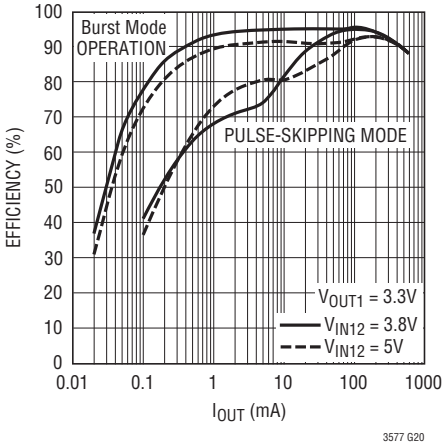


V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{PROG} = 2k

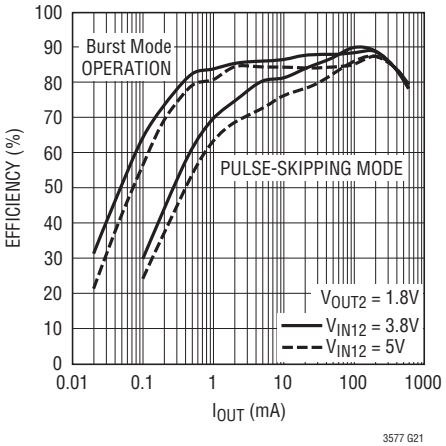
Oscillator Frequency vs Temperature



Step-Down Switching Regulator 1 3.3V Output Efficiency vs I_{OUT1}

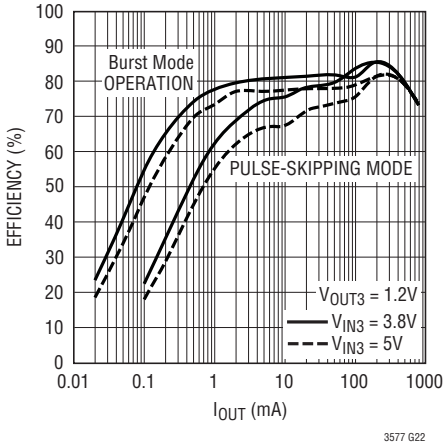


Step-Down Switching Regulator 2 1.8V Output Efficiency vs I_{OUT2}

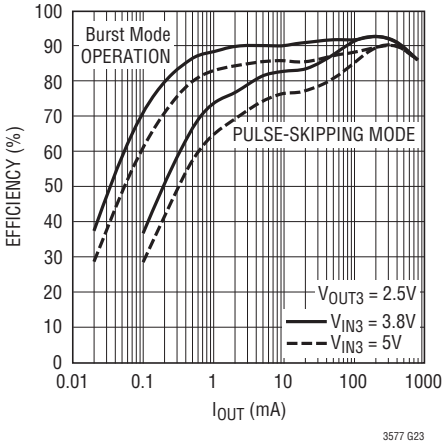


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

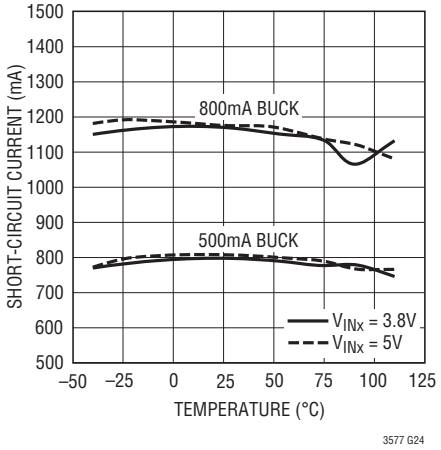
Step-Down Switching Regulator 3 1.2V Output Efficiency vs I_{OUT3}



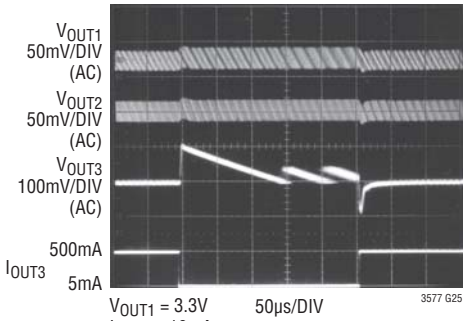
Step-Down Switching Regulator 3 2.5V Output Efficiency vs I_{OUT3}



Step-Down Switching Regulator Short-Circuit Current vs Temperature

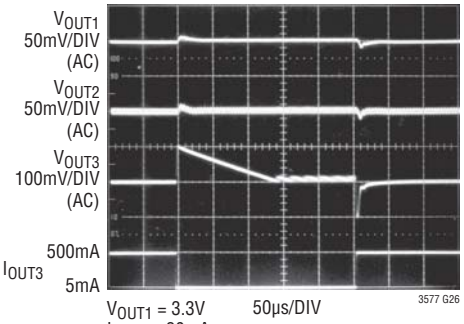


Step-Down Switching Regulator Output Transient (Burst Mode Operation)



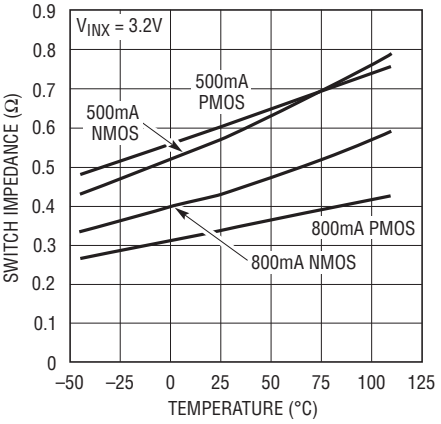
V_{OUT1} = 3.3V 50µs/DIV
I_{OUT1} = 10mA
V_{OUT2} = 1.8V
I_{OUT2} = 20mA
V_{OUT3} = 1.2V
V_{OUT} = V_{BAT} = 3.8V

Step-Down Switching Regulator Output Transient (Pulse-Skipping Mode)

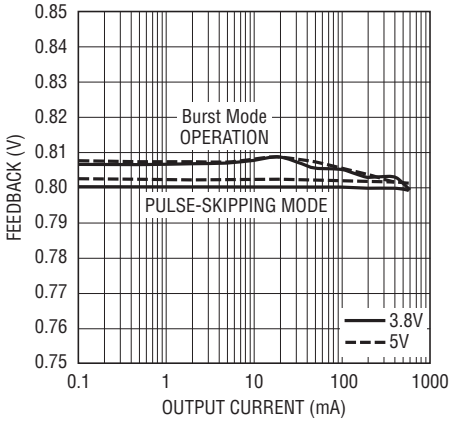


V_{OUT1} = 3.3V 50µs/DIV
I_{OUT1} = 30mA
V_{OUT2} = 1.8V
I_{OUT2} = 20mA
V_{OUT3} = 1.2V
V_{OUT} = V_{BAT} = 3.8V

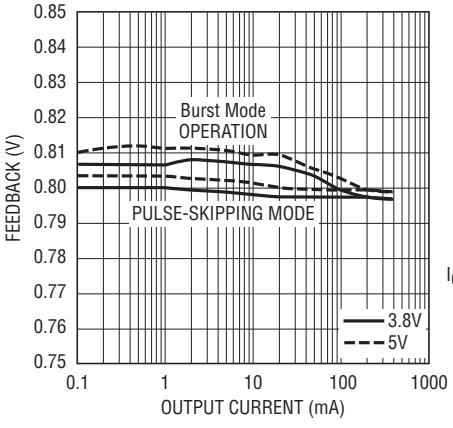
Step-Down Switching Regulator Switch Impedance vs Temperature



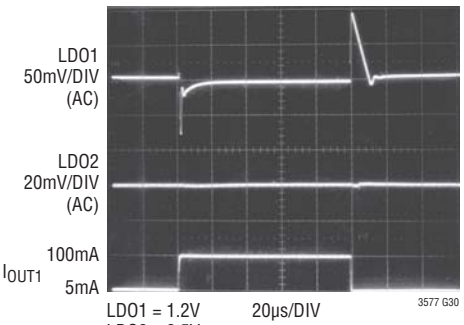
800mA Step-Down Switching Regulator Feedback Voltage vs Output Current



500mA Step-Down Switching Regulator Feedback Voltage vs Output Current



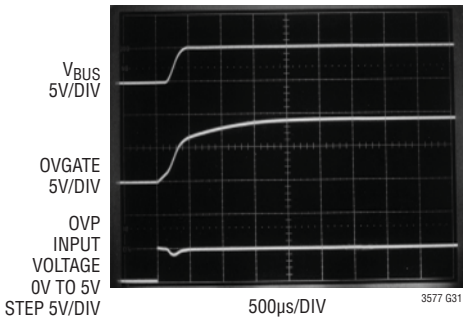
LDO Load Step



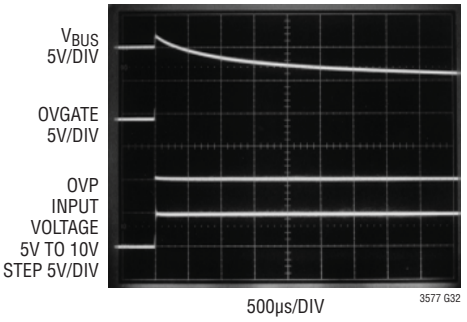
LDO1 = 1.2V 20µs/DIV
LDO2 = 2.5V
I_{LDO2} = 40mA
V_{OUT} = V_{BAT} = 3.8V

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

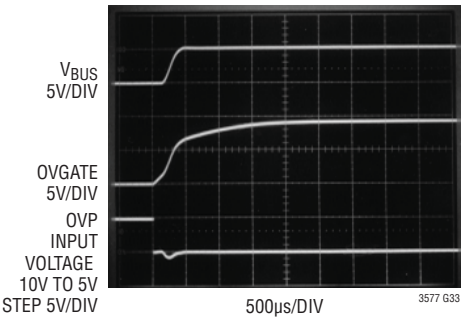
OVP Connection Waveform



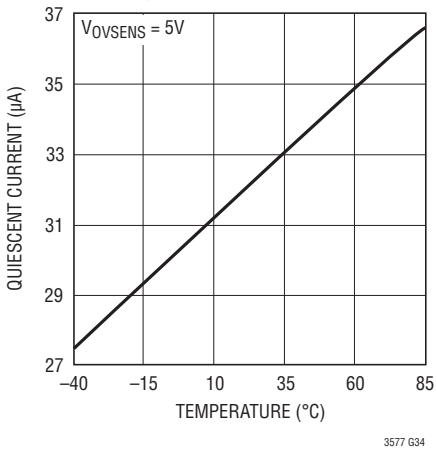
OVP Protection Waveform



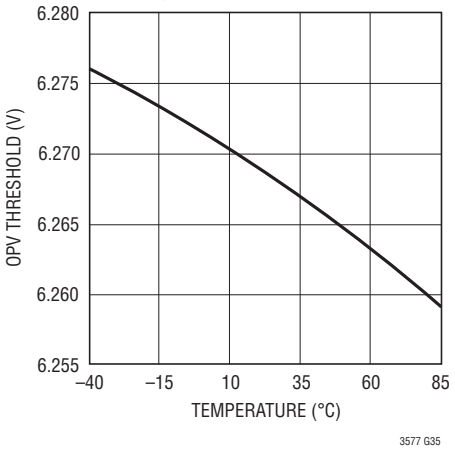
OVP Reconnection Waveform



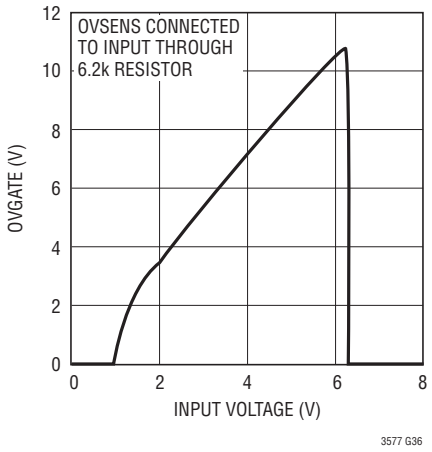
OVSENS Quiescent Current vs Temperature



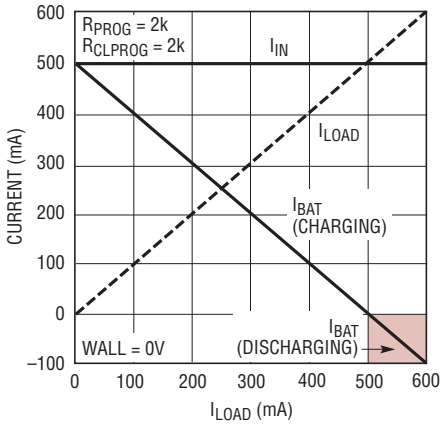
Rising Overvoltage Threshold vs Temperature



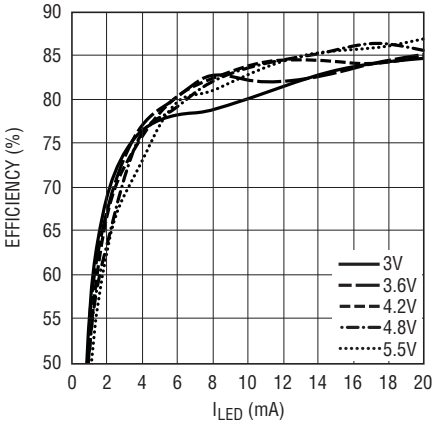
OVGATE vs OVSENS



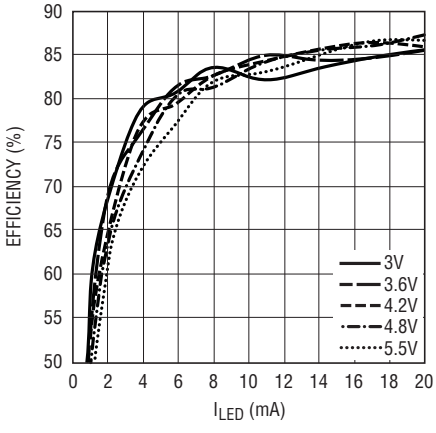
Input and Battery Current vs Load Current



LED Driver Efficiency 10 LEDs

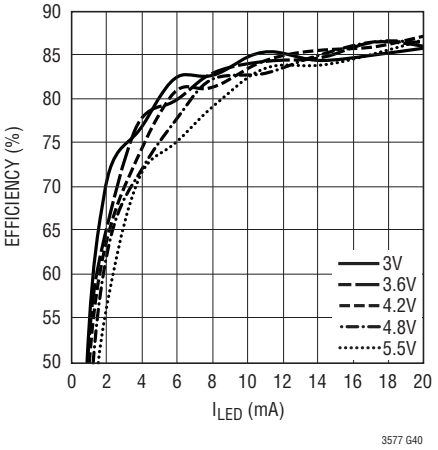


LED Driver Efficiency 8 LEDs

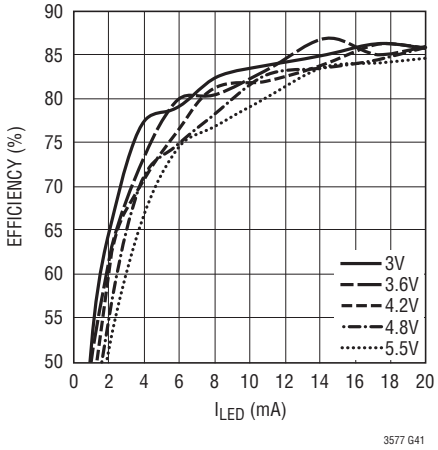


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

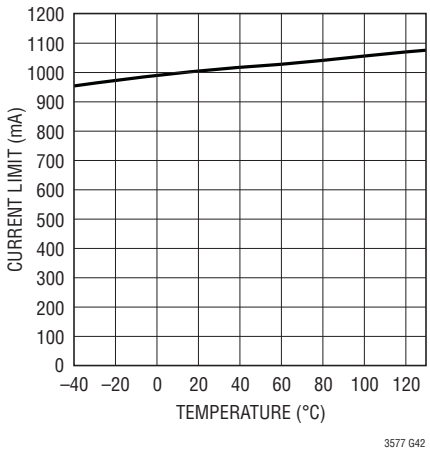
LED Driver Efficiency 6 LEDs



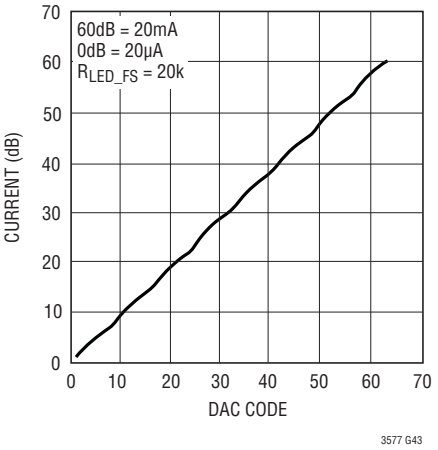
LED Driver Efficiency 4 LEDs



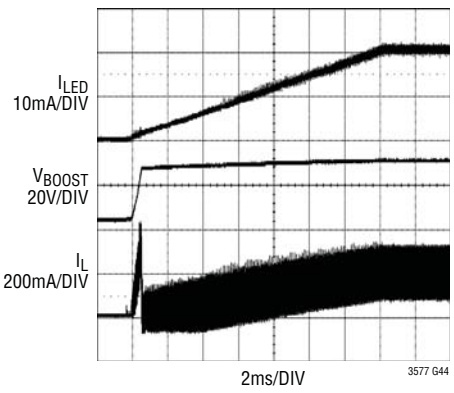
LED Boost Current Limit vs Temperature



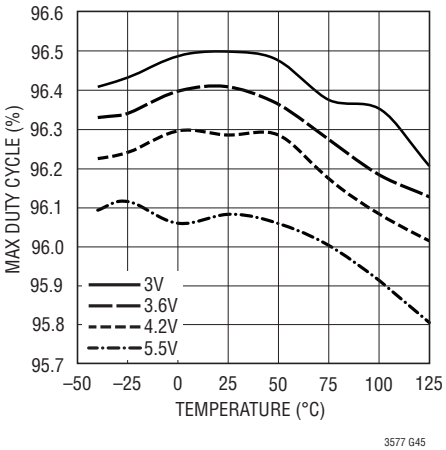
DAC Code vs LED Current



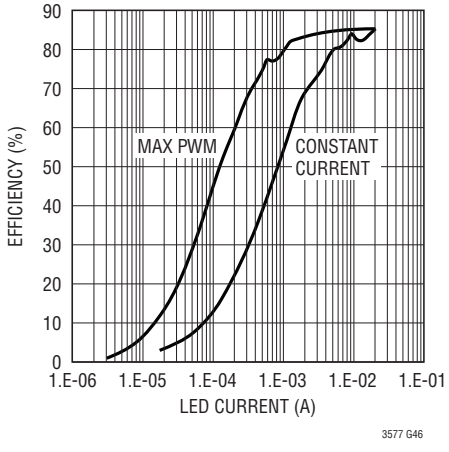
LED Boost Start-Up Transient



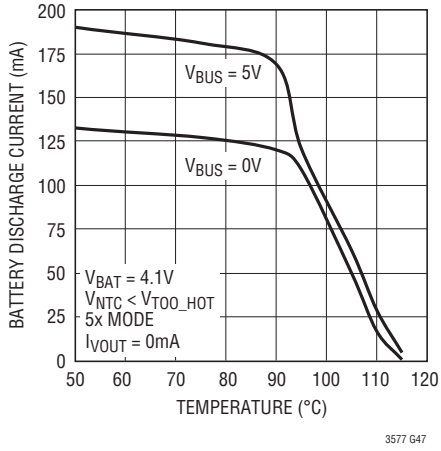
LED Boost Maximum Duty Cycle vs Temperature



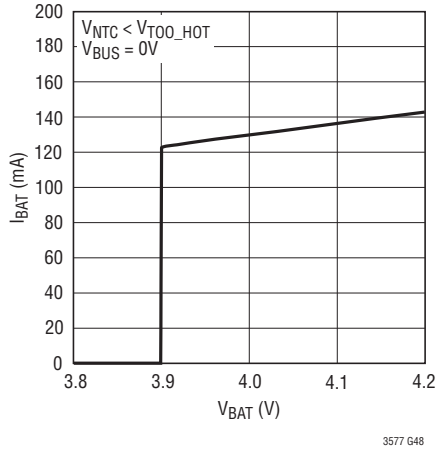
LED PWM vs Constant Current Efficiency



Battery Discharge vs Temperature



Too Hot BAT Discharge



PIN FUNCTIONS

I_{LIM0}, I_{LIM1} (Pins 1, 2): Input Current Control Pins. I_{LIM0} and I_{LIM1} control the input current limit. See Table 1 in the "USB PowerPath Controller" section. Both pins are pulled low by a weak current sink.

LED_FS (Pin 3): A resistor between this pin and ground sets the full-scale output current of the I_{LED} pin.

WALL (Pin 4): Wall Adapter Present Input. Pulling this pin above 4.3V will disconnect the power path from V_{BUS} to V_{OUT}. The $\overline{ACPR}$ pin will also be pulled low to indicate that a wall adapter has been detected.

SW3 (Pin 5): Power Transmission (Switch) Pin for Step-Down Switching Regulator 3 (buck3).

V_{IN3} (Pin 6): Power Input for Step-Down Switching Regulator 3. This pin should be connected to V_{OUT}.

FB3 (Pin 7): Feedback Input for Step-Down Switching Regulator 3 (buck3). This pin servos to a fixed voltage of 0.8V when the control loop is complete.

OVSENSE (Pin 8): Overvoltage Protection Sense Input. OVSENSE should be connected through a 6.2k resistor to the input power connector and the drain of an external N-channel MOS pass transistor. When the voltage on this pin exceeds a preset level, the OVGATE pin will be pulled to GND to disable the pass transistor and protect downstream circuitry.

LED_OV (Pin 9): A resistor between this pin and the boosted LED backlight voltage sets the overvoltage limit on the boost output. If the boost voltage exceeds the programmed limit the LED boost converter will be disabled.

DV_{CC} (Pin 10): Supply Voltage for I^2C Lines. This pin sets the logic reference level of the LTC3577. A UVLO circuit on the DV_{CC} pin forces all registers to all 0s whenever DV_{CC} is <1V. Bypass to GND with a 0.1µF capacitor.

SDA (Pin 11): I^2C Data Input. Serial data is shifted one bit per clock to control the LTC3577. The logic level for SDA is referenced to DV_{CC}.

SCL (Pin 12): I^2C Clock Input. The logic level for SCL is referenced to DV_{CC}.

OVGATE (Pin 13): Overvoltage Protection Gate Output. Connect OVGATE to the gate pin of an external N-channel MOS pass transistor. The source of the transistor should be connected to V_{BUS} and the drain should be connected to the product's DC input connector. In the absence of an overvoltage condition, this pin is connected to an internal charge pump capable of creating sufficient overdrive to fully enhance this transistor. If an overvoltage condition is detected, OVGATE is brought rapidly to GND to prevent damage. OVGATE works in conjunction with OVSENSE to provide this protection.

PWR_ON (Pin 14): Logic Input Used to Keep Buck DC/DCs Enabled After Power-Up. May also be used to enable the buck DC/DCs directly (sequence = buck1 → buck2 → buck3). See the "Pushbutton Interface Operation" section for more information.

$\overline{ON}$ (Pin 15): Pushbutton Input. A weak internal pull-up forces $\overline{ON}$ high when left floating. A normally open pushbutton is connected from $\overline{ON}$ to ground to force a low state on this pin.

PBSTAT (Pin 16): Open-drain output is a de-bounced and buffered version of $\overline{ON}$ to be used for processor interrupts.

WAKE (Pin 17): Open-Drain Output. The WAKE pin indicates the operating state of the buck DC/DCs. If WAKE is Hi-Z, the buck DC/DCs are enabled and either up or powering up. A low on WAKE indicates that the buck DC/DCs are either powered down or are powering down. See the "Pushbutton Interface Operation" section for more information.

SW (Pins 18,19,20): Power Transmission (Switch) Pin for LED Boost Converter. See the "LED Backlight/Boost Operation" section for circuit hook-up and component selection. I^2C is used to control LED driver enable. I^2C default is LED driver off.

PG_DCDC (Pin 21): Open-Drain Output. PG_DCDC goes high impedance 230ms after all buck DC/DCs are in regulation (within 8% of final value).

PIN FUNCTIONS

I_{LED} (Pin 22): Series LED Backlight Current Sink Output. This pin is connected to the cathode end of the series LED backlight string. The current drawn through the series LEDs can be programmed via a 6-bit 60dB DAC and dimmed via an internal 4-bit PWM function. I^2C is used to control LED driver enable, brightness, gradation (soft on/soft off). I^2C default is LED driver off, current = 0mA.

V_{INLDO1} (Pin 23): Input Supply of Low Dropout Linear Regulator 1 (LDO1). This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO2_FB (Pin 24): Feedback Voltage Input for Low Dropout Linear Regulator 2 (LDO2). LDO2 output voltage is set using an external resistor divider between LDO2 and LDO2_FB.

FB2 (Pin 25): Feedback Input for Step-Down Switching Regulator 2 (buck2). This pin servos to a fixed voltage of 0.8V when the control loop is complete.

FB1 (Pin 26): Feedback Input for Step-Down Switching Regulator 1 (buck1). This pin servos to a fixed voltage of 0.8V when the control loop is complete.

LDO1_FB (Pin 27): Feedback Voltage Input for Low Dropout Linear Regulator 1 (LDO1). LDO1 output voltage is set using an external resistor divider between LDO1 and LDO1_FB.

LDO1 (Pin 28): Output of Low Dropout Linear Regulator 1. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO2 (Pin 29): Output of Low Dropout Linear Regulator 2. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

V_{INLDO2} (Pin 30): Input Supply of Low Dropout Linear Regulator 2 (LDO2). This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

SW2 (Pin 31): Power Transmission (Switch) Pin for Step-Down Switching Regulator 2 (buck2).

V_{IN12} (Pin 32): Power Input for Step-Down Switching Regulators 1 and 2. This pin will generally be connected to V_{OUT}.

SW1 (Pin 33): Power Transmission (Switch) Pin for Step-Down Switching Regulator 1 (buck1).

NTCBIAS (Pin 34): Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will bias the NTC thermistor.

NTC (Pin 35): The NTC pin connects to a battery's thermistor to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it drops back into range. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground.

PROG (Pin 36): Charge Current Program and Charge Current Monitor Pin. Connecting a resistor from PROG to ground programs the charge current:

$$I_{CHG} = \frac{1000V}{R_{PROG}} (A)$$

If sufficient input power is available in constant current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current.

IDGATE (Pin 37): Ideal Diode Gate Connection. This pin controls the gate of an optional external P-channel MOSFET transistor used to supplement the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. It is important to maintain high impedance on this pin and minimize all leakage paths.

BAT (Pin 38): Single Cell Li-Ion Battery Pin. Depending on available power and load, a Li-Ion battery on BAT will either deliver system power to V_{OUT} through the ideal diode or be charged from the battery charger.

V_{OUT} (Pin 39): Output Voltage of the PowerPath Controller and Input Voltage of the Battery Charger. The majority of the portable product should be powered from V_{OUT}. The LTC3577 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted input current from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance multilayer ceramic capacitor.

PIN FUNCTIONS

V_{BUS} (Pin 40): USB Input Voltage. V_{BUS} will usually be connected to the USB port of a computer or a DC output wall adapter. V_{BUS} should be bypassed with a low impedance multilayer ceramic capacitor.

$\overline{ACPR}$ (Pin 41): Wall Adapter Present Output (Active Low). A low on this pin indicates that the wall adapter input comparator has had its input pulled above its input threshold (typically 4.3V). This pin can be used to drive the gate of an external P-channel MOSFET to provide power to V_{OUT} from a power source other than a USB port.

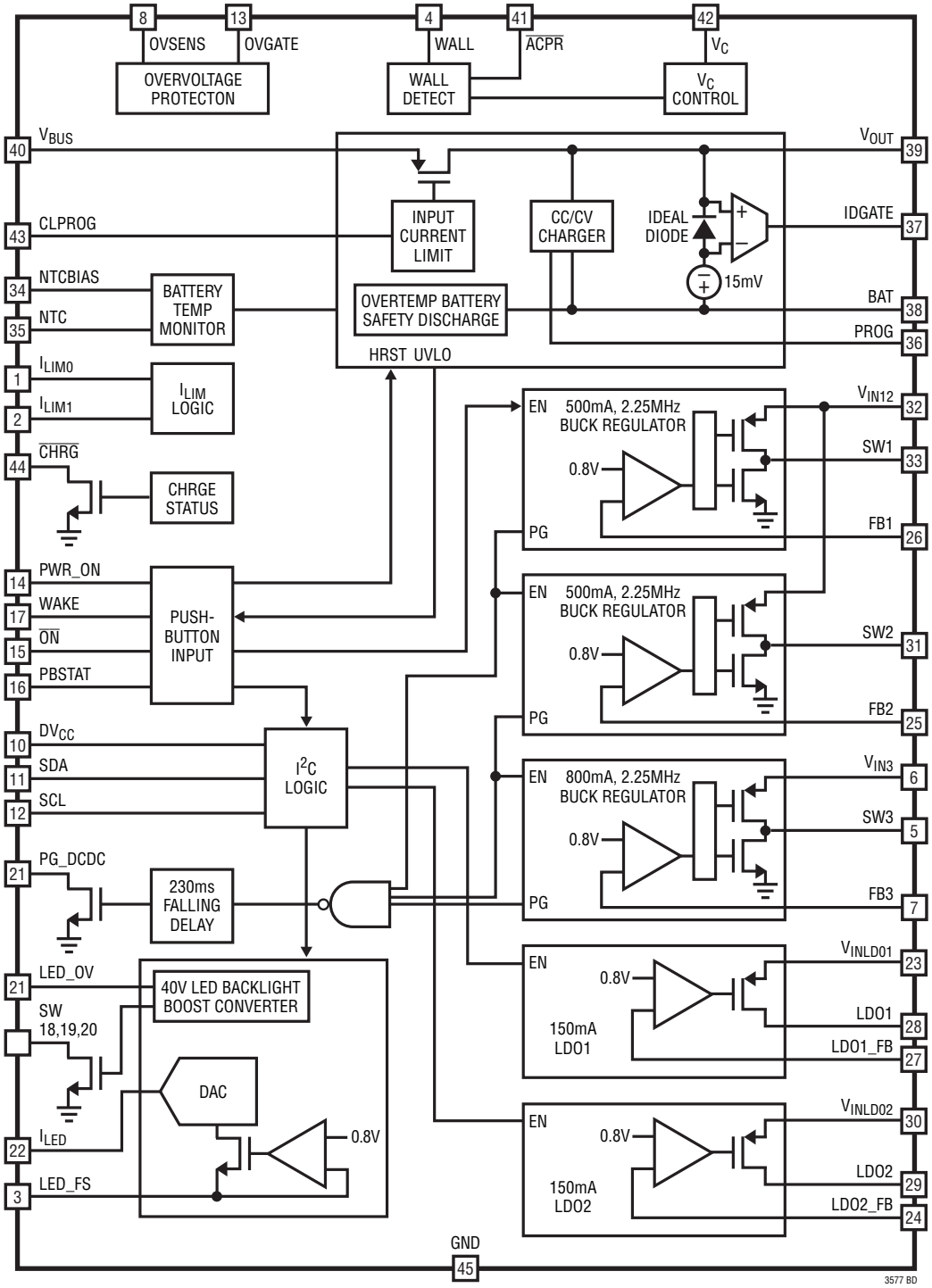
V_C (Pin 42): High Voltage Buck Regulator Control Pin. This pin can be used to drive the V_C pin of an approved external high voltage buck switching regulator. The V_C pin is designed to work with the LT®3480, LT3653 and LT3505. Consult factory for additional approved high voltage buck regulators. See the "External HV Buck Control through the VC Pin" section for operating information.

CLPROG (Pin 43): Input Current Program and Input Current Monitor Pin. A resistor from CLPROG to ground determines the upper limit of the current drawn from the V_{BUS} pin (i.e., the input current limit). A precise fraction of the input current, h_{CLPROG}, is sent to the CLPROG pin. The input PowerPath delivers current until the CLPROG pin reaches 2V (10x mode), 1V (5x mode) or 0.2V (1x mode). Therefore, the current drawn from V_{BUS} will be limited to an amount given by h_{CLPROG} and R_{CLPROG}. In USB applications the resistor R_{CLPROG} should be set to no less than 2.1k.

$\overline{CHRG}$ (Pin 44): Open-Drain Charge Status Output. The $\overline{CHRG}$ pin indicates the status of the battery charger. If $\overline{CHRG}$ is high then the charger is near the float voltage (charge current less than 1/10th programmed charge current) or charging is complete and charger is disabled. A low on $\overline{CHRG}$ indicates that the charger is enabled. For more information see the "Charge Status Indication" section.

Ground (Exposed Pad Pin 45): The exposed package pad is ground and must be soldered to PCB ground for electrical contact and rated thermal performance.

BLOCK DIAGRAM



OPERATION

PowerPath OPERATION

Introduction

The LTC3577 is a highly integrated power management IC that features:

– PowerPath controller
– Battery charger
– Ideal diode
– Input overvoltage protection
– Pushbutton controller
– Three step-down switching regulators
– High voltage buck regulator V_C controller
– Two low dropout linear regulators
– 40V LED backlight controller

Designed specifically for USB applications, the PowerPath controller incorporates a precision input current limit which communicates with the battery charger to ensure that input current does not violate the USB average input current specification. The ideal diode from BAT to V_{OUT} guarantees that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS}. The LTC3577 also has the ability to receive power from a wall adapter or other non-current-limited power source. Such a power supply can be connected to the V_{OUT} pin of the LTC3577 through an external device such as a power Schottky or FET as shown in Figure 1. The LTC3577 has the unique ability to use the output, which is powered by an external supply, to charge the battery while providing power to the load. A comparator on the WALL pin is configured to detect the presence of the wall adapter and shut off the connection to the USB. This prevents reverse conduction from V_{OUT} to V_{BUS} when a wall adapter is present. The LTC3577 provides a V_C output pin which can be used to drive the V_C pin of an external high voltage buck switching regulator such as the LT3480, LT3653 or LT3505 to provide power to the V_{OUT} pin. The V_C control circuitry adjusts the regulation point of the switching regulator to

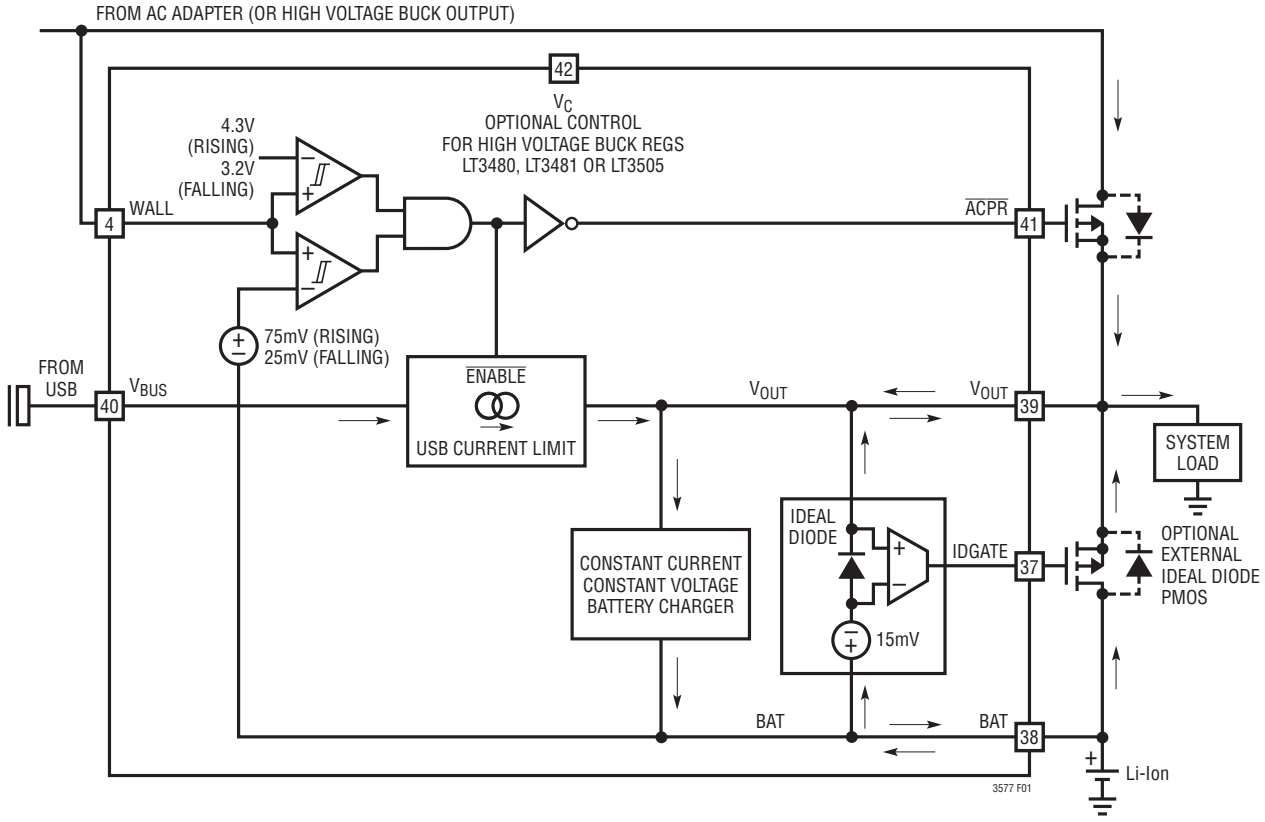


Figure 1. Simplified PowerPath Block Diagram

OPERATION

a small voltage above the BAT pin voltage. This control method provides a high input voltage, high efficiency battery charger and PowerPath function.

The LTC3577 also includes a pushbutton input to control the three synchronous step-down switching regulators and system reset. The three 2.25MHz constant frequency current mode step-down switching regulators provide 500mA, 500mA and 800mA each and support 100% duty cycle operation as well as Burst Mode operation for high efficiency at light load. No external compensation components are required for the switching regulators.

The onboard LED backlight boost circuitry can drive up to 10 series LEDs and includes versatile digital dimming via the I^2C input. The I^2C input also controls two 150mA low dropout (LDO) linear regulators.

All regulators can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory or other logic circuitry.

USB PowerPath Controller

The input current limit and charge control circuits of the LTC3577 are designed to limit input current as well as control battery charge current as a function of I_{VOUT}. V_{OUT} drives the combination of the external load, the three step-down switching regulators, two LDOs, LED backlight and the battery charger.

If the combined load does not exceed the programmed input current limit, V_{OUT} will be connected to V_{BUS} through an internal 200mΩ P-channel MOSFET. If the combined load at V_{OUT} exceeds the programmed input current limit, the battery charger will reduce its charge current by the amount necessary to enable the external load to be satisfied while maintaining the programmed input current. Even if the battery charge current is set to exceed the allowable USB current, the average input current USB specification will not be violated. Furthermore, load current at V_{OUT} will always be prioritized and only excess available current will be used to charge the battery. The current out of the CLPROG pin is a fraction ($1/h_{CLPROG}$) of the V_{BUS} current. When a programming resistor is connected from CLPROG to GND, the voltage on CLPROG represents the input current:

$$I_{VBUS} = I_{BUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet h_{CLPROG}$$

where I_{BUSQ} and h_{CLPROG} are given in the Electrical Characteristics table.

The input current limit is programmed by the I_{LIM0} and I_{LIM1} pins. The LTC3577 can be configured to limit input current to one of several possible settings as well as be deactivated (USB suspend). The input current limit will be set by the appropriate servo voltage and the resistor on CLPROG according to the following expression:

$$I_{VBUS} = I_{BUSQ} + \frac{0.2V}{R_{CLPROG}} \bullet h_{CLPROG} \ (1x\ Mode)$$

$$I_{VBUS} = I_{BUSQ} + \frac{1V}{R_{CLPROG}} \bullet h_{CLPROG} \ (5x\ Mode)$$

$$I_{VBUS} = I_{BUSQ} + \frac{2V}{R_{CLPROG}} \bullet h_{CLPROG} \ (10x\ Mode)$$

Under worst-case conditions, the USB specification for average input current will not be violated with an R_{CLPROG} resistor of 2.1k or greater. Table 1 shows the available settings for the I_{LIM0} and I_{LIM1} pins:

Table 1. Controlled Input Current Limit

I_{LIM1}	I_{LIM0}	$I_{BUS(LIM)}$
0	0	100mA (1x)
0	1	1A (10x)
1	0	Suspend
1	1	500mA (5x)

Notice that when I_{LIM0} is high and I_{LIM1} is low, the input current limit is set to a higher current limit for increased charging and current availability at V_{OUT}. This mode is typically used when there is a higher power, non-USB source available at the V_{BUS} pin.

OPERATION

Ideal Diode from BAT to V_{OUT}

The LTC3577 has an internal ideal diode as well as a controller for an optional external ideal diode. Both the internal and the external ideal diodes respond quickly whenever V_{OUT} drops below BAT. If the load increases beyond the input current limit, additional current will be pulled from the battery via the ideal diodes. Furthermore, if power to V_{BUS} (USB) or V_{OUT} (external wall power or high voltage regulator) is removed, then all of the application power will be provided by the battery via the ideal diodes. The ideal diodes are fast enough to keep V_{OUT} from dropping significantly with just the recommended output capacitor (see Figure 2). The ideal diode consists of a precision amplifier that enables an on-chip P-channel MOSFET whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. The resistance of the internal ideal diode is approximately 200mΩ. If this is sufficient for the application, then no external components are necessary. However, if lower resistance is needed, an external P-channel MOSFET can be added from BAT to V_{OUT}. The IDGATE pin of the LTC3577 drives the gate of the external P-channel MOSFET for automatic ideal diode control. The source of the MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the IDGATE pin can control an external P-channel MOSFET having extremely low on-resistance.

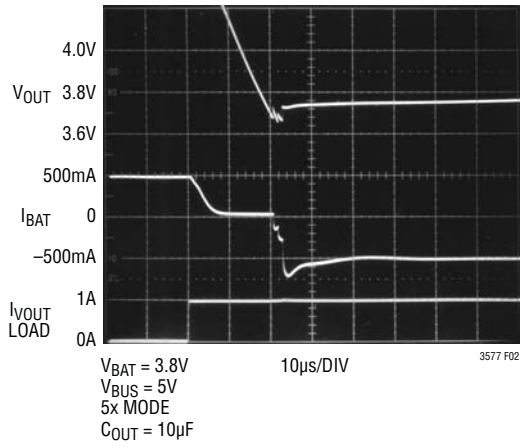


Figure 2. Ideal Diode Transient Response

Using the WALL Pin to Detect the Presence of an External Power Source

The WALL input pin can be used to identify the presence of an external power source (particularly one that is not subject to a fixed current limit like the USB V_{BUS} input). Typically, such a power supply would be a 5V wall adapter output or the low voltage output of a high voltage buck regulator (specifically, LT3480, LT3653 or LT3505). When the wall adapter output (or buck regulator output) is connected directly to the WALL pin, and the voltage exceeds the WALL pin threshold, the USB power path (from V_{BUS} to V_{OUT}) will be disconnected. Furthermore, the $\overline{ACPR}$ pin will be pulled low. In order for the presence of an external power supply to be acknowledged, both of the following conditions must be satisfied:

1. The WALL pin voltage must exceed approximately 4.3V.
2. The WALL pin voltage must be greater than 75mV above the BAT pin voltage.

The input power path (between V_{BUS} and V_{OUT}) is re-enabled and the $\overline{ACPR}$ pin is pulled high when either of the following conditions is met:

1. The WALL pin voltage falls to within 25mV of the BAT pin voltage.
2. The WALL pin voltage falls below 3.2V.

Each of these thresholds is suitably filtered in time to prevent transient glitches on the WALL pin from falsely triggering an event.

External HV Buck Control Through the V_C Pin

The WALL, $\overline{ACPR}$ and V_C pins can be used in conjunction with an external high voltage buck regulator such as the LT3480, LT3505 or LT3653 to provide power directly to the V_{OUT} pin as shown in Figures 3 to 5 (Consult factory for complete list of approved high voltage buck regulators). When the WALL pin voltage exceeds 4.3V, V_C pin control circuitry is enabled and drives the V_C pin of the LT3480, LT3505 or LT3653. The V_C pin control circuitry is designed so that no compensation components are required on the V_C node. The voltage at the V_{OUT} pin is regulated to the larger of (BAT + 300mV) or 3.6V as shown in Figure 6.

OPERATION

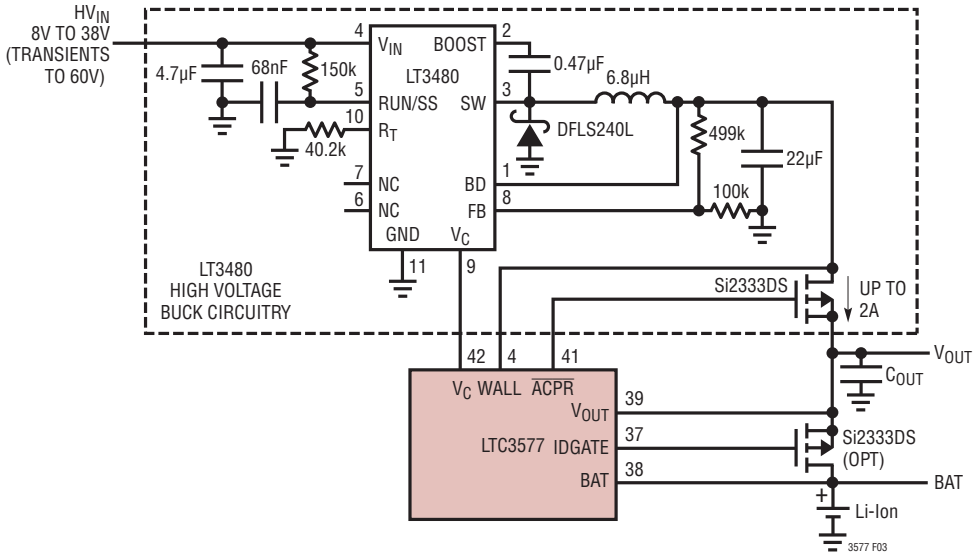


Figure 3. LT3480 Buck Control Using V_C (800kHz Switching)

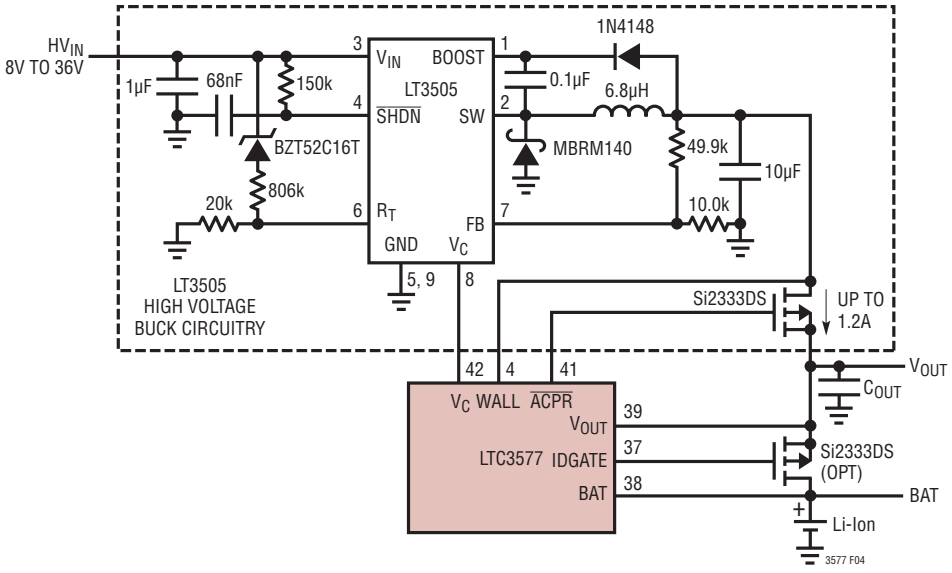


Figure 4. LT3505 Buck Control Using V_C (2.2MHz Switching with Frequency Foldback)

OPERATION

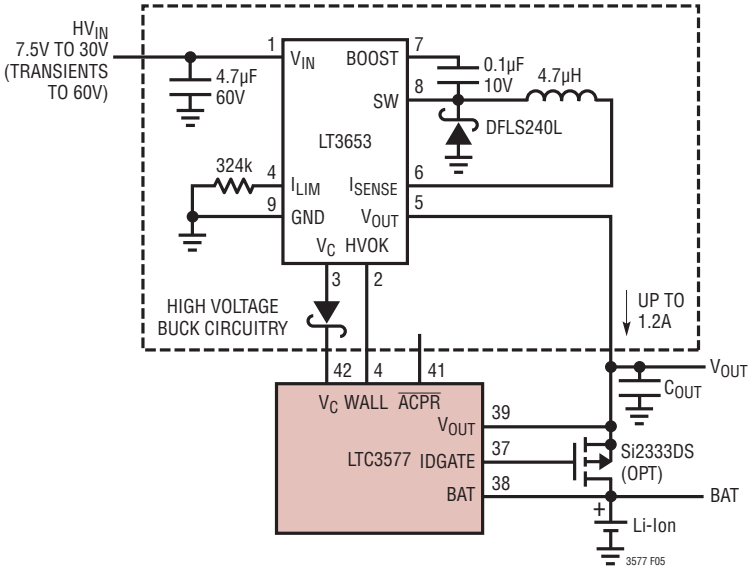


Figure 5. LT3653 Buck Control Using V_C

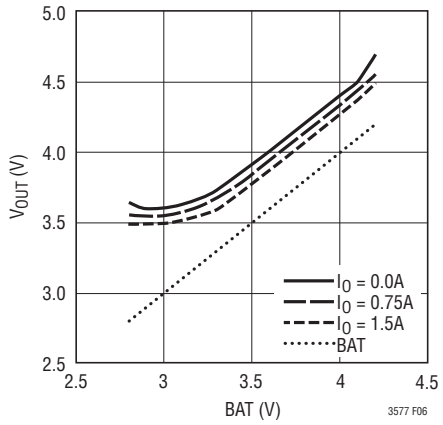


Figure 6. V_{OUT} Voltage vs Battery Voltage (LT3480)

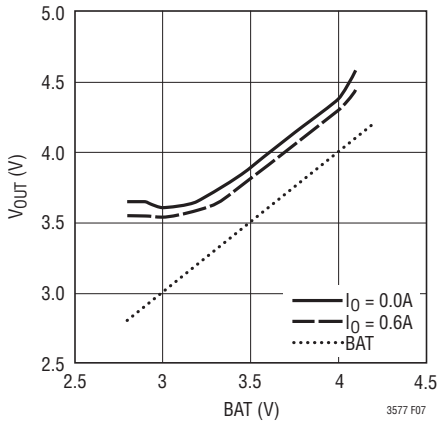


Figure 7. V_{OUT} Voltage vs Battery Voltage (LT3505)

OPERATION

The feedback network of the high voltage buck regulator should be set to generate an output voltage higher than 4.4V (be sure to include the output voltage tolerance of the buck regulator). The V_C control of the LTC3577 overdrives the local V_C control of the external high voltage buck. Therefore, once the V_C control is enabled, the output voltage is set independent of the buck regulator feedback network.

This technique provides a significant efficiency advantage over the use of a 5V buck to drive the battery charger. With a simple 5V buck output driving V_{OUT}, battery charger efficiency is approximately:

$$\eta_{CHARGER} = \eta_{BUCK} \bullet \frac{V_{BAT}}{5V}$$

where η_{BUCK} is the efficiency of the high voltage buck regulator and 5V is the output voltage of the buck regulator. With a typical buck efficiency of 87% and a typical battery voltage of 3.8V, the total battery charger efficiency is approximately 66%. Assuming a 1A charge current, this works out to nearly 2W of power dissipation just to charge the battery!

With the V_C control technique, battery charger efficiency is approximately:

$$\eta_{CHARGER} = \eta_{BUCK} \bullet \frac{V_{BAT}}{0.3V + V_{BAT}}$$

With the same assumptions as above, the total battery charger efficiency is approximately 81%. This example works out to just 900mW of power dissipation. For applications, component selection and board layout information beyond those listed here please refer to the respective high voltage buck regulator data sheet.

Suspend Mode

When I_{LIM0} is pulled low and I_{LIM1} is pulled high the LTC3577 enters suspend mode to comply with the USB specification. In this mode, the power path between V_{BUS} and V_{OUT} is put in a high impedance state to reduce the V_{BUS} input current to 50µA. If no other power source is available to drive WALL and V_{OUT}, the system load connected to V_{OUT} is supplied through the ideal diodes connected to BAT.

V_{BUS} Undervoltage Lockout (UVLO) and Undervoltage Current Limit (UVCL)

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the input current limit circuitry off until V_{BUS} rises above the rising UVLO threshold (3.8V) and at least 50mV above V_{OUT}. Hysteresis on the UVLO turns off the input current limit if V_{BUS} drops below 3.7V or 50mV below V_{OUT}. When this happens, system power at V_{OUT} will be drawn from the battery via the ideal diode. To minimize the possibility of oscillation in and out of UVLO when using resistive input supplies, the input current limit is reduced as V_{BUS} falls below 4.45V (typ).

Battery Charger

The LTC3577 includes a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out of temperature charge pausing. When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.85V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than one-half hour, the battery charger automatically terminates. Once the battery voltage is above 2.85V, the battery charger begins charging in full power constant current mode. The current delivered to the battery will try to reach $1000V/R_{PROG}$. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The USB current limit programming will always be observed and only additional current will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. When the battery voltage approaches the float voltage, the charge current begins to decrease as the LTC3577 enters constant voltage mode. Once the battery charger detects that it has entered constant voltage mode, the four hour safety

OPERATION

timer is started. After the safety timer expires, charging of the battery will terminate and no more current will be delivered.

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 4.0V for LTC3577-1 and 4.1V for LTC3577). In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, the timer will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for more than 1.3ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS}, is removed and then replaced).

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1000th of the battery charge current is delivered to PROG which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1000 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = \frac{1000V}{I_{CHG}},\ I_{CHG} = \frac{1000V}{R_{PROG}}$$

In either the constant-current or constant-voltage charging modes, the PROG pin voltage will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than I_{CHG} due to limited input current available and prioritization with the system load drawn from V_{OUT}.

Thermal Regulation

To prevent thermal damage to the IC or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to approximately 110°C. Thermal regulation protects the LTC3577 from excessive temperature due to high power operation or high ambient thermal conditions and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC3577 or external components. The benefit of the LTC3577 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. An open-drain output, the $\overline{CHRG}$ pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing. When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, i.e., the charger enters constant voltage mode and the charge current has dropped to one-tenth of the programmed value, the $\overline{CHRG}$ pin is released (high impedance). The $\overline{CHRG}$ pin does not respond to the C/10 threshold if the LTC3577 is in input current limit. This prevents false end-of-charge indications due to insufficient power available to the battery charger. Even though charging is stopped during an NTC fault, the $\overline{CHRG}$ pin will stay low indicating that charging is not complete.

Battery Charger Stability Considerations

The LTC3577's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND. Furthermore, a 4.7µF capacitor in series with a 0.2Ω to 1Ω resistor from BAT to GND is required to keep ripple voltage low when the battery is disconnected.

OPERATION

High value, low ESR multilayer ceramic chip capacitors reduce the constant-voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the battery charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

NTC Thermistor and Battery Voltage Reduction

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. To use this feature connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a bias resistor, R_{NOM}, from NTCBIAS to NTC. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25). The LTC3577 will pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 54k (for a Vishay "Curve 1" thermistor, this corresponds to approximately 40°C). If the battery charger is in constant voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC3577 is also designed to pause charging when the value of the NTC thermistor increases to 3.17 times the value of R25. For a Vishay "Curve 1" thermistor this resistance, 317k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. The typical NTC circuit is shown in Figure 8.

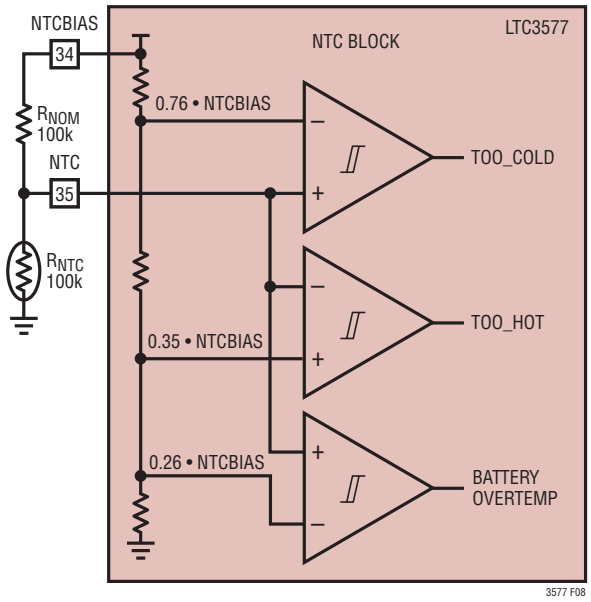


Figure 8. Typical NTC Thermistor Circuit

To improve safety and reliability the battery voltage is reduced when the battery temperature becomes excessively high. When the resistance of the NTC thermistor drops to about 0.35 times the value of R25 or approximately 35k (for a Vishay "Curve 1" thermistor, this corresponds to approximately 50°C) the NTC enables circuitry to monitor the battery voltage. If the battery voltage is above the battery discharge threshold (about 3.9V) then the battery discharge circuitry is enabled and draws about 140mA from the battery when V_{BUS} = 0V and about 180mA when V_{BUS} = 5V. As the battery voltage approaches the discharge threshold the discharge current is linearly reduced until it reaches 0mA at which point the discharge circuitry is disabled. Reducing the discharge current in this fashion keeps the circuit from causing oscillations on V_{BAT} due to battery ESR.

When the charger is disabled an internal watchdog timer samples the NTC thermistor for about 150µs every 150ms and will enable the battery monitoring circuitry if the battery temperature exceeds the NTC TOO_HOT threshold. If adding a capacitor to the NTC pin for filtering the time constant must be much less than 150µs so that the NTC pin can settle to its final value during the sampling period. A time constant of less than 10µs is recommended. Once the battery monitoring circuitry is enabled it will remain enabled and monitoring the battery voltage until the battery

OPERATION

temperature falls back below the discharge temperature threshold. The battery discharge circuitry is only enabled if the battery voltage is greater than the battery discharge threshold.

Alternate NTC Thermistors and Biasing

The LTC3577 provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C, respectively (assuming a Vishay "Curve 1" thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique follows.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used in the following examples, has a nominal value of 100k and follows the Vishay "Curve 1" resistance-temperature characteristic.

In the following explanation, this notation is used.

R25 = Value of the thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of the thermistor at the hot trip point

r_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

r_{HOT}= Ratio of $R_{NTC|HOT}$ to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 9)

R1 = Optional temperature range adjustment resistor (see Figure 9)

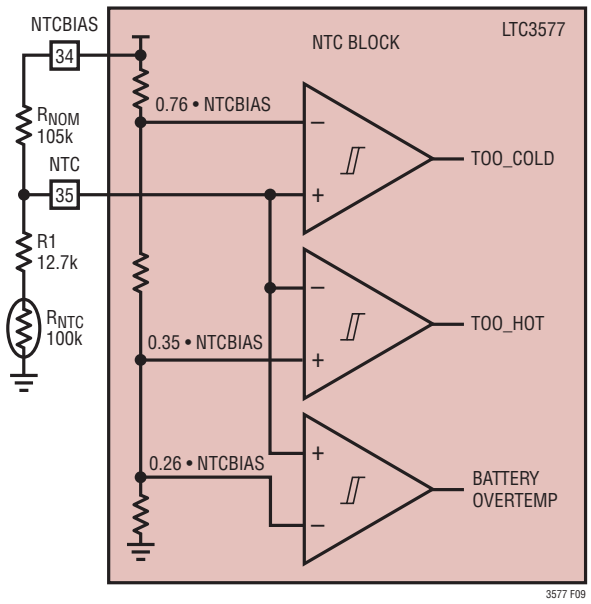


Figure 9. NTC Thermistor Circuit with Additional Bias Resistor

The trip points for the LTC3577's temperature qualification are internally programmed at 0.35 • V_{NTC} for the hot threshold and 0.76 • V_{NTC} for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM}+R_{NTC|HOT}} \bullet NTCBIAS = 0.35 \bullet NTCBIAS$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM}+R_{NTC|COLD}} \bullet NTCBIAS = 0.76 \bullet NTCBIAS$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$R_{NTC|HOT}$ = 0.538 • R_{NOM}

and

$R_{NTC|COLD}$ = 3.17 • R_{NOM}

By setting R_{NOM} equal to R25, the above equations result in r_{HOT} = 0.538 and r_{COLD} = 3.17. Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

OPERATION

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the non-linear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.538} \bullet R25$$

$$R_{NOM} = \frac{r_{COLD}}{3.17} \bullet R25$$

where r_{HOT} and r_{COLD} are the resistance ratios at the desired hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC.

Consider an example where a 60°C hot trip point is desired. From the Vishay Curve 1 R-T characteristics, r_{HOT} is 0.2488 at 60°C. Using the above equation, R_{NOM} should be set to 46.4k. With this value of R_{NOM}, the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in "temperature gain" of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 9. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \bullet R25$$

$$R1 = 0.536 \bullet R_{NOM} - r_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay Curve 1 thermistor choose

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \bullet 100k = 104.2k$$

the nearest 1% value is 105k.

$$R1 = 0.536 \bullet 105k - 0.4368 \bullet 100k = 12.6k$$

the nearest 1% value is 12.7k. The final solution is shown in Figure 9 and results in an upper trip point of 45°C and a lower trip point of 0°C.

Overvoltage Protection (OVP)

The LTC3577 can protect itself from the inadvertent application of excessive voltage to V_{BUS} or WALL with just two external components: an N-channel FET and a 6.2k resistor. The maximum safe overvoltage magnitude will be determined by the choice of the external NMOS and its associated drain breakdown voltage.

The overvoltage protection module consists of two pins. The first, OVSENS, is used to measure the externally applied voltage through an external resistor. The second, OVGATE, is an output used to drive the gate pin of an external FET. The voltage at OVSENS will be lower than the OVP input voltage by (I_{OVSENS} • 6.2k) due to the OVP circuit's quiescent current. The OVP input will be 200mV to 400mV higher than OVSENS under normal operating conditions. When OVSENS is below 6V, an internal charge pump will drive OVGATE to approximately 1.88 • OVSENS. This will enhance the N-channel FET and provide a low impedance connection to V_{BUS} or WALL which will, in turn, power the LTC3577. If OVSENS should rise above 6V (6.35V OVP input) due to a fault or use of an incorrect wall adapter, OVGATE will be pulled to GND, disabling the external FET to protect downstream circuitry. When the voltage drops below 6V again, the external FET will be re-enabled.

In an overvoltage condition, the OVSENS pin will be clamped at 6V. The external 6.2k resistor must be sized appropriately to dissipate the resultant power. For example, a 1/10W 6.2k resistor can have at most $\sqrt{PMAX \bullet 6.2k\Omega} = 24V$ applied across its terminals. With the 6V at OVSENS, the maximum overvoltage magnitude that this resistor can withstand is 30V. A 1/4W 6.2k resistor raises this value to 45V.

The charge pump output on OVGATE has limited output drive capability. Care must be taken to avoid leakage on this pin, as it may adversely affect operation.

Dual Input Overvoltage Protection

It is possible to protect both V_{BUS} and WALL from overvoltage damage with several additional components, as shown in Figure 10. Schottky diodes D1 and D2 pass the larger of V1 and V2 to R1 and OVSENS. If either V1 or V2 exceeds 6V plus $V_{F(SCHOTTKY)}$, OVGATE will be pulled to GND and both the WALL and USB inputs will be protected.

OPERATION

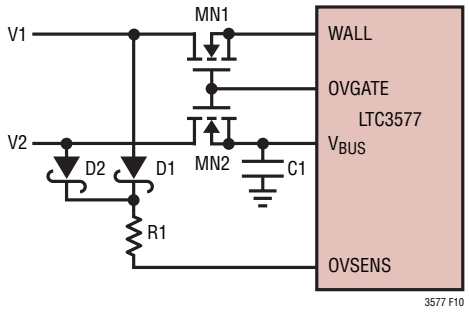
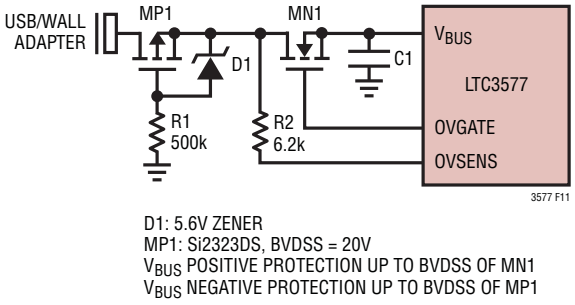


Figure 10. Dual Input Overvoltage Protection



D1: 5.6V ZENER
MP1: Si2323DS, BVDSS = 20V
V_{BUS} POSITIVE PROTECTION UP TO BVDSS OF MN1
V_{BUS} NEGATIVE PROTECTION UP TO BVDSS OF MP1

Figure 11. Dual Polarity Voltage Protection

Each input is protected up to the drain-source breakdown, BVDSS, of MN1 and MN2. R1 must also be rated for the power dissipated during maximum overvoltage. See the "Overvoltage Protection" section for an explanation of this calculation. Table 2 shows some NMOS FETs that are suitable for overvoltage protection.

Table 2. Recommended Overvoltage FETs

NMOS FET	BVDSS	R_{ON}	PACKAGE
Si1472DH	30V	82mΩ	SC70-6
Si2302ADS	20V	60mΩ	SOT-23
Si2306BDS	30V	65mΩ	SOT-23
Si2316BDS	30V	80mΩ	SOT-23
IRLML2502	20V	35mΩ	SOT-23

Reverse Input Voltage Protection

The LTC3577 can also be easily protected against the application of reverse voltage as shown in Figure 10. D1 and R1 are necessary to limit the maximum VGS seen by MP1 during positive overvoltage events. D1's breakdown voltage must be safely below MP1's BVGS. The circuit shown in Figure 11 offers forward voltage protection up to MN1's BVDSS and reverse voltage protection up to MP1's BVDSS.

LOW DROPOUT LINEAR REGULATOR OPERATION

LDO Operation and Voltage Programming

The LTC3577 contains two 150mA adjustable output LDO regulators. To enable the LDOs write a 1 to the LDO1EN and/or LDO2EN I^2C registers. The LDOs can be disabled three ways: 1) Write a 0 to the LDO1EN and LDO2EN registers; 2) Bring DV_{CC} below the DV_{CC} undervoltage threshold; 3) Enter the power-down pushbutton state.

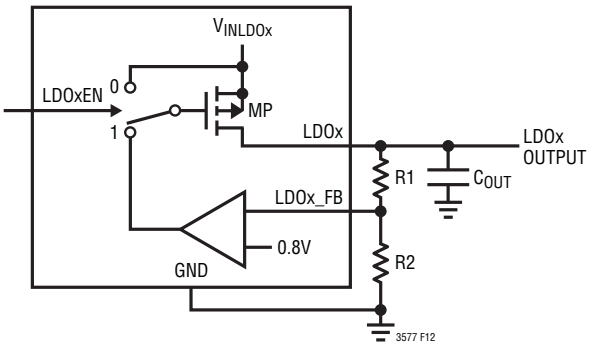


Figure 12. LDO Application Circuit

The LDOs are further disabled if V_{OUT} falls below the V_{OUT} UVLO threshold and cannot be enabled until the UVLO condition is removed.

When disabled all LDO circuitry is powered off leaving only a few nanoamps of leakage current on the LDO supply. The LDO outputs are individually pulled to ground through internal resistors when disabled.

The power good status bits of LDO1 and LDO2 are available in I^2C through the read-back registers PGLDO[1] and PGLDO[2] for LDO1 and LDO2 respectively. The power good comparators for both LDOs are sampled when the I^2C port receives the correct I^2C read address.

Figure 12 shows the LDO application circuit. The full-scale output voltage for each LDO is programmed using a resistor divider from the LDO output (LDO1 or LDO2) connected to the feedback pins (LDO1_FB or LDO2_FB) such that:

$$V_{LDOx} = 0.8V \bullet \left(\frac{R1}{R2} + 1\right)$$

OPERATION

For stability, each LDO output must be bypassed to ground with a minimum 1µF ceramic capacitor (C_{OUT}).

LDO Operating as a Current Limited Switch

The LDO can be used as a current limited switch by simply connecting the LDOx_FB input to ground. In this case the LDOx output will be pulled up to V_{INLDOx} through the LDO's internal current limit (about 300mA). Enabling the LDO via the I^2C interface effectively connects LDOx and V_{INLDOx}, while disabling the LDO disconnected LDOx from V_{INLDOx}.

STEP-DOWN SWITCHING REGULATOR OPERATION

Introduction

The LTC3577 includes three 2.25MHz constant frequency current mode step-down switching regulators providing 500mA, 500mA and 800mA each. All step-down switching regulators can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory or other logic circuitry. All step-down switching regulators support 100% duty cycle operation (low dropout mode) when the input voltage drops very close to the output voltage and are also capable of Burst Mode operation for highest efficiencies at light loads. Burst Mode operation is individually selectable for each step-down switching regulator through the I^2C register bits BK1BRST, BK2BRST and BK3BRST. The step-down switching regulators also include soft-start to limit inrush current when powering on, short-circuit current protection, and switch node slew limiting circuitry to reduce EMI radiation. No external compensation components are required for the switching regulators. The regulators are sequenced up and down together through the pushbutton interface (see the "Pushbutton Interface" section for more information). It is recommended that the step-down switching regulator input supplies (V_{IN12} and V_{IN3}) be connected to the system supply pin (V_{OUT}). This is recommended because the undervoltage lockout circuit on the V_{OUT} pin (V_{OUT} UVLO) disables the step-down switching regulators when the V_{OUT} voltage drops below the V_{OUT} UVLO threshold. If driving the step-down switching regulator input supplies from a voltage other than V_{OUT} the regulators should not be operated outside the specified operating range as operation is not guaranteed beyond this range.

Output Voltage Programming

Figure 13 shows the step-down switching regulator application circuit. The full-scale output voltage for each step-down switching regulator is programmed using a resistor divider from the step-down switching regulator output connected to the feedback pins (FB1, FB2 and FB3) such that:

$$V_{OUTx} = 0.8V \bullet \left(\frac{R1}{R2} + 1\right)$$

Typical values for R1 are in the range of 40k to 1M. The capacitor C_{FB} cancels the pole created by feedback resistors and the input capacitance of the FB pin and also helps to improve transient response for output voltages much greater than 0.8V. A variety of capacitor sizes can be used for C_{FB} but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response.

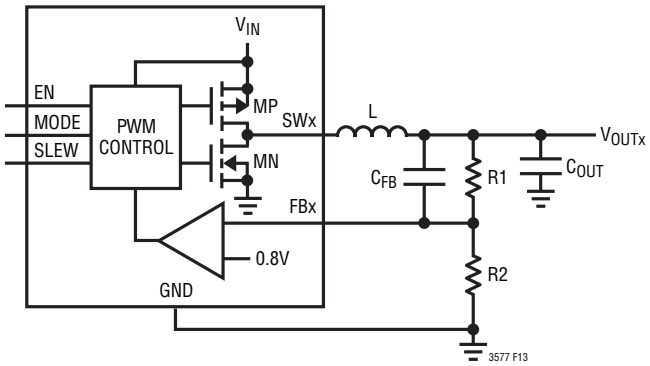


Figure 13. Step-Down Switching Regulator Application Circuit

PG_DCDC Operation

The PG_DCDC pin is an open-drain output used to indicate that all step-down switching regulators are enabled and have reached their final regulation voltage. A 230ms delay is included from the time all switching regulators reach 92% of their regulation value to allow a system controller ample time to reset itself. PG_DCDC may be used as a power-on reset to a microprocessor powered by the step-down switching regulators. PG_DCDC is an

OPERATION

open-drain output and requires a pull-up resistor to an appropriate power source. Optimally the pull-up resistor is connected to one of the step-down switching regulator output voltages so that power is not dissipated while the regulators are disabled.

Operating Modes

The step-down switching regulators include two possible operating modes to meet the noise/power needs of a variety of applications. In pulse-skipping mode, an internal latch is set at the start of every cycle, which turns on the main P-channel MOSFET switch. During each cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the internal latch, which causes the main P-channel MOSFET switch to turn off and the N-channel MOSFET synchronous rectifier to turn on. The N-channel MOSFET synchronous rectifier turns off at the end of the 2.25MHz cycle or if the current through the N-channel MOSFET synchronous rectifier drops to zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary compensation is internal to the step-down switching regulator requiring only a single ceramic output capacitor for stability. At light loads in pulse-skipping mode, the inductor current may reach zero on each pulse which will turn off the N-channel MOSFET synchronous rectifier. In this case, the switch node (SW1, SW2 or SW3) goes high impedance and the switch node voltage will ring. This is discontinuous operation, and is normal behavior for a switching regulator. At very light loads in pulse-skipping mode, the step-down switching regulators will automatically skip pulses as needed to maintain output regulation. At high duty cycle (V_{OUTX} approaching V_{INX}) it is possible for the inductor current to reverse at light loads causing the stepped down switching regulator to operate continuously. When operating continuously, regulation and low noise output voltage are maintained, but input operating current will increase to a few milliamps.

In Burst Mode operation, the step-down switching regulators automatically switch between fixed frequency PWM operation and hysteretic control as a function of the load current. At light loads the step-down switching regulators control the inductor current directly and use a hysteretic control loop to minimize both noise and switching losses. While operating in Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The step-down switching regulator then goes into sleep mode, during which the output capacitor provides the load current. In sleep mode, most of the switching regulator's circuitry is powered down, helping conserve battery power. When the output voltage drops below a pre-determined value, the step-down switching regulator circuitry is powered on and another burst cycle begins. The sleep time decreases as the load current increases. Beyond a certain load current point (about 1/4 rated output load current) the step-down switching regulators will switch to a low noise constant frequency PWM mode of operation, much the same as pulse-skipping operation at high loads.

For applications that can tolerate some output ripple at low output currents, Burst Mode operation provides better efficiency than pulse-skipping at light loads. The step-down switching regulators allow mode transition on-the-fly, providing seamless transition between modes even under load. This allows the user to switch back and forth between modes to reduce output ripple or increase low current efficiency as needed. Burst Mode operation is individually selectable for each step-down switching regulator through the I^2C register bits BK1BRST, BK2BRST and BK3BRST.

Shutdown

The step-down switching regulators are shut down when the pushbutton circuitry is in the power-down, power off or hard reset states. In shutdown all circuitry in the step-down switching regulator is disconnected from the switching regulator input supply leaving only a few nanoamps of leakage current. The step-down switching regulator outputs are individually pulled to ground through internal 10k resistors on the switch pin (SW1, SW2 or SW3) when in shutdown.

Dropout Operation

It is possible for a step-down switching regulator's input voltage to approach its programmed output voltage (e.g., a battery voltage of 3.4V with a programmed output voltage of 3.3V). When this happens, the PMOS switch duty cycle

OPERATION

increases until it is turned on continuously at 100%. In this dropout condition, the respective output voltage equals the regulator's input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

Soft-Start Operation

Soft-start is accomplished by gradually increasing the peak inductor current for each step-down switching regulator over a 500µs period. This allows each output to rise slowly, helping minimize inrush current required to charge up the switching regulator output capacitor. A soft-start cycle occurs whenever a given switching regulator is enabled. A soft-start cycle is not triggered by changing operating modes. This allows seamless output transition when actively changing between operating modes.

Slew Rate Control

The step-down switching regulators contain new patent pending circuitry to limit the slew rate of the switch node (SW1, SW2 and SW3). This new circuitry is designed to transition the switch node over a period of a few nanoseconds, significantly reducing radiated EMI and conducted supply noise while maintaining high efficiency. Since slowing the slew rate of the switch nodes causes efficiency loss, the slew rate of the step-down switching regulators is adjustable via the I^2C registers SLEWCTL1 and SLEWCTL2. This allows the user to optimize efficiency or EMI as necessary with four different slew rate settings. The power-up default is the fastest slew rate (highest efficiency) setting.

Figures 14 and 15 show the efficiency and power loss graph for Buck3 programmed for 1.2V and 2.5V outputs. Note that the power loss curves remain fairly constant for both graphs yet changing the slew rate has a larger effect on the 1.2V output efficiency. This is mainly because for a given output current the 2.5V output is delivering more than 2x the power than the 1.2V output. Efficiency will always decrease and show more variation to slew rate as the programmed output voltage is decreased.

Low Supply Operation

An undervoltage lockout circuit on V_{OUT} (V_{OUT} UVLO) shuts down the step-down switching regulators when V_{OUT} drops below about 2.7V. It is recommended that the step-down switching regulator input supplies (V_{IN12}, V_{IN3}) be connected to the power path output (V_{OUT}) directly. This UVLO prevents the step-down switching regulators from operating at low supply voltages where loss of regulation or other undesirable operation may occur. If driving the step-down switching regulator input supplies from a voltage other than the V_{OUT} pin, the regulators should not be operated outside the specified operating range as operation is not guaranteed beyond this range.

Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection

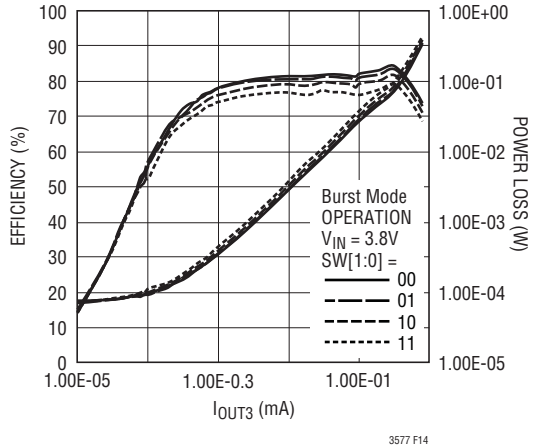


Figure 14. V_{OUT3} (1.2V) Efficiency and Power Loss vs I_{OUT3}

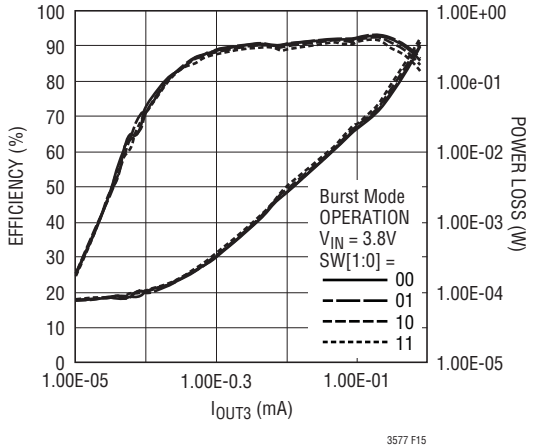


Figure 15. V_{OUT3} (2.5V) Efficiency and Power Loss vs I_{OUT3}

OPERATION

Table 3. Recommended Inductors for Step-Down Switching Regulators

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE in mm (L × W × H)	MANUFACTURER
DB318C	4.7	1.07	0.1	3.8 × 3.8 × 1.8	Toko
	3.3	1.20	0.07	3.8 × 3.8 × 1.8	www.toko.com
D312C	4.7	0.79	0.24	3.6 × 3.6 × 1.2	
	3.3	0.90	0.20	3.6 × 3.6 × 1.2	
DE2812C	4.7	1.15	0.13*	3.0 × 2.8 × 1.2	
	3.3	1.37	0.105*	3.0 × 2.8 × 1.2	
CDRH3D16	4.7	0.9	0.11	4 × 4 × 1.8	Sumida
	3.3	1.1	0.085	4 × 4 × 1.8	www.sumida.com
CDRH2D11	4.7	0.5	0.17	3.2 × 3.2 × 1.2	
	3.3	0.6	0.123	3.2 × 3.2 × 1.2	
CLS4D09	4.7	0.75	0.19	4.9 × 4.9 × 1	
SD3118	4.7	1.3	0.162	3.1 × 3.1 × 1.8	Cooper
	3.3	1.59	0.113	3.1 × 3.1 × 1.8	www.cooperet.com
SD3112	4.7	0.8	0.246	3.1 × 3.1 × 1.2	
	3.3	0.97	0.165	3.1 × 3.1 × 1.2	
SD12	4.7	1.29	0.117*	5.2 × 5.2 × 1.2	
	3.3	1.42	0.104*	5.2 × 5.2 × 1.2	
SD10	4.7	1.08	0.153*	5.2 × 5.2 × 1.0	
	3.3	1.31	0.108*	5.2 × 5.2 × 1.0	
LPS3015	4.7	1.1	0.2	3.0 × 3.0 × 1.5	Coil Craft
	3.3	1.3	0.13	3.0 × 3.0 × 1.5	www.coilcraft.com

*Typical DCR

process much simpler. The step-down switching regulators are designed to work with inductors in the range of 2.2µH to 10µH. For most applications a 4.7µH inductor is suggested for step-down switching regulators providing up to 500mA of output current while a 3.3µH inductor is suggested for step-down switching regulators providing up to 800mA. Larger value inductors reduce ripple current, which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time, but will reduce the available output current. To maximize efficiency, choose an inductor with a low DC resistance. For a 1.2V output, efficiency is reduced about 2% for 100mΩ series resistance at 400mA load current, and about 2% for 300mΩ series resistance at 100mA load current. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short-circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the step-down converters. Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price versus size, performance, and any radiated EMI requirements than on what the step-down switching regulators requires to operate. The inductor value also has an effect on Burst Mode operation. Lower inductor values will cause Burst Mode switching frequency to increase. Table 3 shows several inductors that work well with the step-down switching regulators. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used at both step-down switching regulator outputs as well as at each step-down switching regulator input supply. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 10µF output capacitor is sufficient for the step-down switching regulator outputs. For good transient response

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and stability the output capacitor for step-down switching regulators should retain at least 4µF of capacitance over operating temperature and bias voltage. Each switching regulator input supply should be bypassed with a 2.2µF capacitor. Consult with capacitor manufacturers for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 4 shows a list of several ceramic capacitor manufacturers.

Table 4. Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

LED BACKLIGHT/BOOST OPERATION

Introduction

The LED driver uses a constant frequency, current mode boost converter to supply power to up to 10 series LEDs. As shown in Figure 16 the series string of LEDs is connected from the output of the boost converter (BOOST) to the I_{LED} pin. Under normal operation the boost converter BOOST output will be driven to a voltage where the I_{LED} pin regulates at 300mV. The I_{LED} pin is a constant-current sink that is programmed via I^2C "LED DAC register". The LED can be further controlled using I^2C to program brightness levels and soft turn-on/turn-off effects. See the "I^2C Interface" section for more information on programming the I_{LED} current. The boost converter also includes an overvoltage protection feature to limit the BOOST output voltage as well as variable slew rate control of the SW pin to reduce EMI.

LED Boost Operation

The LED boost converter is designed for very high duty cycle operation and can boost from 3V to 40V for load currents up to 20mA. The boost converter also features an overvoltage protection feature to protect the output in case of an open circuit in the LED string. The overvoltage protection threshold is set by adjusting R1 in Figure 16 such that:

$$BOOST(MAX) = 800mV \bullet \frac{R1}{10 \bullet R2} + LED\_OV$$

where LED_OV is about 1.0V.

In the case of Figure 16 BOOST(MAX) is set to 40V for a 10-LED string.

Capacitor C3 provides soft-start, limiting the inrush current when the boost converter is first enabled. C3 provides feedback to the I_{LED} pin. This feedback limits the rise time of output voltage and the inrush current while the output capacitor, C2, is charging.

The boost converter will be operated in either continuous conduction mode, discontinuous conduction mode or pulse-skipping mode depending on the inductor current required for regulation.

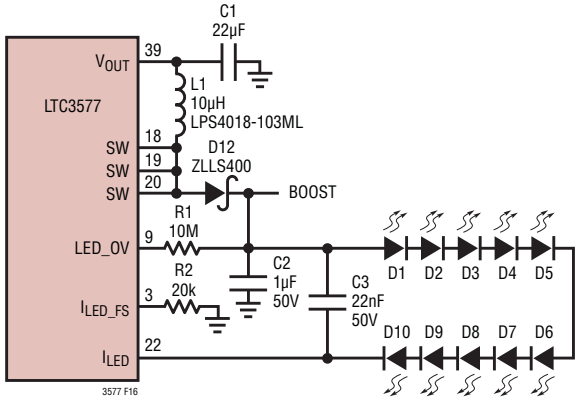

Figure 16. LED Boost Application Circuit

LED Constant Current Sink

The LED driver uses a precision current sink to regulate the LED current up to 20mA. The current sink is programmed via I^2C "LED DAC Register" and utilizes a 6-bit 60dB exponential DAC. This DAC provides accurate current control from 20µA to 20mA with approximately 1dB per step for $I_{LED(FS)}$ = 20mA. The LED current can be approximated by the following equations:

$$I_{LED} = I_{LED(FS)} \bullet 10^{\left(3 \bullet \frac{DAC - 63}{63}\right)}$$

$$I_{LED(FS)} = \frac{0.8V}{R2} \bullet 500 \quad (1)$$

OPERATION

where DAC is the decimal value programmed into the I²C "LED DAC register". For example with $I_{LED(FS)}$ = 20mA and DAC[5:0] = 000000 (0 decimal) I_{LED} equates to 20µA, while DAC[5:0] = 111111 (63 decimal) I_{LED} equates to 20mA. As a final example DAC[5:0] = 101010 is 42 decimal and equates to I_{LED} = 2mA for $I_{LED(FS)}$ = 20mA. The DAC approximates the Equation 1 using the nominal values in Table 5. The differences between the approximation equation and the table are due to design of the DAC using eight linear segments that approximate the exponential function.

Table 5. LED DAC Codes to Output Current

DAC Codes	Output Current	DAC Codes	Output Current
0	20.0µA	32	668µA
1	23.5µA	33	786µA
2	27.0µA	34	903µA
3	30.5µA	35	1.02mA
4	34.0µA	36	1.14mA
5	37.6µA	37	1.26mA
6	41.1µA	38	1.37mA
7	44.6µA	39	1.49mA
8	48.1µA	40	1.61mA
9	56.5µA	41	1.89mA
10	65.0µA	42	2.17mA
11	73.4µA	43	2.45mA
12	81.9µA	44	2.74mA
13	90.3µA	45	3.02mA
14	98.7µA	46	3.30mA
15	107µA	47	3.58mA
16	116µA	48	3.86mA
17	136µA	49	4.54mA
18	156µA	50	5.22mA
19	177µA	51	5.90mA
20	197µA	52	6.58mA
21	217µA	53	7.26mA
22	237µA	54	7.93mA
23	258µA	55	8.61mA
24	278µA	56	9.29mA
25	327µA	57	10.8mA
26	376µA	58	12.4mA
27	424µA	59	13.9mA
28	473µA	60	15.4mA
29	522µA	61	17.0mA
30	571µA	62	18.5mA
31	620µA	63	20.0mA

The full-scale LED current is set using a resistor (R2 in Figure 16) connected between the LED_FS pin and ground. Typically R2 should be set to 20k to give 20mA of LED current at full-scale. The resistance may be increased to decrease the current or the resistance may be decreased to increase the LED current. The DAC has been optimized for best performance at 20mA full-scale. The full-scale current may be adjusted but the accuracy of the output current will be degraded the further it is programmed from 20mA. The LED_FS pin is current limited and will only source about 80µA. This protects the pin and limits the I_{LED} current in a case where LED_FS is shorted to ground, it is not recommended to program the LED current above 25mA.

LED Gradation

The LED driver features an automatic gradation circuit. The gradation circuit ramps the LED current up when the LED driver is enabled and ramps the current down when the LED driver is disabled. The DAC is enabled and disabled with the EN bit of the I²C "LED control register." The gradation function is automatic when enabling and disabling the LED driver; only the gradation speed needs to be programmed to use this function. The gradation speed is set by the GR1 and GR2 bits of the I²C "LED control register" which allows transitions times of approximately 15ms, one-half second, one second and two seconds. See the "I²C Interface" section for more information. The gradation function allows the LEDs to turn on and off gradually as opposed to an abrupt step.

LED PWM vs Constant Current Operation

The LED driver provides both linear LED current mode as well as PWM LED current mode. These modes are selected through the MD1 and MD2 bits of the I²C "LED control register." When both bits are 0 the LED boost converter is in constant current (CC) mode and the I_{LED} current sink is constant whose value is set by the DAC[5:0] bits of the I²C "LED DAC register."

Setting MD1 to 0 and MD2 to 1 selects the LED PWM mode. In this mode the LED driver is pulsed using an internally generated PWM signal. The PWM mode may be used to reduce the LED intensity for a given programmed current.

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When dimming via PWM the LED driver and boost converter are both turned on and off together. This allows some degree of additional control over the LED current, and in some cases may offer a more efficient method of dimming since the boost could be operated at an optimal efficiency point and then pulsed for the desired LED intensity.

The PWM mode, if enabled, is set up using 3 values; PWMNUM[3:0] and PWMDEN[3:0] in the I^2C "LED PWM Register" and PWMCLK, set by PWMC2 and PWMC1 in the I^2C "LED Control Register."

$$\text{Duty Cycle} = \frac{\text{PWMNUM}}{\text{PWMDEN}}$$

$$\text{Frequency} = \frac{\text{PWMCLK}}{\text{PWMDEN}}$$

Table 6. PWM Clock Frequency

PWMC2	PWMC1	PWMCLK
0	0	8.77kHz
0	1	4.39kHz
1	0	2.92kHz
1	1	2.19kHz

Using the PWM control, a 4-bit internally generated PWM is possible as additional dimming. Using these control bits a number of PWM duty cycles and frequencies are available in the 100Hz to 500Hz range. This range was selected to be below the audio range and above the frequency where the PWM is visible.

For example, given PWMC2 = 1, PWMC1 = 0, PWMNUM[3:0] = 0111 and PWMDEN[3:0] = 1100 then the duty cycle will be 58.3% and PWM frequency will be 243Hz.

If PWMNUM is set to 0 then the duty cycle will be 0% and the current sink will effectively be off. If PWMNUM is programmed to a value larger than PWMDEN the duty cycle will be 100% and the current sink will effectively be constant. PWMDEN and PWMNUM may both be changed to result in 73 different duty cycle possibilities and 41 different PWM frequencies between 8.77kHz and 100Hz.

When PWM mode is enabled, a small (2µA) standby current source is always enabled on the I_{LED} pin. The purpose of this is to have some current flowing in the LEDs at all times. This helps to reduce the magnitude of the voltage swing on the I_{LED} pin as the current is pulsed on and off.

Fixed Boost Output

Setting MD1 to 1 and MD2 to 0 selects the fixed high voltage boost mode. This mode can be used to generate output voltages at or greater than V_{OUT}. When configured as a boost converter the I_{LED} pin becomes the feedback pin, and will regulate the output voltage such that the voltage on the I_{LED} pin is 800mV.

Figure 17 shows a fixed 12V output generated using the boost converter in the fixed high voltage boost mode. Any output voltage up to 40V may be programmed by selecting appropriate values for the R1 and R2 voltage divider from the equation:

$$V_{BOOST} = 0.8V \bullet \left(\frac{R1}{R2} + 1\right)$$

Values for R2 should be kept below 24.3k to keep the pole at I_{LED} beyond cross over.

The boost is designed primarily as a high voltage, high duty cycle converter. When operating with a lower boost ratio, a larger output capacitor, 10µF, should be used. Operating with a very low duty cycle will cause cycle skipping which will increase ripple.

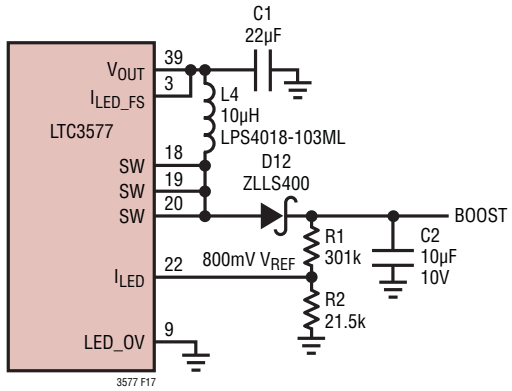

Figure 17. Fixed 12V/75mA Boost Output Application

OPERATION

To keep the average steady-state inductor current below 300mA the maximum output current is reduced as programmed output voltage increases. The output current available is given by:

$$I_{BOOST(MAX)} = 300mA \bullet \frac{V_{OUT(MIN)}}{V_{BOOST}}$$

Note that the maximum boost output current must be set by the minimum V_{OUT} operating voltage. If the boost converter is allowed to operate down to the V_{OUT} UVLO then 2.5V must be assumed as the minimum operating V_{OUT} voltage.

Inductor Selection

The LED boost converter is designed to work with a 10µH inductor. The inductor must be able to handle a peak current of 1A and should have a low ESR value for good efficiency. Table 7 shows several inductors that work well with the LED boost converter. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Diode Selection

When boosting to increasingly higher voltages, parasitic capacitance at the switch pin becomes an increasing large component of the switching loses. For this reason it is important to minimize the capacitance on the switch node. The diode selected should be sized to handle the peak inductor current and the average output current. At high boost voltages a diode with the lowest possible junction capacitance will often result in a more efficient solution than one with a lower forward drop.

I²C OPERATION

I²C Interface

The LTC3577 may communicate with a bus master using the standard I²C 2-wire interface. The Timing Diagram shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines. The LTC3577 is both a slave receiver and slave transmitter. The I²C control signals, SDA and SCL are scaled internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the bus pull-up resistors.

The I²C port has an undervoltage lockout on the DV_{CC} pin. When DV_{CC} is below approximately 1V, the I²C serial port is cleared, the LTC3577 is set to its default configuration of all zeros.

Table 7. Recommended Inductors for Boost Switching Regulators

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE in mm (L × W × H)	MANUFACTURER
DB62LCB	10	1.22	0.118	6.2 × 6.2 × 2	Toko www.toko.com
CDRH4D16NP-100M	10	10.5	0.155	4.8 × 4.8 × 1.8	Sumida www.sumida.com
SD18-100-R	10	1.28	0.158*	5.2 × 5.2 × 1.8	Cooper www.cooperet.com
LPS4018-103	10	1.1	0.200	4.0 × 4.0 × 1.8	Coil Craft www.coilcraft.com

*Typical

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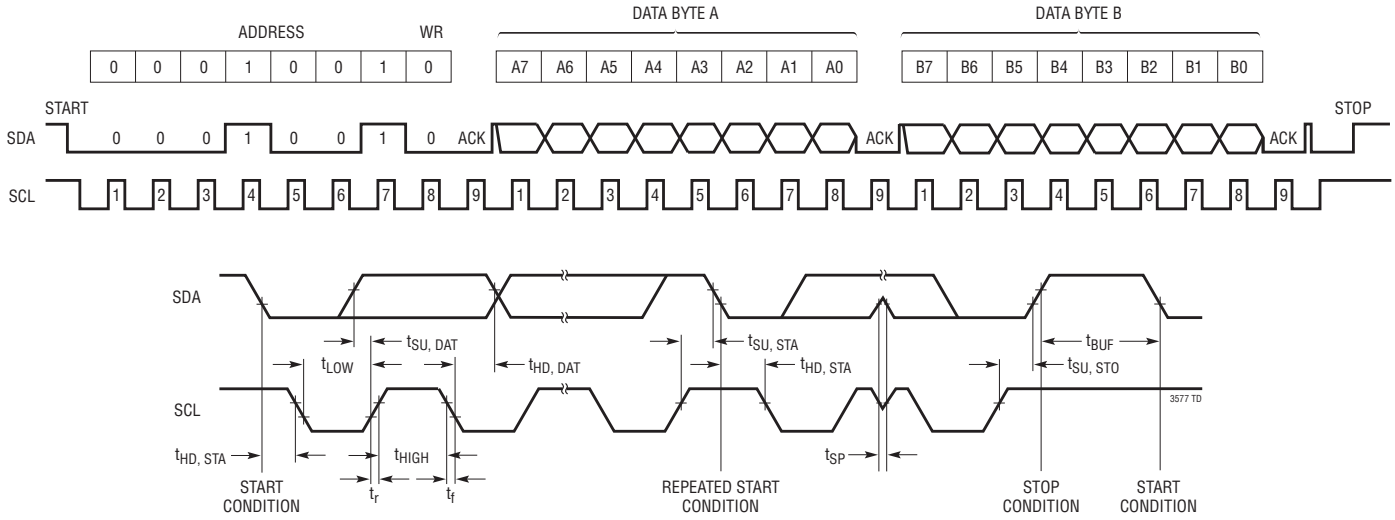
I²C Timing Diagram



I²C Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

I²C START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LTC3577, the master may transmit a STOP condition which commands the LTC3577 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for communication with another I²C device.

I²C Byte Format

Each byte sent to or received from the LTC3577 must be 8 bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC3577 most significant bit (MSB) first.

I²C Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. When the LTC3577 is written to (write address), it acknowledges its write address as well as the subsequent two data bytes. When it is read from (read address), the LTC3577 acknowledges its read address only. The bus master should acknowledge receipt of information from the LTC3577.

An acknowledge (active LOW) generated by the LTC3577 lets the master know that the latest byte of information was received. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock cycle. The LTC3577 pulls down the SDA line during the write acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

When the LTC3577 is read from, it releases the SDA line so that the master may acknowledge receipt of the data. Since the LTC3577 only transmits one byte of data, a master not acknowledging the data sent by the LTC3577 has no I²C specific consequence on the operation of the I²C port.

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I²C Slave Address

The LTC3577 responds to a 7-bit address which has been factory programmed to b'0001001[R/W]'. The LSB of the address byte, known as the read/write bit, should be 0 when writing data to the LTC3577 and 1 when reading data from it. Considering the address an eight bit word, then the write address is 0x12 and the read address is 0x13. The LTC3577 will acknowledge both its read and write address.

I²C Sub-Addressed Writing

The LTC3577 has four command registers for control input. They are accessed by the I²C port via a sub-addressed writing system.

Each write cycle of the LTC3577 consists of exactly three bytes. The first byte is always the LTC3577's write address. The second byte represents the LTC3577's sub-address. The sub address is a pointer which directs the subsequent data byte within the LTC3577. The third byte consists of the data to be written to the location pointed to by the sub-address. The LTC3577 contains control registers at only four sub-address locations: 0x00, 0x01, 0x02 and 0x03. Writing to sub-addresses outside the four sub-addresses listed is not recommended as it can cause data in one of the four listed sub-addresses to be overwritten.

I²C Bus Write Operation

The master initiates communication with the LTC3577 with a START condition and the LTC3577's write address. If the address matches that of the LTC3577, the LTC3577 returns an acknowledge. The master should then deliver the sub-address. Again the LTC3577 acknowledges and the cycle is repeated for the data byte. The data byte is transferred to an internal holding latch upon the return of its acknowledge by the LTC3577. This procedure must be repeated for each sub-address that requires new data. After one or more cycles of [ADDRESS][SUB-ADDRESS][DATA], the master may terminate the communication with a STOP condition. Alternatively, a REPEAT-START condition can be initiated by the master and another chip on the I²C bus can be addressed. This cycle can continue indefinitely and the LTC3577 will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP can be sent and the LTC3577 will update its command latches with the data that it had received.

I²C Bus Read Operation

The bus master reads the status of the LTC3577 with a START condition followed by the LTC3577 read address. If the read address matches that of the LTC3577, the LTC3577 returns an acknowledge. Following the acknowledgement of its read address the LTC3577 returns one bit of status information for each of the next 8 clock cycles. A STOP command is not required for the bus read operation.

I²C Input Data

There are 4 bytes of data that can be written to on the LTC3577. The bytes are accessed through the sub-addresses 0x00 to 0x03. At first power application (V_{BUS}, WALL or BAT) all bits default to 0. Additionally all bits are cleared to 0 when DV_{CC} drops below its undervoltage lock out or if the pushbutton enters the power-down (PDN1 or PDN2) state.

Table 8. LDO and Buck Control Register

LDO and BUCK CONTROL REGISTER		**ADDRESS:** 00010010 **SUB-ADDRESS:** 00000000
BIT	**NAME**	**FUNCTION**
B0	LDO1EN	Enable LDO 1
B1	LDO2EN	Enable LDO 2
B2	BK1BRST	Buck1 Burst Mode Enable
B3	BK2BRST	Buck2 Burst Mode Enable
B4	BK3BRST	Buck2 Burst Mode Enable
B5	SLEWCTL1	Buck SW Slew Rate: 00 = 1ns, 01 = 2ns, 10 = 4ns, 11 = 8ns
B6	SLEWCTL2	
B7	N/A	Not Used—No Effect on Operation

Table 8 shows the first byte of data that can be written to at sub-address 0x00. This byte of data is referred to as the "LDO and buck control register."

Bits B0 and B1 enable and disable the LDOs. Writing 1 to B0 or B1 will enable LDO1 or LDO2 respectively, while writing a 0 will disable the respective LDO.

OPERATION

Bits B2, B3, and B4 set the operating modes of the step-down switching regulators (bucks). Writing 1 to any of these three registers will put that respective buck converter in the high efficiency Burst Mode operation, while a 0 will enable the low noise pulse-skipping mode operation.

The B5 and B6 bits adjust the slew rate of all SW pins together so they all slew at the same rate. It is recommended that the fastest slew rate (B6:B5 = 00) be used unless EMI is an issue in the application as slower slew rates cause reduced efficiency.

Table 9. I²C LED Control Register

LED CONTROL REGISTER		ADDRESS: 00010010 SUB-ADDRESS: 00000001
BIT	**NAME**	**FUNCTION**
B0	EN	Enable: 1 = Enable 0 = Off
B1	GR2	Gradation GR[2:1]: 00 = 15ms, 01 = 460ms, 10 = 930ms, 11 = 1.85s
B2	GR1	
B3	MD1	Mode MD[2:1]: 00 = CC Boost, 10 = PWM Boost; 01 = HV Boost
B4	MD2	
B5	PWMC1	PWM CLK PWMC[2:1]: 00 = 8.77kHz, 01 = 4.39kHz, 10 = 2.92kHz, 11 = 2.19kHz
B6	PWMC2	
B7	SLEWLED	LED SW Slew Rate: 0/1 = Fast/Slow

Table 9 shows the second byte of data that can be written to at sub-address 0x01. This byte of data is referred to as the "LED control register."

Bit B0 enables and disables the LED boost circuitry. Writing a 1 to B0 enables the LED boost circuitry, while writing a 0 disables the LED boost circuitry.

Bits B1 and B2 are the LED gradation which sets the ramp up and down time of the LED current when enabled or disabled. The gradation function allows the LEDs to turn on/off gradually as opposed to an abrupt step.

Bits B3 and B4 set the operating mode of the LED boost circuitry. The operating modes are: B4:B3 = 00 LED constant current (CC) boost operation; B4:B3 = 10 LED PWM boost operation; B4:B3 = 01 fixed high voltage (HV) output boost operation; B4:B3 = 11 not supported, do not use. See the "LED Backlight/Boost Operation" section for more information on the operating modes.

Bits B5 and B6 set the PWM clock speed as shown in Table 9 of the "LED Backlight/Boost Operation" section.

Bit B7 sets the slew rate of the LED boost SW pin. Setting B7 to 0 results in the fastest slew rate and provides the most efficient mode of operation. Setting B7 to 1 should only be used in cases where EMI due to SW slewing is an issue as the slower slew rate causes a loss in efficiency.

See the "LED Backlight/Boost Operation" section for more detailed operating information.

Table 10 shows the third byte of data that can be written to at sub-address 0x02. This byte of data is referred to as the "LED DAC register." The LED current source utilizes a 6-bit 60dB exponential DAC. This DAC provides accurate current control from 20µA to 20mA with approximately 1dB per step with $I_{LED(FS)}$ programmed to 20mA. The LED current can be approximated by the following equation:

$$I_{LED} = I_{LED(FS)} \bullet 10^{\left(3 \bullet \frac{DAC - 63}{63}\right)}$$

where DAC is the decimal value programmed into the I²C "LED DAC register." For example with $I_{LED(FS)}$ = 20mA and DAC[5:0] = 101010 (42 decimal) I_{LED} equates to 2mA.

Table 10. I²C LED DAC Register

LED DAC REGISTER		ADDRESS: 00010010 SUB-ADDRESS: 00000010
BIT	**NAME**	**FUNCTION**
B0	DAC[0]	6-Bit Log DAC Code
B1	DAC[1]	
B2	DAC[2]	
B3	DAC[3]	
B4	DAC[4]	
B5	DAC[5]	
B6	N/A	Not Used—No Effect On Operation
B7	N/A	Not Used—No Effect On Operation

OPERATION

Table 11 shows the final byte of data that can be written to at sub-address 0x03. This byte of data is referred to as the "LED PWM register". See the "LED PWM vs Constant Current Operation" section for detailed information on how to set the values of this register.

Table 11. LED PWM Register

LED PWM REGISTER		ADDRESS: 00010010 SUB-ADDRESS: 00000011
BIT	**NAME**	**FUNCTION**
B0	PWMDEN[0]	PWM DENOMINATOR
B1	PWMDEN[1]	
B2	PWMDEN[2]	
B3	PWMDEN[3]	
B4	PWMNUM[0]	PWM NUMERATOR
B5	PWMNUM[1]	
B6	PWMNUM[2]	
B7	PWMNUM[3]	

I²C Output Data

One status byte may be read from the LTC3577. Table 12 represents the status byte information. A 1 read back in the any of the bit positions indicates that the condition is true. For example, 1 read back from bit A3 indicate that LDO1 is enabled and regulating correctly. A status read from the LTC3577 captures the status information when the LTC3577 acknowledges its read address.

Table 12. I²C READ Register

STATUS REGISTER		ADDRESS: 00010011 SUB-ADDRESS: None
BIT	**NAME**	**FUNCTION**
A0	CHARGE	Charge Status (1 = Charging)
A1	STAT[0]	STAT[1:0]; 00 = No Fault 01 = TOO COLD/HOT 10 = BATTERY OVERTEMP 11 = BATTERY FAULT
A2	STAT[1]	
A3	PGLDO[1]	LDO1 Power Good
A4	PGLDO[2]	LDO2 Power Good
A5	PGBCK[1]	Buck1 Power Good
A6	PGBCK[2]	Buck2 Power Good
A7	PGBCK[3]	Buck3 Power Good

Bit A7 shows the power good status of buck3. A 1 indicates that buck3 is enabled and is regulating correctly. A 0 indicates that either buck3 is not enabled, or that the buck3 is enabled, but is out of regulation by more than 8%.

Bit A6 shows the power good status of buck2. A 1 indicates that buck2 is enabled and is regulating correctly. A 0 indicates that either buck2 is not enabled, or that the buck2 is enabled, but is out of regulation by more than 8%.

Bit A5 shows the power good status of buck1. A 1 indicates that buck1 is enabled and is regulating correctly. A 0 indicates that either buck1 is not enabled, or that the buck1 is enabled, but is out of regulation by more than 8%.

Bit A4 shows the power good status of LDO2. A 1 indicates that LDO2 is enabled and is regulating correctly. A 0 indicates that either LDO2 is not enabled, or that the LDO2 is enabled, but is out of regulation by more than 8%.

Bit A3 shows the power good status of LDO1. A 1 indicates that LDO1 is enabled and is regulating correctly. A 0 indicates that either LDO1 is not enabled, or that the LDO1 is enabled, but is out of regulation by more than 8%.

Bits A2 and A1 indicate the fault status of the charger circuit and are decoded in Table 12. The "too cold/hot" state indicates that the thermistor temperature is out of the valid charging range (either below 0°C or above 40°C for a curve 1 thermistor) and that charging has paused until a return to valid temperature. The battery overtemp state indicates that the battery's thermistor has reached a critical temperature (above 50°C for a curve 1 thermistor) and that long-term battery capacity may be seriously compromised if the condition persists. The battery fault state indicates that an attempt was made to charge a low battery (typically < 2.85V) but that the low voltage condition persisted for more than 1/2 hour. In this case charging has terminated.

Bit A0 indicates the status of the battery charger. A 1 indicates that the charger is enabled and is in the constant current charge state. In this case the battery is being charged unless the NTC thermistor is outside its valid charge range in which case charging is temporarily suspended but not complete. Charging will continue once the

OPERATION

battery has returned to a valid charging temperature. A 0 in bit A0 indicates that charging has entered the end-of-charge state ($h_{C/10}$) and is near V_{FLOAT} or that charging has been terminated. Charging can be terminated by reaching the end of the charge timer or by a battery fault as described previously.

I²C WRITE REGISTER MAP (see the "I²C Input Data" section for more details, all registers default to 0 when reset)

LDO and BUCK CONTOL REGISTER		**ADDRESS:** 00010010 **SUB-ADDRESS:** 00000000
BIT	**NAME**	**FUNCTION**
B0	LDO1EN	Enable LDO 1
B1	LDO2EN	Enable LDO 2
B2	BK1BRST	Buck1 Burst Mode Enable
B3	BK2BRST	Buck2 Burst Mode Enable
B4	BK3BRST	Buck2 Burst Mode Enable
B5	SLEWCTL1	Buck SW Slew Rate: 00 = 1ns, 01 = 2ns, 10 = 4ns, 11 = 8ns
B6	SLEWCTL2	
B7	N/A	Not Used—No Effect On Operation

LED CONTROL REGISTER		**ADDRESS:** 00010010 **SUB-ADDRESS:** 00000001
BIT	**NAME**	**FUNCTION**
B0	EN	Enable: 1= Enable 0 = Off
B1	GR2	Gradation GR[2:1]: 00 = 15ms, 01 = 460ms, 10 = 930ms, 11 = 1.85 Seconds
B2	GR1	
B3	MD1	Mode MD[2:1]: 00 = CC Boost, 10 = PWM Boost, 01 = HV Boost
B4	MD2	
B5	PWMC1	PWM CLK PWMC[2:1]: 00 = 8.77kHz, 01 = 4.39kHz, 10 = 2.92kHz, 11 = 2.19kHz
B6	PWMC2	
B7	SLEWLED	LED SW Slew rate: 0/1 = Fast/Slow

LED DAC REGISTER		**ADDRESS:** 00010010 **SUB-ADDRESS:** 00000010
BIT	**NAME**	**FUNCTION**
B0	DAC[0]	6-Bit Log DAC Code
B1	DAC[1]	
B2	DAC[2]	
B3	DAC[3]	
B4	DAC[4]	
B5	DAC[5]	
B6	N/A	Not Used—No Effect On Operation
B7	N/A	Not Used—No Effect On Operation

LED PWM REGISTER		**ADDRESS:** 00010010 **SUB-ADDRESS:** 00000011
BIT	**NAME**	**FUNCTION**
B0	PWMDEN[0]	PWM Denominator
B1	PWMDEN[1]	
B2	PWMDEN[2]	
B3	PWMDEN[3]	
B4	PWMNUM[0]	PWM Numerator
B5	PWMNUM[1]	
B6	PWMNUM[2]	
B7	PWMNUM[3]	

PUSHBUTTON INTERFACE OPERATION

State Diagram/Operation

Figure 18 shows the LTC3577 pushbutton state diagram. Upon first application of power (V_{BUS}, WALL or BAT) an internal power-on reset (POR) signal places the pushbutton circuitry into the power-down (PDN1) state. One second after entering the PDN1 state the pushbutton circuitry will transition into the hard reset (HR) state. The following events cause the state machine to transition out of HR into the power-up (PUP1) state:

1) ON input low for 400ms (PB400MS)

2) Application of external power (EXTPWR)

3) PWR_ON input going high (PWR_ON)

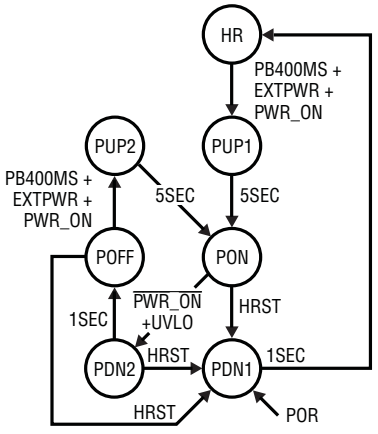


Figure 18. Pushbutton State Diagram

OPERATION

Upon entering the PUP1 state, the pushbutton circuitry will sequence up the three step-down switching regulators in numerical order. LDO1, LDO2 and LED backlight are enabled via I^2C and do not take part in the power-up sequence of the pushbutton. Five seconds after entering the PUP1 state, the pushbutton circuitry will transition into the power-on (PON) state. Note that the PWR_ON input must be brought high before entering the PON state if the part is to remain in the PON state.

PWR_ON going low, or V_{OUT} dropping to its undervoltage lockout (V_{OUT} UVLO) threshold will cause the state machine to leave the PON state and enter the power-down (PDN2) state. The PDN1 and PDN2 states reset the I^2C registers effectively shutting down the LDOs and LED backlight as well as disable all switching regulators together. The one second delay before leaving either power-down state allows all LTC3577 generated supplies to power down completely before they can be re-enabled.

The same three events used to exit HR are also used to exit the POFF state and enter PUP2 state. The PUP2 state operates in the same manner as the PUP1 state previously described.

The hard reset (HRST) event is generated by pressing and holding the pushbutton ($\overline{ON}$ input low) for 5 seconds. For a valid HRST event to occur the initial pushbutton application must start in the PUP1, PUP2 or PON state, but can end in any state. If a valid HRST event is present in PON, PDN2 or POFF, then the state machine will transition to the PDN1 state and subsequently transition to the HR state one second later.

In the HR state all supplies are disabled and the PowerPath circuitry is placed in an ultralow quiescent state to minimize battery drain. If no external charging supply is present (WALL or V_{BUS}) then the ideal diode is shut down disconnecting V_{OUT} from BAT. The ultralow power consumption in the HR state makes it ideal for shipping or long term storage, minimizing battery drain. In the HR state the battery monitoring circuit wakes up the charger every 150ms to sample the NTC thermistor for overtemperature battery condition. To sample the NTC thermistor, the ideal diode is turned on charging V_{OUT} up to V_{BAT}. As a consequence, any system load on V_{OUT} will show up as a load on V_{BAT}. Figure 26 shows an optional circuit to disconnect the system load from V_{OUT}.

Power-Up via Pushbutton Timing

The timing diagram, Figure 19, shows the LTC3577 powering up through application of the external pushbutton. For this example the pushbutton circuitry starts in the POFF or HR state with a battery connected and all buck disabled. Pushbutton application ($\overline{ON}$ low) for 400ms transitions the pushbutton circuitry into the PUP state which brings WAKE Hi-Z for 5 seconds. WAKE going Hi-Z sequences buck1-3 up in numerical order. WAKE will stay Hi-Z if PWR_ON is driven high before the 5 seconds PUP period is over. If PWR_ON is low or goes low after the 5 second period, WAKE will go low and buck1-3 will be shut down together. PG_DCDC is asserted once all enabled bucks are within 8% of their regulation voltage for 230ms.

PBSTAT does not go low impedance with $\overline{ON}$ going low during the power-up pushbutton application. PBSTAT will go low impedance with $\overline{ON}$ on subsequent pushbutton applications once in the PUP1, PUP2 or PON states.

The LDOs and LED backlight can be enabled and disabled at any time via I^2C once in the PUP1, PUP2 or PON states. The PWR_ON input can be driven via a µP/µC or by one of the buck outputs through a high impedance (100kΩ typ) to keep the bucks enabled as described above.

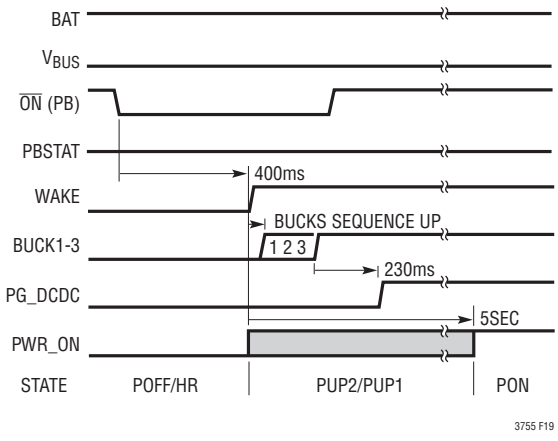


Figure 19. Power-Up via Pushbutton Timing

OPERATION

Power-Up via External Power Timing

The timing diagram, Figure 20, shows the LTC3577 powering up through application of the external power (V_{BUS} or WALL). For this example the pushbutton circuitry starts in the POFF or HR state with a battery connected and all buck disabled. 100ms after WALL or V_{BUS} application the WAKE output goes Hi-Z for 5 seconds. The 100ms delay time allows the applied supply to settle. WAKE going Hi-Z sequences buck1-3 up in numerical order. WAKE will stay Hi-Z if the PWR_ON input is driven high before the 5 seconds PUP period is over. If PWR_ON is low or goes low after the 5 second period, WAKE will go low and buck1-3 will be shut down together. PG_DCDC is asserted once all enabled bucks are within 8% of their regulation voltage for 230ms.

The LDOs and LED backlight can be enabled and disabled via I^2C any time after entering the PUP1, PUP2 or PON state. The PWR_ON input can be driven via a µP/µC or one of the buck outputs through a high impedance (100kΩ typ) to keep the bucks enabled as described above.

Without a battery present initial power application causes a power on reset which puts the pushbutton circuitry in the PDN2 state and subsequently the HR state 1 second later. In this case the pushbutton must be applied to enter the PUP1 state after initial power application.

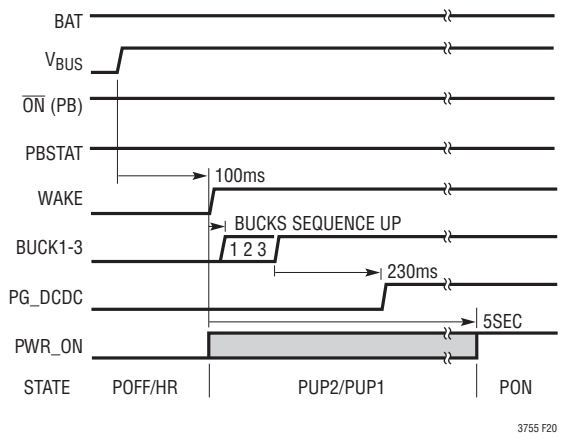


Figure 20. Power-Up via External Power Timing

Power-Up via PWR_ON Timing

The timing diagram, Figure 21, shows the LTC3577 powering up by driving PWR_ON high. For this example the pushbutton circuitry starts in the POFF or HR state with a battery connected and all bucks disabled. 50ms after PWR_ON goes high the WAKE output goes Hi-Z for 5 seconds. WAKE going Hi-Z sequences buck1-3 up in numerical order. WAKE will stay Hi-Z as long as PWR_ON is high at the end of the 5 second PUP period. If PWR_ON is low or goes low after the 5 second period, WAKE will go low and buck1-3 will be shut down together. PG_DCDC is asserted once all enabled bucks are within 8% of their regulation voltage for 230ms.

The LDOs and LED backlight can be enabled and disabled via I^2C any time after entering the PUP1, PUP2 or PON state.

Powering up via PWR_ON is useful for applications containing an always on µC. This allows the µC to power the application up and down for house keeping and other activities outside the user's control.

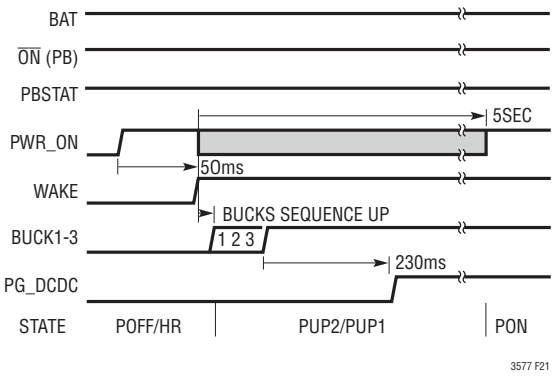


Figure 21. Power-Up via PWR_ON Timing

OPERATION

Power-Down via Pushbutton Timing

The timing diagram, Figure 22, shows the LTC3577 powering down by µC/µP control. For this example the pushbutton circuitry starts in the PON state with a battery connected and all bucks enabled. In this case the pushbutton is applied ($\overline{ON}$ low) for at least 50ms, which generates a low impedance on the PBSTAT output. After receiving the PBSTAT the µC/µP will drive the PWR_ON input low. 50ms after PWR_ON goes low the WAKE output will go low and the pushbutton circuitry will enter the PDN2 state. The bucks are disabled together at once upon entering the PDN2 state. Once entering the PDN2 state a 1 second wait time is initiated before entering the POFF state. During this 1 second time $\overline{ON}$ and PWR_ON inputs as well as external power application are ignored to allow all LTC3577 generated supplies to go low. Though the above assumes a battery present, the same operation would take place with a valid external supply (V_{BUS} or WALL) with or without a battery present.

Upon entering the PDN2 state the LDOs and LED backlight I^2C registers are cleared effectively disabling both. If this is not desirable the LDOs and LED backlight should be disabled via I^2C prior to entering the PDN2 state.

Holding $\overline{ON}$ low through the 1 second power-down period will not cause a power-up event at end of the 1 second period. The $\overline{ON}$ input must be brought high following the power-down event and then go low again to establish a valid power-up event.

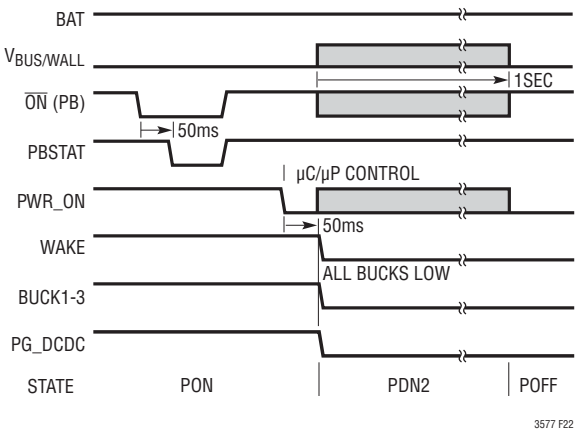


Figure 22. Power-Down via Pushbutton Timing

UVLO Minimum Off-Time Timing (Low Battery)

The timing diagram, Figure 23, assumes the battery is either missing or at a voltage below the V_{OUT} UVLO threshold and the application is running via external power (V_{BUS} or WALL). A glitch on the external supply causes V_{OUT} to drop below the V_{OUT} UVLO threshold temporarily. The V_{OUT} UVLO condition will cause the pushbutton circuitry to transition from the PON state to the PDN2 state. Upon entering the PDN2 state WAKE and PG_DCDC will go low while the bucks, LDOs and LED backlight power down together. If the external supply recovers after entering the PND2 state such that V_{OUT} is no longer in UVLO then the LTC3577 will transition back into the PUP2 state once the PDN2 one second delay is complete. Though not shown in Figure 23, the pushbutton logic briefly visits the POFF state when transitioning between PDN2 and PUP2. Entering the PUP2 state will cause the bucks to sequence up as described previously in the power-up sections. The LDOs and LED backlight must be re-enabled via I^2C once device is powered back up.

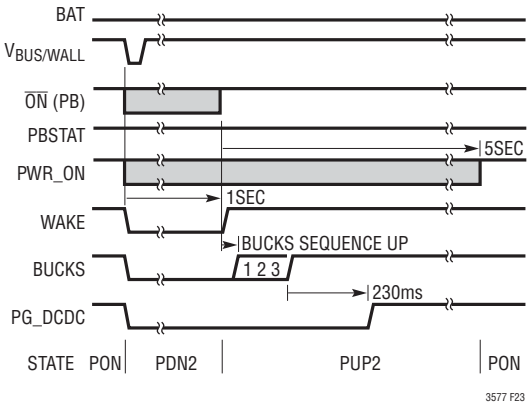


Figure 23. UVLO Minimum Off-Time

OPERATION

Hard Reset Timing

Hard reset provides an ultralow power-down state for shipping or long-term storage as well as a way to power down the application in case of a software lock-up. In the case of software lock-up $\overline{ON}$ is brought low by the user applying the pushbutton. If the user holds the pushbutton for 5 seconds a hard reset event (HRST) will occur placing the pushbutton circuitry in the PDN1 state. At this point the bucks, LDOs and LED backlight will all be shut down and WAKE and PG_DCDC will both go low. Following a 1 second power-down period the pushbutton circuitry will enter the hard reset state (HR).

Holding $\overline{ON}$ low through the 1 second power-down period will not cause a power-up event at end of the 1second period. The $\overline{ON}$ must be brought high following the power-down event and then go low for again for 400ms to establish a valid power-up event as shown in Figure 24.

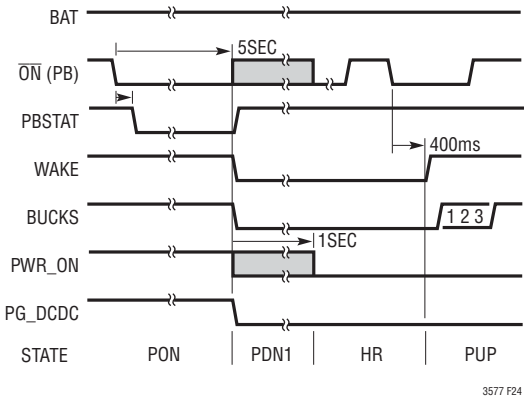


Figure 24. Hard Reset Timing

Power-Up Sequencing

Figure 25 shows the actual power-up sequencing of the LTC3577. Buck1, buck2 and buck3 are all initially disabled (0V). Once the pushbutton has been applied ($\overline{ON}$ low) for 400ms, WAKE goes high and buck1 is enabled. Buck1 slews up and enters regulation once enabled. The actual slew rate is controlled by the soft-start function of buck1 in conjunction with output capacitance and load (see the "Step-Down Switching Regulator Operation" section for more information). When buck1 is within about 8% of final regulation, buck2 is enabled and slews up into regulation. Finally when buck2 is within about 8% of final regulation, buck3 is enabled and slews up into regulation. 230ms after buck3 is within 8% of final regulation the PG_DCDC output will go high impedance (not shown in Figure 25). The regulators in Figure 25 are slewing up with nominal output capacitors and no load. Adding a load or increasing output capacitance on any of the outputs will reduce the slew rate and lengthen the time it takes the regulator to get into regulation. Reducing the slew rate also pushes out the time until the next regulator is enabled proportionally.

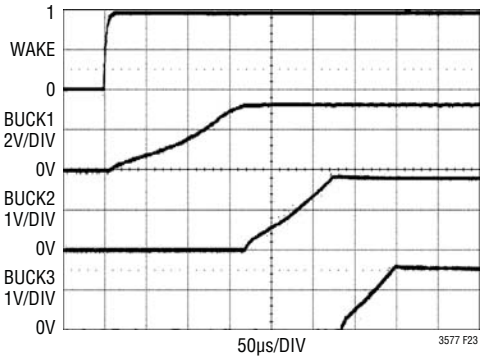


Figure 25. Power-Up Sequencing

OPERATION

LAYOUT AND THERMAL CONSIDERATIONS

Printed Circuit Board Power Dissipation

In order to be able to deliver maximum charge current under all conditions, it is critical that the exposed ground pad on the backside of the LTC3577 package is soldered to a ground plane on the board. Correctly soldered to 2500mm^2 ground plane on a double-sided 1oz. copper board the LTC3577 has a thermal resistance (θ_{JA}) of approximately 45°C/W. Failure to make good thermal contact between the Exposed Pad on the backside of the package and a adequately sized ground plane will result in thermal resistances far greater than 45°C/W.

The conditions that cause the LTC3577 to reduce charge current due to the thermal protection feedback can be approximated by considering the power dissipated in the part. For high charge currents with a wall adapter applied to V_{OUT}, the LTC3577 power dissipation is approximately:

$$P_D = (V_{OUT} - BAT) \bullet I_{BAT} + P_{DREGS}$$

where, P_D is the total power dissipated, V_{OUT} is the system supply voltage, BAT is the battery voltage, and I_{BAT} is the battery charge current. P_{DREGS} is the sum of power dissipated on-chip by the step-down switching, LDO and LED boost regulators.

The power dissipated by a step-down switching regulator can be estimated as follows:

$$P_{D(SWx)} = (BOUTx \bullet I_{OUT}) \bullet \frac{100 - Eff}{100}$$

where BOUTx is the programmed output voltage, I_{OUT} is the load current and Eff is the % efficiency which can be measured or looked up on an efficiency table for the programmed output voltage.

The power dissipated on chip by a LDO regulator can be estimated as follows:

$$P_{DLDOx} = (V_{INLDOx} - LOUTx) \bullet I_{OUT}$$

where LOUTx is the programmed output voltage, V_{INLDOx} is the LDO supply voltage and I_{OUT} is the LDO output load current. Note that if the LDO supply is connected to one of the buck output, then its supply current must be added to the buck regulator load current for calculating the buck power loss.

The power dissipated by the LED boost regulator can be estimated as follows:

$$P_{DLED} = I_{LED} \bullet 0.3V + R_{NSWON} \bullet \left(I_{LED} \bullet \frac{BOOST}{V_{OUT} - 1} \right)^2$$

where BOOST is the output voltage driving the top of the LED string, R_{NSWON} is the on-resistance of the SW N-FET (typically 330mΩ), I_{LED} is the LED programmed current sink.

Thus the power dissipated by all regulators is:

$$P_{DREGS} = P_{DSW1} + P_{DSW2} + P_{DSW3} + P_{DLDO1} + P_{DLDO2} + P_{DLED}$$

It is not necessary to perform any worst-case power dissipation scenarios because the LTC3577 will automatically reduce the charge current to maintain the die temperature at approximately 110°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 110°C - P_D \bullet \theta_{JA}$$

Example: Consider the LTC3577 operating from a wall adapter with 5V (V_{OUT}) providing 1A (I_{BAT}) to charge a Li-Ion battery at 3.3V (BAT). Also assume P_{DREGS} = 0.3W, so the total power dissipation is:

$$P_D = (5V - 3.3V) \bullet 1A + 0.3W = 2W$$

The ambient temperature above which the LTC3577 will begin to reduce the 1A charge current, is approximately

$$T_A = 110°C - 2W \bullet 45°C/W = 20°C$$

OPERATION

The LTC3557 can be used above 20°C, but the charge current will be reduced below 1A. The charge current at a given ambient temperature can be approximated by:

$$P_D = \frac{110°C - T_A}{\theta_{JA}} = (V_{OUT} - BAT) \bullet I_{BAT} + P_{D(REGS)}$$

Thus:

$$I_{BAT} = \frac{\frac{(110°C - T_A)}{\theta_{JA}} - P_{DREGS}}{V_{OUT} - BAT}$$

Consider the above example with an ambient temperature of 55°C. The charge current will be reduced to approximately:

$$I_{BAT} = \frac{\frac{110°C - 55°C}{45°C/W} - 0.3W}{5V - 3.3V}$$

$$I_{BAT} = \frac{1.22W - 0.3W}{1.7V} = 542mA$$

If an external buck switching regulator controlled by the LTC3577 V_C pin is used instead of a 5V wall adapter we see a significant reduction in power dissipated by the LTC3577. This is because the external buck switching regulator will drive the PowerPath output (V_{OUT}) to about 3.6V with the battery at 3.3V. If you go through the example above and substitute 3.6V for V_{OUT} we see that thermal regulation does not kick in until about 83°C. Thus, the external high voltage buck regulator not only allows higher charging currents, but lower power dissipation means a cooler running application.

Printed Circuit Board Layout

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3577:

1. The Exposed Pad of the package (Pin 45) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. The step-down switching regulator input supply pins (V_{IN12} and V_{IN3}) and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It's important to minimizing inductance from these capacitors to the pins of the LTC3577. Connect V_{IN12} and V_{IN3} to V_{OUT} through a short low impedance trace.
3. The switching power traces connecting SW1, SW2, and SW3 to their respective inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching nodes, sensitive nodes such as the feedback nodes (FBx, LDOx_FB and LED_OV) should be kept far away or shielded from the switching nodes or poor performance could result.
4. Connections between the step-down switching regulator inductors and their respective output capacitors should be kept as short as possible. The GND side of the output capacitors should connect directly to the thermal ground plane of the part.
5. Keep the buck feedback pin traces (FB1, FB2, and FB3) as short as possible. Minimize any parasitic capacitance between the feedback traces and any switching node (i.e. SW1, SW2, SW3, and logic signals). If necessary shield the feedback nodes with a GND trace.
6. Connections between the LTC3577 PowerPath pins (V_{BUS} and V_{OUT}) and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part.
7. The boost converter switching power trace connecting SW to the inductor should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the SW node, sensitive nodes such as the feedback nodes (FBx, LDOx_FB and LED_OV) should be kept far away or shielded from this switching node or poor performance could result.

TYPICAL APPLICATIONS

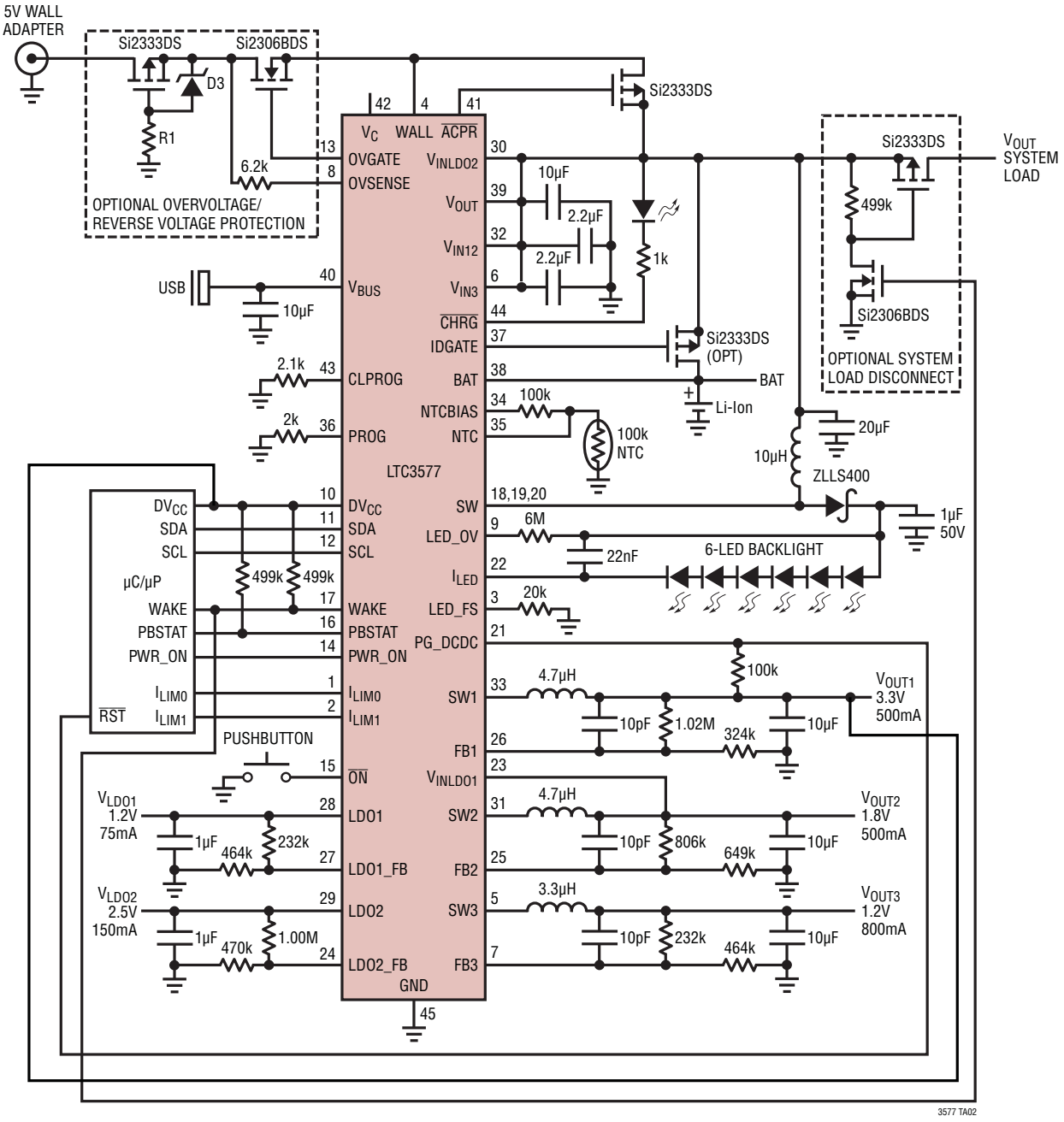


Figure 26. USB Plus 5V Adapter Input Charger, Multichannel Power Supply and PowerPath Controller

TYPICAL APPLICATIONS

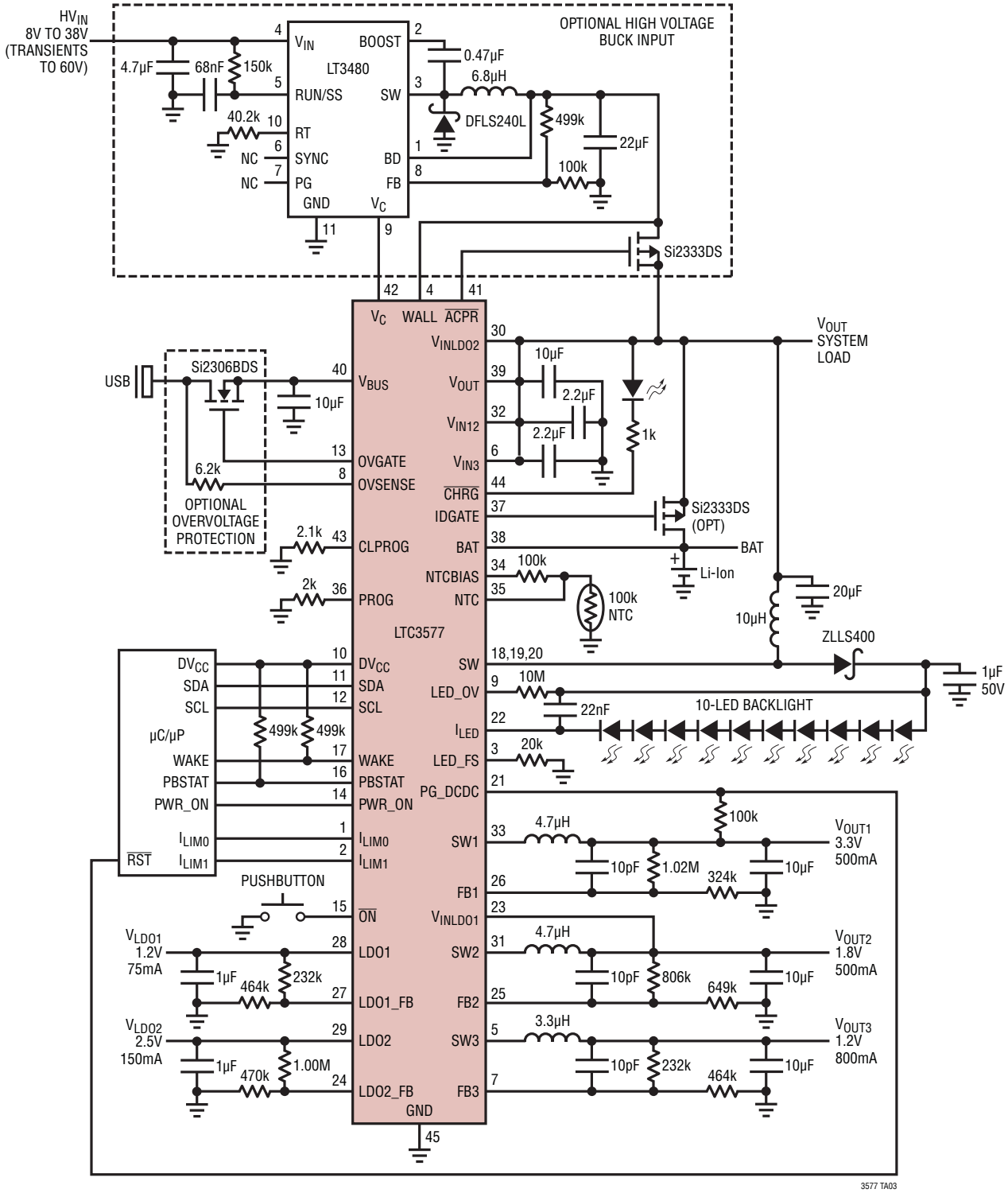
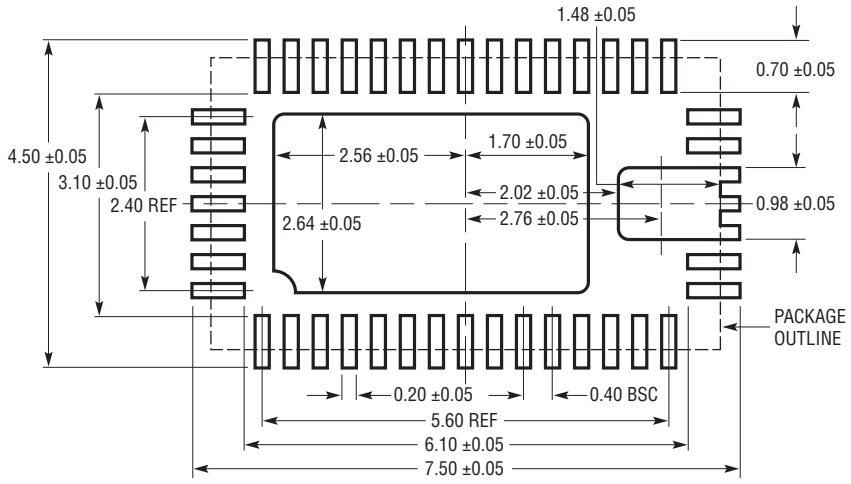


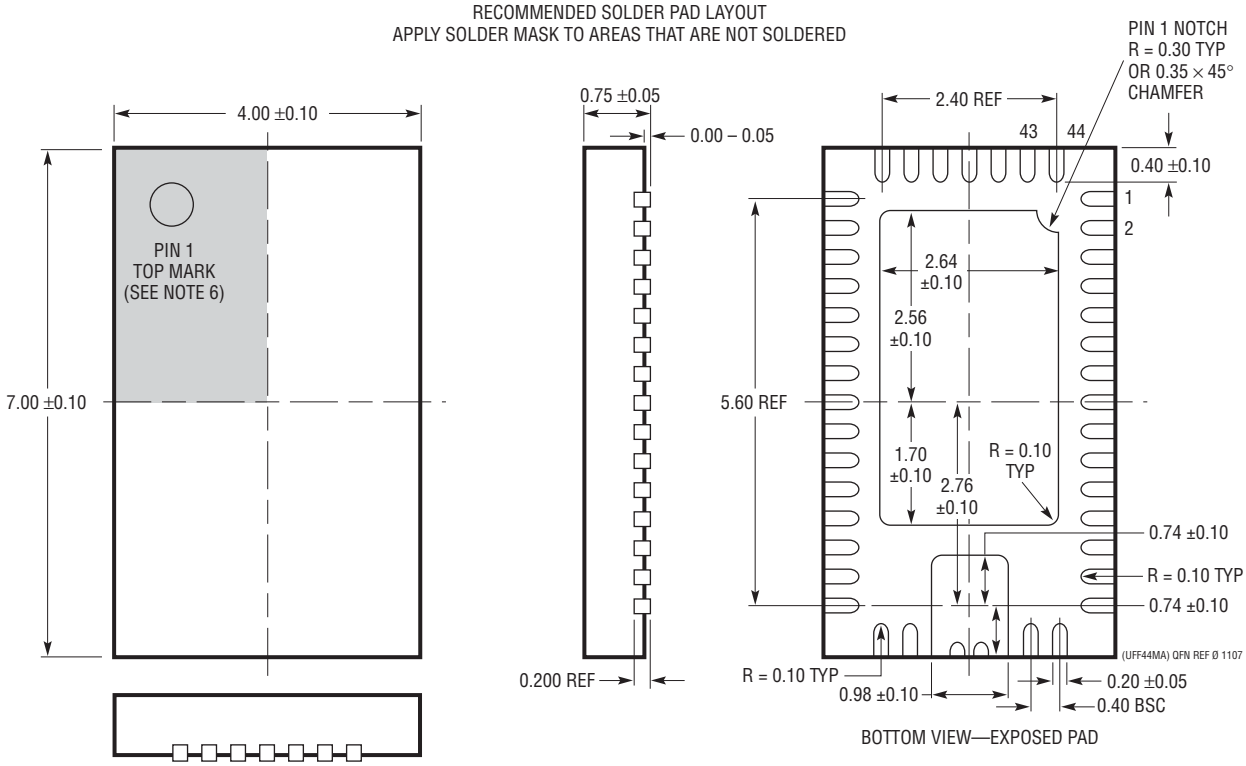
Figure 27. USB Plus HV Input Charger, Multichannel Power Supply and PowerPath Controller

PACKAGE DESCRIPTION

UFF Package
Variation: UFFMA
44-Lead Plastic QFN (4mm × 7mm)
(Reference LTC DWG # 05-08-1762 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	Nov 09	Changes to Features	1
		Change to Absolute Maximum Ratings	3
		Add Note 16	10
		Text Changes to Pin Functions	18
		Changes to Operation Section	44
		Changes to Typical Application Circuits	50, 51

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	Seamless Transition Between Input Power Sources: Li-Ion Battery, USB and 5V Wall Adapter. Two High Efficiency DC/DC Converters: Up to 96%. Full Featured Li-Ion Battery Charger with Accurate USB Current Limiting (500mA/100mA). Pin Selectable Burst Mode Operation. Hot Swap™ Output for SDIO and Memory Cards. 24-Lead 4mm × 4mm QFN Package
LTC3456	2-Cell, Multi-Output DC/DC Converter with USB Power Manager	Seamless Transition Between 2-Cell Battery, USB and AC Wall Adapter Input Power Sources. Main Output: Fixed 3.3V Output, Core Output: Adjustable from 0.8V to $V_{BATT(MIN)}$. Hot Swap Output for Memory Cards. Power Supply Sequencing: Main and Hot Swap Accurate USB Current Limiting. High Frequency Operation: 1MHz. High Efficiency: Up to 92%. 24-Lead 4mm × 4mm QFN Package
LTC3552	Standalone Linear Li-Ion Battery Charger with Adjustable Output Dual Synchronous Buck Converter	Synchronous Buck Converter, Efficiency: >90%, Adjustable Outputs at 800mA and 400mA, Charge Current Programmable Up to 950mA, USB Compatible, 16-Lead 5mm × 3mm DFN Package
LTC3555	I^2C Controlled High Efficiency USB Power Manager Plus Triple Step-Down DC/DC	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, Three Synchronous Buck Regulators, One 1A Buck-Boost Regulator, 4mm × 5mm QFN28 Package
LTC3556	High Efficiency USB Power Manager Plus Dual Buck Plus Buck-Boost DC/DC	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, Two 400mA Synchronous Buck Regulators, One 1A Buck-Boost Regulator, 4mm × 5mm QFN28 Package
LTC3557/ LTC3557-1	USB Power Manager with Li-Ion/Polymer Charger and Triple Synchronous Buck Converter	Complete Multifunction ASSP: Linear Power Manager and Three Buck Regulators Charge Current Programmable Up to 1.5A from Wall Adapter Input, Thermal Regulation Synchronous Buck Efficiency: >95%, ADJ Outputs: 0.8V to 3.6V at 400mA/400mA/600mA Bat-Track Adaptive Output Control, 200m Ideal Diode, 4mm × 4mm QFN28 Package, "-1" Version Has 4.1V Float Voltage.
LTC3566 LTC3567	Switching USB Power Manager with Li-Ion/Polymer Charger, 1A Buck-Boost Converter Plus LDO	Multifunction PMIC: Switchmode Power Manager and 1A Buck-Boost Regulator + LDO, Charge Current Programmable Up to 1.5A from Wall Adapter Input, Thermal Regulation Synchronous Buck-Boost Converters Efficiency: >95%, ADJ Output: Down to 0.8V at 1A, Bat-Track Adaptive Output Control, 180mΩ Ideal Diode, LTC3567 Has I^2C Interface, 4mm × 4mm QFN24 Package
LTC3576/-1	Switching USB Power Manager with USB OTG + Triple Step-Down DC/DCs	Complete Multi-Function PMIC: Bi-Directional Switching Power Manager + 3 Bucks + LDO, ADJ Output Down to 0.8V at 400mA/400mA/1A, Overvoltage Protection, USB On-The-Go, Charge Current Programmable Up to 1.5A from Wall Adapter Input, Thermal Regulation, I^2C, Hi-Voltage Bat-Track Buck Interface, 180mΩ Ideal Diode, 4mm × 6mm QFN-38 Package
LTC3586	Switching USB Power Manager with Li-Ion/Polymer Charger Plus Dual Buck Plus Buck-Boost Plus Boost DC/DC	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, Two 400mA Synchronous Buck Regulators, One 1A Buck-Boost Regulator, One 600mA Boost Regulator, 4mm × 6mm 38-Pin QFN Package
LTC4085/ LTC4085-1	USB Power Manager with Ideal Diode Controller and Li-Ion Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200m Ideal Diode with <50m Option, 4mm × 3mm DFN14 Package, "-1" Version Has 4.1V Float Voltage.
LTC4088	High Efficiency USB Power Manager and Battery Charger	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50m Option, 3.3V/25mA Always-On LDO, 4mm × 3mm DFN14 Package
LTC4088-1	High Efficiency USB Power Manager and Battery Charger with Regulated Output Voltage	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, Automatic Charge Current Reduction Maintains 3.6V Minimum V_{OUT}, Battery Charger Disabled When All Logic Inputs are Grounded, 3mm × 4mm DFN14 Package
LTC4088-2	High Efficiency USB Power Manager and Battery Charger with Regulated Output Voltage	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, Automatic Charge Current Reduction Maintains 3.6V Minimum V_{OUT}, 3mm × 4mm DFN14 Package
LTC4098	USB-Compatible Switchmode Power Manager with OVP	High V_{IN}: 38V Operating, 60V Transient; 66V OVP. Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current from Wall, 600mA Charge Current from USB, 180mΩ Ideal Diode with <50mΩ Option; 3mm × 4mm Ultrathin QFN20 Package

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