



**THE DATASHEET OF
TPD2F702YFKR**



TWO-CHANNEL EMI FILTER FOR AUDIO SPEAKER/AVIF CONNECTOR

 Check for Samples: [TPD2F702](#)

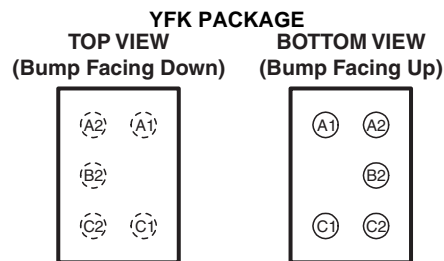
FEATURES

- Two-Channel EMI Filter for Audio Speaker or AVIF Ports
- Best in class EMI Noise Filtering for Audio Applications (-3dB Bandwidth = 1.2MHz)
- > 50 dB Crosstalk Attenuation at 100 MHz
- Integrated ESD Protection Exceeds IEC61000-4-2 (Level 4) at the Connector Ports (Level 4) on the Connector Side
 - ±15-kV Human-Body Model (HBM)
 - ±30-kV IEC 61000-4-2 Contact Discharge
 - ±30-kV IEC 61000-4-2 Air-Gap Discharge

- Pi-Style (C-R-C) Filter Configuration (C1 = 30 pF, R = 15 Ω, C2 = 5000 pF)
- Ultra Low Leakage Current (100-nA max)
- Space-Saving WCSP Package and Flow-Through Pin Mapping
- Industrial Temperature Range: –40°C to 85°C

APPLICATIONS

- Mobile Phones
- PDAs
- Headsets
- Portable Gaming



TERMINAL ASSIGNMENTS

	1	2
A	Ch 1 Input, ESD Level 1	Ch 1 Output, ESD Level 4
B	Depopulated Ball	Ground
C	Ch 2 Input, ESD Level 1	Ch 2 Output, ESD Level 4

DESCRIPTION/ORDERING INFORMATION

The TPD2F702 is a two-channel EMI filter for audio interface applications. With the integration of 5000 pF capacitor in a space saving low noise WCSP package, the TPD2F702 offers superior EMI noise suppression (2MHz to 6GHz) compared to discrete implementation. The device is optimized for AVIF connector or speaker port interfaces. This low-pass filter array also provides system level ESD protection to eliminate the need for external ESD clamps. The TPD2F702 exceeds ±30-kV ratings per IEC6100-4-2 Contact and Air-Gap specifications. It is primarily used in the mobile-phone audio headphone speaker interface, but can be used in other audio applications.

The TPD2F702 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. This filter includes ESD protection circuitry which prevents damage to the application when subjected to ESD surges far exceeding IEC 61000-4-2 (Level 4).

The TPD2F702 is specified for –40°C to 85°C operation.



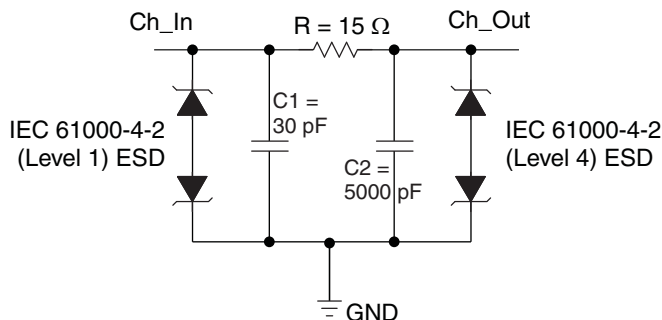
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T _A	PACKAGE ^{(1) (2)}	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	WCSP – YFK Tape and reel	TPD2F702YFKR	5V

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

**SCHEMATIC
(One of Two Channels)**



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V _{IO} Continuous IO voltage	-5.5	5.5	V
Total power dissipation		200	mW
T _A Characterized free-air operating temperature range	-40	85	°C
Reflow temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
V _{IO} Continuous IO voltage	-5	5	V

ESD RATINGS

ESD TYPE	TERMINAL	TYP	UNIT
IEC 61000-4-2 Contact Discharge	Input	±4	kV
	Output	±30	
IEC 61000-4-2 Air-Gap Discharge	Input	±4	kV
	Output	±30	
Human-Body Model	Input	±15	kV
	Output	±15	

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{BR}	DC break-down voltage	I _I = 1 mA	Input pin	±14		±18.2	V
		I _O = 1 mA	Output pin	±14		±18.2	
I _{IO}	Current from input or output	V _I or V _O = 2.5 V	Input, output pins		0.01	0.1	µA
C1	Capacitance of the input terminal	V _I = 0 V, V _{OSC} = 30 mV, f = 100 kHz	Input pin		30		pF
C2	Capacitance of the output terminal	V _O = 0 V, V _{OSC} = 30 mV, f = 100 kHz	Output pin		5000		pF
R	Series resistor			12	15	18	Ω
R _{dyn}	Dynamic resistance	I _I = 1.5 A or I _O = 1.5 A	Output clamp		1		Ω
			Input clamp		3		
f _C	Cut-off frequency	Z _{SOURCE} = 50 Ω, Z _{LOAD} = 50 Ω			1.2		MHz

TYPICAL OPERATING CHARACTERISTICS

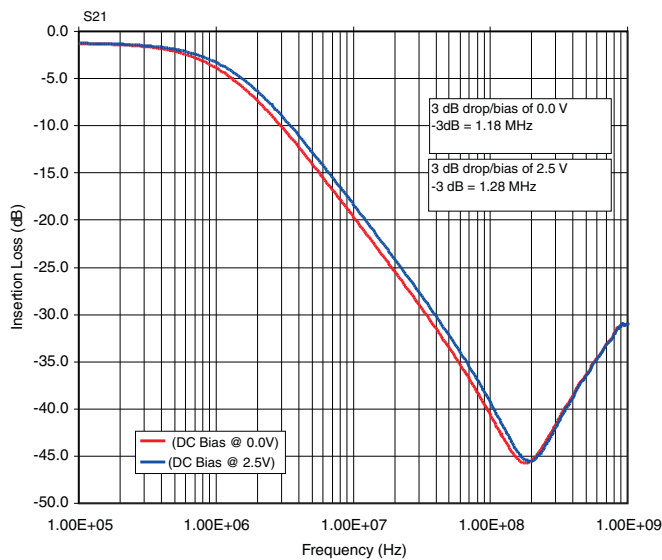


Figure 1. Insertion Loss

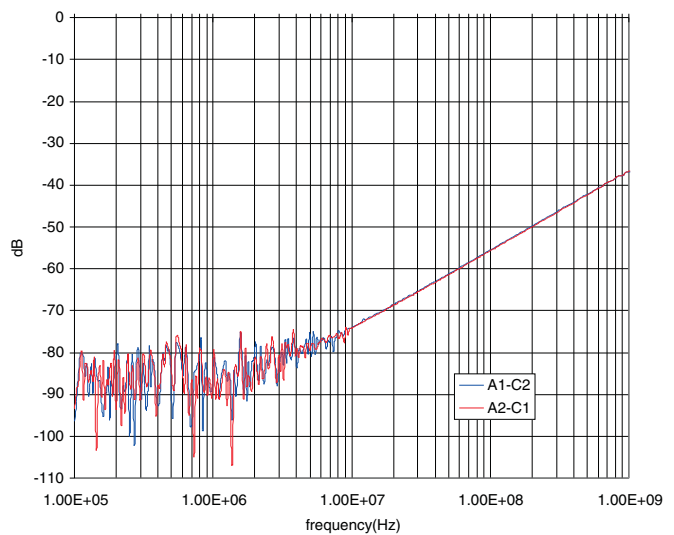


Figure 2. Channel-to-Channel Crosstalk with 50 Ω Termination for the Non-Measuring Pins

TYPICAL OPERATING CHARACTERISTICS (continued)

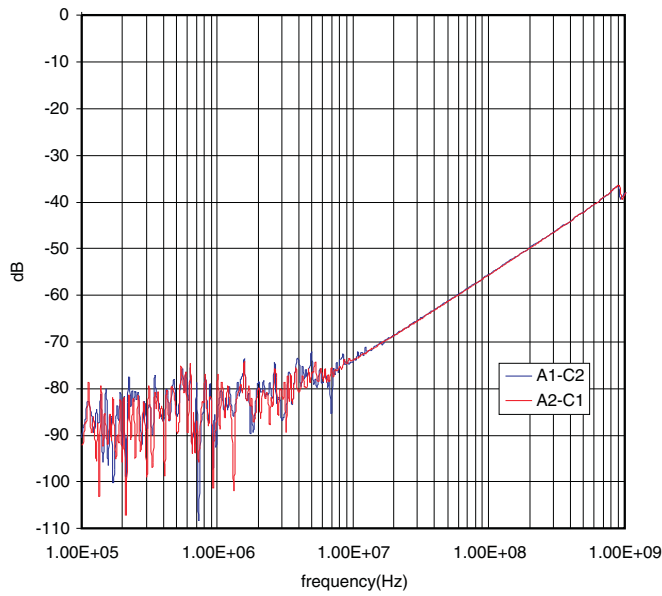


Figure 3. Channel-to-Channel Crosstalk with No Termination for the Non-Measuring Pins

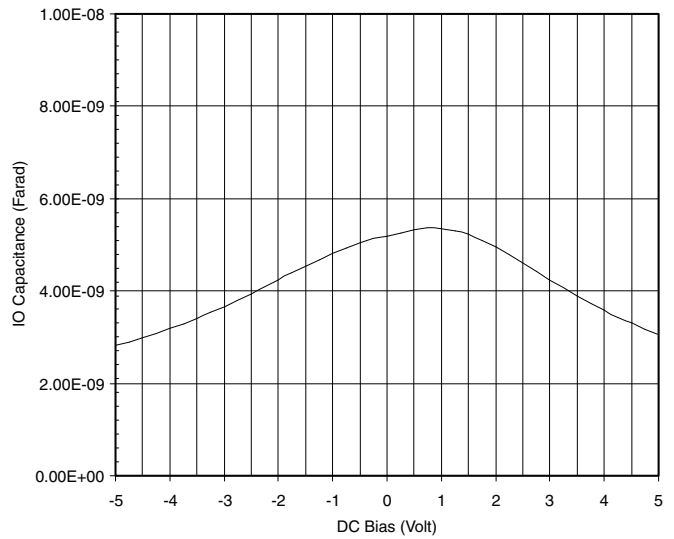


Figure 4. IO Capacitance Versus IO Voltage (Measured at f = 100 kHz)

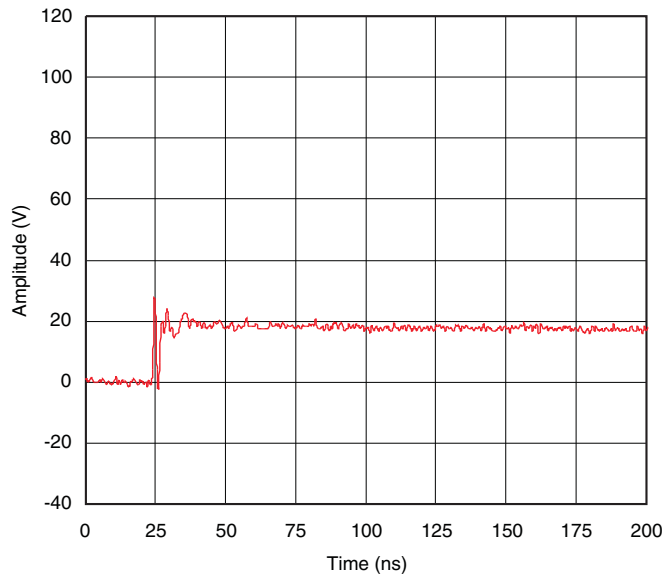


Figure 5. IEC Clamping Waveforms +8 kV Contact, Out Stressed and In Measured

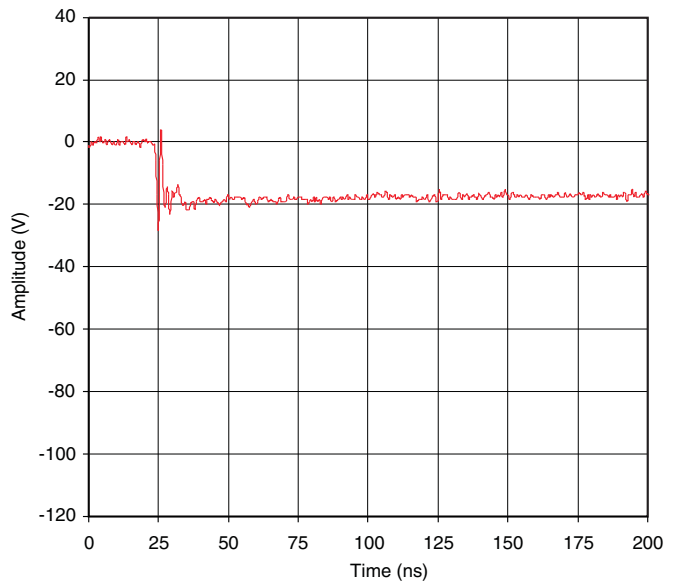


Figure 6. IEC Clamping Waveforms -8 kV Contact, Out Stressed and In Measured

TYPICAL OPERATING CHARACTERISTICS (continued)

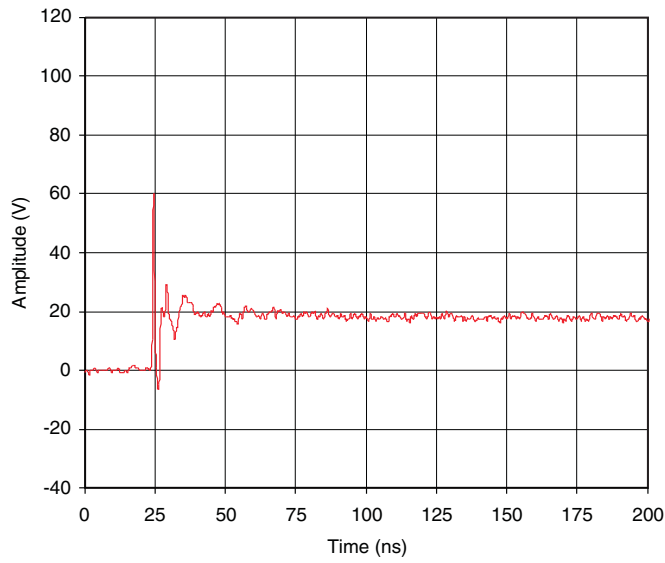


Figure 7. IEC Clamping Waveforms +15 kV Contact, Out Stressed and In Measured

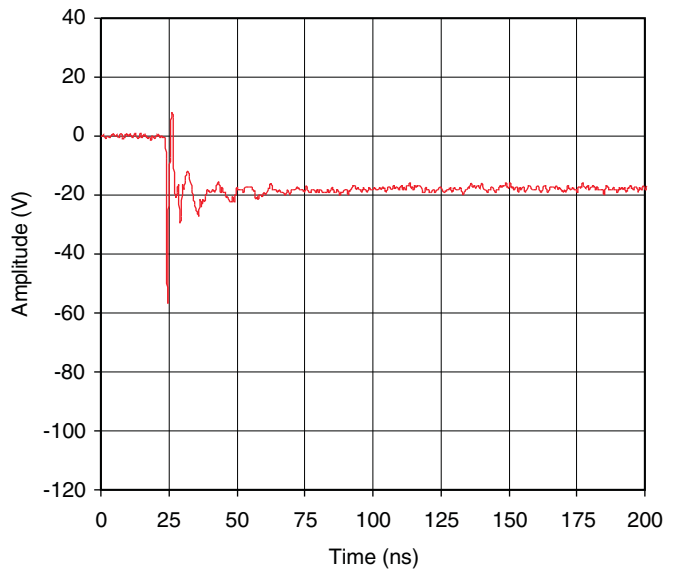


Figure 8. IEC Clamping Waveforms -15 kV Contact, Out Stressed and In Measured

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2F702YFKR	DSBGA	YFK	5	0	180.0	8.4	1.02	1.42	0.62	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



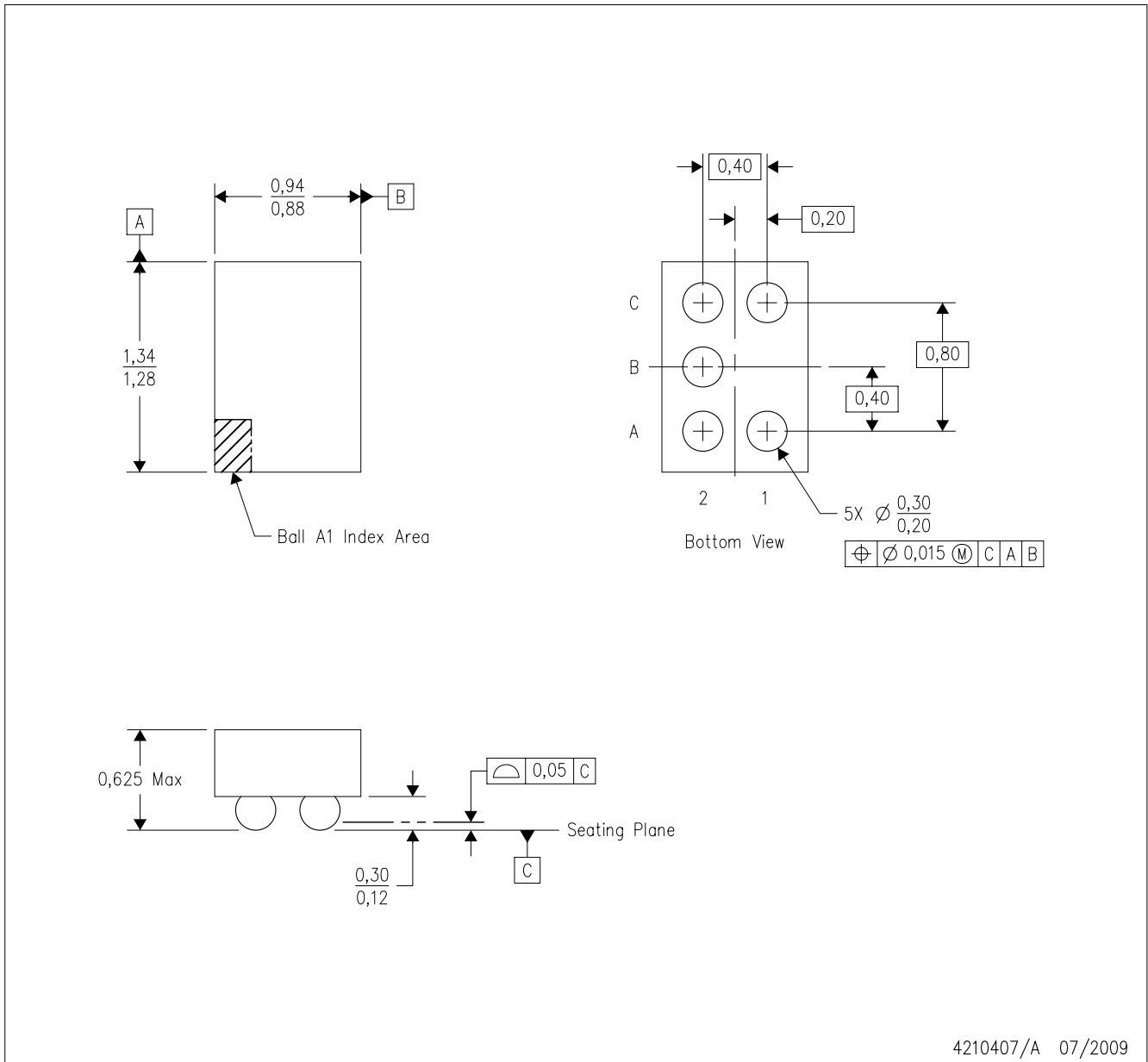
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2F702YFKR	DSBGA	YFK	5	0	210.0	185.0	35.0

MECHANICAL DATA

YFK (R-XBGA-N5)

(CUSTOM) DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This is a Pb-free solder ball design.

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