5V/3.3V D FLIP-FLOP WITH RESET AND DIFFERENTIAL CLOCK

ECL Pro®
SY10EP51V

FEATURES

- **3.3V and 5V power supply options**
- **320ps typical propagation delay**
- **Maximum frequency > 3GHz typical**
- **75KΩ internal input pulldown resistor**
- **Transistor count: 143**
- **Available in 8-Pin (3mmx3mm) MSOP, SOIC and MLF® (2mmx2mm) packages**

ECL Pro®

DESCRIPTION

The SY10EP51V is a D flip-flop with reset and differential clock. The device is pin and functionally equivalent to the EL51 device.

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when CLK is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the CLK. The differential clock inputs of the EP51V allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to V_{EE} and the /CLK input will be biased a $V_{CC}/2$.

PIN NAMES

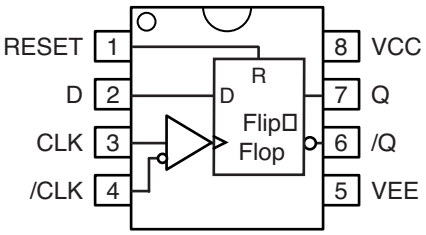
Pin	Function
CLK, /CLK	ECL Clock Inputs
RESET	ECL Asynchronous Reset
D	ECL Data Input
Q, /Q	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

TRUTH TABLE

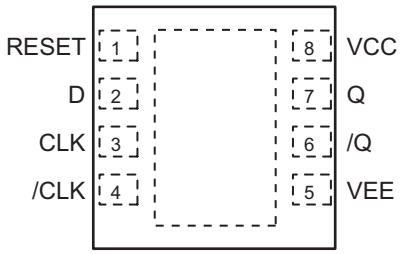
D	RESET	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

PACKAGE/ORDERING INFORMATION



8-Pin SOIC and MSOP Packages



8-Pin (2mmx2mm) MLF®

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10EP51VKC	K8-1	Commercial	HP51	Sn-Pb
SY10EP51VKCTR[2]	K8-1	Commercial	HP51	Sn-Pb
SY10EP51VZC	Z8-1	Commercial	HEP51V	Sn-Pb
SY10EP51VZCTR[2]	Z8-1	Commercial	HEP51V	Sn-Pb
SY10EP51VKI	K8-1	Industrial	HP51	Sn-Pb
SY10EP51VKITR[2]	K8-1	Industrial	HP51	Sn-Pb
SY10EP51VZI	Z8-1	Industrial	HEP51V	Sn-Pb
SY10EP51VZITR[2]	Z8-1	Industrial	HEP51V	Sn-Pb
SY10EP51VKG[3]	K8-1	Industrial	HP51 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP51VKGTR[2, 3]	K8-1	Industrial	HP51 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP51VMGTR[2, 3]	MLF-8	Industrial	H51 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP51VZG[3]	Z8-1	Industrial	HEP51V with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP51VZGTR[2, 3]	Z8-1	Industrial	HEP51V with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
$V_{CC} - V_{EE}$	Power Supply Voltage		6V	V
V_{IN}	Input Voltage (V_{CC} = 0V, V_{IN} not more negative than V_{EE}) Input Voltage (V_{EE} = 0V, V_{IN} not more positive than V_{CC})		–6.0 to 0 +6.0 to 0	V V
I_{OUT}	Output Current	–Continuous –Surge	50 100	mA
T_{LEAD}	Lead Temperature (soldering, 20sec.)		+260	°C
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient)	–Still-Air (SOIC) –500lfpm (SOIC) –Still-Air (MSOP) –500lfpm (MSOP) –Still-Air (MLF®) –500lfpm (MLF®)	160 109 206 155 93 87	°C/W °C/W °C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)	(SOIC) (MSOP) (MLF®)	39 39 60	°C/W

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

5V PECL DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V, V_{EE} = 0V(2)

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current(3)	—	35	40	—	35	40	—	35	40	mA
V_{OH}	Output HIGH Voltage(4)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Outuput LOW Voltage(4)	3050	3190	3315	3050	3255	3380	3050	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3790	—	4115	3855	—	4180	3915	—	4240	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3065	—	3390	3130	—	3455	3190	—	3515	mV
V_{IHCMR}	Input HIGH Voltage(5) Common Mode Range	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.25V to +0.5V.

Note 3. V_{CC} = 0V, V_{EE} = V_{EE} (min.) to V_{EE} (max.), all other pins floating.

Note 4. All loading with 50Ω to V_{CC} –2.0V.

Note 5. V_{IHCMR}(min) varies 1:1 with V_{EE}, V_{IHCMR}(max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

3.3V LVPECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 3.3V, V_{EE} = 0V[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current[3]	—	35	40	—	35	40	—	35	40	mA
V_{OH}	Output HIGH Voltage[4]	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Outuput LOW Voltage[4]	1350	1490	1615	1350	1555	1680	1350	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090	—	2415	2155	—	2480	2215	—	2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365	—	1690	1430	—	1755	1490	—	1815	mV
V_{IHCMR}	Input HIGH Voltage[5] Common Mode Range (Diff.)	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	μA

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary –0.3V to +0.5V.

Note 3. V_{CC} = 0V, V_{EE} = V_{EE}(min.) to V_{EE}(max.), all other pins floating.

Note 4. All loading with 50Ω to V_{CC} –2.0V.

Note 5. V_{IHCMR}(min) varies 1:1 with V_{EE}, V_{IHCMR}(max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NECL/LVECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 0V, V_{EE} = –5.5V to –3.0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current[2]	—	35	40	—	35	40	—	35	40	mA
V_{OH}	Output HIGH Voltage[3]	–1135	–1010	–0885	–1070	–0945	–0820	–1010	–0885	–0760	mV
V_{OL}	Outuput LOW Voltage[3]	–1950	–1810	–1685	–1950	–1745	–1620	–1950	–1685	–1560	mV
V_{IH}	Input HIGH Voltage	–1210	—	–0885	–1145	—	–0820	–1085	—	–0760	mV
V_{IL}	Input LOW Voltage	–1935	—	–1610	–1870	—	–1545	–1810	—	–1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range[4]	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	μA

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. V_{CC} = 0V, V_{EE} = V_{EE}(min) to V_{EE}(max), all other pins floating.

Note 3. All loading with 50Ω to V_{CC} –2.0V.

Note 4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC ELECTRICAL CHARACTERISTICS

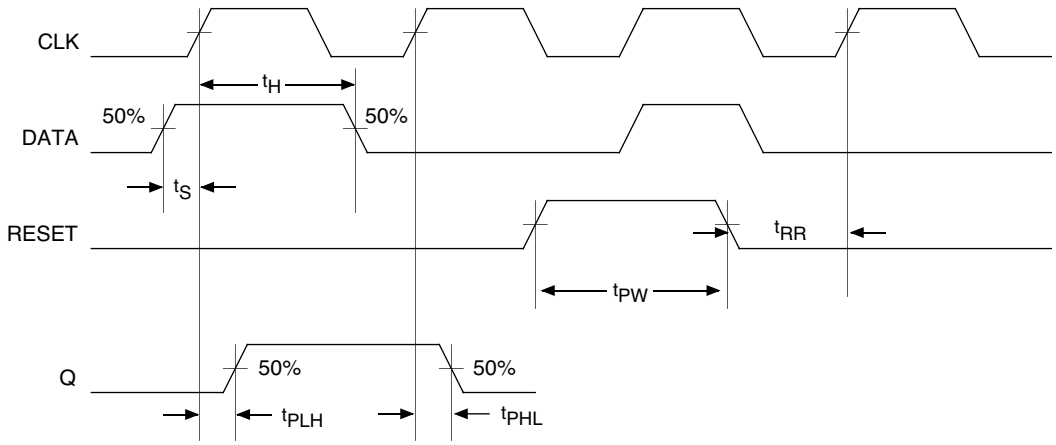
V_{CC} = 0V, V_{EE} = –3.0V to –5.5V; V_{CC} = 3.0V to 5.5V, V_{EE} = 0V[1]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency[2]	3	—	—	3	—	—	3	—	—	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output Differential CLK, /CLK → Q, /Q RESET → Q, /Q	 250 260	 300 310	 350 450	 270 210	 320 320	 370 475	 300 280	 350 320	 420 500	ps
t_{RR}	Reset Recovery	150	—	—	150	—	—	150	—	—	ps
t_S	Setup Time	100	—	—	100	80	—	100	—	—	ps
t_H	Hold Time	100	—	—	100	40	—	100	—	—	ps
t_{PW}	Minimum Pulse Width RESET	500	440	—	500	440	—	500	440	—	ps
t_r t_f	Output Rise/Fall Times Q, /Q (20% to 80%)	70	120	170	80	130	180	100	150	200	ps

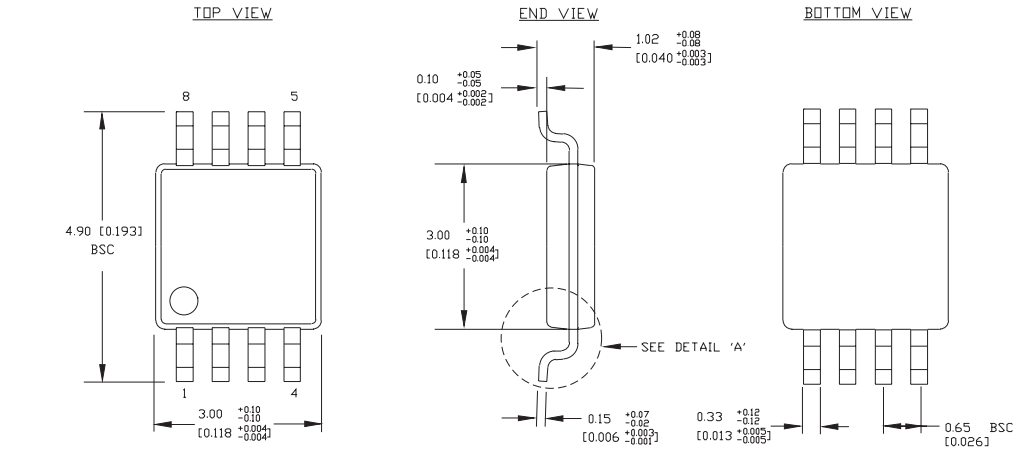
Note 1. Measured using 750mV source, 50% duty cycle clock source. All loading with 50Ω to V_{CC} –2.0V.

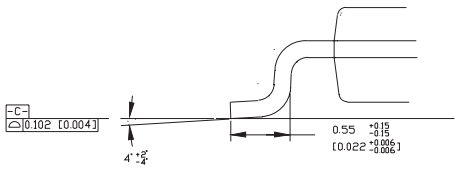
Note 2. f_{MAX} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

TIMING DIAGRAMS



8-PIN MSOP (K8-1)



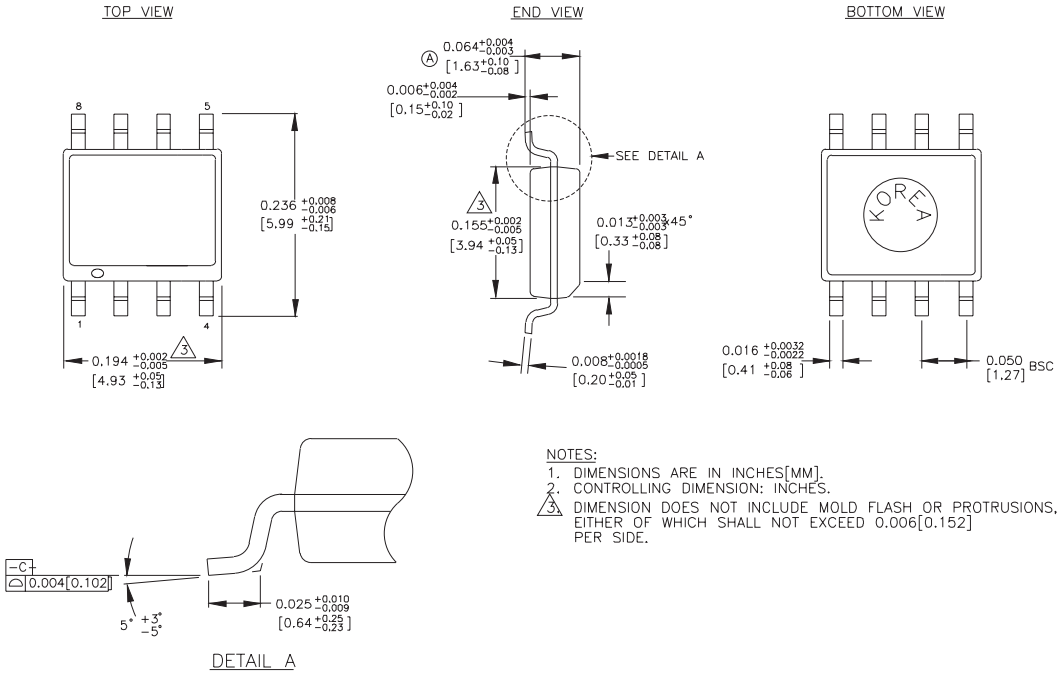


DETAIL A

NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

Rev. 01

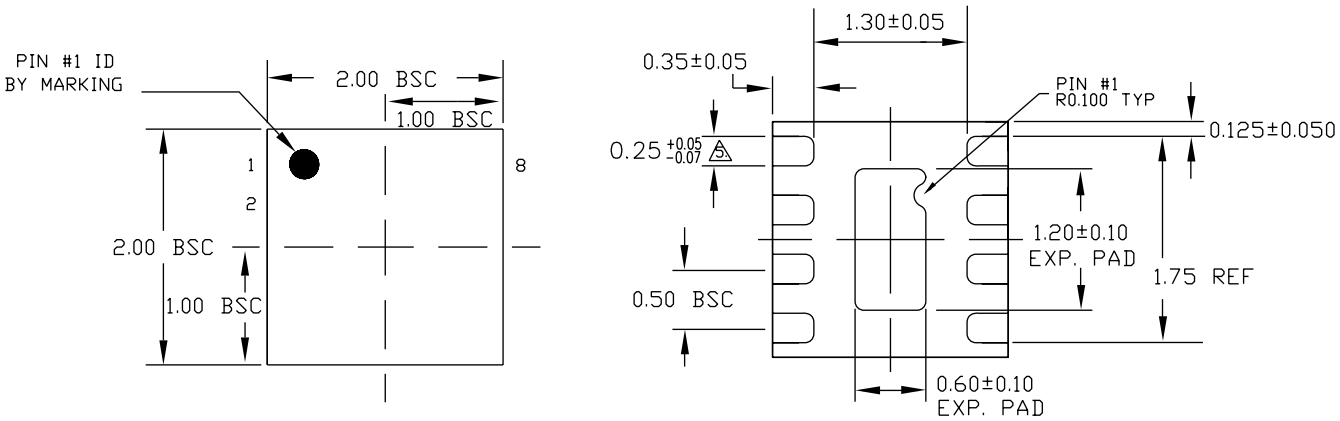
8-PIN PLASTIC SOIC (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

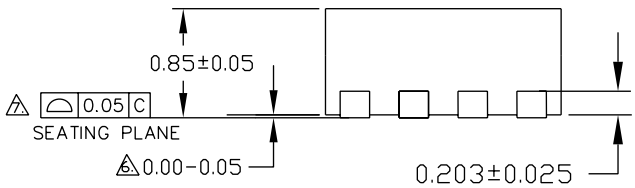
Rev. 03

8-PIN PLASTIC MLF® (MLF-8)



TOP VIEW

BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

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