THE DATASHEET OF

TPS61166DSKR

WHITE LED DRIVER WITH INTEGRATED POWER DIODE AND FAST BURST MODE DIMMING

FEATURES

- **IC Supply Range: 2.5-V to 6-V**
- **Power Stage Input Range: 4.5-V to 10-V**
- **Integrated 1.1-A / 20-V Internal Switch FET and Power Diode**
- **Drive up to 5 LEDs in Series**
- **Fast on/off LED Current Within 1-μs in Brightness Dimming**
- **Burst PWM Dimming Method With Frequency Range From 60-Hz to 40-kHz**
- **Built-in Soft Start-up**
- **Over Load Protection**
- **Over Voltage Protection**
- **2.5 × 2.5 × 0.8 mm SON Package**

APPLICATIONS

- **Small Form Factor LCD Backlight**
- **Mobile Phone**
- **Digital Camera**
- **Personal Camcorder**
- **Single Lens Reflex**

DESCRIPTION

The TPS61166 is a boost converter with a 20-V rated integrated switch FET and power diode that drives up to 5 LEDs in series. This device integrates a high side switch FET that can turn on/off the LED current within 1-μs of the applied external PWM signal. The high side switch also provides input-to-output isolation during IC shutdown.

The default white LED current is set with the external sensor resistor R1, and the feedback voltage is regulated to 200-mV, as shown in the typical application circuit. The LED current can be adjusted using a pulse width modulation (PWM) signal through the PWM pin. The LED current is synchronized to the PWM signal. The device does not discharge the output ceramic capacitor during dimming, thus reducing audible noise when dimming.

Separating the IC input (VIN pin) and power stage input (VBAT pin) makes the device flexible enough to support single- or two-cell Li-ion battery applications. Other protection features include 1.1-A peak-to-peak over current protection (OCP), over voltage protection (OVP), over load protection (OLP), and thermal shutdown. The TPS61166 is available in a 2.5 mm × 2.5 mm SON package with thermal pad.

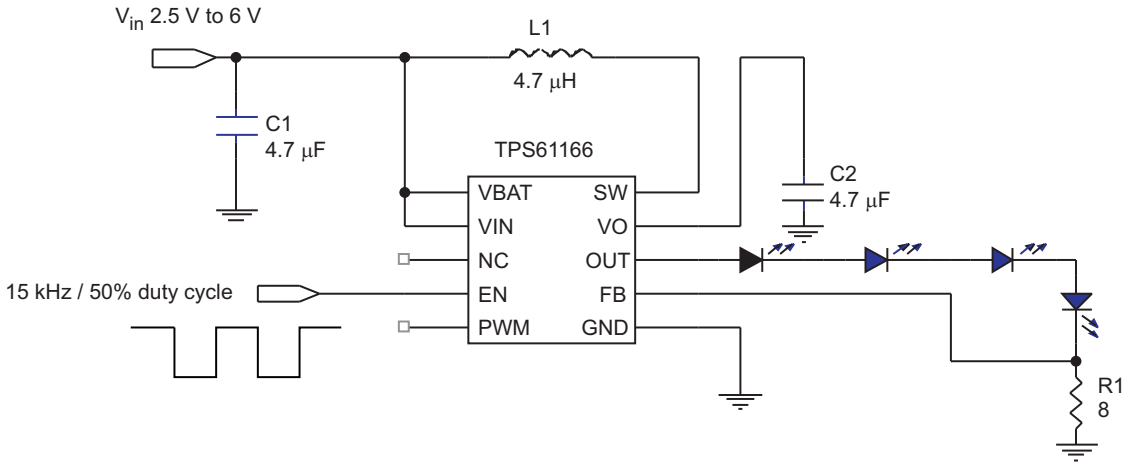


Figure 1. Single Cell Li-Ion Battery Typical Application

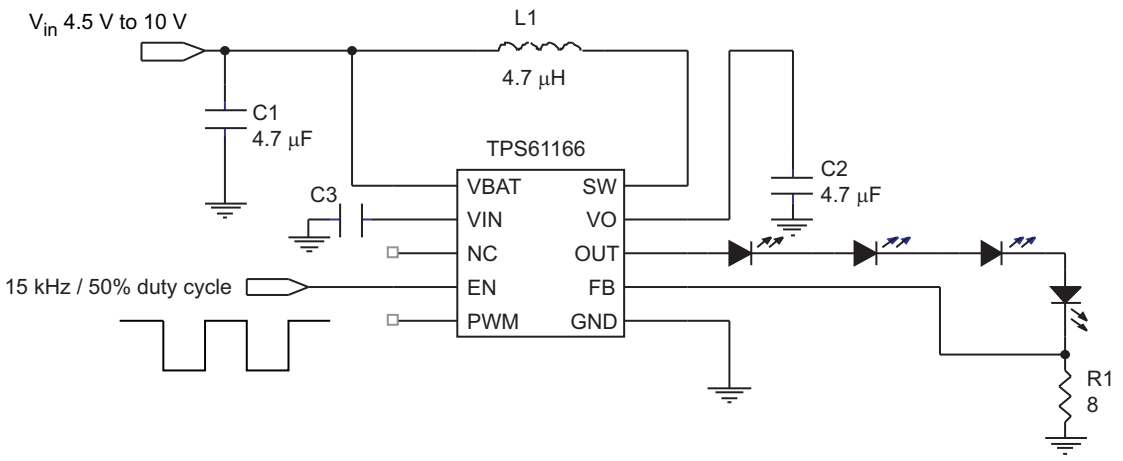


Figure 2. Two Cell Li-Ion Battery Typical Application

ORDERING INFORMATION(1)

PART NUMBER	OVER VOLTAGE PROTECTION	PACKAGE MARKING
TPS61166DSK(2)	18V (TYP)	OAO

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com
(2) The DSK package is available in tape and reel. Add R suffix (TPS61166DSKR) to order quantities of 3000 parts per reel, or add T suffix (TPS61166DSKT) to order 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE / UNITS
Supply voltage on pin VBAT(2)	–0.3 V to 10 V
Voltage on pins VIN, EN, and PWM(2)	–0.3 V to 7 V
Voltage on pins SW, VO, and OUT(2)	–0.3 V to 20 V
Voltage on pin FB(2)	–0.3 V to 3 V
HBM ESD rating (3)	2 kV
Operating temperature range, T_A	–40°C to 85°C
Maximum operating junction temperature, T_J	150°C
Storage temperature, T_{st}	–55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal
(3) The Human body model (HBM) is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The testing is done according JEDECs EIA/JESD22-A114

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE θ_{JA}(1)	THERMAL RESISTANCE θ_{JP}	THERMAL RESISTANCE θ_{JC}	POWER RATING $T_A \le 25°C$(1)	DERATING FACTOR ABOVE $T_A = 25°C$(1)
DSK	60.6°C/W	6.3°C/W	40°C/W	1650 mW	17 mW/°C

(1) Thermal ratings are determined assuming a high K PCB design according to JEDEC standard JESD51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BAT}	Battery input voltage range	4.5		10	V
V_{in}	IC Input voltage range	2.5		6	V
V_o	Output voltage at VO pin			17	V
L	Inductor(1)	2.2	4.7	10	µH
f_{dim}	PWM signal frequency	0.06		40	kHz
C_{in}	Input capacitor	4.7			µF
C_o	Output capacitor at VO pin(1)	1	4.7	10	µF
C3	Pre-regulator capacitor at VIN pin(2)	0.1			µF
T_J	Operating junction temperature	–40		125	°C
T_A	Operating free-air temperature	–40		85	°C

(1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.
(2) For a two cell Li-ion battery application or input supply above 6 V as shown in Figure 2, C3 is needed for the internal pre-regulator. Otherwise, C3 is not needed as shown in Figure 1.

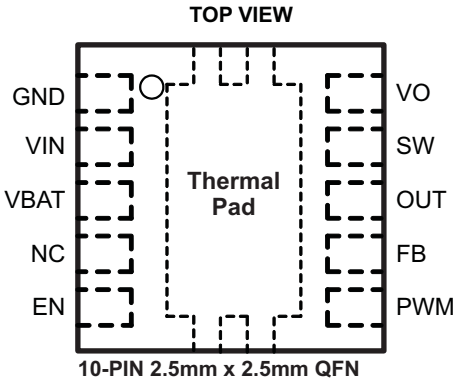
ELECTRICAL CHARACTERISTICS

VIN=3.6V, EN=VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	IC input voltage range, VIN		2.5		6	V
V_{BAT}	Battery input voltage range, VBAT		4.5		10	V
I_Q	Operating quiescent current into VIN	Device PWM switching no load		0.9	1.5	mA
I_{SD}	Shutdown current	EN = GND, VIN = 6 V			1	µA
UVLO	Undervoltage lockout threshold	VIN falling		1.5	1.55	V
V_{hys}	Undervoltage lockout hysterisis			50		mV
ENABLE AND PWM CONTROL						
V_{ENH}	EN and PWM logic high voltage	VIN = 2.5 V to 6 V	1.2			V
V_{ENL}	En and PWM logic low voltage	VIN = 2.5 V to 6 V			0.3	V
R_{EN}	EN and PWM pull down resistor		400	800	1600	kΩ
T_{off}	EN pulse width to shutdown	EN high to low			1	ms
VOLTAGE CONTROL						
V_{REF}	Voltage feedback regulation voltage		194	200	206	mV
I_{FB}	Voltage feedback input bias current				200	nA
f_S	Oscillator frequency		1.0	1.2	1.4	MHz
D_{max}	Maximum duty cycle	V_{FB} = 0.1 V, T_A = 85°C	90%	93%		
T_{min_on}	Minimum on pulse width			65		ns
POWER SWITCH, ISOLATION FET						
$R_{DS(ON)N}$	N-channel MOSFET on-resistance	VIN = 3 V		0.25	0.4	Ω
$R_{DS(ON)iso}$	Isolation FET on-resistance	VO = 5 V		2.5	4	Ω
		VO = 3.5 V		4.5		
I_{LN_N}	N-channel leakage current	V_{DS} = 20 V, T_A = 25°C			1	µA
I_{LN_iso}	Isolation FET leakage current	V_{DS} = 20 V, T_A = 25°C			1	µA
V_F	Power diode forward voltage	Current = 500 mA		0.8		V
OC, ILIM, OVP SC AND SS						
I_{LIM}	N-Channel MOSFET current limit		0.9	1.1	1.5	A
V_{ovp}	Over voltage protection threshold	Measured on the VO pin	18	19		V
V_{ovp_hys}	Over voltage protection hysteresis			0.6		V
I_{OL}	Over load protection		200	300		mA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			150		°C
$T_{hysteresis}$	Thermal shutdown hysteresis			15		°C

DEVICE INFORMATION

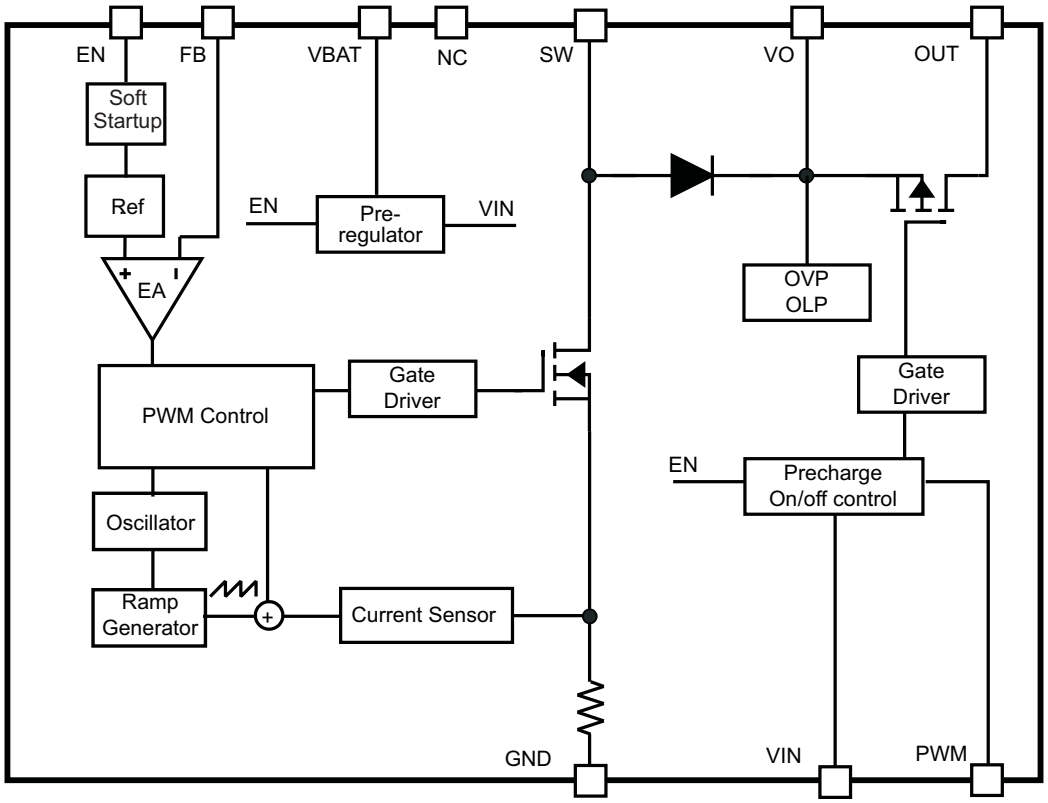
PIN ASSIGNMENTS



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	2	I	IC Supply voltage input.
VO	10	O	Output of the boost converter. When the output voltage exceeds the over voltage protection (OVP) threshold, the power switch turns off until VO drops below the over voltage protection hysteresis.
OUT	8	O	Isolation switch is between this pin and the VO pin. Connect the anode of the LED to this pin.
GND	1	–	Ground of the IC.
VBAT	3	I	Battery supply voltage input. It can be tied with VIN pin when using a signal Li-ion battery.
EN	5	I	Enable pin (HIGH = enable). When the pin is pulled low for 1 ms, the IC turns off and consumes less than 1-µA current. For a 2-cell battery application, a logic high signal turns on the internal pre-regulator and enables the IC. Therefore, do not connect the EN pin to the VIN pin in the Figure 2 application.
PWM	6	I	Control LED on/off. A PWM signal from 60 Hz to 40 kHz connects to the pin for LED brightness control.
FB	7	I	Cathode of the LED connects to this pin. Its voltage is regulated at 0.2 V. An external resistor connected to this pin programs the LED current.
SW	9	I	Switching node of the IC where the PWM switching operates.
NC	4	–	No connect pin. Connect to ground is recommended, or can float.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

(Figure 1), L = TOKO #A915_Y-4R7M, VIN = 3.6 V, LOAD = 4 LEDS unless otherwise noted			FIGURE
η	LED Efficiency	vs Led current; Five LEDs (14.5 V)	3
η	LED Efficiency	vs Led current; Four LEDs (11.5 V)	4
η	LED Efficiency	vs Led current; Three LEDs (8.5 V)	5
V_{FB}	FB voltage	vs Input voltage	6
V_{FB}	FB voltage	vs VBAT voltage	7
V_{FB}	FB voltage	vs Free-air temperature	8
	Switch current limit	vs Free-air temperature	9
	PWM dimming operation	1 kHz with 30% duty cycle	10
	PWM dimming operation	15 kHz with 10% duty cycle	11
	PWM switch operation	15 kHz with 10% duty cycle	12
	PWM dimming linearity	100 Hz, 1 kHz, 40 kHz;	13
	PWM dimming linearity (zoom in)	100 Hz, 1 kHz, 40 kHz;	14
	Over voltage protection		15
	Soft start up in PWM dimming		16
	Soft start up with EN and PWM tied together		17

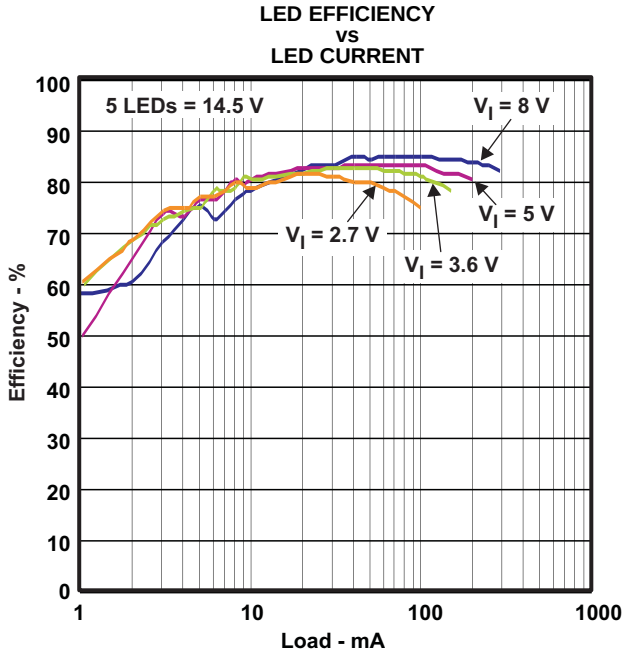


Figure 3.

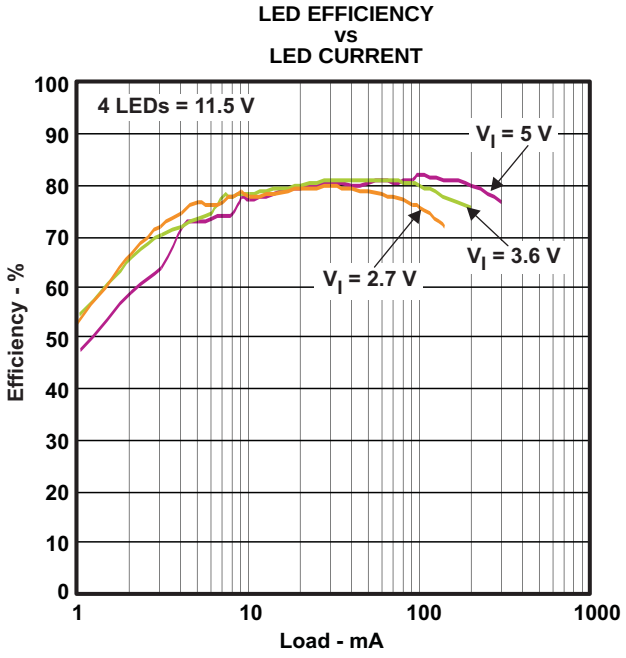


Figure 4.

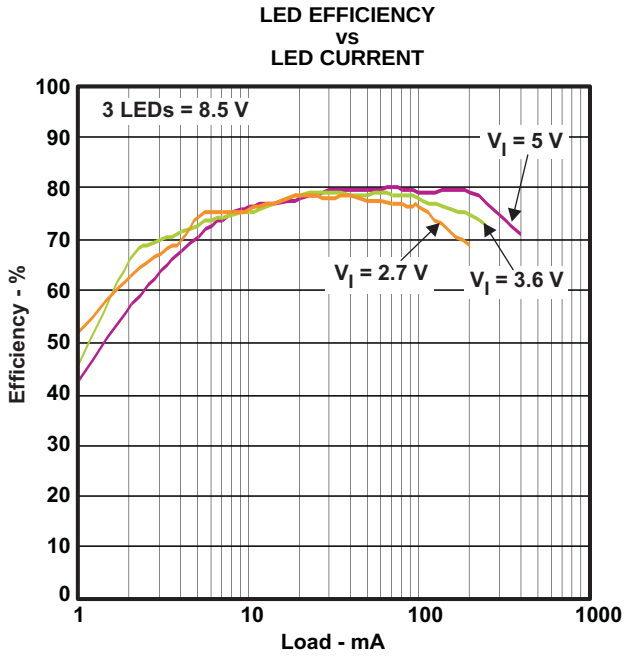


Figure 5.

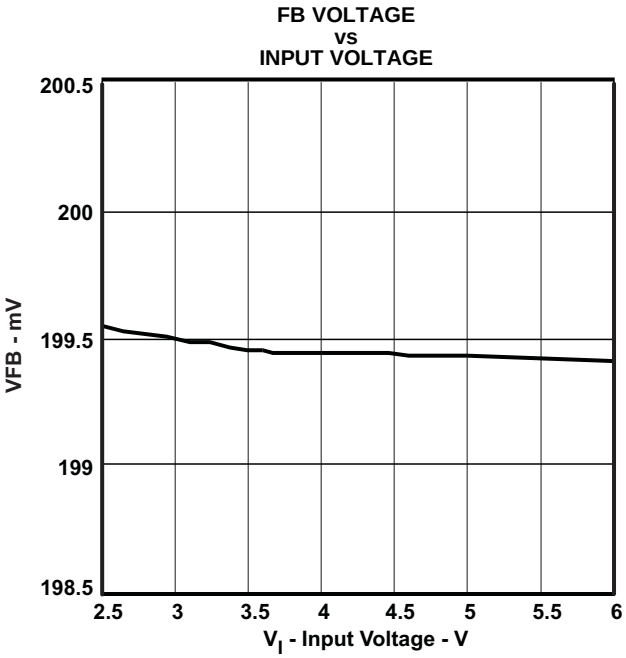


Figure 6.

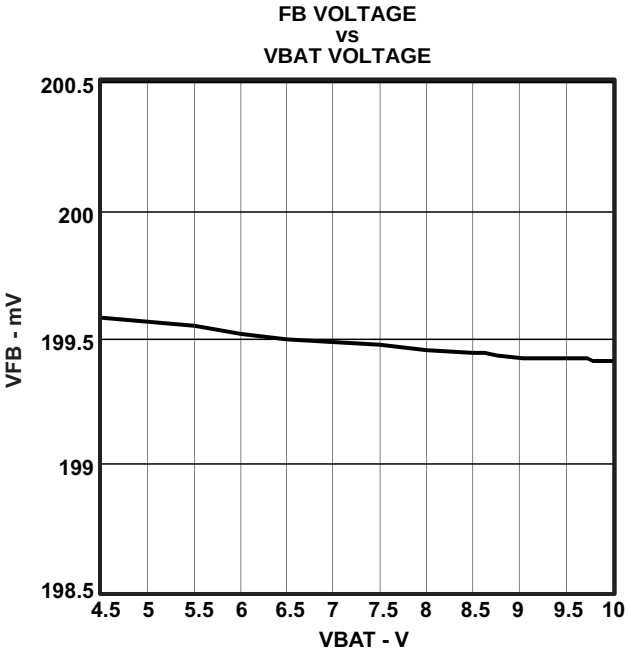


Figure 7.

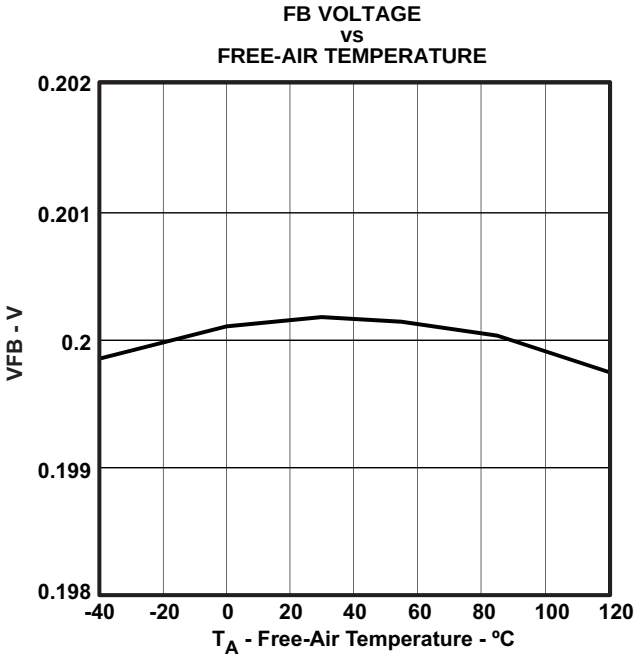


Figure 8.

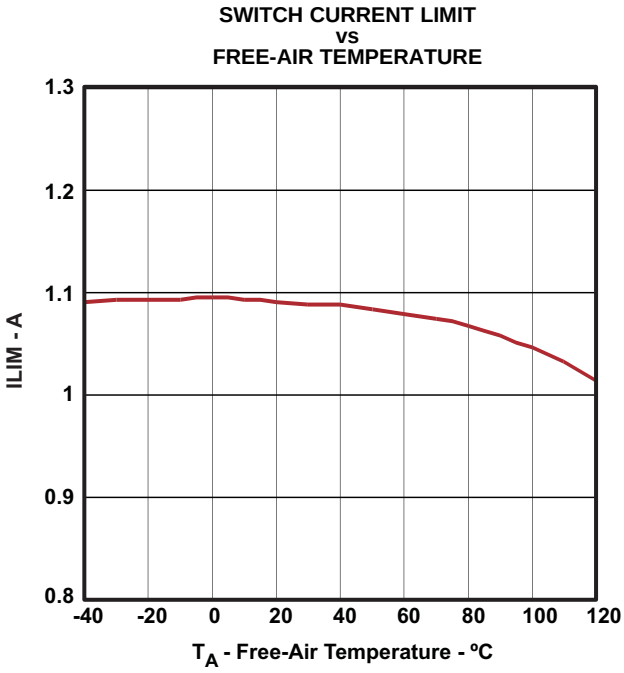


Figure 9.

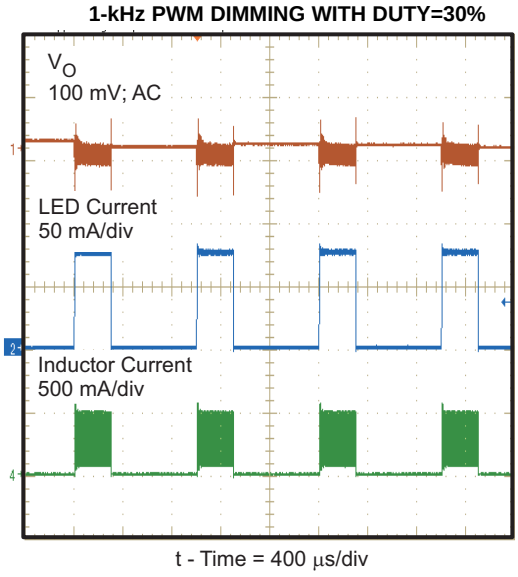


Figure 10.

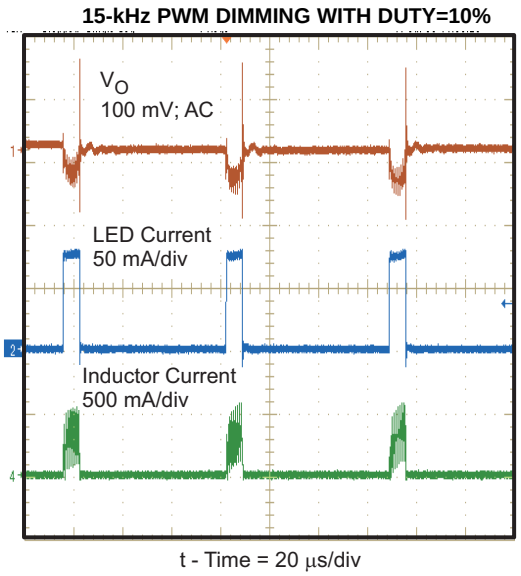


Figure 11.

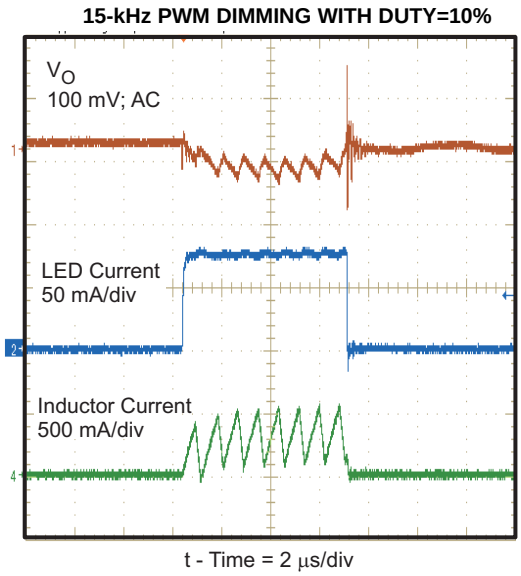


Figure 12.

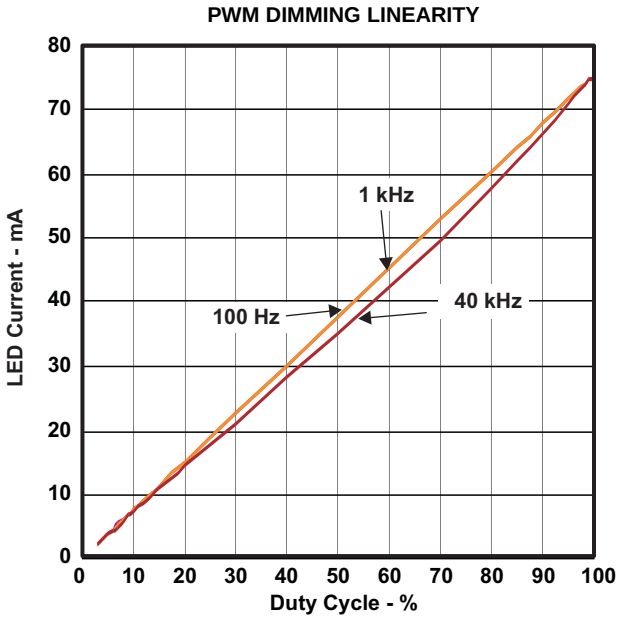


Figure 13.

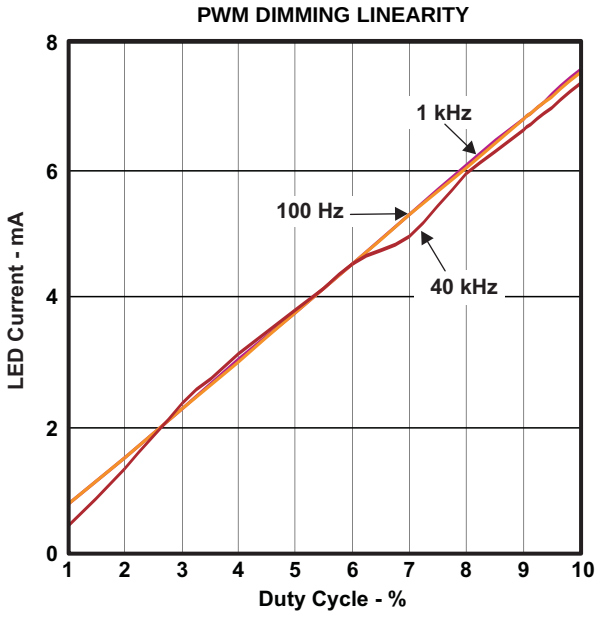


Figure 14.

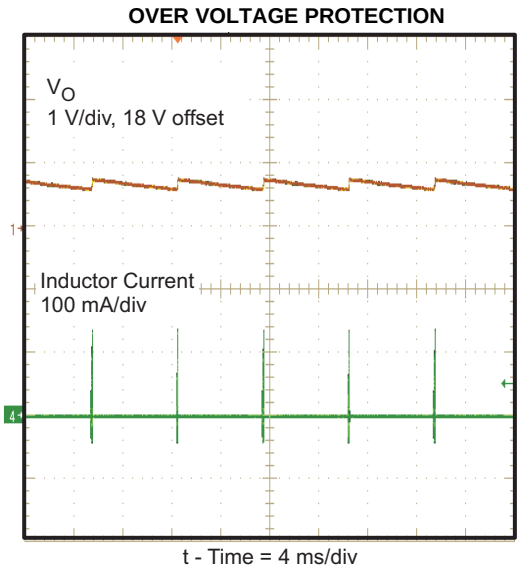


Figure 15.

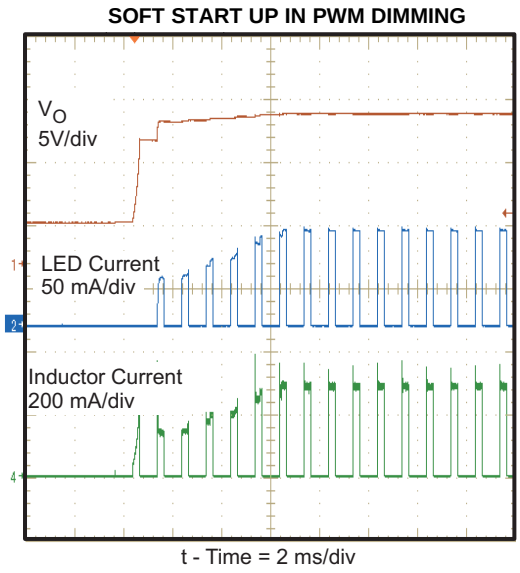


Figure 16.

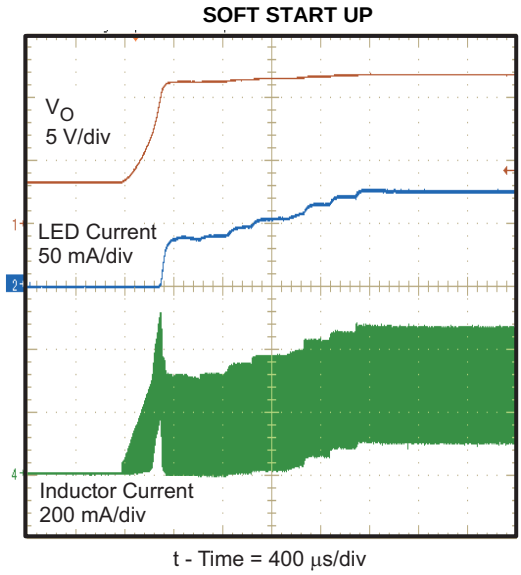


Figure 17.

DETAILED DESCRIPTION

OPERATION

The TPS61166 adopts peak current-mode control with a constant pulse-width-modulation (PWM) frequency of 1.2-MHz. PWM operation turns on the PWM switch at the beginning of each switching cycle. The input voltage is applied across the inductor and the inductor current ramps up. In this mode, the output capacitor is discharged by the load current. When the inductor current hits the threshold set by the error amplifier output, the PWM switch is turned off, and the power diode is forward-biased. The inductor transfers its stored energy to replenish the output capacitor. This operation repeats in the next switching cycle. The error amplifier compares the FB pin voltage with an internal reference, and its output determines the duty cycle of the PWM switching. This closed-loop system requires frequency compensation for stable operation. The device has a built-in compensation circuit that can accommodate a wide range of input and output voltages. To avoid the sub-harmonic oscillation intrinsic to current-mode control, the IC also integrates the slope compensation, which adds an artificial slope to the current ramp.

The device integrates a high side switch FET between the VO pin and the OUT pin to turn LEDs on/off quickly. The LED current is synchronous with the external PWM signal that is applied to the PWM pin. The delay between the PWM signal and the rising/falling edge of the LED current is less than 1-µs. The IC's isolation switch prevents the output capacitor from discharging during dimming, thus reducing the ceramic output capacitor's audible noise to neglible levels.

STARTUP AND SHUTDOWN

The TPS61166 starts to turn on the isolation FET and PWM switch when the EN pin is pulled high. In the boost power stage, the IC ramps up the over-current limit of the PWM switch to 1.1-A in 8 steps, and each step takes 213-µs. This ensures that the VO pin voltage rises slowly to reduce input inrush current. The Vgs of the isolation switch is self-clamped by the VO pin voltage, so that the high on-resistance of the switch during startup limits the output current.

When the EN pin is pulled low for 1-ms, the IC stops the PWM switch and turns off the isolation switch, providing isolation between input and output. In the shutdown mode, less than 1-µA input current is consumed by the IC.

UNDER VOLTAGE LOCKOUT (UVLO), OVER LOAD PROTECTION (OLP), AND OVER VOLTAGE PROTECTION (OVP)

An under voltage lockout circuit prevents improper operation of the device for input voltages below 1.55-V. When the input voltage is below the undervoltage threshold, both the PWM switch and isolation switch remain off.

If the current passing through the isolation switch is above the over load limit of 300-mA (I_{OL},typ) for 1.5-µs, the TPS61166 is switched off until the fault clears and the EN pin toggles. Over load protection is disabled until the over current limit ramp is completed during startup.

To prevent the PWM switch and the output capacitor from exceeding maximum voltage ratings, an over votlage protection circuit turns off the boost switch as soon as the output voltage at the VO pin exceeds the OVP threshold. Simultaneously, the isolation switch opens. The regulator resumes PWM switching after the VO pin voltage falls 0.6 V below the threshold. This function provides protection for open LED protection as well.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the isolation and PWM switches when the typical junction temperature of 150°C is exceeded. The thermal shutdown has a hysteresis of 15°C, typical.

APPLICATION INFORMATION

SWITCH DUTY CYCLE

The maximum switch duty cycle (D) of the TPS61166 is 90% (MIN). The duty cycle of a boost converter in continuous conduction mode (CCM) is given by:

$$D = \frac{Vout + 0.8\ V - Vin}{Vout + 0.8\ V} \quad (1)$$

where Vout = $\sum V_{FWD(LED)}$+200mV. The duty cycle must be lower than the specification in the application; otherwise the output voltage cannot be regulated.

LED CURRENT PROGRAMMING

The FB voltage is regulated to a low 0.2-V reference voltage. LED current is programmed externally using a current sense resistor R1 in series with the LED string. The value of R1 is calculated using Equation 2:

$$I_{LED} = \frac{200\ mV}{R1} \quad (2)$$

The output current tolerance depends on FB accuracy and current sensor resistor accuracy. Maximum LED current can be calculated using Equation 3.

$$I_{out\_MAX} = (I_{LIM} - \frac{\Delta I_L}{2}) \times (1 - D)$$

$$\Delta I_L = \frac{1}{\left[L \times f_{SW} \times \left(\frac{1}{VO + 0.8\ V - VIN} + \frac{1}{VIN}\right)\right]} \quad (3)$$

Where

ΔI_L = Inductor peak to peak current;
L = Selected inductor value;
f_{SW} = Converter switching frequency (typically 1.2-MHz);

For instance, the TPS61166 can support 4 LEDs (equivalent output voltage of 14-V) with 160-mA output current at 3.3-V input supply at typical conditions.

LED BRIGHTNESS DIMMING

A PWM signal applied to the PWM pin can adjust the LED brightness. The signal controls whether the isolation switch is on or off; therefore LED current is directly proportion to the duty cycle of the PWM signal. During the on periods, LED current is defined by the value as described in Equation 2.

The recommended PWM signal frequency range is 60-Hz to 40-kHz. The IC needs several µ-seconds to settle the LED current after the isolation switch turns on. This settling time affects the LED current linearity at low duty cycle. A 1% duty cycle is the minimum recommended duty cycle for a PWM dimming signal with 1-kHz frequency, and 0.1% is recommended for a 100-Hz frequency.

The isolation switch ON time determines the maximum PWM frequency. The ON time must be at least twice as long as one switch cycle of $2/f_{s(max)}$ = 2/1.4MHz = 1.2-µs. A PWM dimming frequency above 40 kHz may be acceptable, but needs to be fully tested by the user.

INDUCTOR SELECTION

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications: inductor value, saturation current, and dc resistance. Considering inductor value alone is not enough.

The saturation current of the inductor should be higher than the peak switch current as calculated in the following equations:

$$I_{L\_peak} = I_{L\_DC} + \frac{\Delta I_L}{2}$$

$$I_{L\_DC} = \frac{Vout \times Iout}{Vin \times \eta} \quad (4)$$

Where

I_{L_DC} = Inductor average current
η = Estimated converter efficiency

The inductor value should not be outside the 2.2 µH to 10 µH range listed in the recommended operating conditions table, otherwise internal slope compensation and loop compensation are ineffective.Table 1 lists the recommended inductors for the TPS61166.

Table 1. Recommended Inductors for the TPS61166

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L×W×H mm)	VENDOR
#A915_Y-4R7M	4.7	45	1.5	5.2x5.2x3.0	Toko
#A915_Y-100M	10	90	1.09	5.2x5.2x3.0	Toko
VLS4012-4R7M	4.7	132	1.1	4.0x4.0x1.2	TDK
VLS4012-100M	10	240	0.82	4.0x4.0x1.2	TDK
CDRH3D23/HP	4.7	95.5	1.6	4.0x4.0x2.5	Sumida
LPS4012-472ML	4.7	175	1.6	4.0x4.0x1.2	Coilcraft

INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by Equation 5:

$$C_{out} = \frac{D \times I_{out}}{Fs \times V_{ripple}} \quad (5)$$

where, V_{ripple} = peak to peak output ripple. The ESR impact on the output ripple must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging, and ac signal. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The dc bias can also significantly reduce capacitance. A ceramic capacitor can loose as much as 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage.

At least a 4.7-µF input capacitor is recommended. The output requires a capacitor in the range of 1 µF to 10 µF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

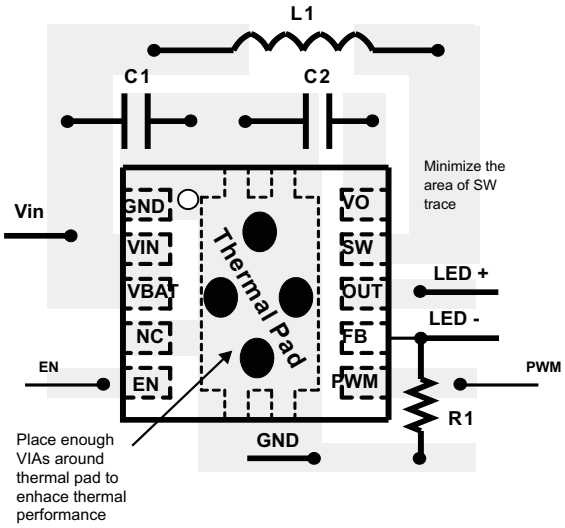
The popular vendors for high value ceramic capacitors are:

- TDK (http://www.component.tdk.com/components.php)
- Murata (http://www.murata.com/cap/index.html)

LAYOUT CONSIDERATIONS

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully performed, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of

high frequency noise (e.g., EMI), proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. The high current path including the switch and output capacitor contains nanosecond rise and fall times and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple.



THERMAL CONSIDERATIONS

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61166. Calculate the maximum allowable dissipation, $P_{D(MAX)}$ and keep the actual dissipation less than or equal to $P_{D(MAX)}$. The maximum-power-dissipation limit is determined using Equation 6:

$$P_{D(MAX)} = \frac{125°C - T_A}{R_{\theta JA}} \quad (6)$$

where

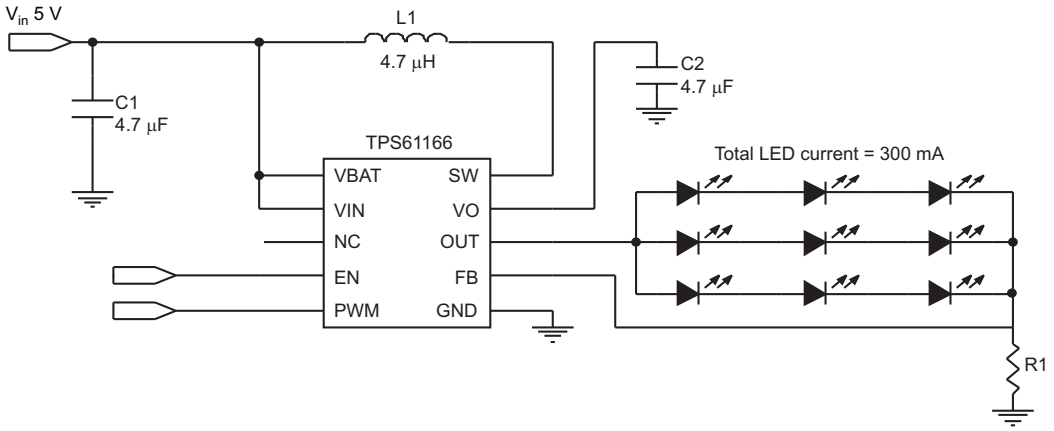
T_A = Maximum ambient temperature for the application.

$R_{\theta JA}$ = Thermal resistance junction-to-ambient listed in the dissipation ratings table.

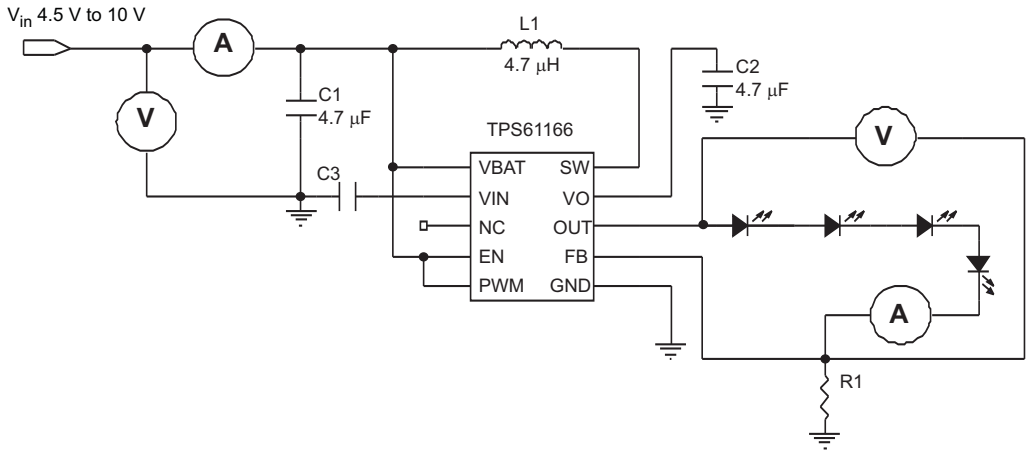
The TPS61166 is available in a thermally enhanced QFN package. This package includes a thermal pad that improves the thermal capabilities of the package. The $R_{\theta JA}$ of the QFN package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered to the analog ground on the PCB. Using thermal vias underneath the thermal pad as illustrated in the layout example. Also, see the QFN/SON PCB Attachment application report (SLUA271).

ADDITIONAL APPLICATION

Multiple LED Strings Bar Application



LED Efficiency Measurement Application



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61166DSKR	ACTIVE	SON	DSK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	OAO	Samples
TPS61166DSKT	ACTIVE	SON	DSK	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	OAO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

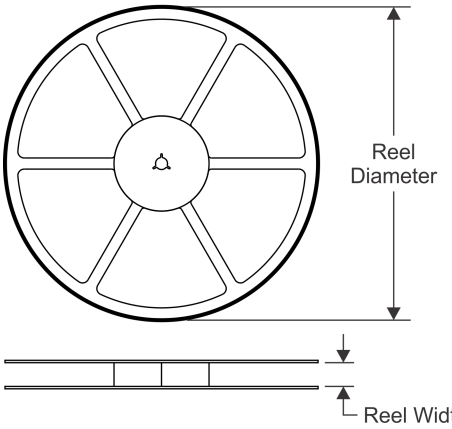
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

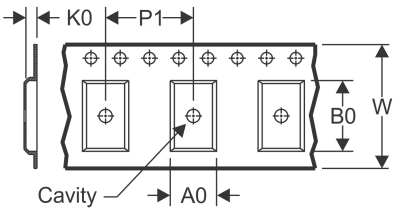
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

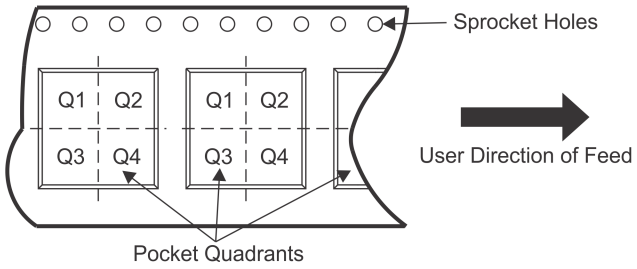


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

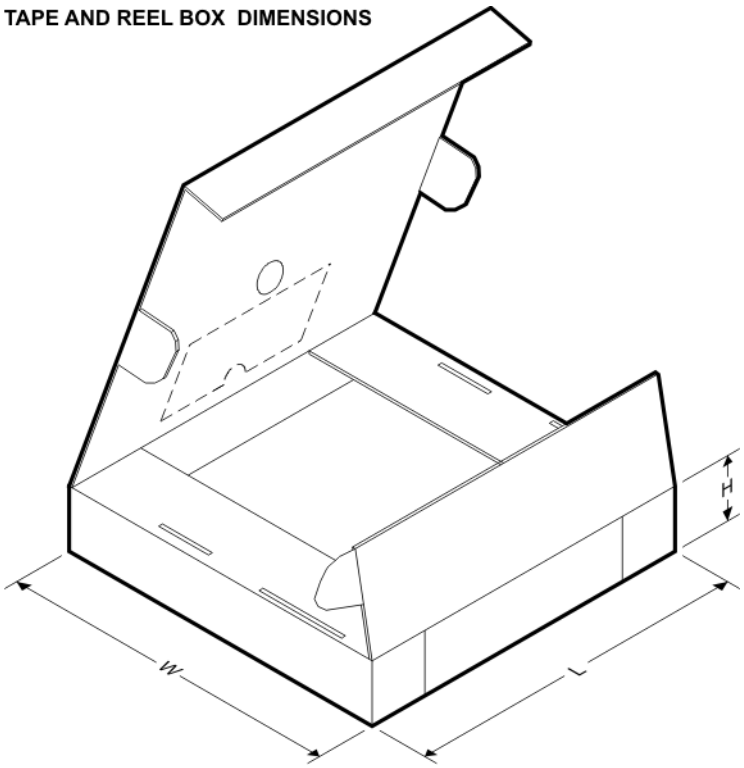
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61166DSKR	SON	DSK	10	3000	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS61166DSKT	SON	DSK	10	250	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2

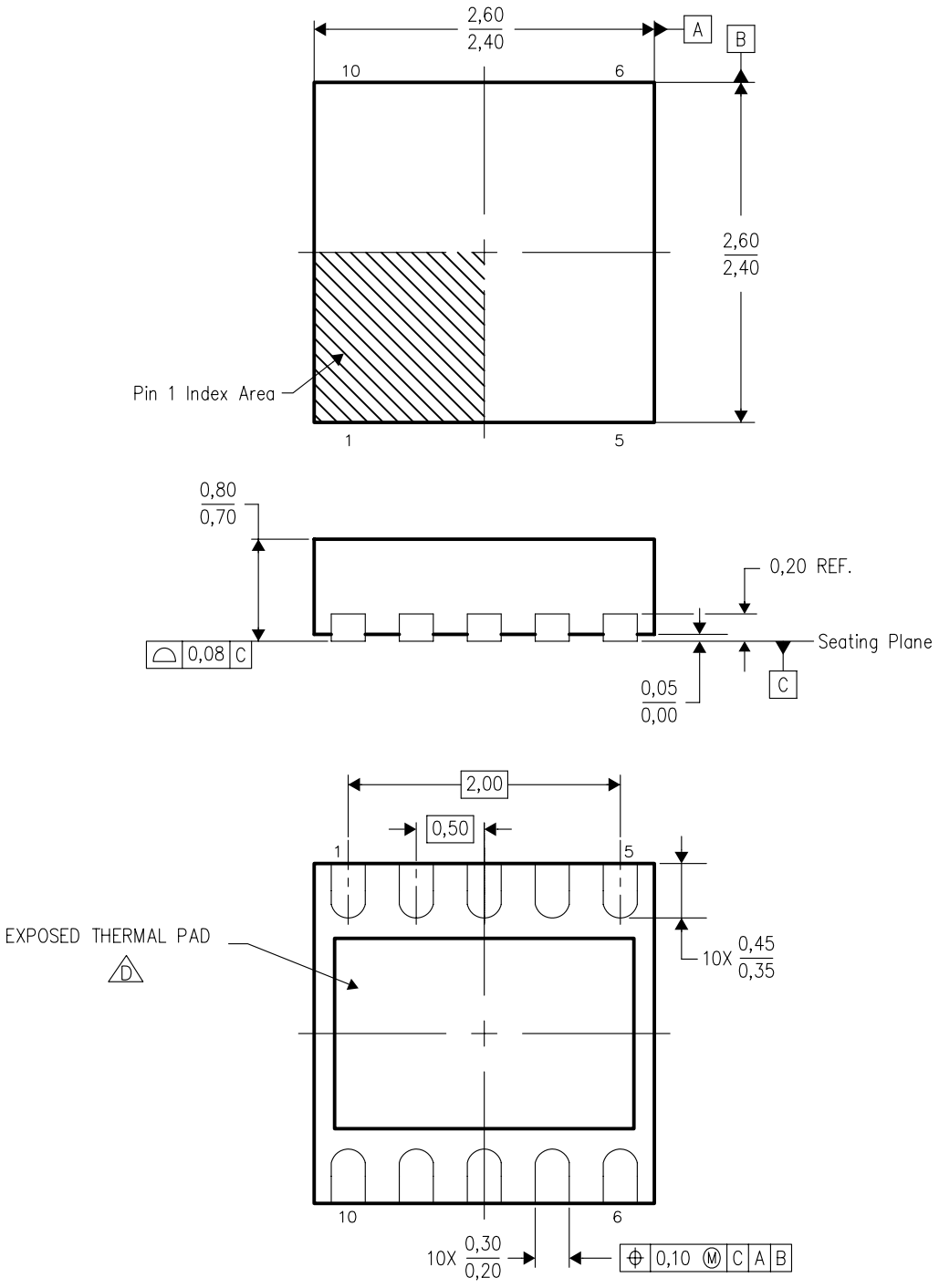
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61166DSKR	SON	DSK	10	3000	203.0	203.0	35.0
TPS61166DSKT	SON	DSK	10	250	203.0	203.0	35.0

DSK (S–PDSO–N10) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

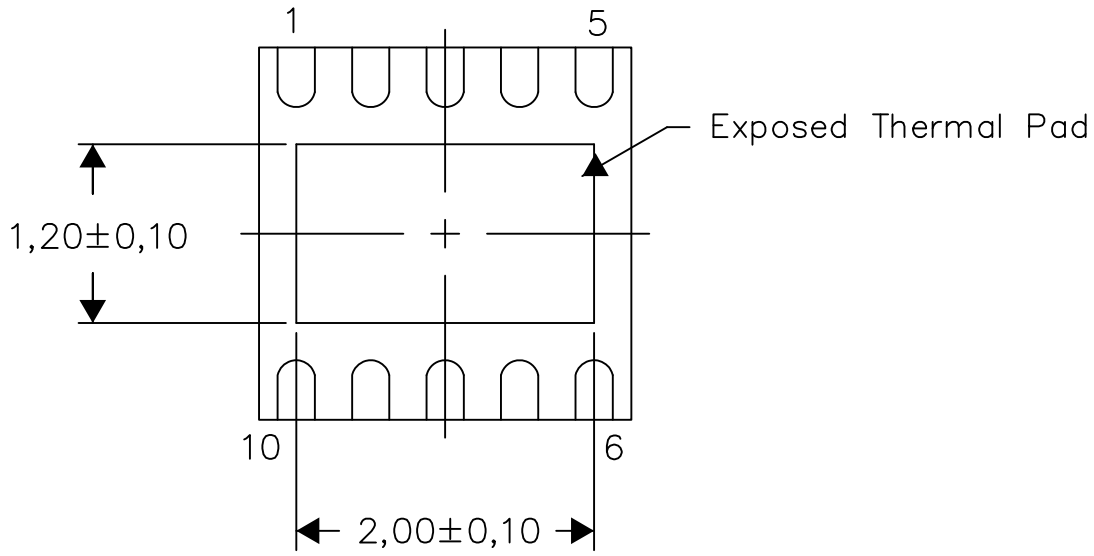
DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



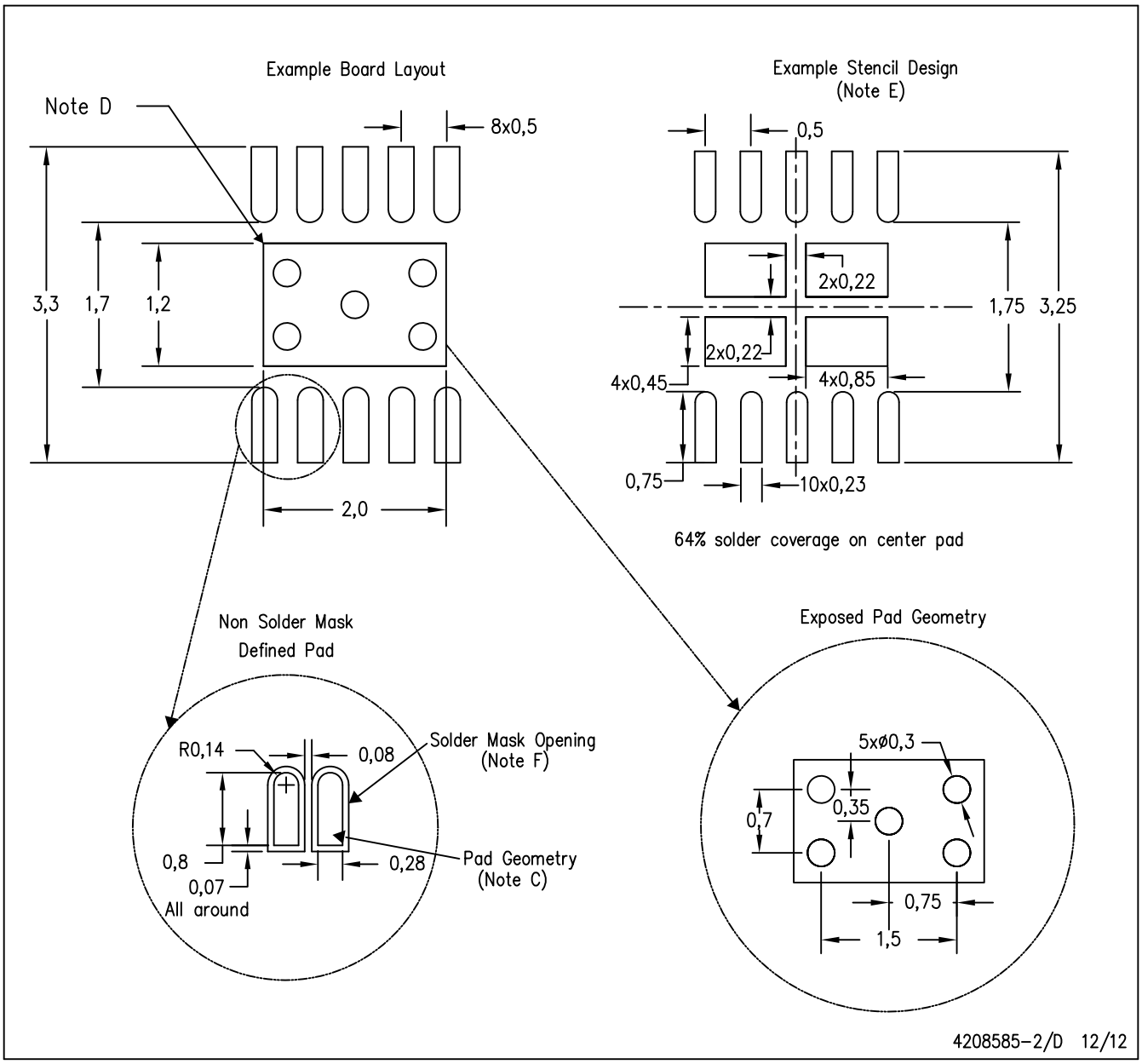
Bottom View

Exposed Thermal Pad Dimensions

4208579–2/E 12/12

NOTE: All linear dimensions are in millimeters

DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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