

LMH2191 Dual Channel 52 MHz Clock Tree Driver

Check for Samples: [LMH2191](#)

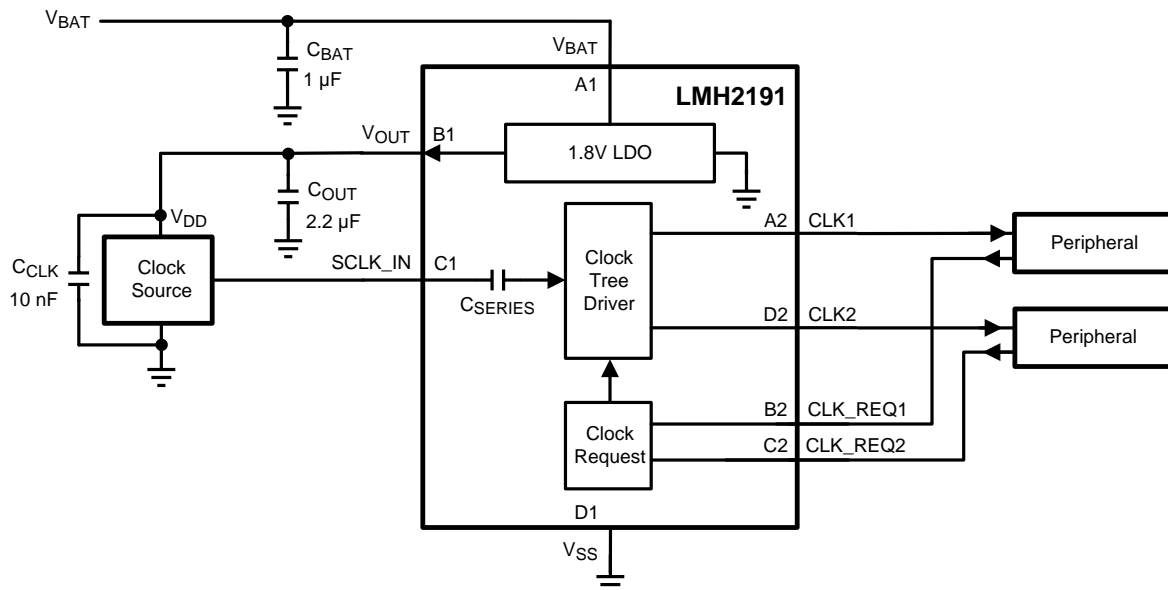
FEATURES

- One Input Clock, Two Output Clocks
- 1.8V Square Wave Clock Outputs
- Inverted Clock Outputs
- Independent Clock Requests
- High Isolation of Supply Noise to Clock Input
- High Output-to-Output Isolation
- Integrated 1.8V Low-Dropout Regulator
 - Low Output-Noise Voltage
 - 10 mA Load Current
- EMI Filtering
- Ultra Low Standby Current
- V_{BAT} Range = 2.5V to 5.5V
- 8-Bump DSBGA Package

APPLICATIONS

- Mobile Handsets
- Portable Equipment

Typical Application



DESCRIPTION

The LMH2191 is a dual-channel clock tree driver that supplies a digital system clock to peripherals in mobile handsets or other applications. It provides a solution to clocking issues such as limited drive capability for fanout or longer traces. It also provides protection of the master clock from varying loads and frequency pulling effects, isolation from noisy modules, and crosstalk isolation. It has very low phase noise which enables it to drive sensitive modules such as Wireless LAN and Bluetooth.

The LMH2191 can be clocked up to 52 MHz and has an independent clock request pin for each clock output which allows the peripheral to control the clock. It features an integrated LDO which provides an ultra low-noise voltage supply with 10 mA external load current which can be used to supply the TCXO or other clock source. The LMH2191 dual clock distributor is offered in a tiny 1.61 mm x 1.063 mm 8-bump DSBGA package. Its small size and low supply current make it ideal for portable applications.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage	$V_{BAT} - V_{SS}$	-0.3V to 6V
	LVC MOS port IO voltage	-0.3V to ($V_{OUT} + 0.3V$)
ESD Tolerance ⁽³⁾	Human Body Model	2000V
	Machine Model	200V
	Charge Device Model	1000V
Output Short Circuit Duration ⁽⁴⁾	LDO	infinite
	Clock Output	infinite
For Soldering Information see http://www.ti.com/lit/SNOA549		
Storage Temperature Range		-65°C to 150°C
Junction Temperature ⁽⁵⁾		150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the Electrical Characteristics Tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human body model, applicable std. MIL-STD-883, Method 3015.7. Machine model, applicable std. JESD22–A115–A (ESD MM std of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22–C101–C. (ESD FICDM std. of JEDEC)
- (4) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

OPERATING RATINGS⁽¹⁾

Supply Voltage ($V_{BAT} - V_{SS}$)		2.5V to 5.5V
Input Clock, SCLK_IN	Frequency	10 MHz to 52 MHz
	Duty Cycle	45% to 55%
Temperature Range		-40°C to +85°C
Package Thermal Resistance θ_{JA} ⁽²⁾		Board specification: 4LCELLPHONE
Package YFX		153 °C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the Electrical Characteristics Tables.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3.5 V ELECTRICAL CHARACTERISTICS⁽¹⁾

Unless otherwise specified, all limits are specified at $T_J = 25^\circ\text{C}$, $V_{\text{BAT}} = 3.5\text{V}$, $C_{\text{BAT}} = 1\mu\text{F}$, $C_{\text{OUT}} = 2.2\mu\text{F}$ ⁽²⁾, $f_{\text{SCLK_IN}} = 26\text{ MHz}$, $I_{\text{OUT}} = 1\text{ mA}$, **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min ⁽³⁾	Typ ⁽⁴⁾	Max ⁽³⁾	Units
Supply Current⁽⁵⁾⁽⁶⁾						
I_{DD}	Supply Current	Active Mode SCLK_IN = 19.2 MHz; both clock outputs toggling; C_{LOAD} CLK1/2 = 0pF; $I_{\text{OUT}} = 0\text{mA}$		1.4	1.65 1.7	mA
		Active Mode SCLK_IN = 19.2 MHz; both clock outputs toggling; C_{LOAD} for CLK1/2 = 33.5pF; $I_{\text{OUT}} = 0\text{mA}$		3.7	4.45 4.50	mA
		Active Mode SCLK_IN = 26 MHz, both clock outputs toggling, C_{LOAD} for CLK1/2 = 0pF, $I_{\text{OUT}}=0\text{mA}$		1.9	2.15 2.25	mA
		Active Mode SCLK_IN = 26 MHz, both clock outputs toggling, C_{LOAD} for CLK1/2 = 33.5 pF, $I_{\text{OUT}}=0\text{mA}$		5	5.80 5.95	mA
		In shutdown. Input clock not active. CLK_REQ1/2=Low		0.1	1	μA
		In shutdown. Input clock toggling. CLK_REQ1/2=Low		0.1	1	μA
C_{PD}	Power Dissipation Capacitance per CLK output	C_{LOAD} for CLK1,2 = 0pF, Defined with respect to $V_{\text{OUT}} = 1.8\text{V}$		20	23.0 24.0	pF
Clock Outputs (CLK1/2) Figure 1, Figure 2						
$t_{\text{PD_LH}}$	Propagation Delay - Low to High	50% to 50%; $C_{\text{LOAD}} = 33\text{ pF}$; measured on CLK1		6.1	10.5	ns
$t_{\text{PD_HL}}$	Propagation Delay - High to Low	50% to 50%; $C_{\text{LOAD}} = 33\text{ pF}$; measured on CLK1		6.1	10.5	
t_{SKEW}	Skew Between Outputs (Either Edge)	CLK1 to CLK2. 50% to 50%		1.5	3.1	
t_{RISE}	Rise Time ⁽⁷⁾	For C_L between 33.5 pF - 50 pF, 20% to 80%; typical value based on 40 pF load	2.1	3.7	5.9	ns
t_{FALL}	Fall Time ⁽⁷⁾	For C_L between 33.5 pF - 50 pF, 20% to 80%; typical value based on 40pF load	2	3.5	5	
CLK_DC	Output Clock Duty Cycle	For C_L between 33.5 pF - 50 pF	42	50	58	%
Jitter _{RMS}	Additive RMS period Jitter	$f_{\text{SCLK_IN}} = 26\text{ MHz}$, BW = 100 Hz to 1MHz	CLK1		95	fs
			CLK2		110	

- (1) Electrical Table values apply only for factory testing (ATE) conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
- (2) C_{BAT} , C_{OUT} : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
- (3) Limits are 100% production tested at 25°C. Limits over temperature range are specified through correlations using statistical quality control (SQC) method.
- (4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (5) Supply current depends on switching frequency and load.
- (6) Positive current is current flowing into the device.
- (7) This parameter is specified by design and/or characterization and is not tested in production.

3.5 V ELECTRICAL CHARACTERISTICS⁽¹⁾ (continued)

Unless otherwise specified, all limits are specified at $T_J = 25^\circ\text{C}$, $V_{\text{BAT}} = 3.5\text{V}$, $C_{\text{BAT}} = 1\mu\text{F}$, $C_{\text{OUT}} = 2.2\mu\text{F}$ ⁽²⁾, $f_{\text{SCLK_IN}} = 26\text{MHz}$, $I_{\text{OUT}} = 1\text{mA}$, **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min ⁽³⁾	Typ ⁽⁴⁾	Max ⁽³⁾	Units		
CLK1 Phase Noise	Additive Phase Noise	All outputs enabled at 26 MHz	f = 100 Hz		-128		dBc/Hz	
			f = 1 kHz		-144			
			f = 10 kHz		-150			
			f = 100 kHz		-160			
			f = 1 MHz		-163			
		All outputs enabled at 19.2 MHz	f = 100 Hz		-127			
			f = 1 kHz		-146			
			f = 10 kHz		-153			
			f = 100 kHz		-161			
			f = 1 MHz		-163			
CLK2 Phase Noise	Additive Phase Noise	All outputs enabled at 26 MHz	f = 100 Hz		-127		dBc/Hz	
			f = 1 kHz		-142			
			f = 10 kHz		-148			
			f = 100 kHz		-160			
			f = 1 MHz		-162			
		All outputs enabled at 19.2 MHz	f = 100 Hz		-129			
			f = 1 kHz		-144			
			f = 10 kHz		-151			
			f = 100 kHz		-163			
			f = 1 MHz		-164			
V_{OH}	CLK1/2 Output Voltage High Level	$I_{\text{OH}} = -2\text{mA}$ (equivalent output load 800 Ω)	1.6			V		
V_{OL}	CLK1/2 Output Voltage Low Level	$I_{\text{OL}} = 2\text{mA}$			0.2			
R_{OFF}	Output Impedance when disabled	with other output enabled (LDO enabled)	grounded					
		Both outputs disabled (LDO disabled)	diode to ground					
System Clock Input (SCLK_IN)								
$V_{\text{I-pp}}$	SCLK_IN peak- to- peak input level ⁽⁷⁾	For duty cycle variation < 1%	0.6	1	1.8	V		
I_{IH}	Current into SCLK_IN pin (Input HIGH)	SCLK_IN = 1.8V, CLK_REQ1/2=Low		0	0.1	μA		
I_{IL}	Current into SCLK_IN pin (Input LOW)	SCLK_IN = 0V, CLK_REQ1/2=Low	-0.1	0				
C_{IN}	Input Capacitance ⁽⁸⁾	CLK_REQ1/2=High		7.5	13	pF		
R_{IN}	Input Resistance ⁽⁸⁾	CLK_REQ1/2=High see Application Note: Input Impedance		14	20	k Ω		
Switching Characteristics: System Clock Input								
$f_{\text{SCLK_IN}}$	System Clock		10	26	52	MHz		
CLK_DC	Input Clock Duty Cycle		45	50	55	%		

(8) This parameter is specified by design and/or characterization and is not tested in production.

3.5 V ELECTRICAL CHARACTERISTICS⁽¹⁾ (continued)

Unless otherwise specified, all limits are specified at $T_J = 25^\circ\text{C}$, $V_{\text{BAT}} = 3.5\text{V}$, $C_{\text{BAT}} = 1\mu\text{F}$, $C_{\text{OUT}} = 2.2\mu\text{F}$ ⁽²⁾, $f_{\text{SCLK_IN}} = 26\text{ MHz}$, $I_{\text{OUT}} = 1\text{ mA}$, **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min ⁽³⁾	Typ ⁽⁴⁾	Max ⁽³⁾	Units	
Clock Request Inputs (CLK_REQ1/2)							
t_{SET}	Setup Time from CLK_REQx to SCLK_IN, to enable CLKx (Figure 3)		12	6.2		ns	
V_{IH}	CLK_REQ1/2 logic HIGH input level. (clock output = ON) ⁽⁹⁾	$V_{\text{BAT}} = 2.5\text{V}$	1.4			V	
		$V_{\text{BAT}} = 3.5\text{V}$	1.4				
		$V_{\text{BAT}} = 5.5\text{V}$	1.4				
V_{IL}	CLK_REQ1/2 logic LOW input level. (clock output = OFF)	$V_{\text{BAT}} = 2.5\text{V}$			0.4	V	
		$V_{\text{BAT}} = 3.5\text{V}$			0.4		
		$V_{\text{BAT}} = 5.5\text{V}$			0.4		
I_{IH}	Current into CLK_REQ pin	$V_{\text{IH}} = 1.8\text{V}$, 200 k Ω pull down resistor (Input HIGH)		8.5	14	μA	
I_{IL}	Current into CLK_REQ pin	$V_{\text{IL}} = V_{\text{SS}}$, (Input LOW)	-0.2	0		μA	
LDO							
V_{OUT}	Output Voltage	$I_{\text{OUT}} = 1\text{ mA}$	1.73	1.8	1.88	V	
I_{LOAD}	Load Current ⁽¹⁰⁾	$V_{\text{OUT}} > 1.7\text{V}$	0		10	mA	
V_{DO}	Dropout Voltage ⁽¹¹⁾	$I_{\text{OUT}} = 10\text{ mA}$ $V_{\text{out}} = 1.7\text{V}$		125		mV	
I_{SC}	Short Circuit Current Limit			300		mA	
PSRR	Power Supply Rejection Ratio	V_{BAT} ripple = 200 mV _{PP} , $I_{\text{OUT}} = 10\text{ mA}$	$f = 100\text{ Hz}$		92		dB
			$f = 217.5\text{ Hz}$		90		
			$f = 1\text{ kHz}$		78		
			$f = 10\text{ kHz}$		60		
			$f = 100\text{ kHz}$		50		
			$f = 1\text{ MHz}$		50		
			$f = 3.25\text{ MHz}$		42		
E_{N}	Output Noise Voltage ⁽¹²⁾	BW = 10 Hz to 100 kHz, CLK_REQ1/2=High, Input clock not active		18		μV_{RMS}	
T_{SHTDWN}	Thermal Shutdown	Temperature		160		$^\circ\text{C}$	
		Hysteresis		20			
ΔV_{OUT}	Line Transient	$V_{\text{BAT}} = 2.8\text{V}$ to 3.4V in $30\mu\text{s}$, $I_{\text{OUT}} = 1\text{ mA}$	-1			mV	
		$V_{\text{BAT}} = 3.4\text{V}$ to 2.8V in $30\mu\text{s}$, $I_{\text{OUT}} = 1\text{ mA}$			1		
	Load Transient	$I_{\text{OUT}} = 0\text{ mA}$ to 10 mA in $10\mu\text{s}$	-15				mV
		$I_{\text{OUT}} = 10\text{ mA}$ to 0 mA in $10\mu\text{s}$			10		
	Overshoot on Startup				20	mV	
R_{OUT}	DC Output Resistance			5		Ω	
T_{ON}	Turn on Time	From rising edge of CLK_REQ1 to 95% of $V_{\text{OUT}}(\text{NOM})$		200	260 350	μs	

(9) Clock Request Inputs can tolerate logic high input levels up to V_{BAT} .

(10) The device maintains stable, regulated output voltage without a load.

(11) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

(12) The noise figure is the noise of the LDO only; harmonics of the output clocks are excluded.

TIMING DIAGRAMS

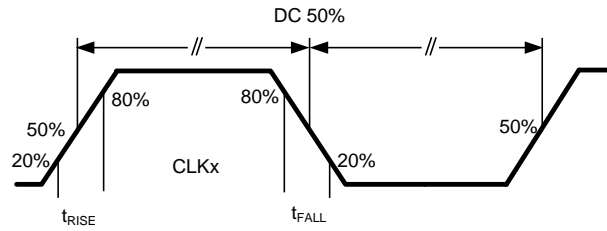


Figure 1. Rise / Fall time and Duty Cycle Waveform for Clock Outputs

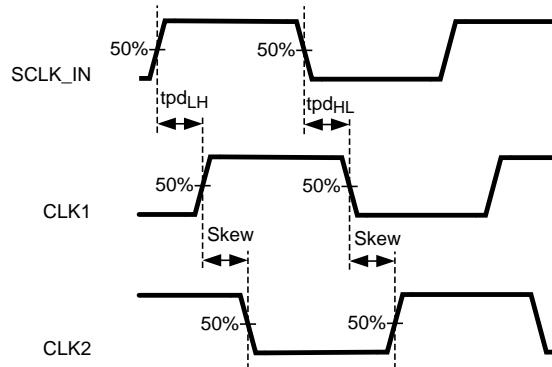


Figure 2. Clock Output Timing Waveforms

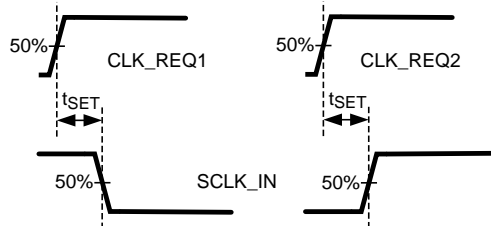


Figure 3. Clock Request Timing Waveforms

Connection Diagram

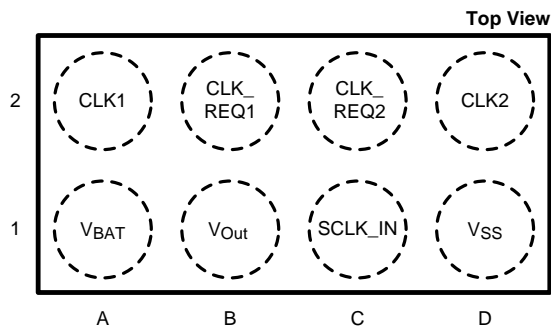


Figure 4. 8-Bump DSBGA
See YFX0008 Package

PIN DESCRIPTIONS

Pin	Pin Name	Port / Direction	Type ⁽¹⁾	Description
C1	SCLK_IN	Host	Input	Source Clock Input
A2	CLK1	Peripheral	Output	Clock Output 1
B2	CLK_REQ1	Peripheral	Input	Clock Request Input 1 Clock1 = ON at high level
D2	CLK2	Peripheral	Output	Clock Output 2
C2	CLK_REQ2	Peripheral	Input	Clock Request Input 2 Clock2 = ON at high level
A1	V _{BAT}	Battery / Input	Power	Power Supply
B1	V _{out}	LDO / Output	Power	Power Supply to Clock Source and clock outputs
D1	V _{SS}	Ground	Ground	Ground Pin

(1) I = Input, O = Output, I/O = Input / Output

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, $T_A = 25^\circ\text{C}$, $V_{\text{BAT}} = 3.5\text{V}$, $f_{\text{SCLK_IN}} = 26\text{ MHz}$, $C_{\text{OUT}} = 2.2\ \mu\text{F}$

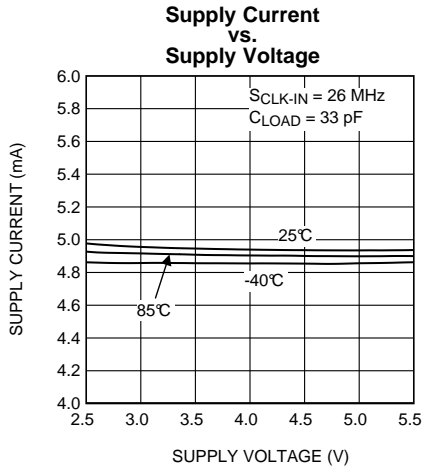


Figure 5.

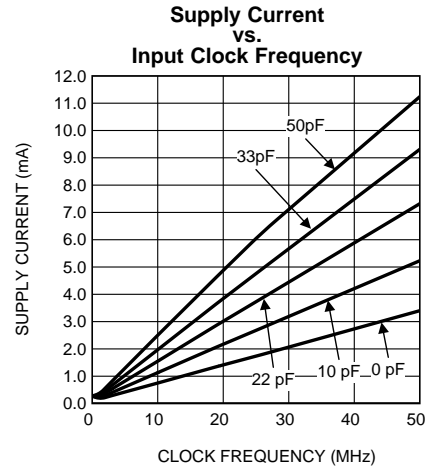


Figure 6.

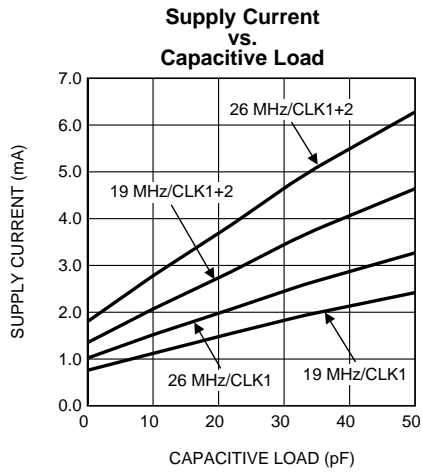


Figure 7.

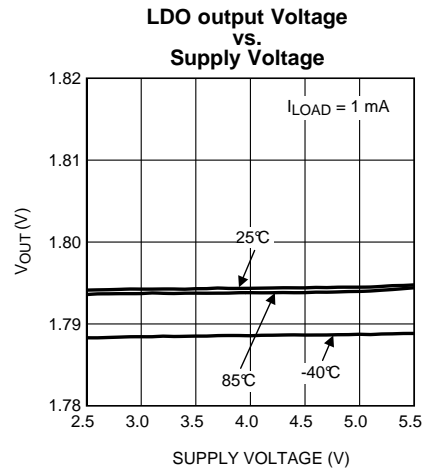


Figure 8.

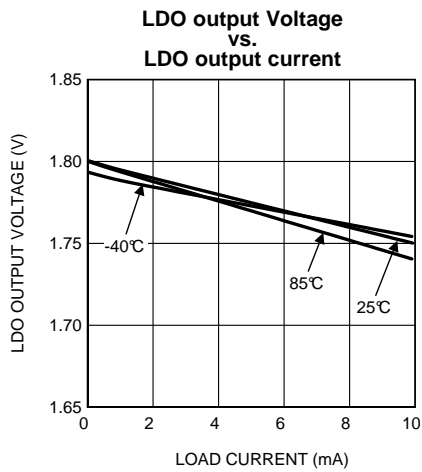


Figure 9.

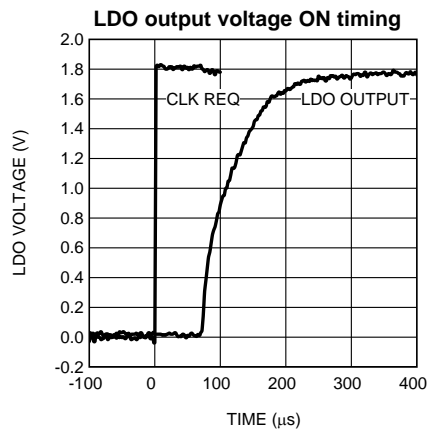


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $T_A = 25^\circ\text{C}$, $V_{BAT} = 3.5\text{V}$, $f_{SCLK_IN} = 26\text{ MHz}$, $C_{OUT} = 2.2\ \mu\text{F}$

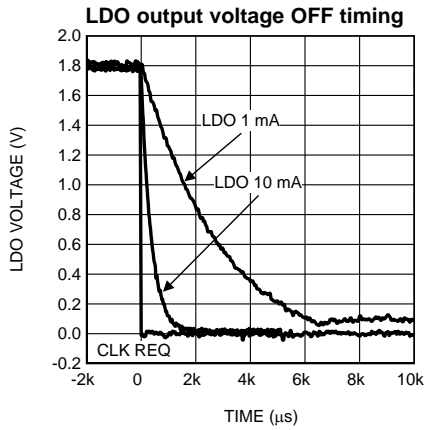


Figure 11.

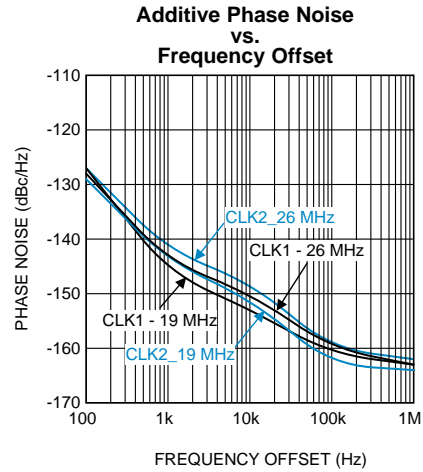


Figure 12.

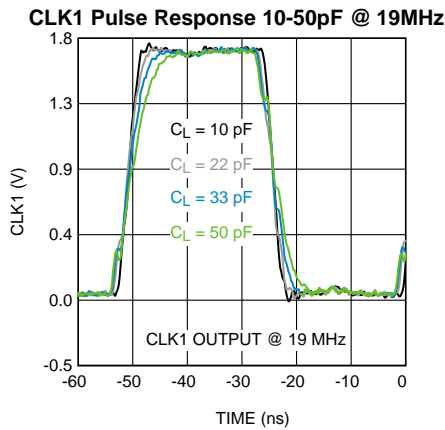


Figure 13.

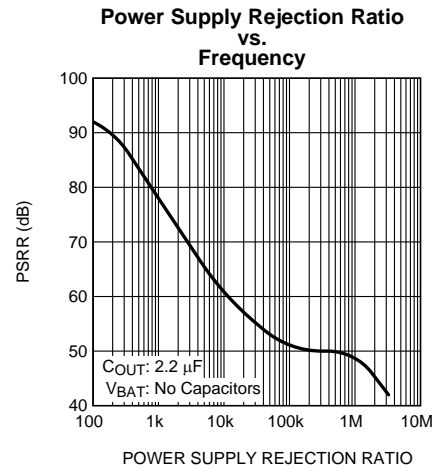


Figure 14.

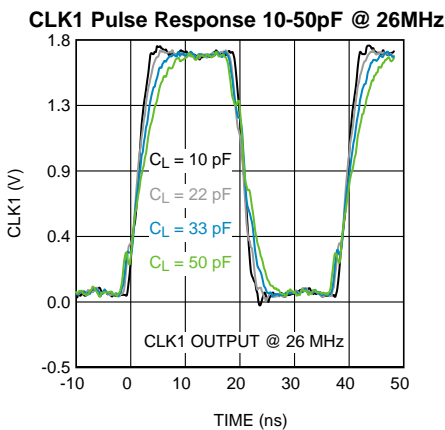


Figure 15.

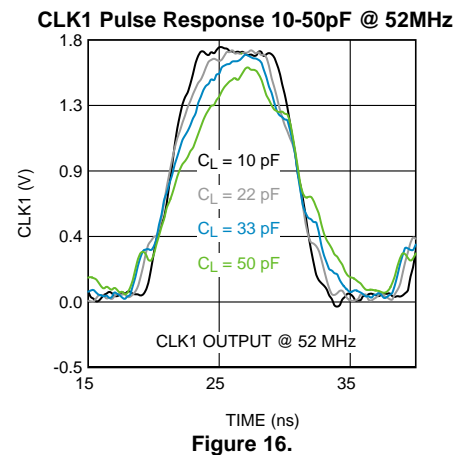


Figure 16.

APPLICATION INFORMATION

The LMH2191 is a complete 52 MHz clocking conditioner and clock tree driver. The LMH2191 is used to supply a common clock to mobile phone peripherals such as Bluetooth, Wireless LAN, and/or Digital Video Broadcast-H (DVB-H). The high isolation between the clock outputs ensures that the peripherals don't disrupt each other. Its excellent phase noise characteristics prevent the clock quality from deteriorating. A typical LMH2191 setup is depicted in [Figure 17](#).

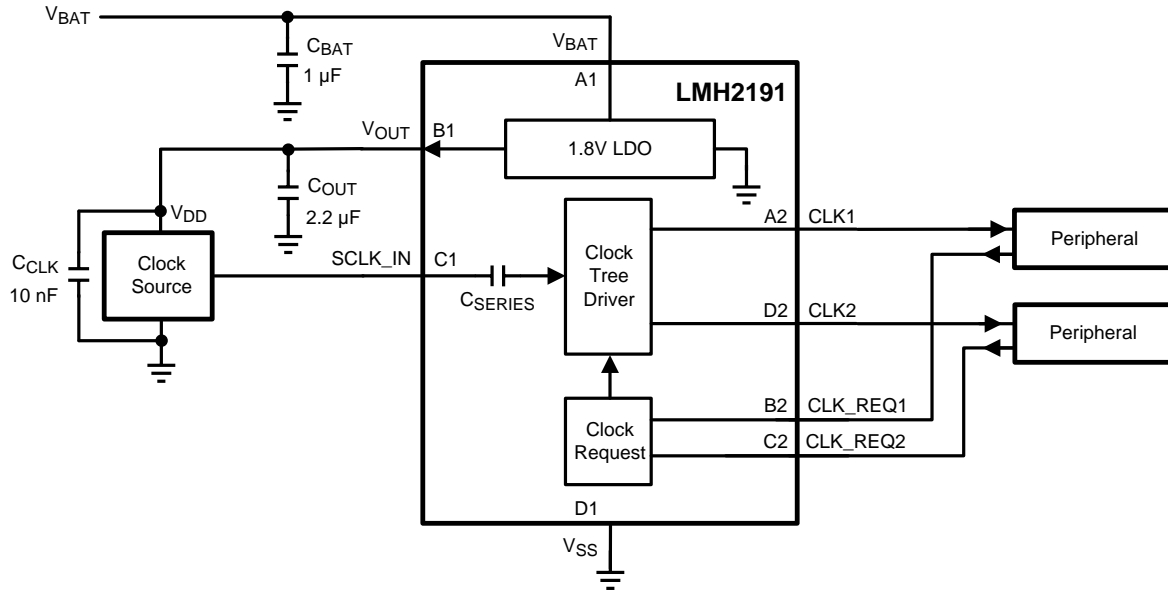


Figure 17. LMH2191 Typical Application Schematic

The internal structure of the LMH2191 is depicted in the block diagram of [Figure 18](#).

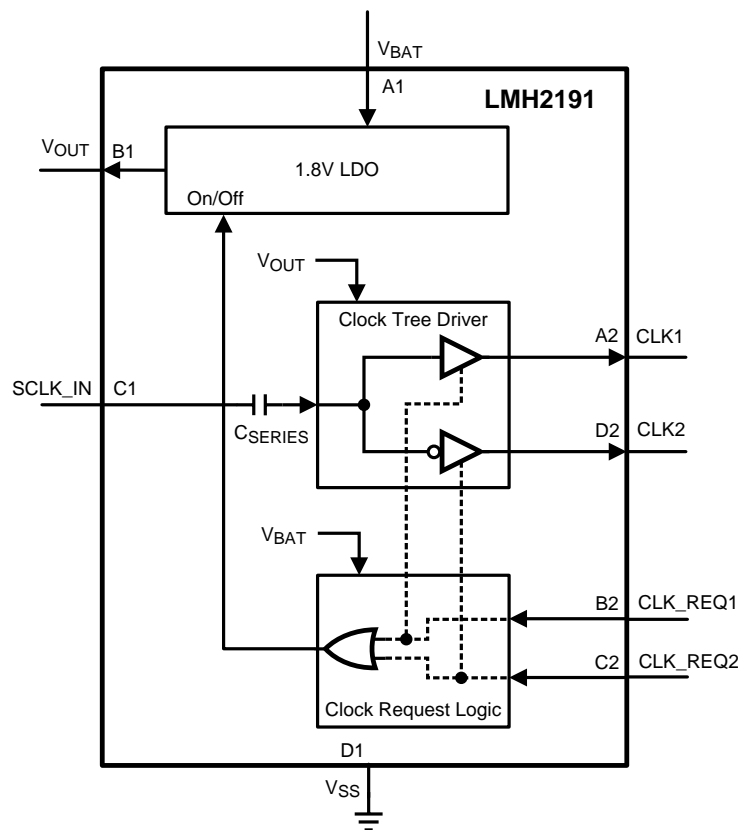


Figure 18. Block Diagram

The LMH2191 clock distribution circuit is comprised of 3 blocks:

- Clock tree driver
- Clock request logic
- Low Dropout Regulator (LDO)

The clock tree driver provides a clean clock to 2 separately connected peripheral devices. Independent clock request inputs allow the peripheral to control when the particular clock should be enabled. Furthermore, both clock request inputs control the LDO output voltage, e.g., when both request inputs are low (no CLK1 and no CLK2 output required), the LDO voltage is disabled. The LDO provides a low-noise, high-PSRR supply voltage that enables low phase noise on the clock outputs, and low quiescent current for portable applications. It can also be used to supply the TCXO. The following sections provide a detailed description of each block.

CLOCK TREE DRIVER

The clock tree driver consists of one input that drives 2 outputs. It is supplied by a high-precision voltage regulator of 1.8V, the LDO. The Clock outputs are enabled when the appropriate Clock Request inputs are logic high.

Clock Tree Driver Input

The source clock input (SCLK_IN) is the input for the clock tree driver. This input has an internally connected coupling capacitor (C_{SERIES}) with a value of 33pF. In shutdown mode (when both CLK_REQ inputs are low), the input stage is completely switched off to prevent unnecessary power consumption when the source clock is still present.

Due to the internal coupling capacitor, the clock signal is DC biased, since the coupling capacitor prevents the internal biasing of the input circuitry to be affected by the external DC voltage. Because of the coupling capacitor, the minimum clock frequency is 10 MHz. It is assumed that the input signal is a sine wave or a typical TCXO waveform (the signal from a TCXO has slow edges), enabling the control loop to adjust to a duty cycle of 50% if the input signal differs slightly from 50% duty cycle. The duty cycle is an important timing parameter for the peripheral equipment. The circuit that adjust the duty cycle is shown in [Figure 19](#).

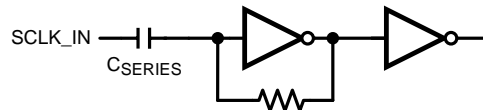


Figure 19. Clock Duty Cycle Regulation

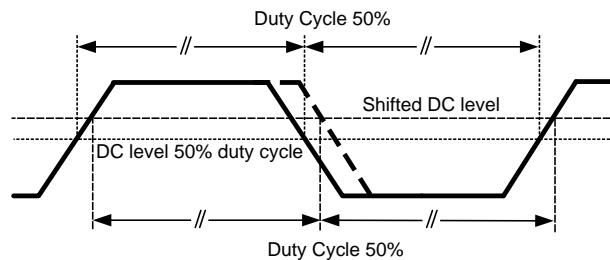


Figure 20. Duty Cycle adjust levels

In order to achieve a duty cycle of 50%, the edges of the incoming clock signal (SCLK_IN) are used to move the switching point to the level that is needed to create the 50% duty cycle. The simplified input circuit consists of an inverter and a feedback resistor. Together with the input series capacitor of about 30 pF, the circuit creates a DC level depending on the duty cycle of the incoming clock signal. When the duty cycle is exactly 50%, the DC level is in the middle of the upper and lower pulse level. When the duty cycle differs from 50%, the DC level shifts slightly to maintain the duty cycle level at 50%. (See Duty Cycle adjust levels of [Figure 20](#).) As explained above, the slow edges of the SCLK_IN signal are important to make the control loop work.

Input Impedance

The input impedance can be split up into two parts: the DC input resistance and the AC input impedance. Due to the used series capacitor in the input signal path the DC resistance is infinite. The AC input impedance is formed by the circuit drawn in [Figure 19](#). This circuit consists of an inverter and a feedback resistor. A signal fed to the input pin is connected to the inverter input which has a high input impedance and is in parallel to the feedback resistor of 30 kΩ. The other pin of the feedback resistor is connected to the output of the inverter which means that the input current is higher than it would be if it were connected to a decoupled supply connection. For this reason the AC input resistance can be much lower than the connected feedback resistor of 30 kΩ. The input resistance is dependant on the amplitude of the input signal. When an input amplitude of 1.8V is used (the same amplitude as the output of the inverter), the input impedance is theoretical half the value of the feedback resistor. When the amplitude of the input signal lowers, the input resistance becomes lower too. With an input signal of 1V_{PP}, the input impedance will be about 10 kΩ.

Clock Tree Driver Outputs

The LMH2191's clock tree driver outputs have a drive strength that make each output capable of driving a capacitive load up to 50 pF, together with a minimum of EMI. Further reduction of EMI is achieved by the inversion of the CLK2 output. (See [Figure 21](#).) Both the drive strength and the capacitive load make the edges of the output pulse relative slow which is favorable for EMI reduction.

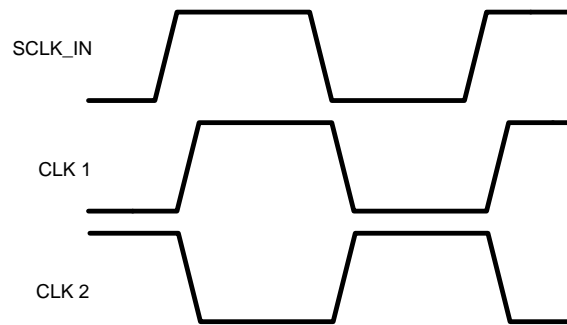


Figure 21. Clock Outputs

CLOCK REQUEST LOGIC

A clock request input is provided for each clock output. This allows the peripheral device to control when it wants to receive a clock. In case the application does not have clock request functionality, the CLKx_REQ can be hard wired to a logic high level to enable the clock output continuously. The clock request inputs have logic levels compatible with 1.8V logic, but can tolerate logic high levels up to V_{BAT} .

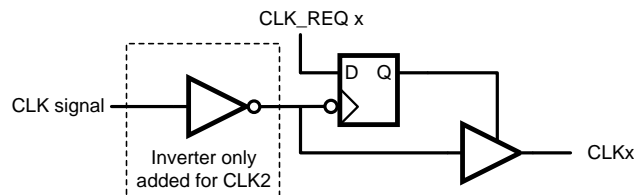


Figure 22. Enabling the output

The clock request logic enables an independent control of the clock tree driver outputs, CLK1 and CLK2, as well as an LDO disable when both request inputs are low.

The on and off switching of the clock output drivers is done synchronously with the clock input in order to prevent glitches at the clock output. For this the clock request signal is connected to the D input of a latch. The Q output of this latch enables the clock output driver (see Figure 22). For the CLK1 output the CLK input signal is connected via an inverter to the clock input of the latch. In this way the latch enables and disables the CLK1 output buffer on the falling edge of the clock signal. For the CLK2 output an extra inverter is inserted prior to the latch circuit, and the CLK2 output buffer is enabled and disabled on the rising edge of the clock input signal (equal to the falling edge of the CLK2 output signal).

LOW DROPOUT REGULATOR

The linear and Low-Dropout regulator (LDO) is used to regulate the input voltage, V_{BAT} , thus generating a well-defined ultra low noise 1.8V supply voltage. This allows the LMH2191 to suppress V_{BAT} supply voltage ripple and noise for the TCXO and the internal Clock Path. Voltage ripple and noise would distort clock edges causing extra phase noise on the distributed clock signal.

The LDO is powered up whenever a Clock Request is active; it supports overheating detection and will switch off in case overheating occurs. The recommended sequence for powering up the LDO is to raise a clock request to a high level with the supply already powered up. Thus the LDO stays in shutdown mode with sub μA current consumption until an output clock is actually needed. The LDO will power up within the turn-on time of about 200 μs (as specified in the data sheet tables). Alternatively, the clock request input can be hard wired to V_{BAT} which powers up the LDO simultaneously with V_{BAT} . A drawback is that the LDO and clock path (and if connected, the TCXO) will always draw current when V_{BAT} is powered up. Also, in this setup, care should be taken with supplies with an excessive long startup time of more than about 25 ms. Under this condition the LDO could exhibit excessive long turn-on delay (order of seconds.)

LAYOUT RECOMMENDATIONS

As with any other device, careful attention must be paid to the board layout. If the board isn't properly designed, the performance of the device can be less than desired. Care should be taken that the SCLK_IN input trace and the output traces of CLK1 and CLK2 are as short as possible to reduce extra capacitive load observed by the clock outputs. Also proper de-coupling close to the device is necessary. Table 1 depicts the advised component values. TI suggests to use the evaluation board, available from the Texas Instruments web site www.ti.com, as a guide for layout and as an aid in device testing and characterization.

Table 1. Recommended Component Values

Symbol	Parameter	Min	Typ	Max	Units
$C_{BAT}^{(1)}$	Capacitor on V_{BAT}	0.47	1		μF
$C_{OUT}^{(1)}$	Capacitor on V_{OUT}	1	2.2		
ESR	Equivalent Series Resistance	5		500	$m\Omega$

(1) C_{BAT} , C_{OUT} : Low-ESR Surface-Mount Ceramic Capacitors (MLCC's) used in setting electrical characteristics.

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH2191TME/NOPB	ACTIVE	DSBGA	YFX	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5	Samples
LMH2191TMX/NOPB	ACTIVE	DSBGA	YFX	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

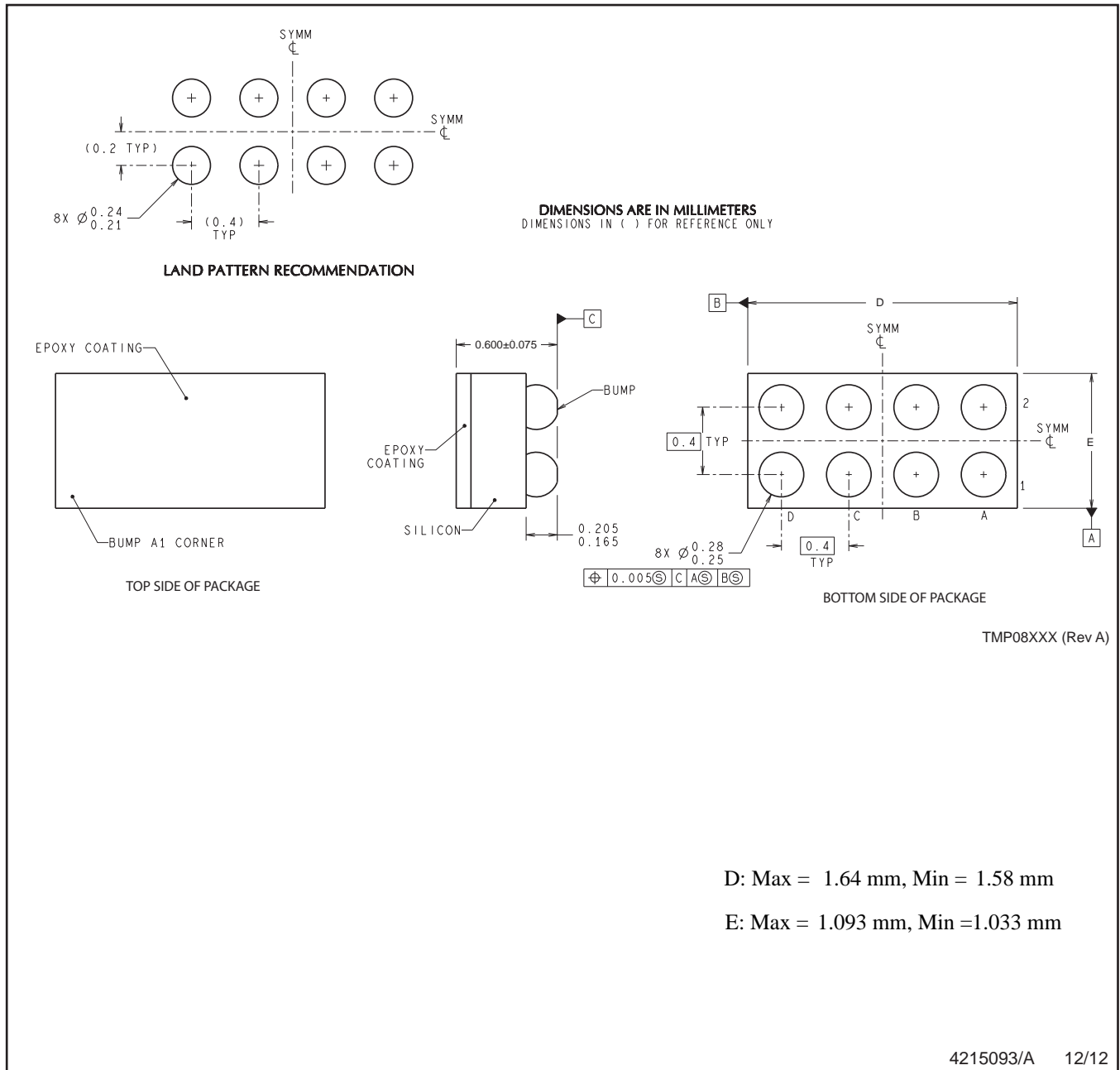
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH2191TME/NOPB	DSBGA	YFX	8	250	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1
LMH2191TMX/NOPB	DSBGA	YFX	8	3000	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH2191TME/NOPB	DSBGA	YFX	8	250	210.0	185.0	35.0
LMH2191TMX/NOPB	DSBGA	YFX	8	3000	210.0	185.0	35.0

YFX0008



D: Max = 1.64 mm, Min = 1.58 mm

E: Max = 1.093 mm, Min = 1.033 mm

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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