THE DATASHEET OF

INA220BQDGSRQ1

INA220-Q1 Automotive Grade, 26-V, Bi-Directional, Zero-Drift, Low- or High-Side, I²C-Compatible Current/Power Monitor

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the following results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- High- or Low-Side Sensing
- Senses Bus Voltages from 0 V to 26 V
- Reports Current, Voltage, and Power
- 16 Programmable Addresses
- High Accuracy: 0.5% (Maximum) Over Temperature
- User-Programmable Calibration
- Fast (2.56-MHz) I²C- or SMBUS-Compatible Interface
- VSSOP-10 Package

2 Applications

- Electric Power Steering (EPS) Systems
- Body Control Modules
- Brake Systems
- Electronic Stability Control (ESC) Systems

3 Description

The INA220-Q1 device is a current shunt and power monitor with an I²C- or SMBUS-compatible interface. The INA220-Q1 device monitors both shunt drop and supply voltage. A programmable calibration value, combined with an internal multiplier, enables direct readouts in amperes. An additional multiplying register calculates power in watts. The I²C- or SMBUS-compatible interface features 16 programmable addresses. The separate shunt input on the INA220-Q1 device allows it to be used in systems with low-side sensing.

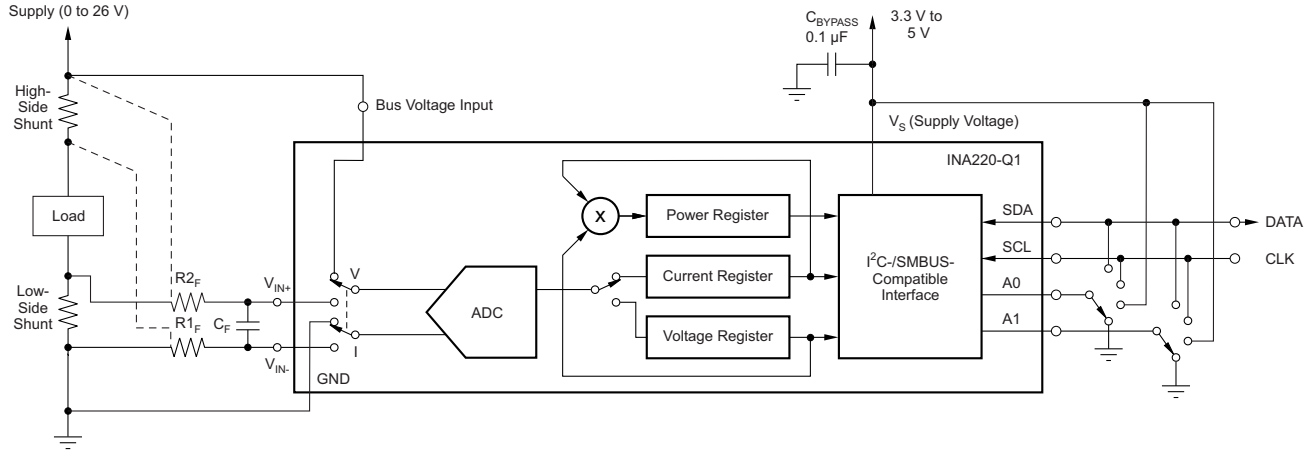
The INA220-Q1 device senses across shunts on buses that can vary from 0 to 26 V, useful for low-side sensing or CPU power supplies. The device uses a single 3- to 5.5-V supply, drawing a maximum of 1 mA of supply current. The INA220-Q1 device operates from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA220-Q1	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

General Load, Low- or High-Side Sensing



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2012) to Revision B — **Page**

- Changed part number to INA220-Q1 ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed "Two-wire" to "I^2C- or SMBUS-compatible" throughout document ... 1
- Deleted the *Ordering Information* table ... 1
- Corrected errors in graphics ... 1
- Added automotive part numbers to *Related Products* ... 3
- Changed pin names in *Pin Configuration and Functions* ... 3
- Added common-mode definition to *Absolute Maximum Ratings* ... 4
- Changed IN+ and IN– pin input impedance to input bias current ... 5
- Changed Power register to Bus Voltage register ... 10
- Replaced *Programming the INA220B-Q1* with *Programming the INA220-Q1 Calibration Register* ... 12
- Replaced *PROGRAMMING THE INA220 POWER MEASUREMENT ENGINE* with *Calibration Register and Scaling* ... 12
- Updated Table 2 based on one-time sample of devices ... 17
- Changed Power register to Bus Voltage register ... 23
- Corrected register values in *Detailed Design Procedure* and Table 8 ... 26
- Changed *Configure, Measure, and Calculate Example* table to Table 8 and removed first column ... 26

Changes from Original (June 2012) to Revision A — **Page**

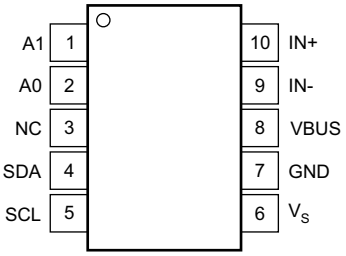
- Device went from preview to production ... 1

5 Related Products

PART NUMBER	DESCRIPTION
INA212-Q1	Automotive, 26-V, Bi-Directional, Zero-Drift, Precision, Low-/High-Side, Volt. Out Current Sense Amp
INA225-Q1	Automotive, 36-V Prog. Gain, Bi-Directional, Zero-Drift, High-Speed Voltage Out Current Sense Amp
INA226-Q1	Automotive, 36-V, Ultra-High Accuracy, Low-/High-Side, I2C Out Current/Power Monitor w/ Alert
INA282-Q1	Automotive, 80-V, Bi-Directional, High Accuracy, Low-/High-Side, Voltage Out Current Shunt Monitor
INA300-Q1	Automotive, 36-V Low-/High-Side, Overcurrent Protection Comparator
INA3221-Q1	Automotive 26-V, Triple, Bi-Directional, Zero-Drift, I2C Out Current/Voltage Monitor w/ Alerts

6 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A1	Digital Input	Address pin. Connect to GND, SCL, SDA, or V_S. Table 1 shows pin settings and corresponding addresses.
2	A0	Digital Input	Address pin. Connect to GND, SCL, SDA, or V_S. Table 1 shows pin settings and corresponding addresses.
3	NC	—	No internal connection
4	SDA	Digital I/O	Serial bus data line
5	SCL	Digital Input	Serial bus clock line
6	V_S	Analog	Power supply, 3 V to 5.5 V
7	GND	Analog	Ground
8	VBUS	Analog Input	Bus voltage input
9	IN–	Analog Input	Negative differential shunt voltage. Connect to negative side of shunt resistor. Bus voltage is measured from this pin to ground.
10	IN+	Analog Input	Positive differential shunt voltage. Connect to positive side of shunt resistor.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage			6	V
	Analog inputs IN+, IN–	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–26	26	V
		Common-mode (V_{IN+} + V_{IN-}) / 2	–0.3	26	V
V_{VBUS}	Voltage at VBUS pin		–0.3	26	V
V_{SDA}	Voltage at SDA pin		GND – 0.3	6	V
V_{SCL}	Voltage at SCL pin		GND – 0.3	V_S + 0.3	V
	Input current into any pin			5	mA
	Open-drain digital output current			10	mA
	Operating temperature		–40	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) IN+ and IN– may have a differential voltage of –26 to 26 V; however, the voltage at these pins must not exceed the range of –0.3 to 26 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	(V_{IN+} + V_{IN-}) / 2		12		V
V_S	Supply voltage		3.3		V
T_A	Ambient temperature	–25		85	ºC

7.4 Thermal Information

THERMAL METRIC(1)		INA220-Q1 DGS (10 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	86.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	85	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, V_{SHUNT} = (V_{IN+} – $V_{IN–}$) = 32 mV, V_{VBUS} = 12 V, PGA = /1, and BRNG(1) = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{SHUNT}	Full-scale current sense (input) voltage range	PGA = /1	0		±40	mV
		PGA = /2	0		±80	mV
		PGA = /4	0		±160	mV
		PGA = /8	0		±320	mV
	Bus voltage (input voltage)(2)	BRNG = 1	0		32	V
		BRNG = 0	0		16	V
	Common-mode rejection	V_{IN+} = 0 to 26 V	100	120		dB
V_{OS}	Offset voltage, RTI(3)	PGA = /1		±10	±50	µV
		PGA = /2		±20	±75	µV
		PGA = /4		±30	±75	µV
		PGA = /8		±40	±100	µV
		T_A = –40°C to 85°C		0.16		µV/°C
PSRR	Offset voltage versus power supply, RTI(3)	V_S = 3 to 5.5 V		10		µV/V
	Current sense gain error			±40		m%
		T_A = –40°C to 85°C		1		m%/°C
I_{IN+}, $I_{IN–}$	Input bias current at IN+ and IN–	Active mode		20		µA
	VBUS pin input impedance(4)	Active mode		320		kΩ
	IN+ pin input leakage(5)	Power-down mode		0.1	±0.5	µA
	IN– pin input leakage(5)	Power-down mode		0.1	±0.5	µA
DC ACCURACY						
	ADC basic resolution			12		bits
	Shunt voltage	1-LSB step size		10		µV
	Bus voltage	1-LSB step size		4		mV
	Current measurement error			±0.2%	±0.3%	
		T_A = –40°C to 85°C			±0.5%	
	Bus voltage measurement error	V_{BUS} = 12 V		±0.2%	±0.5%	
		T_A = –40°C to 85°C			±1%	
	Differential nonlinearity			±0.1		LSB
ADC TIMING						
	ADC conversion time	12-bit		532	586	µs
		11-bit		276	304	µs
		10-bit		148	163	µs
		9-bit		84	93	µs
	Minimum convert input low time		4			µs
SMBus						
	SMBus timeout(6)			28	35	ms

(1) BRNG is bit 13 of the Configuration Register 00h (see Figure 19).
(2) This parameter only expresses the full-scale range of the ADC scaling. In no event should more than 26 V be applied to this device.
(3) Referred-to-input (RTI)
(4) The input impedance of this pin may vary approximately ±15%.
(5) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of the table. Negative leakage currents can occur under different input conditions.
(6) SMBus timeout in the INA220-Q1 resets the interface any time SCL or SDA is low for more than 28 ms.

Electrical Characteristics (continued)

at T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, V_{SHUNT} = (V_{IN+} – $V_{IN–}$) = 32 mV, V_{VBUS} = 12 V, PGA = /1, and BRNG[1] = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (SDA as Input, SCL, A0, A1)						
	Input capacitance			3		pF
	Leakage input current	$0 \le V_{IN} \le V_S$		0.1	1	µA
V_{IH}	Input logic-level high		0.7 (V_S)		6	V
V_{IL}	Input logic-level low		–0.3		0.3 (V_S)	V
	Hysteresis			500		mV
OPEN-DRAIN DIGITAL OUTPUTS (SDA)						
	Logic 0 output level	I_{SINK} = 3 mA		0.15	0.4	V
	High-level output leakage current	$V_{OUT} = V_S$		0.1	1	µA
POWER SUPPLY						
	Operating supply range		3		5.5	V
	Quiescent current			0.7	1	mA
	Quiescent current, power-down mode			6	15	µA
	Power-on reset threshold			2		V

7.6 Typical Characteristics

at T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, V_{SHUNT} = (V_{IN+} – $V_{IN–}$) = 32 mV, PGA = /1, and BRNG = 1, unless otherwise noted.

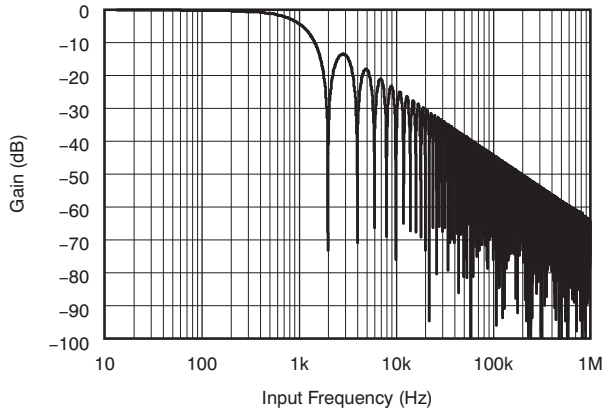


Figure 1. Frequency Response

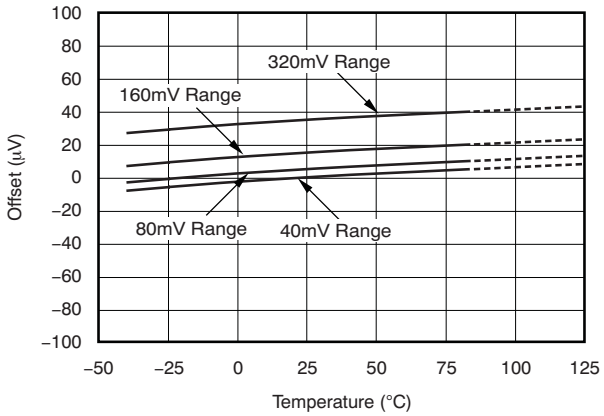


Figure 2. ADC Shunt Offset vs Temperature

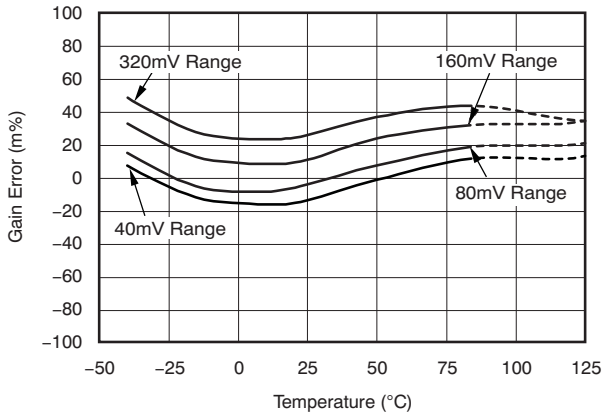


Figure 3. ADC Shunt Gain Error vs Temperature

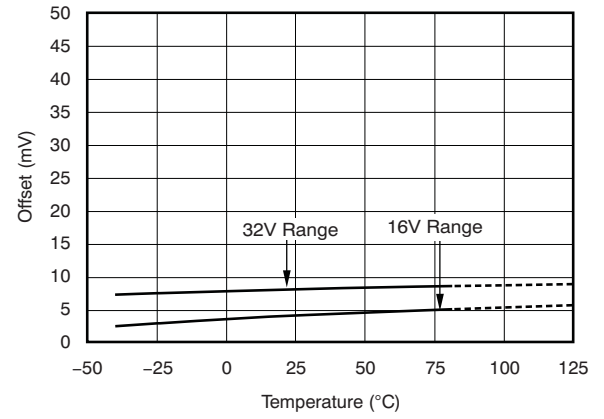


Figure 4. ADC Bus Voltage Offset vs Temperature

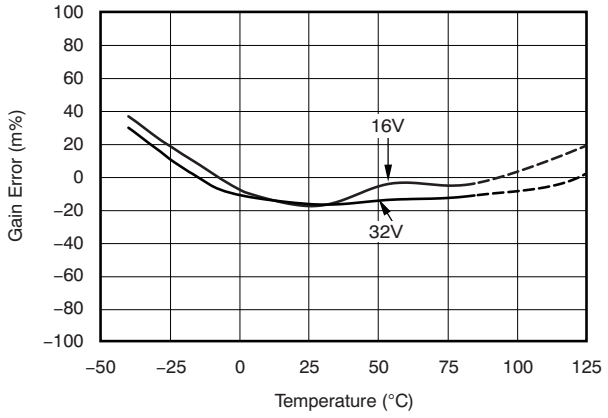


Figure 5. ADC Bus Gain Error vs Temperature

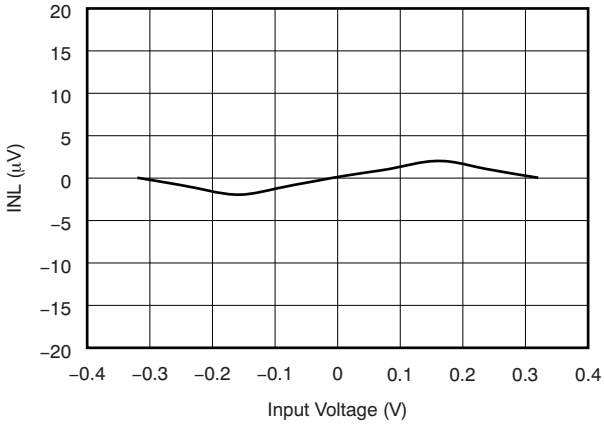


Figure 6. Integral Nonlinearity vs Input Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, V_{SHUNT} = (V_{IN+} – $V_{IN–}$) = 32 mV, PGA = /1, and BRNG = 1, unless otherwise noted.

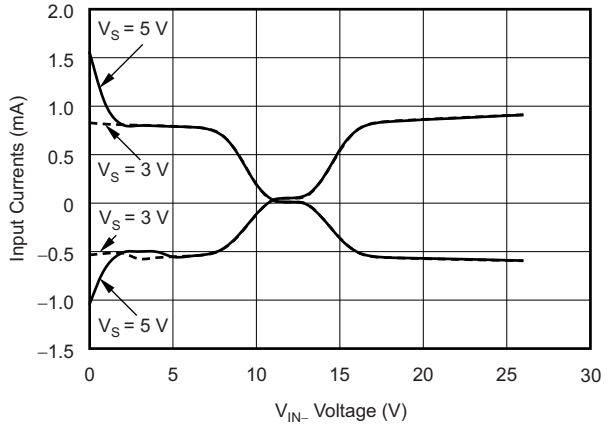


Figure 7. Input Currents With Large Differential Voltages (V_{IN+} at 12 V, Sweep Of $V_{IN–}$)

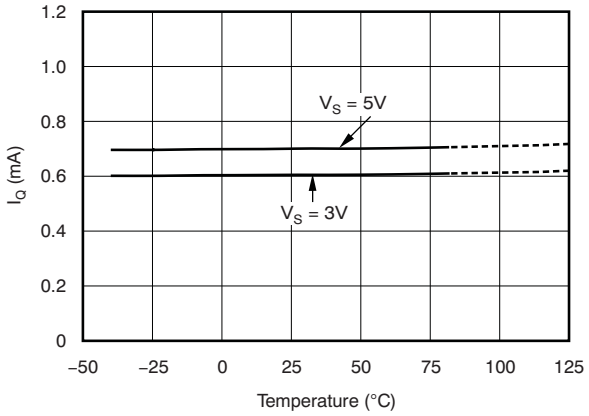


Figure 8. Active I_Q vs Temperature

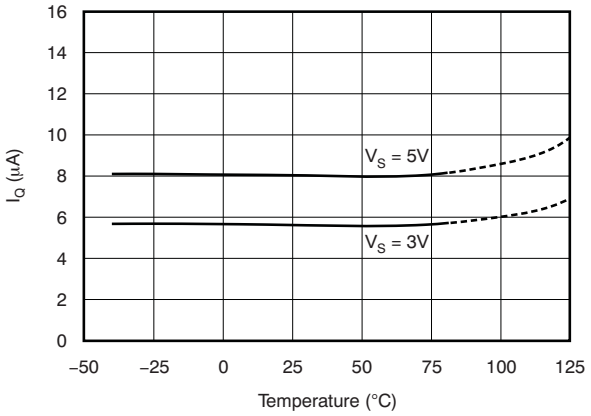


Figure 9. Shutdown I_Q vs Temperature

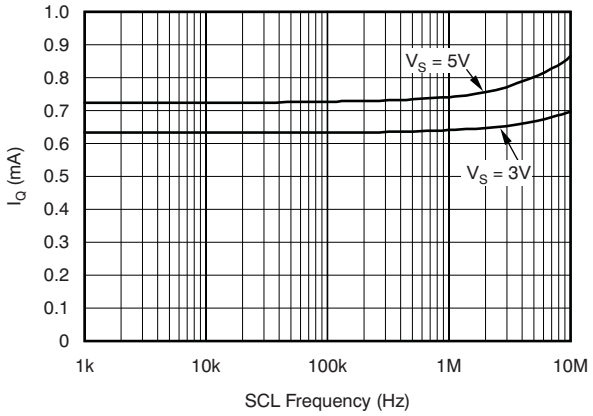


Figure 10. Active I_Q vs Clock Frequency

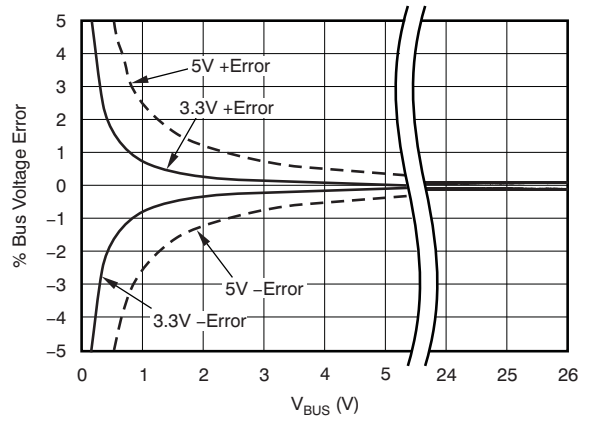


Figure 11. Total Percent Bus Voltage Error vs Supply Voltage

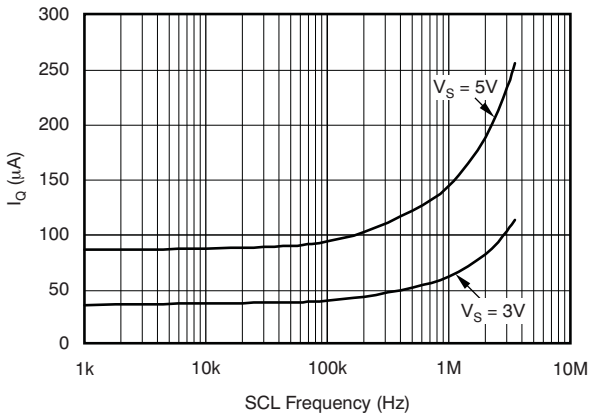


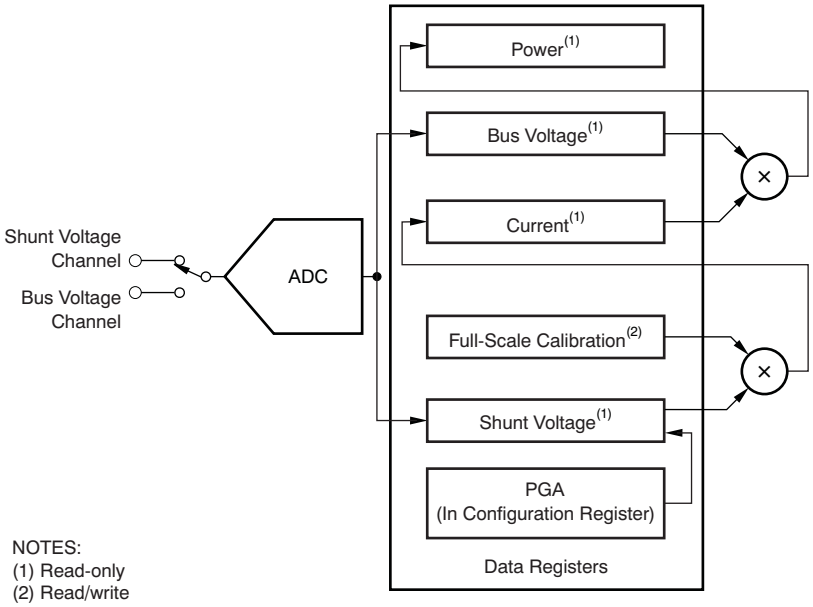
Figure 12. Shutdown I_Q vs Clock Frequency

8 Detailed Description

8.1 Overview

The INA220-Q1 is a digital current sense amplifier with an I^{2}C- and SMBus-compatible interface. It provides digital current, voltage, and power readings necessary for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for measurement resolution as well as continuous-versus-triggered operation. Detailed register information appears at the end of this data sheet, beginning with Table 3. See *Functional Block Diagram* for a block diagram of the INA220-Q1 device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Basic ADC Functions

The two analog inputs to the INA220-Q1, IN+ and IN–, connect to a shunt resistor in the bus of interest. Bus voltage is measured at VBUS pin. The INA220-Q1 is typically powered by a separate supply from 3 to 5.5 V. The bus being sensed can vary from 0 to 26 V. It requires no special considerations for power-supply sequencing (for example, a bus voltage can be present with the supply voltage off, and vice-versa). The INA220-Q1 senses the small drop across the shunt for shunt voltage, and senses the voltage with respect to ground from VBUS pin for the bus voltage.

When the INA220-Q1 is in the normal operating mode (that is, MODE bits of the Configuration register are set to 111), it continuously converts the shunt voltage up to the number set in the shunt voltage averaging function (Configuration register, SADC bits). The device then converts the bus voltage up to the number set in the bus voltage averaging (Configuration register, BADC bits). The Mode control in the Configuration register also permits selecting modes to convert only voltage or current, either continuously or in response to an event (triggered).

All current and power calculations are performed in the background and do not contribute to conversion time; conversion times shown in *Electrical Characteristics* can be used to determine the actual conversion time.

Power-down mode reduces the quiescent current and turns off current into the INA220-Q1 inputs, avoiding any supply drain. Full recovery from power-down requires 40 µs. ADC off mode (set by the Configuration register, MODE bits) stops all conversions.

In triggered mode, writing any of the triggered convert modes into the Configuration register (even if the desired mode is already programmed into the register) triggers a single-shot conversion.

Feature Description (continued)

Although the INA220-Q1 can be read at any time, and the data from the last conversion remain available, the Conversion Ready bit (Bus Voltage register, CNVR bit) is provided to help coordinate one-shot or triggered conversions. The Conversion Ready bit is set after all conversions, averaging, and multiplication operations are complete.

The Conversion Ready bit clears under any of these conditions:

- Writing to the Configuration register, except when configuring the MODE bits for power down or ADC off (disable) modes
- Reading the Bus Voltage register

8.3.1.1 Power Measurement

Current and bus voltage are converted at different points in time, depending on the resolution and averaging mode settings. For instance, when configured for 12-bit and 128-sample averaging, up to 68 ms in time between sampling these two values is possible. Again, these calculations are performed in the background and do not add to the overall conversion time.

8.3.1.2 PGA Function

If larger full-scale shunt voltages are desired, the INA220-Q1 provides a PGA function that increases the full-scale range up to 2, 4, or 8 times (320 mV). Additionally, the bus voltage measurement has two full-scale ranges: 16 or 32 V.

8.4 Device Functional Modes

8.4.1 Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The INA220-Q1 offers several options for filtering by choosing resolution and averaging in the Configuration register. These filtering options can be set independently for either voltage or current measurement.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500-kHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be dealt with by incorporating filtering at the input of the INA220-Q1. The high frequency enables the use of low-value series resistors on the filter for negligible effects on measurement accuracy. In general, filtering the INA220-Q1 input is only necessary if there are transients at exact harmonics of the 500-kHz (±30%) sampling rate (>1 MHz). Filter using the lowest possible series resistance and ceramic capacitor. TI recommends values of 0.1 to 1 µF. Figure 13 shows the INA220-Q1 with an additional filter added at the input.

Overload conditions are another consideration for the INA220-Q1 inputs. The INA220-Q1 inputs are specified to tolerate 26 V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). It must be remembered that removing a short to ground can result in inductive kickbacks that could exceed the 26-V differential and common-mode rating of the INA220-Q1. Inductive kickback voltages are best dealt with by Zener-type transient-absorbing devices combined with sufficient energy storage capacitance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications with no large electrolytics present. This problem occurs because an excessive dV/dt can activate the ESD protection in the INA220-Q1 in systems where large currents are available. Testing has demonstrated that the addition of 10-Ω resistors in series with each input of the INA220-Q1 sufficiently protects the inputs against dV/dt failure up to the 26-V rating of the INA220-Q1. These resistors have no significant effect on accuracy.

Device Functional Modes (continued)

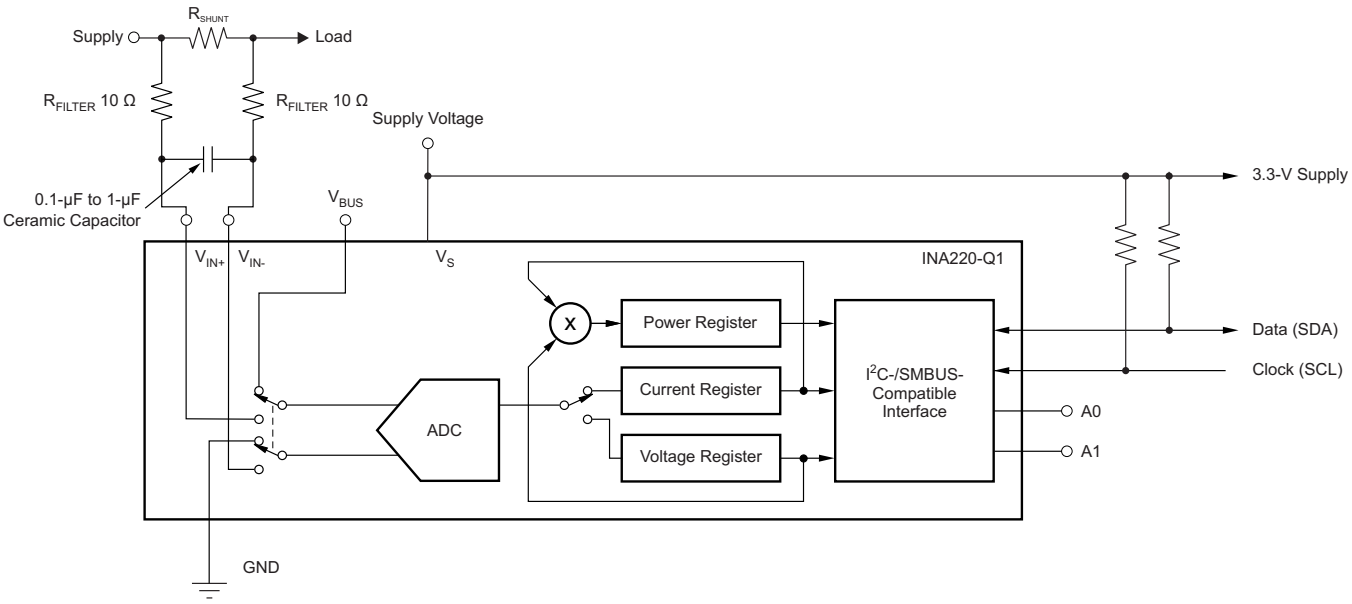


Figure 13. INA220-Q1 With Input Filtering

8.5 Programming

8.5.1 Programming the INA220-Q1 Calibration Register

Register Details shows the default power-up states of the registers. These registers are volatile, and if programmed to anything other than default values, they must be reprogrammed at every device power-up. The Calibration Register is calculated based on Equation 1. This equation includes the term Current_LSB, which is the programmed value for the LSB for the Current Register (04h). The Current_LSB value is used to convert the value in the Current Register (04h) to the actual current in amperes. The highest resolution for the Current Register (04h) can be obtained by using the smallest allowable Current_LSB based on the maximum expected current as shown in Equation 2. While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current Register (04h) and Power Register (03h) to amperes and watts respectively. The R_{SHUNT} term is the value of the external shunt used to develop the differential voltage across the input pins. The Power Register (03h) is internally set to be 20 times the programmed Current_LSB (see Equation 3).

$$Cal = \text{trunc}\left(\frac{0.04096}{Current\_LSB \times R_{SHUNT}}\right) \quad (1)$$

where

- 0.04096 is an internal fixed value used to ensure scaling is maintained properly
- Current_LSB is the programmed value for the LSB for the Current Register (04h)

$$Current\_LSB = \frac{Maximum\ Expected\ Current}{2^{15}} \quad (2)$$

$$Power\_LSB = 20\ Current\_LSB \quad (3)$$

Programming (continued)

Shunt voltage is calculated by multiplying the Shunt Voltage Register contents with the Shunt Voltage LSB of 10 µV. The Bus Voltage register bits are not right-aligned. To compute the value of the Bus Voltage, Bus Voltage Register contents must be shifted right by three bits. This shift puts the BD0 bit in the LSB position so that the contents can be multiplied by the Bus Voltage LSB of 4-mV to compute the bus voltage measured by the device. After programming the Calibration Register, the value expected in the Current Register (04h) can be calculated by multiplying the Shunt Voltage register contents by the Calibration Register and then dividing by 4096 as shown in Equation 4. To obtain a value in amperes, the Current register value is multiplied by the programmed Current_LSB.

$$\text{Current Register} = \frac{\text{Shunt Voltage Register} \times \text{Calibration Register}}{4096} \tag{4}$$

The value expected in the Power register (03h) can be calculated by multiplying the Current register value by the Bus Voltage register value and then dividing by 5000 as shown in Equation 5. Power Register content is multiplied by Power LSB which is 20 times the Current_LSB for a power value in watts.

$$\text{Power Register} = \frac{\text{Current Register} \times \text{Bus Voltage Register}}{5000} \tag{5}$$

8.5.2 Programming the INA220-Q1 Power Measurement Engine

8.5.2.1 Calibration Register and Scaling

The Calibration register makes it possible to set the scaling of the Current and Power registers to whatever values are most useful for a given application. One strategy may be to set the Calibration register such that the largest possible number is generated in the Current register or Power register at the expected full-scale point; this approach yields the highest resolution. The Calibration register can also be selected to provide values in the Current and Power registers that either provide direct decimal equivalents of the values being measured, or yield a round LSB number. After these choices have been made, the Calibration register also offers possibilities for end-user system-level calibration, where the value is adjusted slightly to cancel total system error. After determining the exact current by using an external ammeter, the value of the Calibration Register can then be adjusted based on the measured current result of the INA220-Q1 to cancel the total system error as shown in Equation 6.

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left(\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{INA220\_Current}}\right) \tag{6}$$

8.5.3 Simple Current Shunt Monitor Usage (No Programming Necessary)

The INA220-Q1 can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default 12-bit resolution, 320-mV shunt full-scale range (PGA = /8), 32-V bus full-scale range, and continuous conversion of shunt and bus voltage.

Without programming, current is measured by reading the shunt voltage. The Current register and Power register are only available if the Calibration register contains a programmed value.

8.5.4 Bus Overview

The INA220-Q1 offers compatibility with both I^2C and SMBus interfaces. The I^2C and SMBus protocols are essentially compatible with one another.

The I^2C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is being addressed. Two lines, SCL and SDA, connect the INA220-Q1 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions.

Programming (continued)

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an *Acknowledge* bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a START or STOP condition.

After all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from low to high while SCL is high. The INA220-Q1 includes a 28-ms timeout on its interface to prevent locking up an SMBus.

8.5.4.1 Serial Bus Address

To communicate with the INA220-Q1, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The INA220-Q1 has two address pins, A0 and A1. Table 1 describes the pin logic levels for each of the 16 possible addresses. The state of pins A0 and A1 is sampled on every bus communication and should be set before any activity on the interface occurs. The address pins are read at the start of each communication event.

Table 1. INA220-Q1 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V_S	1000001
GND	SDA	1000010
GND	SCL	1000011
V_S	GND	1000100
V_S	V_S	1000101
V_S	SDA	1000110
V_S	SCL	1000111
SDA	GND	1001000
SDA	V_S	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_S	1001101
SCL	SDA	1001110
SCL	SCL	1001111

8.5.4.2 Serial Interface

The INA220-Q1 operates only as a slave device on the I^2C bus and SMBus. Connections to the bus are made by the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The INA220-Q1 supports the transmission protocol for fast (1-kHz to 400-kHz) and high-speed (1-kHz to 2.56-MHz) modes. All data bytes are transmitted most significant byte first.

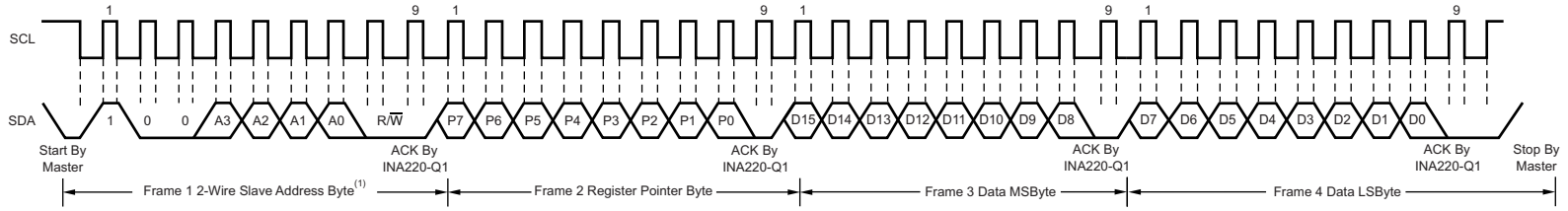
8.5.5 Writing to and Reading from the INA220-Q1

Accessing a particular register on the INA220-Q1 is accomplished by writing the appropriate value to the register pointer. Refer to Table 3 for a complete list of registers and corresponding addresses. The value for the register pointer, as shown in Figure 17, is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit LOW. Every write operation to the INA220-Q1 requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit LOW. The INA220-Q1 then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register to which data will be written. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The INA220-Q1 acknowledges receipt of each data byte. The master may terminate data transfer by generating a START or STOP condition.

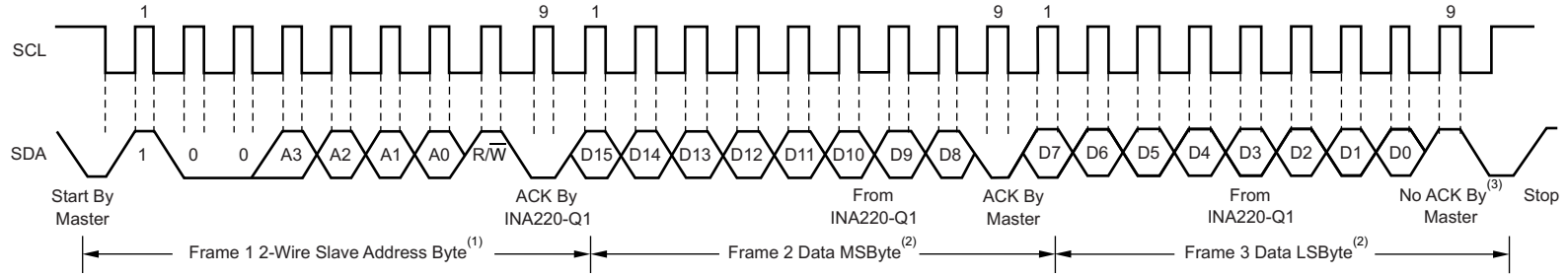
When reading from the INA220-Q1, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit LOW, followed by the register pointer byte. No additional data are required. The master then generates a START condition and sends the slave address byte with the R/$\overline{W}$ bit HIGH to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a *Not Acknowledge* after receiving any data byte, or generating a START or STOP condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the INA220-Q1 retains the register pointer value until it is changed by the next write operation.

Figure 14 and Figure 15 show write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte. Figure 16 shows the timing diagram for the SMBus Alert response operation. Figure 17 shows a typical register pointer configuration.



(1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 14. Timing Diagram for Write Word Format

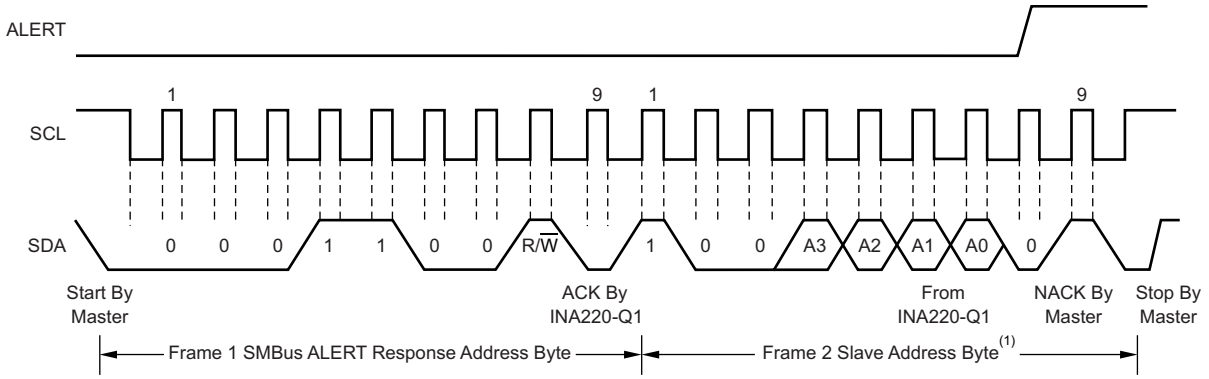


(1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 17.

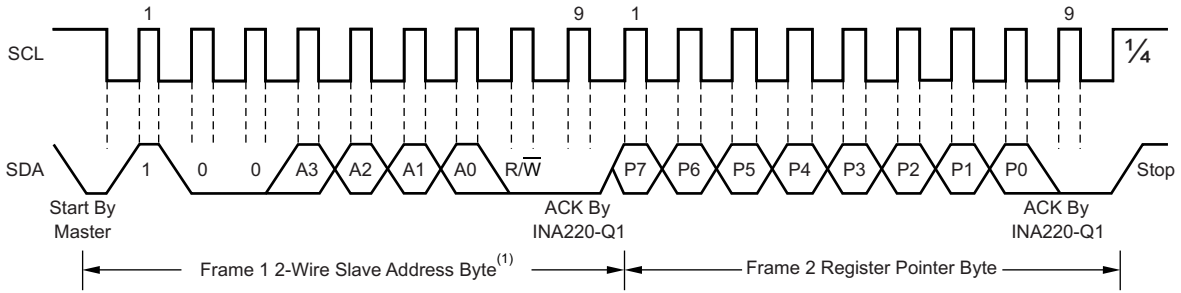
(3) ACK by Master can also be sent.

Figure 15. Timing Diagram for Read Word Format



(1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 16. Timing Diagram for SMBus Alert



(1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 17. Typical Register Pointer Set

8.5.5.1 High-Speed Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup devices. The master generates a start condition followed by a valid serial byte containing high-speed (HS) master code *00001XXX*. This transmission is made in fast (400 kbps) or standard (100 kbps) (F/S) mode at no more than 400 kbps. The INA220-Q1 does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 2.56-Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.56 Mbps are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A STOP condition ends the HS-mode and switches all the internal filters of the INA220-Q1 to support the F/S mode. See Table 2 and Figure 18 for timing.

Table 2. Bus Timing Diagram Definitions(1)

		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	2.56	MHz
$t_{(BUF)}$	Bus free time between STOP and START condition	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time	600		160		ns
$t_{(SUSTO)}$	STOP condition setup time	600		160		ns
$t_{(HDDAT)}$	Data hold time	0	900	0	90	ns
$t_{(SUDAT)}$	Data setup time	100		10		ns
$t_{(LOW)}$	SCL clock LOW period	1300		250		ns
$t_{(HIGH)}$	SCL clock HIGH period	600		60		ns
t_FDA	Data fall time		300		150	ns
t_FCL	Clock fall time		300		40	ns
t_RCL	Clock rise time		300		40	ns
t_RCL	Clock rise time for SCLK ≤ 100 kHz		1000			ns

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not production tested. Condition: A0=A1=0.

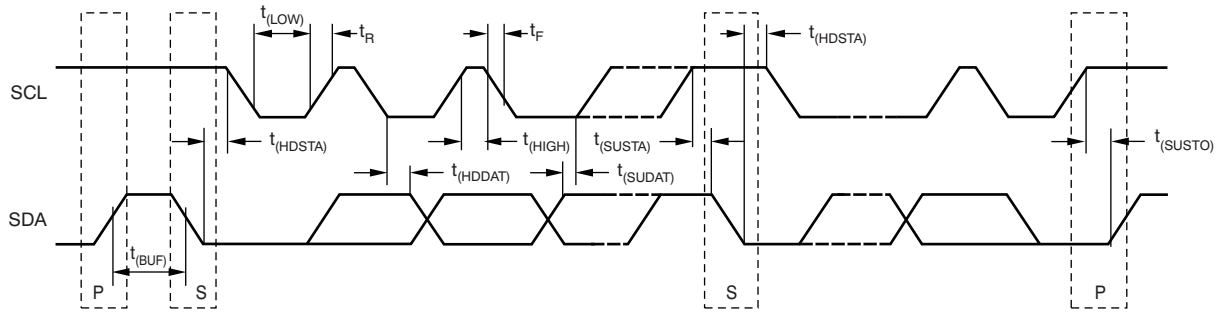


Figure 18. Bus Timing Diagram

8.5.5.2 Power-Up Conditions

Power-up conditions apply to a software reset through the RST bit (bit 15) in the Configuration register, or the I^2C bus General Call Reset.

8.6 Register Maps

8.6.1 Register Information

The INA220-Q1 uses a bank of registers for holding configuration settings, measurement results, and status information. Table 3 summarizes the INA220-Q1 registers; *Functional Block Diagram* illustrates the registers.

Register contents are updated 4 µs after completion of the write command. Therefore, a 4-µs delay is required between completion of a write to a given register and a subsequent read of that register (without changing the pointer) when using SCL frequencies in excess of 1 MHz.

Table 3. Summary of Register Set

POINTER ADDRESS	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE(1)
HEX			BINARY	HEX	
00	Configuration	All-register reset, settings for bus voltage range, PGA gain, ADC resolution/averaging.	00111001 10011111	399F	R/$\overline{W}$
01	Shunt voltage	Shunt voltage measurement data.	Shunt voltage	—	R
02	Bus voltage	Bus voltage measurement data.	Bus voltage	—	R
03	Power(2)	Power measurement data.	00000000 00000000	0000	R
04	Current(2)	Contains the value of the current flowing through the shunt resistor.	00000000 00000000	0000	R
05	Calibration	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/$\overline{W}$

(1) Type: **R** = Read only, **R/$\overline{W}$** = Read/Write.
(2) The Power register and Current register default to 0 because the Calibration register defaults to 0, yielding a zero current value until the Calibration register is programmed.

8.6.2 Register Details

All INA220-Q1 registers 16-bit registers are actually two 8-bit bytes through the I^2C- or SMBUS-compatible interface.

8.6.2.1 Configuration Register (address = 00h) [reset = 399Fh]

Figure 19. Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	—	BRNG	PG1	PG0	BADC 4	BADC 3	BADC 2	BADC 1	SADC 4	SADC 3	SADC 2	SADC 1	MODE 3	MODE 2	MODE 1
R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

RST: **Reset Bit**

Bit 15 — Setting this bit to 1 generates a system reset that is the same as power-on reset. Resets all registers to default values; this bit self-clears.

BRNG: **Bus Voltage Range**

Bit 13 — 0 = 16-V FSR
1 = 32-V FSR (default value)

PG: **PGA (Shunt Voltage Only)**

Bits 11, 12 — Sets PGA gain and range. Note that the PGA defaults to ÷8 (320-mV range). Table 4 shows the gain and range for the various product gain settings.

Table 4. PG Bit Settings [12:11](1)

PG1	PG0	GAIN	RANGE
0	0	1	±40 mV
0	1	/2	±80 mV
1	0	/4	±160 mV
1	1	/8	±320 mV

(1) Shaded values are default.

BADC: **BADC Bus ADC Resolution/Averaging**

Bits 7–10 — These bits adjust the Bus ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Bus Voltage Register (02h).

SADC: **SADC Shunt ADC Resolution/Averaging**

Bits 3–6 — These bits adjust the Shunt ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Shunt Voltage Register (01h).
BADC (Bus) and SADC (Shunt) ADC resolution/averaging and conversion time settings are shown in Table 5.

Table 5. ADC Settings (SADC [6:3], BADC [10:7])(1)

ADC4	ADC3	ADC2	ADC1	Mode/Samples	Conversion Time
0	X(2)	0	0	9-bit	84 µs
0	X(2)	0	1	10-bit	148 µs
0	X(2)	1	0	11-bit	276 µs
0	X(2)	1	1	12-bit	532 µs
1	0	0	0	12-bit	532 µs
1	0	0	1	2	1.06 ms
1	0	1	0	4	2.13 ms
1	0	1	1	8	4.26 ms
1	1	0	0	16	8.51 ms

(1) Shaded values are default.
(2) X = Don't care

Table 5. ADC Settings (SADC [6:3], BADC [10:7])[0] (continued)

ADC4	ADC3	ADC2	ADC1	Mode/Samples	Conversion Time
1	1	0	1	32	17.02 ms
1	1	1	0	64	34.05 ms
1	1	1	1	128	68.10 ms

MODE: **Operating Mode**

Bits 0–2 Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 6.

Table 6. Mode Settings [2:0](1)

MODE3	MODE2	MODE1	MODE
0	0	0	Power-down
0	0	1	Shunt voltage, triggered
0	1	0	Bus voltage, triggered
0	1	1	Shunt and bus, triggered
1	0	0	ADC off (disabled)
1	0	1	Shunt voltage, continuous
1	1	0	Bus voltage, continuous
1	1	1	Shunt and bus, continuous

(1) Shaded values are default.

8.6.3 Data Output Registers

8.6.3.1 Shunt Voltage Register (address = 01h)

The Shunt Voltage register stores the current shunt voltage reading, V_{SHUNT}. Shunt Voltage register bits are shifted according to the PGA setting selected in the Configuration register (00h). When multiple sign bits are present, they are all the same value. Negative numbers are represented in 2's complement format. Generate the 2's complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting the MSB = 1. Extend the sign to any additional sign bits to form the 16-bit word.

Example: For a value of V_{SHUNT} = –320 mV:

1. Take the absolute value (include accuracy to 0.01 mV) → 320.00
2. Translate this number to a whole decimal number → 32000
3. Convert it to binary → 111 1101 0000 0000
4. Complement the binary result : 000 0010 1111 1111
5. Add 1 to the complement to create the 2's-complement formatted result → 000 0011 0000 0000
6. Extend the sign and create the 16-bit word: 1000 0011 0000 0000 = 8300h (Remember to extend the sign to all sign-bits, as necessary based on the PGA setting.)

At PGA = /8, full-scale range = ±320 mV (decimal = 32000). For V_{SHUNT} = +320 mV, Value = 7D00h; For V_{SHUNT} = –320 mV, Value =8300h; and LSB = 10 µV.

Figure 20. Shunt Voltage Register at PGA = /8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SD14_8	SD13_8	SD12_8	SD11_8	SD10_8	SD9_8	SD8_8	SD7_8	SD6_8	SD5_8	SD4_8	SD3_8	SD2_8	SD1_8	SD0_8

At PGA = /4, full-scale range = ±160 mV (decimal = 16000). For V_{SHUNT} = +160 mV, Value = 3E80h; For V_{SHUNT} = –160 mV, Value = C180h; and LSB = 10 µV.

Figure 21. Shunt Voltage Register at PGA = /4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SIGN	SD13_4	SD12_4	SD11_4	SD10_4	SD9_4	SD8_4	SD7_4	SD6_4	SD5_4	SD4_4	SD3_4	SD2_4	SD1_4	SD0_4

At PGA = /2, full-scale range = ±80 mV (decimal = 8000). For V_{SHUNT} = +80 mV, Value = 1F40h; For V_{SHUNT} = –80 mV, Value = E0C0h; and LSB = 10 µV.

Figure 22. Shunt Voltage Register at PGA = /2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SIGN	SIGN	SD12_2	SD11_2	SD10_2	SD9_2	SD8_2	SD7_2	SD6_2	SD5_2	SD4_2	SD3_2	SD2_2	SD1_2	SD0_2

At PGA = /1, full-scale range = ±40 mV (decimal = 4000). For V_{SHUNT} = +40 mV, Value = 0FA0h; For V_{SHUNT} = –40 mV, Value = F060h; and LSB = 10 µV.

Figure 23. Shunt Voltage Register at PGA = /1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SIGN	SIGN	SIGN	SD11_1	SD10_1	SD9_1	SD8_1	SD7_1	SD6_1	SD5_1	SD4_1	SD3_1	SD2_1	SD1_1	SD0_1

Table 7. Shunt Voltage Register Format[1]

V_{SHUNT} Reading (mV)	Decimal Value	PGA = /8 (D15:D0)	PGA = /4 (D15:D0)	PGA = /2 (D15:D0)	PGA = /1 (D15:D0)
320.02	32002	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.01	32001	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.00	32000	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.99	31999	0111 1100 1111 1111	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.98	31998	0111 1100 1111 1110	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
160.02	16002	0011 1110 1000 0010	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.01	16001	0011 1110 1000 0001	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.00	16000	0011 1110 1000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
159.99	15999	0011 1110 0111 1111	0011 1110 0111 1111	0001 1111 0100 0000	0000 1111 1010 0000
159.98	15998	0011 1110 0111 1110	0011 1110 0111 1110	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
80.02	8002	0001 1111 0100 0010	0001 1111 0100 0010	0001 1111 0100 0000	0000 1111 1010 0000
80.01	8001	0001 1111 0100 0001	0001 1111 0100 0001	0001 1111 0100 0000	0000 1111 1010 0000
80.00	8000	0001 1111 0100 0000	0001 1111 0100 0000	0001 1111 0100 0000	0000 1111 1010 0000
79.99	7999	0001 1111 0011 1111	0001 1111 0011 1111	0001 1111 0011 1111	0000 1111 1010 0000
79.98	7998	0001 1111 0011 1110	0001 1111 0011 1110	0001 1111 0011 1110	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
40.02	4002	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0000
40.01	4001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0000
40.00	4000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000
39.99	3999	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111
39.98	3998	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110
⋮	⋮	⋮	⋮	⋮	⋮
0.02	2	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010
0.01	1	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001
0	0	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000
–0.01	–1	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111
–0.02	–2	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110
⋮	⋮	⋮	⋮	⋮	⋮
–39.98	–3998	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010
–39.99	–3999	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001
–40.00	–4000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000
–40.01	–4001	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0110 0000
–40.02	–4002	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–79.98	–7998	1110 0000 1100 0010	1110 0000 1100 0010	1110 0000 1100 0010	1111 0000 0110 0000
–79.99	–7999	1110 0000 1100 0001	1110 0000 1100 0001	1110 0000 1100 0001	1111 0000 0110 0000
–80.00	–8000	1110 0000 1100 0000	1110 0000 1100 0000	1110 0000 1100 0000	1111 0000 0110 0000
–80.01	–8001	1110 0000 1011 1111	1110 0000 1011 1111	1110 0000 1100 0000	1111 0000 0110 0000
–80.02	–8002	1110 0000 1011 1110	1110 0000 1011 1110	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–159.98	–15998	1100 0001 1000 0010	1100 0001 1000 0010	1110 0000 1100 0000	1111 0000 0110 0000
–159.99	–15999	1100 0001 1000 0001	1100 0001 1000 0001	1110 0000 1100 0000	1111 0000 0110 0000
–160.00	–16000	1100 0001 1000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.01	–16001	1100 0001 0111 1111	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.02	–16002	1100 0001 0111 1110	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–319.98	–31998	1000 0011 0000 0010	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–319.99	–31999	1000 0011 0000 0001	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.00	–32000	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.01	–32001	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.02	–32002	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000

(1) Out-of-range values are shown in gray shading.

8.6.3.2 Bus Voltage Register (address = 02h)

The Bus Voltage register stores the most recent bus voltage reading, V_{BUS}.

At full-scale range = 32 V (decimal = 8000, hex = 1F40), and LSB = 4 mV.

Figure 24. Bus Voltage Register (BRNG = 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	CNVR	OVF

At full-scale range = 16 V (decimal = 4000, hex = 0FA0), and LSB = 4 mV.

Figure 25. Bus Voltage Register (BRNG = 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	CNVR	OVF

CNVR: **Conversion Ready**

Bit 1

Although the data from the last conversion can be read at any time, the INA220-Q1 Conversion Ready bit (CNVR) indicates when data from a conversion is available in the data output registers. The CNVR bit is set after all conversions, averaging, and multiplications are complete. CNVR will clear under the following conditions:

1.) Writing a new mode into the Operating Mode bits in the Configuration Register (except for Power-Down or Disable)

2.) Reading the Bus Voltage register

OVF: **Math Overflow Flag**

Bit 0

The Math Overflow Flag (OVF) is set when the Power or Current calculations are out of range. It indicates that current and power data may be meaningless.

8.6.3.3 Power Register (address = 03h) [reset = 00h]

Full-scale range and LSB are set by the Calibration register. See *Programming the INA220-Q1 Calibration Register*.

Figure 26. Power Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The Power register records power in watts by multiplying the values of the current with the value of the bus voltage according to the Equation 5:

8.6.3.4 Current Register (address = 04h) [reset =00h]

Full-scale range and LSB depend on the value entered in the Calibration register. See *Programming the INA220-Q1 Calibration Register*. Negative values are stored in 2's complement format.

Figure 27. Current Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The value of the Current register is calculated by multiplying the value in the Shunt Voltage register with the value in the Calibration register according to the Equation 4.

8.6.4 Calibration Register

8.6.4.1 Calibration Register (address = 05h) [reset = 00h]

Current and power calibration are set by bits FS15 to FS1 of the Calibration register. Note that bit FS0 is not used in the calculation. This register sets the current that corresponds to a full-scale drop across the shunt. Full-scale range and the LSB of the current and power measurement depend on the value entered in this register. See the *Programming the INA220-Q1 Calibration Register*. This register is suitable for use in overall system calibration. Note that the 0 POR values are all default.

Figure 28. Calibration Register(1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) FS0 is a *void* bit and will always be 0. It is not possible to write a 1 to FS0. CALIBRATION is the value stored in FS15:FS1.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA220-Q1 is a digital current-shunt monitor with an I²C- and SMBus-compatible interface. It provides digital current, voltage, and power readings necessary for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for measurement resolution, and continuous-versus-triggered operation. See Table 3 for detailed register information. See Figure 29 for a block diagram of the INA220-Q1.

9.2 Typical Application

Figure 29 shows a typical application circuit for the INA220-Q1. Use a 0.1-µF ceramic capacitor for power-supply bypassing, placed as closely as possible to the supply and ground pins.

The input filter circuit consisting of R_{F1}, R_{F2}, and C_F is not necessary in most applications. If the need for filtering is unknown, reserve board space for the components and install 0-Ω resistors unless a filter is needed. See *Filtering and Input Considerations*.

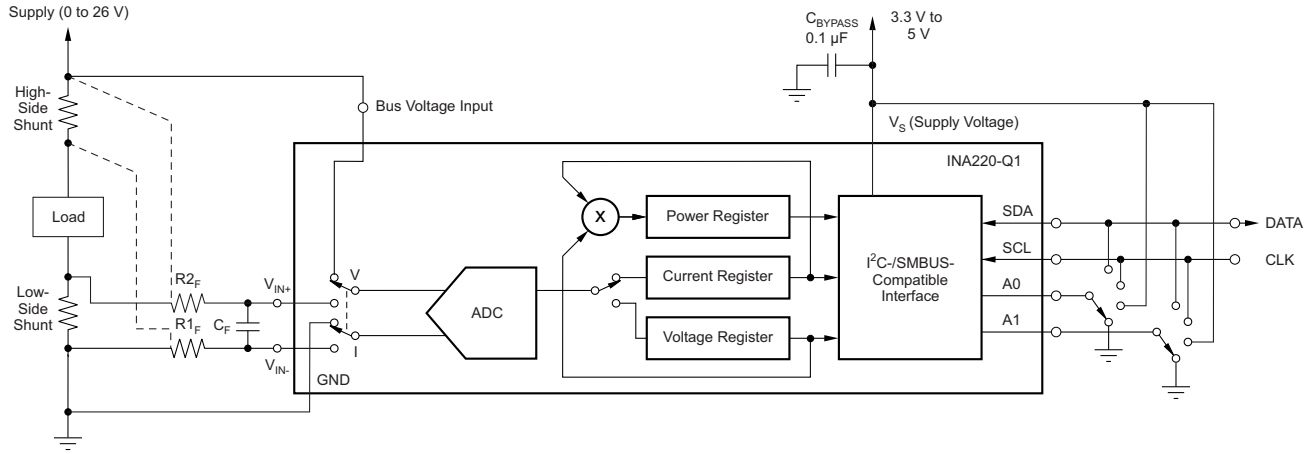


Figure 29. General Load, Low- or High-Side Sensing

9.2.1 Design Requirements

The INA220-Q1 measures the voltage across a current-sensing resistor (R_{SHUNT}) when current passes through the resistor. The device also measures the bus supply voltage, and calculates power when calibrated. This section goes through the steps to program the device for power measurements, and shows the register results in Table 8. The Conditions for the example circuit is: Maximum expected load current = 15 A, Nominal load current = 10 A, VCM = 12 V, R_{SHUNT} = 2 mΩ, V_{SHUNT} FSR = 40 mV (PGA = /1), and BRNG = 0 (VBUS range = 16 V).

9.2.2 Detailed Design Procedure

In this example, the 10-A load creates a differential voltage of 20 mV across a 2-mΩ shunt resistor. The voltage present at the IN– pin is equal to the common-mode voltage minus the differential drop across the resistor. The bus voltage for the INA220-Q1 is measured at the external VBUS input pin, which in this example is connected to the IN– pin to measure the voltage level delivered to the load. For this example, the voltage at the IN– pin is 11.98 V. For this particular range (40-mV full-scale), this small difference is not a significant deviation from the 12-V common-mode voltage. However, at larger full-scale ranges, this deviation can be much larger.

Typical Application (continued)

Note that the Bus Voltage register bits are not right-aligned. To compute the value of the Bus Voltage register contents using the LSB of 4 mV, the register must be shifted right by three bits. This shift puts the BD0 bit in the LSB position so that the contents can be multiplied by the 4-mV LSB value to compute the bus voltage measured by the device. The shifted value of the bus voltage register contents is now equal to BB3h, a decimal equivalent of 2995. This value of 2995 multiplied by the 4-mV LSB results in a value of 11.98 V.

The Calibration register (05h) is set to provide the device information about the current shunt resistor that was used to create the measured shunt voltage. By knowing the value of the shunt resistor, the device can then calculate the amount of current that created the measured shunt voltage drop. The first step when calculating the calibration value is setting the current LSB. The Calibration register value is based on a calculation that has its precision capability limited by the size of the register and the Current register LSB. The device can measure bidirectional current; thus, the MSB of the Current register is a sign bit that allows for the rest of the 15 bits to be used for the Current register value. For this example, the minimum current LSB would be 457.78 µA/bit assuming a maximum expected current of 15 A using Equation 2. For this example, a value of 1 mA/bit was chosen for the current LSB. Setting the current LSB to this value allows for sufficient precision while serving to simplify the math as well. Using Equation 1 results in a Calibration register value of 20480 or 5000h.

The Current register (04h) is internally calculated by multiplying the shunt voltage contents by the Calibration register and then dividing by 4096 using Equation 4. For this example, the shunt voltage of 2000 is multiplied by the Calibration register of 20480 and then divided by 4096 to yield a Current register value of 10000 (2710h).

The Power register (03h) is internally calculated by multiplying the Current register value of 10000 by the Bus Voltage register value of 2995 and then dividing by 5000 using Equation 5. For this example, the Power register contents are 5990 (1766h). Multiplying this result by the power LSB that is 20 times the 1×10^{-3} current LSB, or 20×10^{-3}, results in a power calculation of 5990 × 20 mW/bit, which equals 119.8 W. This result matches what is expected for this register. A manual calculation for the power being delivered to the load would use 11.98 V (12 VCM – 20 mV shunt drop) multiplied by the load current of 10 A to give a 119.8-W result.

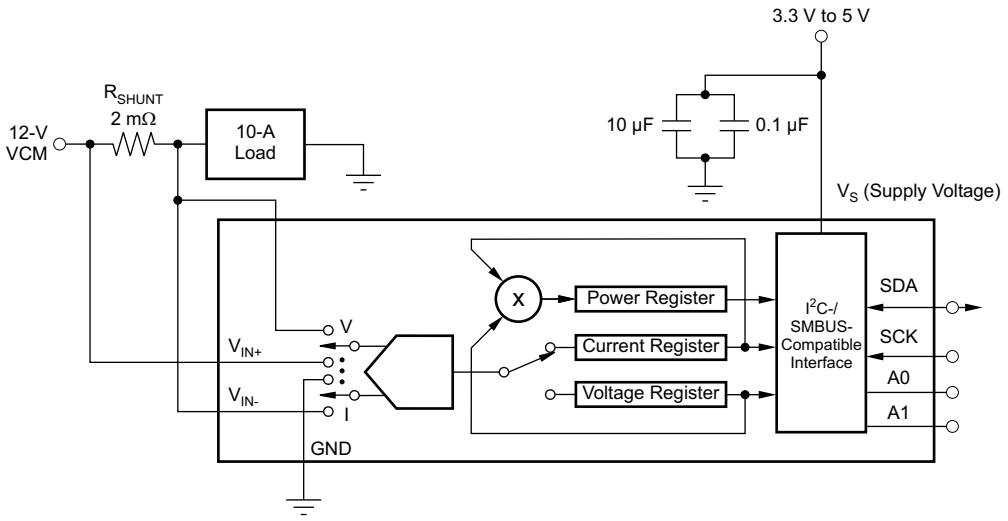


Figure 30. Example Circuit Configuration

Typical Application (continued)

9.2.2.1 Register Results for the Example Circuit

Table 8 shows the register readings for the Calibration example.

Table 8. Register Results (1)

REGISTER NAME	ADDRESS	CONTENTS	ADJ	DEC	LSB	VALUE
Configuration	00h	019Fh				
Shunt	01h	07D0h		2000	10 µV	20 mV
Bus	02h	5D98h	0BB3	2995	4 mV	11.98 V
Calibration	05h	5000h		20480		
Current	04h	2710h		10000	1 mA	10.0 A
Power	03h	1766h		5990	20 mW	119.8 W

(1) Conditions: load = 10 A, V_{CM} = 12 V, R_{SHUNT} = 2 mΩ, V_{SHUNT} FSR = 40 mV, and V_{BUS} = 16 V.

9.3 System Examples

Figure 31, Figure 32, and Figure 33 show the INA220-Q1 in additional circuit configurations for current, voltage, and power monitoring applications.

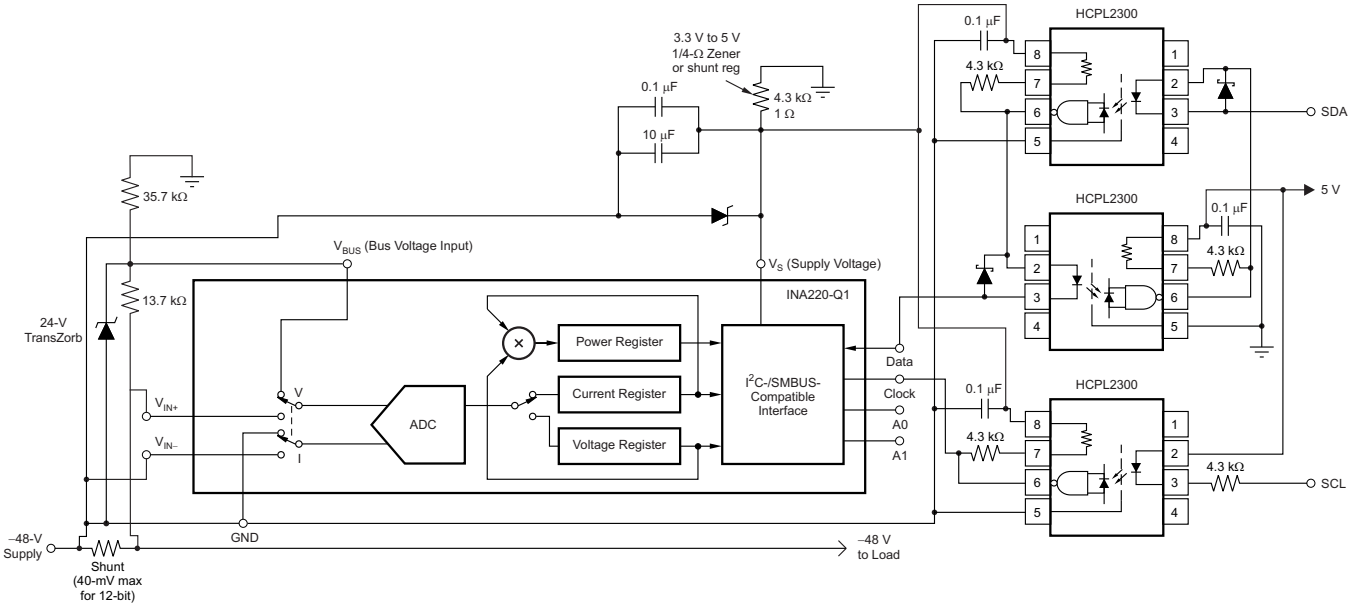


Figure 31. –48-V Telecom Current, Voltage, and Power Sense With Isolation

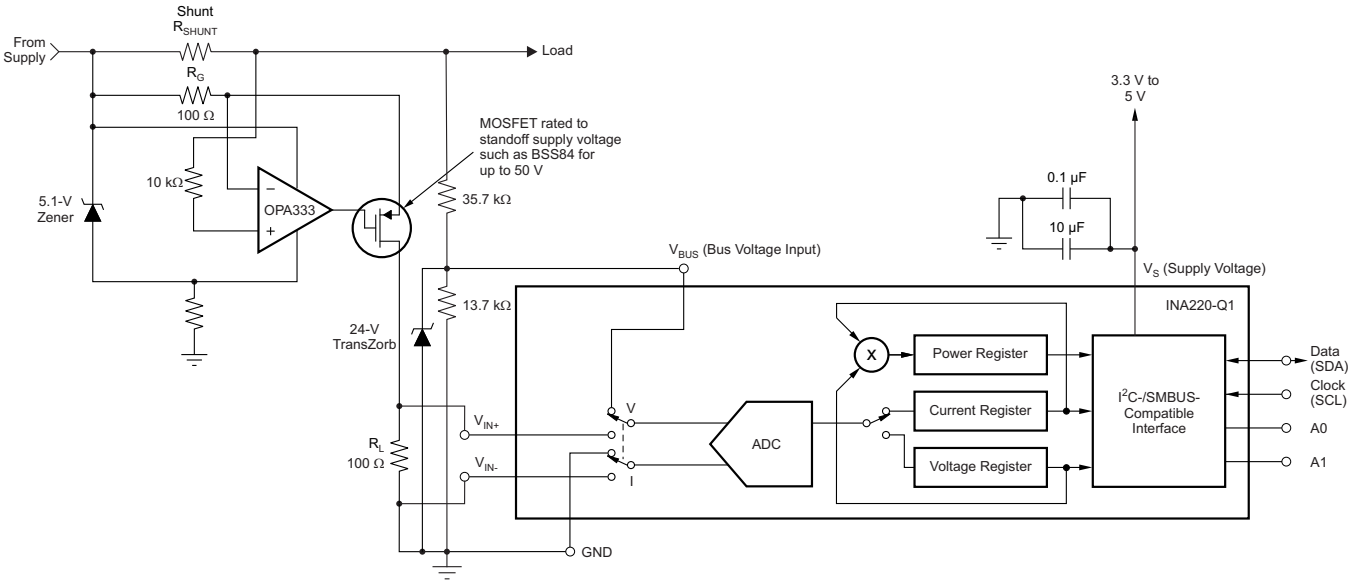


Figure 32. 48-V Telecom Current, Voltage, and Power Sense

System Examples (continued)

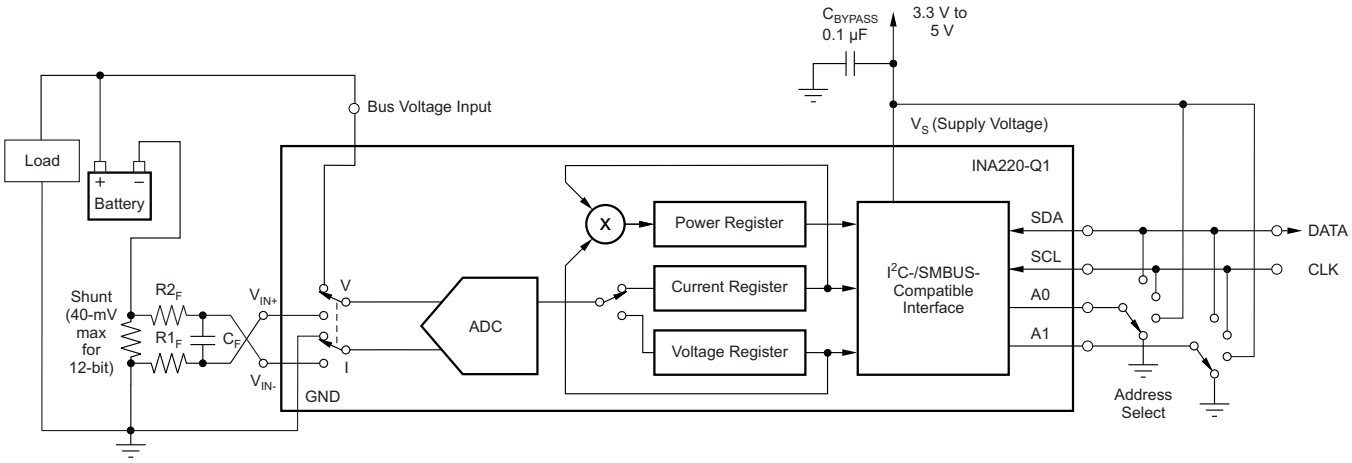


Figure 33. General Source Low-Side Sensing

10 Power Supply Recommendations

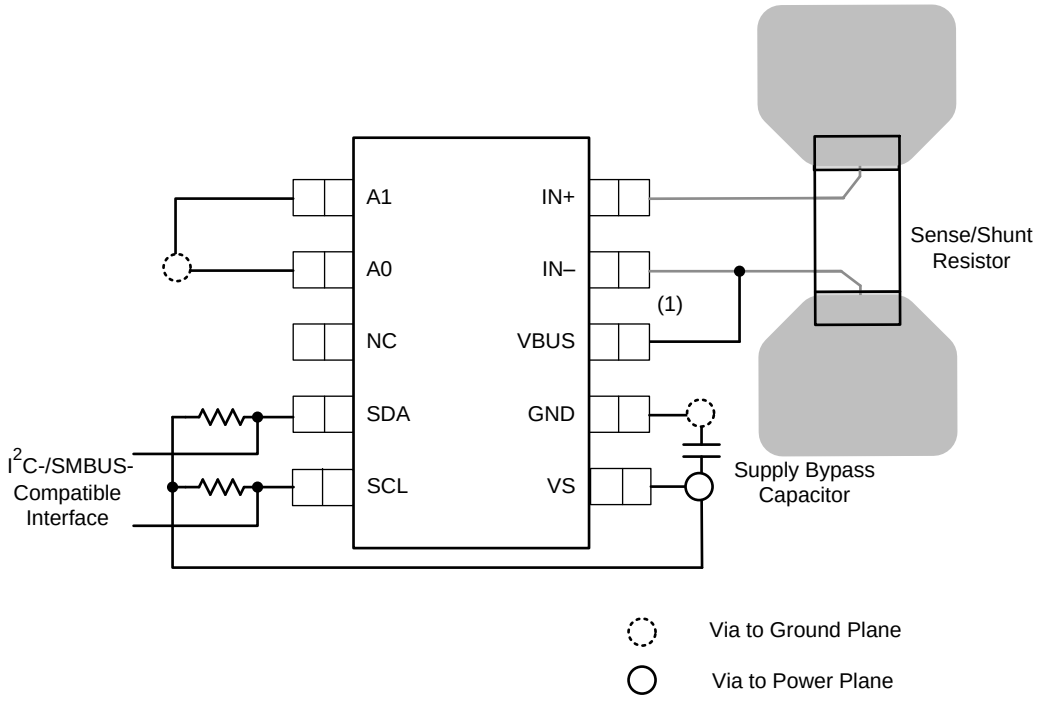
The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power supply voltage, V_S. For example, the voltage applied to the V_S power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 26 V. Note also that the device can withstand the full 0-V to 26-V range at the input terminals, regardless of whether the device has power applied or not. Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device to ensure stability. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

11 Layout

11.1 Layout Guidelines

Connect the input pins (IN+ and IN–) to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques ensure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

11.2 Layout Example



(1) Connect the VBUS pin to the power supply rail

Figure 34. Layout Recommendation

12 Device and Documentation Support

12.1 Related Documentation

For related documentation see the following:

- OPA333-Q1 *1.8-V Micropower CMOS Operational Amplifier Zero-Drift Series*, SBOS522
- TPS249x *Positive High-Voltage Power-Limiting Hotswap Controller*, SLVS503

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA220BQDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	IPUQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

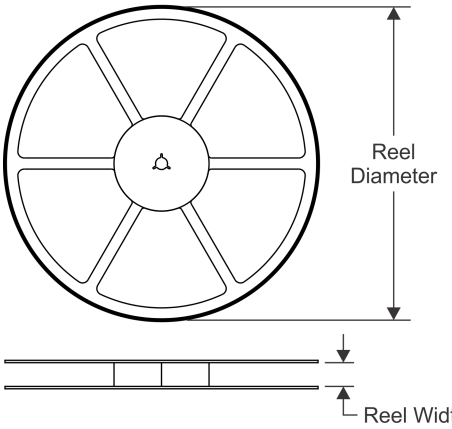
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

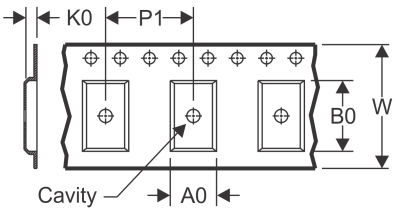
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

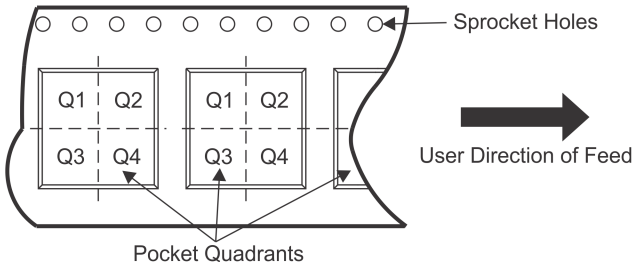


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

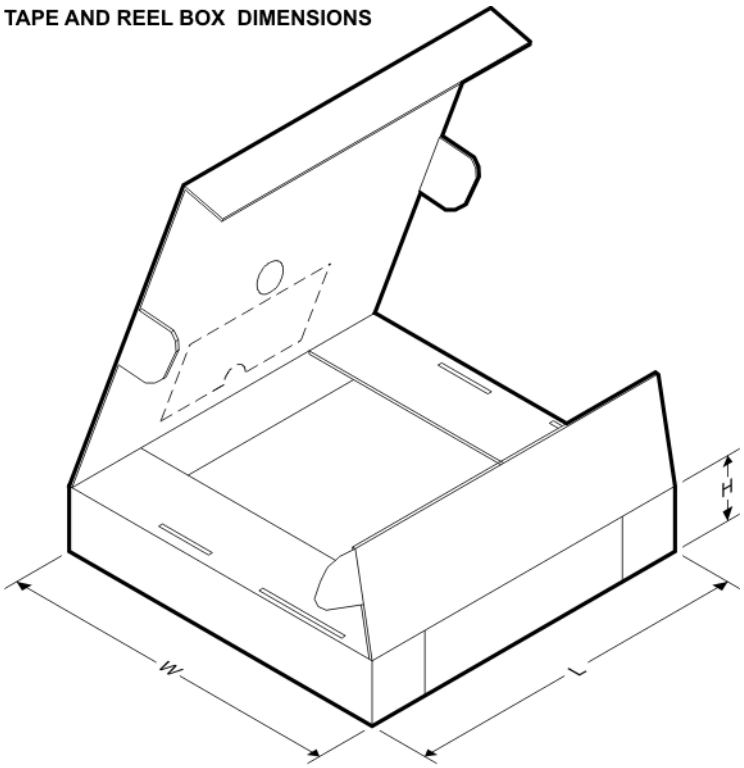
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA220BQDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

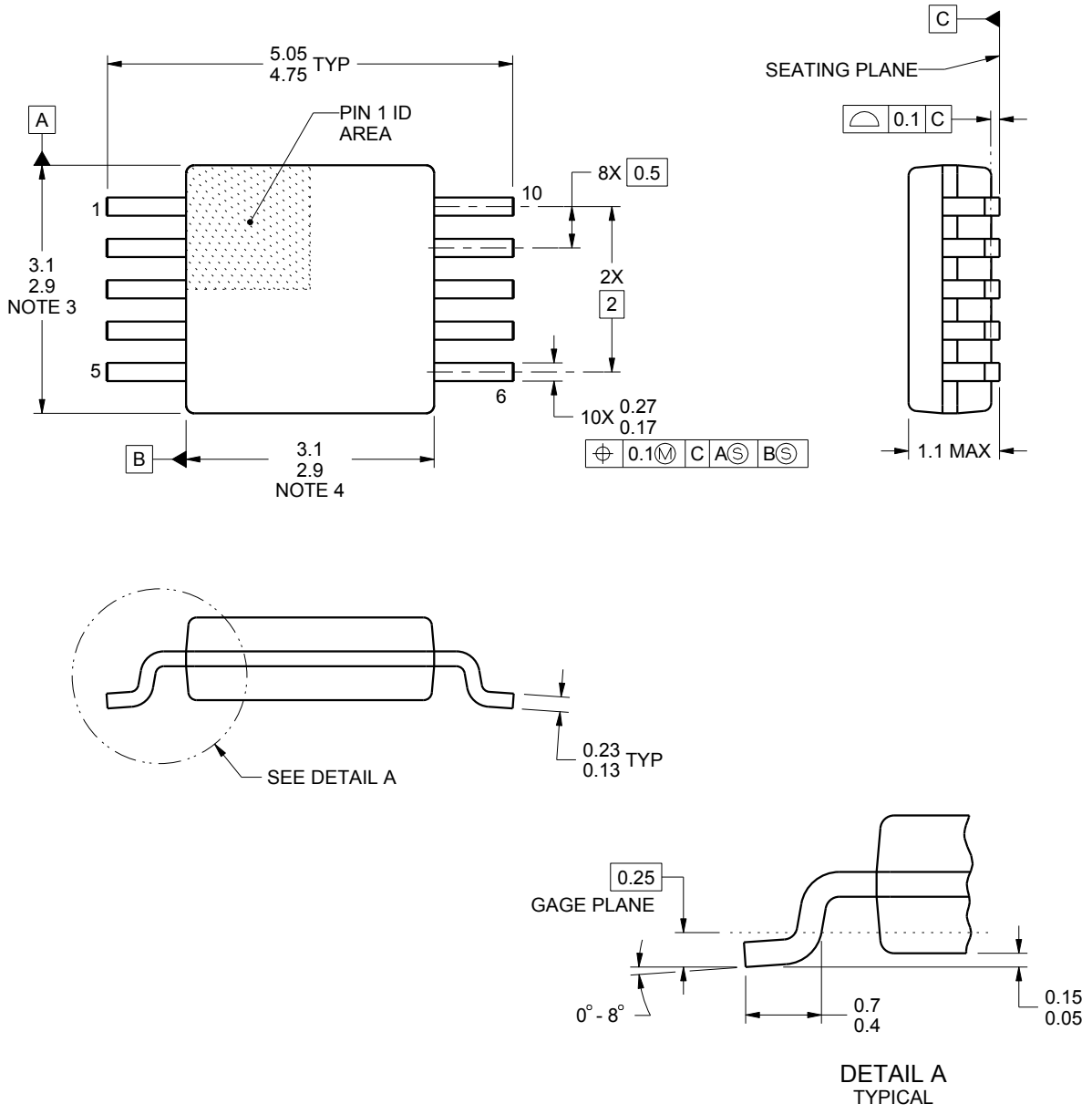
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA220BQDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGS0010A

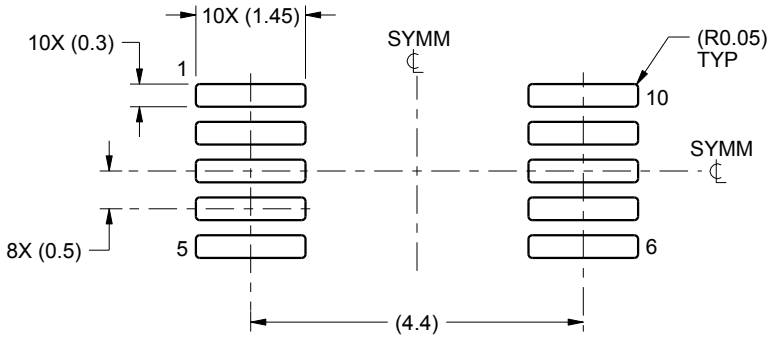
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

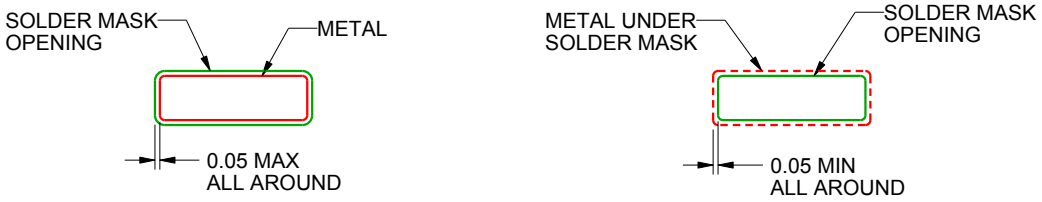


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

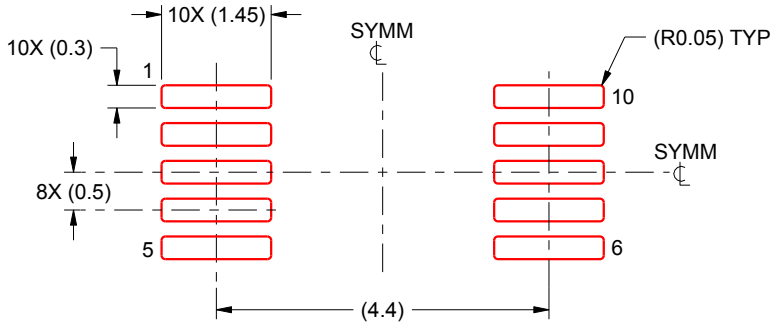


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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- Alternative Solution
- Excess Inventory Management