THE DATASHEET OF

SAK-C868-1SG BA

Data Sheet, V 1.0, May 2003

C868

8-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

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C868

Revision History:	**2003-05**	V 1.0
Previous Version:	-	

Page	Subjects (major changes since last revision)
	Current data updated
	Description of I2C included

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C868

Advance Information

- C800 core :
  –Fully compatible to standard 8051 microcontroller
  –Superset of the 8051 architecture with 8 datapointers
- 40 MHz internal CPU clock
  –external clock of *6.67 - 10.67* MHz at 50% duty cycle
  –*300* ns instruction cycle time (@37.5 MHz CPU clock)
- 8 Kbyte on-chip Program ROM for C868-1R and 8 KByte on-chip Program RAM for C868-1S
- In-system programming support for programming the XRAM(C868-1R) or XRAM/ Program RAM(C868-1S)
  –This feature is realized through 4KB Boot ROM
- 256 byte on-chip RAM
- 256 byte on-chip XRAM

(further features are on the next page)

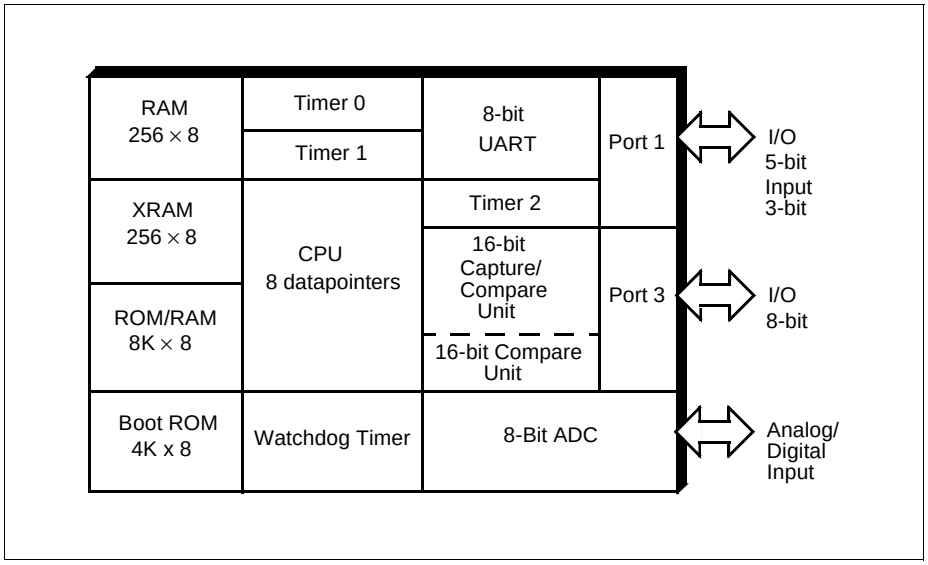

Figure 1 C868 Functional Units

- One 8-bit and one 5 bits general purpose push-pull I/O ports
  – Enhanced sink current of 10 mA on Port 1/3 (total max current of 43 mA @ 100^{o}C)
- Three 16-bit timers/counters
  –Timer 0 / 1 (C501 compatible)
  –Timer 2 (up/down counter feature)
  –Timer 1 or 2 can be used for serial baudrate generator
- Capture/compare unit for PWM signal generation
  –3-channel, 16-bit capture/compare unit
  –1-channel, 16-bit compare unit
- Full duplex serial interface (UART)
- 5 channel 8-bit A/D Converter
  – Start of conversion can be synchronized to capture/compare timer 12/13.
- 13 interrupt vectors with four priority levels
- Programmable 16-bit Watchdog Timer
- Brown out detection
- Power Saving Modes
  –Slow-down mode
  –Idle mode (can be combined with slow-down mode)
  –Power-down mode with wake up capability through $\overline{\text{INT0}}$ or RxD pins.
- Single power supply of 3.3V, internal voltage regulator for core voltage of 2.5V.
- P-DSO-28-1, P-TSSOP-38-1 packages
- Temperature ranges:
  SAF-C868-1RR BA, SAF-C868-1SR BA, SAF-C868-1RG BA, SAF-C868-1SG BA, SAF-C868A-1RR BA, SAF-C868A-1SR BA, SAF-C868A-1RG BA, SAF-C868A-1SG BA, SAF-C868P-1SR BA, SAF-C868P-1SG BA T_A = – 40 to 85 ^{o}C
  SAK-C868-1RR BA, SAK-C868-1SR BA, SAK-C868-1RG BA, SAK-C868-1SG BA, SAK-C868A-1RR BA, SAK-C868A-1SR BA, SAK-C868A-1RG BA, SAK-C868A-1SG BA, SAK-C868P-1SR BA, SAK-C868P-1SG BA T_A = – 40 to 125 ^{o}C

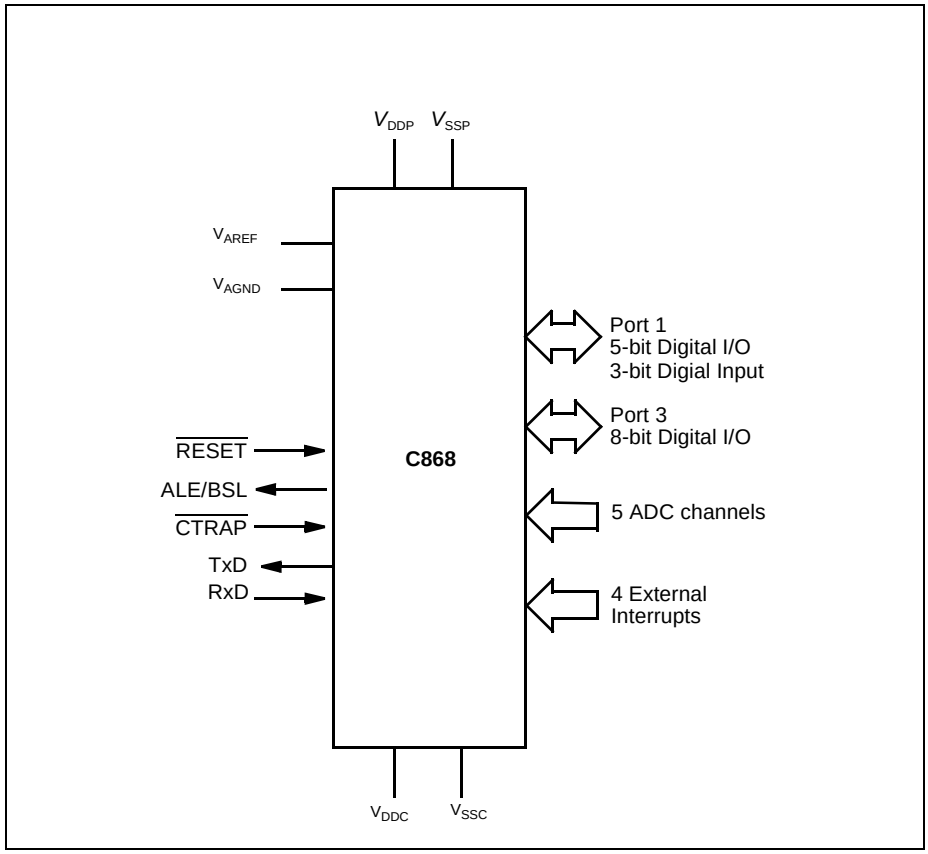

Figure 2 Logic Symbol

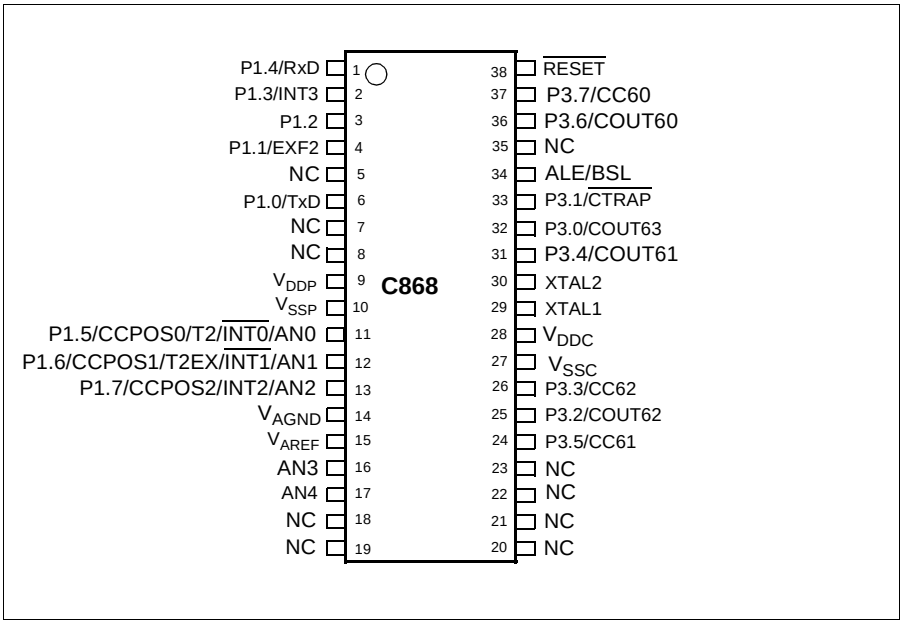

Figure 3 C868 Pin Configuration P-TSSOP-38 Package (top view**)**

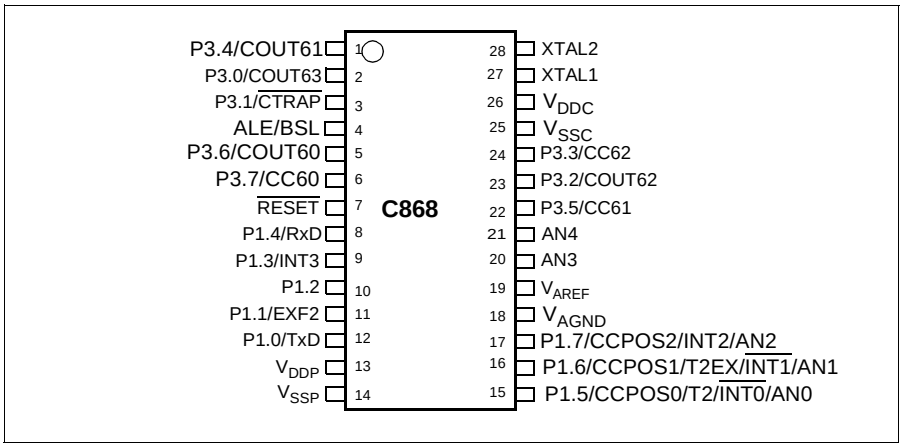

Figure 4 C868 Pin Configuration P-DSO-28 Package (top view)

Table 1 Pin Definitions and Functions

Symbol	Pin Numbers		I/O*)	Function
	P-DSO-28	P-TSSOP-38		
P1.0–P1.4	12-8	6,4-1	I/O	**Port 1** is a combination of 5 bits of push-pull bidirectional I/O ports and 3 bits of input ports. As alternate digital functions, port 1 contains the interrupt 3, timer 2 overflow flag, receive data input and transmit data output of serial interface. The alternate functions are assigned to the pins of port 1 as follows:
P1.5-P1.7	15-17	11-13	I	
	12	6		P1.0/TxD Transmit data of serial interface
	11	4		P1.1/EXF2 Timer 2 overflow flag
	10	3		P1.2
	9	2		P1.3/INT3 Interrupt 3
	8	1		P1.4/RxD Receive data of serial interface, Use as wakeup source from powerdown if bit WS of PMCON0 is set.
				The input ports are also interrupt ports, input to the timer2, CCU6 modules and ADC:
	15	11	I	P1.5/Input to Counter 2/External Interrupt 0 Input/ Analog Input Channel 0 External interrupt input or Hall input signal, counter 2 input or input channel 0 to the ADC unit. Use as wakeup source from powerdown if bit WS of PMCON0 is cleared.
	16	12	I	P1.6/Timer 2 Trigger/External Interrupt 1 Input/ Analog Input Channel 1 External interrupt input or Hall input signal, input channel 1 to the ADC unit, trigger to Timer 2.
	17	13	I	P1.7/External Interrupt 2 Input/ Analog Input Channel 2 External interrupt input or Hall input signal and input channel 2 to the ADC unit.

*)I=Input
O=Output

Table 1 Pin Definitions and Functions

Symbol	Pin Numbers		I/O*)	Function
	P-DSO-28	P-TSSOP-38		
P3.0–P3.7	2,3,23,24,1,22,5,6	32,33,25,26,31,24,36,37	I/O	**Port 3** is an 8-bit push-pull bidirectional I/O port. This port also serves as alternate functions for the CCU6 functions. The functions are assigned to the pins of port 3 as follows : 2 32 P3.0/COUT63 16 bit compare channel output 3 33 P3.1/CTRAP CCU trap input 23 25 P3.2/COUT62 Output of capture/compare ch 2 24 26 P3.3/CC62 Input/output of capture/compare ch 2 1 31 P3.4/COUT61 Output of capture/compare ch 1 22 24 P3.5/CC61 Input/output of capture/compare ch 1 5 36 P3.6/COUT60 Output of capture/compare ch 0 6 37 P3.7/CC60 Input/output of capture/compare ch 0
V_{AREF}	19	15	–	**Reference voltage** for the A/D converter.
V_{AGND}	18	14	–	**Reference ground** for the A/D converter.
AN4	21	17	I	**Analog Input Channel 4** is input channel 4 to the ADC unit.
AN3	20	16	I	**Analog Input Channel 3** is input channel 3 to the ADC unit.
$\overline{\text{RESET}}$	7	38	I	**$\overline{\text{RESET}}$** A low level on this pin for two machine cycle while the oscillator is running resets the device.
ALE/BSL	4	34	I/O	**Address Latch Enable/Bootstrap Mode** A low level on this pin during reset allows the device to go into the bootstrap mode. After reset, this pin will output the address latch enable signal. The ALE can be disabled by bit EALE in SFR SYSCON0.
V_{SSP}	14	10	–	**IO Ground** (0V)
V_{DDP}	13	9	–	**IO Power Supply** (+3.3V)

*)I=Input
O=Output

Table 1 Pin Definitions and Functions

Symbol	Pin Numbers		I/O*)	Function
	P-DSO-28	P-TSSOP-38		
V_{SSC}	25	27	–	**Core Ground** (0V)
V_{DDC}	26	28	O	**Core Internal Reference** (+2.5V) Connect 2*68 - 470nF ceramic capacitor across this pin and core ground.
NC	–	5,7,8,18, 19,20,21, 22,23,35	–	**Not connected**
XTAL1	27	29	I	**XTAL1** Output of the inverting oscillator amplifier.
XTAL2	28	30	O	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generation circuits. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected.

*)I=Input
O=Output

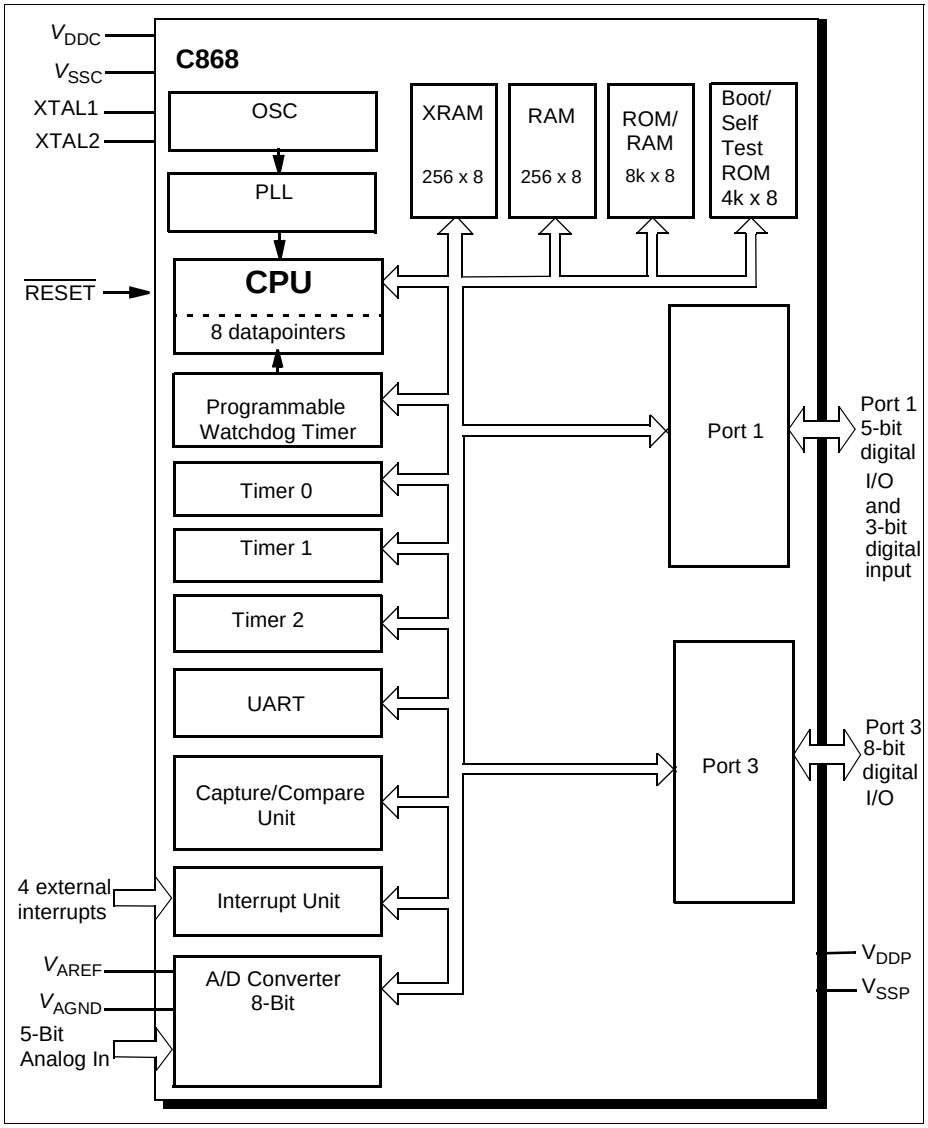

Figure 5 Block Diagram of the C868

CPU

The C868 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 10.67 MHz external crystal (giving a 40MHz CPU clock), 58% of the instructions execute in 300 ns.

PSW

Program Status Word Register **[Reset value: 00_H]**

$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$
CY	**AC**	**F0**	**RS1**	**RS0**	**OV**	**F1**	**P**
rwh	rwh	rw	rw	rw	rwh	rw	rwh

Field	Bits	Typ	Description
P	0	rwh	**Parity Flag** Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.
F1	1	rw	**General Purpose Flag**
OV	2	rwh	**Overflow Flag** Used by arithmetic instructions.
RS0 **RS1**	3 4	rw	**Register Bank select control bits** These bits are used to select one of the four register banks. **Table 2 :** **RS1** / **RS0** / **Function** 0 / 0 / Bank 0 selected, data address 00_H-07_H 0 / 1 / Bank 1 selected, data address 08_H-$0F_H$ 1 / 0 / Bank 2 selected, data address 10_H-17_H 1 / 1 / Bank 3 selected, data address 18_H-$1F_H$
F0	5	rw	**General Purpose Flag**
AC	6	rwh	**Auxiliary Carry Flag** Used by instructions which execute BCD operations.
CY	7	rwh	**Carry Flag** Used by arithmetic instructions.

Memory Organization

The C868 CPU manipulates operands in the following five address spaces:

- up to 8 Kbyte of RAM internal program memory : 8K ROM for C868-1R
  : 8K RAM for C868-1S
- 4 Kbyte of internal Self test and Boot ROM
- 256 bytes of internal data memory
- 256 bytes of internal XRAM data memory
- 128 byte special function register area

Figure 0-1 illustrates the memory address spaces of the C868.

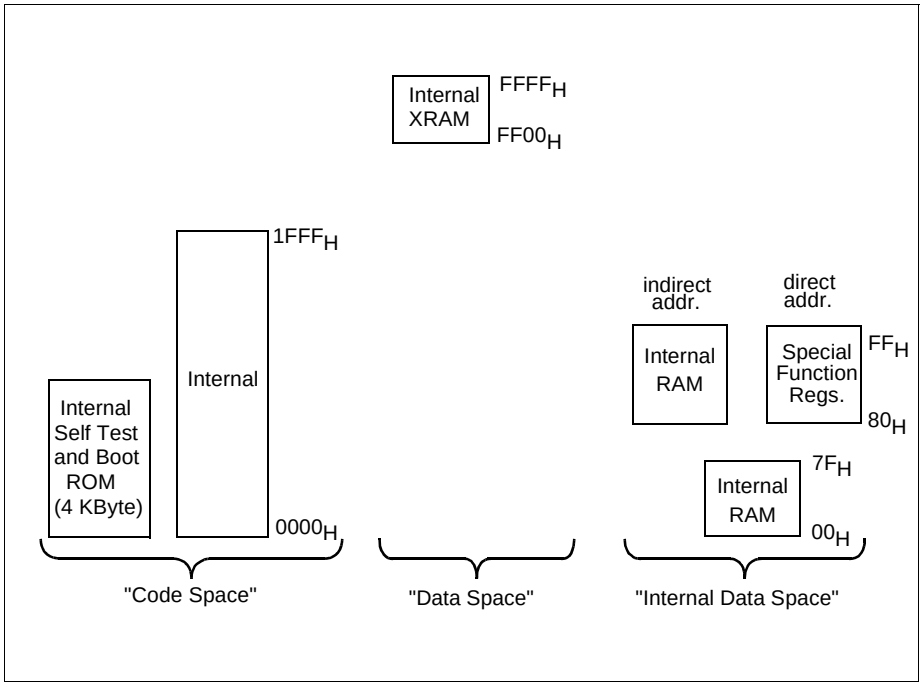

Figure 0-1 C868 Memory Map

The various chip modes supported are shown in **Figure 6**.

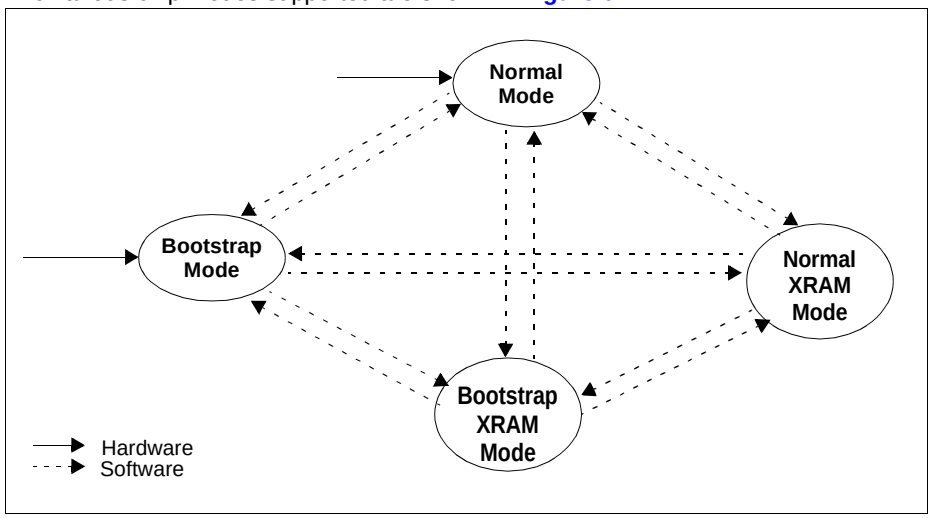

Figure 6 Entry and exit of Chip Modes

A valid hardware reset would, of course, override any of the above entry or exit procedures.

Table 0-1 Hardware and Software Selection of Chipmodes

Operating Mode (Chipmode)	Hardware Selection	Software Selection
Normal Mode	ALE/BSL pin = high RESET rising edge	ALE/BSL = don't care; setting bits BSLEN, SWAP = 0,0; execute unlocking sequence
Normal XRAM Mode	Not possible	setting bits BSLEN,SWAP = 0,1; execute unlocking sequence
Bootstrap XRAM Mode	Not possible	setting bits BSLEN,SWAP = 1,1; execute unlocking sequence
Bootstrap Mode	ALE/BSL pin = low RESET rising edge	ALE/BSL = don't care; setting bits BSLEN, SWAP = 1,0; execute unlocking sequence

Table 3 Normal Memory Configuration

Chip Mode	Memory Space	Memory Boundary
Normal	Code Space	ROM/RAM: 0000_H to $1FFF_H$
	Internal Data Space	XRAM: $FF00_H$ to $FFFF_H$
Bootstrap	Code Space	Boot ROM: 0000_H to $0FFF_H$
	Internal Data Space	XRAM: $FF00_H$ to $FFFF_H$ ROM/RAM: 0000_H to $1FFF_H$
Normal XRAM	Code Space	XRAM: $FF00_H$ to $FFFF_H$
	Data Space	ROM/RAM: 0000_H to $1FFF_H$
Bootstrap XRAM	Code Space	Boot ROM: 0000_H to $0FFF_H$ XRAM: $FF00_H$ to $FFFF_H$
	Data Space	ROM/RAM: 0000_H to $1FFF_H$

Bootstrap loader

The C868, includes a bootstrap mode, which is activated by setting the ALE/BSL pin at logic low with a pulldown and TxD pin at logic high with a pullup at the rising edge of the RESET. Or it can be entered by software, that is by setting BSLEN bit and resetting SWAP bit in SFR SYSCON1 accompany by an unlock sequence.

In the bootstrap mode, software routines of the bootstrap loader located in the boot ROM will be executed. Its purpose is to allow the easy and quick programming of the internal SRAM (0000_H to $1FFF_H$) or XRAM ($FF00_H$ to $FFFF_H$) via serial interface (UART) while the MCU is in-circuit. It also provides a way to program SRAM or XRAM through bootstrapping from an external SPI or I2C EEPROM.

The first action of the bootstrap loader is to detect the presence of EEPROM and its type, SPI or I2C, and check the first byte of the serial EEPROM. If the first byte is $0A5_H$, the MCU would enter Phase A to download from the EEPROM. Otherwise, it will enter Phase B to establish a serial communication with the connected host. Bootstrapping from the serial EEPROM can also be done in phase B if it is invoked by the host.

Phase B consists of two functional parts that represent two phases:

- Phase I: Establish a serial connection and automatically synchronize to the transfer speed (baud rate) of the serial communication partner (host).
- Phase II: Perform the serial communication with the host. The host controls the communication by sending special header information, which select one of the working modes. These modes are:

Table 4 Serial Communication Modes of Phase B

Modes	Description
0	Transfer a customer program from the host to the SRAM (0000_H to $1FFF_H$) or XRAM ($FF00_H$ -$FFFF_H$). Then return to the beginning of phase II and wait for the next command from the host.
1	Execute a customer program in the XRAM at start address $FF00_H$.
2	Execute a customer program in the SRAM at start address 0000_H.
3	Transfer a customer program from the SPI EEPROM to the SRAM (0000_H to $1FFF_H$) or XRAM ($FF00_H$ -$FFFF_H$). Then return to the beginning of phase II and wait for the next command from the host.
4	Transfer a customer program from the I2C EEPROM to the SRAM (0000_H to $1FFF_H$) or XRAM ($FF00_H$ -$FFFF_H$). Then return to the beginning of phase II and wait for the next command from the host.
5-9	reserved

The phases of the bootstrap loader are illustrated in **Figure 7**.

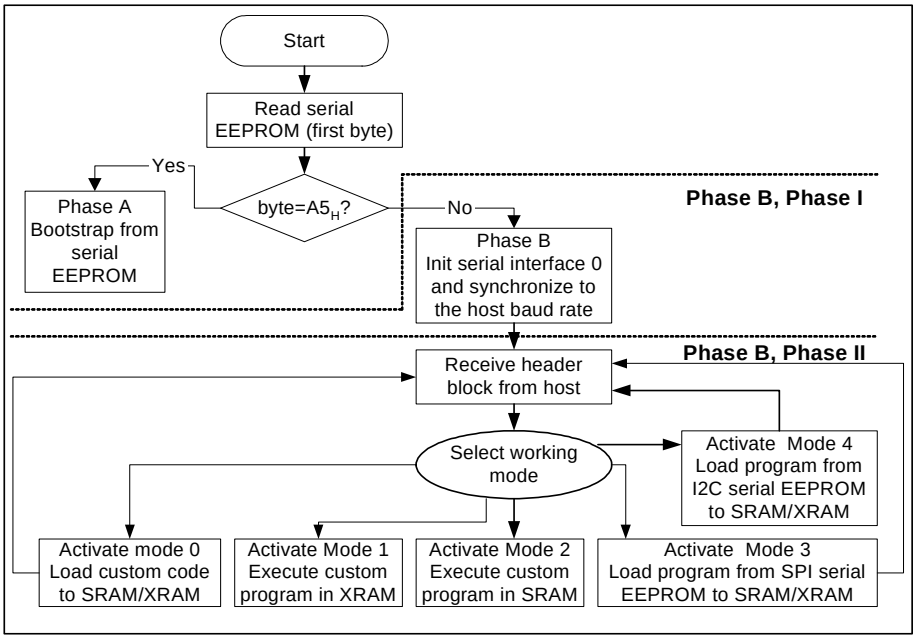

Figure 7 The phases of the Bootstrap Loader

The serial communication is activated in phase B. Using a full duplex serial cable (RS232), the MCU must be connected to the serial port of the host computer as shown in **Figure 8**.

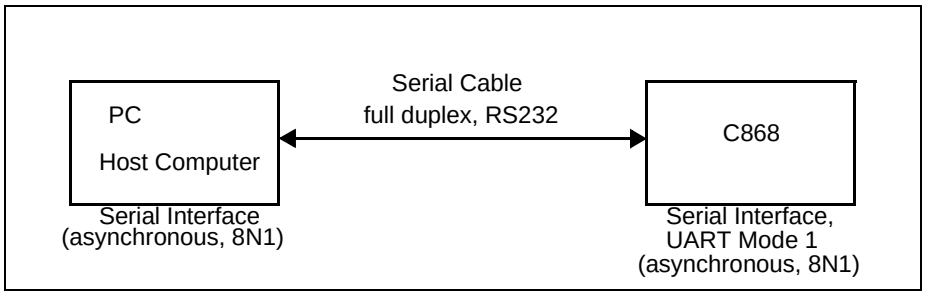

Figure 8 Bootstrap Loader Interface to the PC

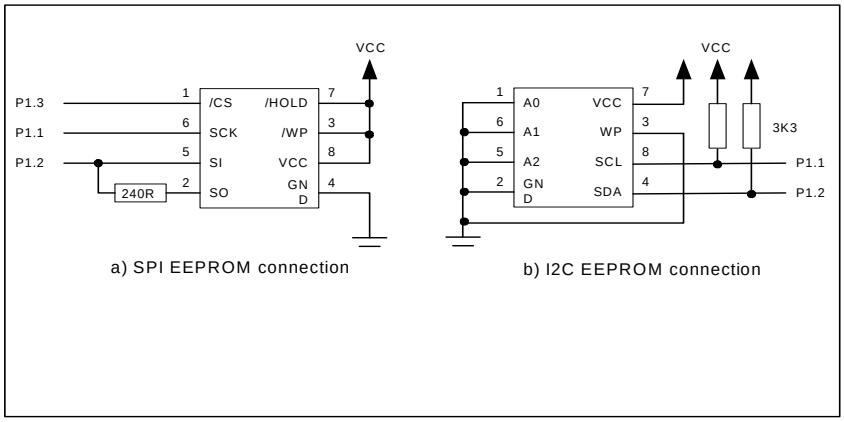

Figure 9 EEPROM connections for a) SPI and b) I2C

Reset and Brownout

The reset input is an active low input. An internal Schmitt trigger is used at the input for noise rejection. The $\overline{\text{RESET}}$ pin must be held low for at least tbd usec. But the CPU will only exit from reset condition after the PLL lock had been detected.

During $\overline{\text{RESET}}$ at transition from low to high, C868 will go into normal mode if ALE/BSL is high and bootstrap loading mode if ALE/BSL is low. A pullup to V_{DDP} or pulldown to ground is recommended for pin ALE/BSL. TXD should have a pullup to V_{DDP} and should not be stimulated externally during reset, as a logic low at this pin will cause the chip to go into test mode if ALE/BSL is low.

Figure 10 shows the possible reset circuits, note that the $\overline{\text{RESET}}$ pin does not have an internal pullup resistance.

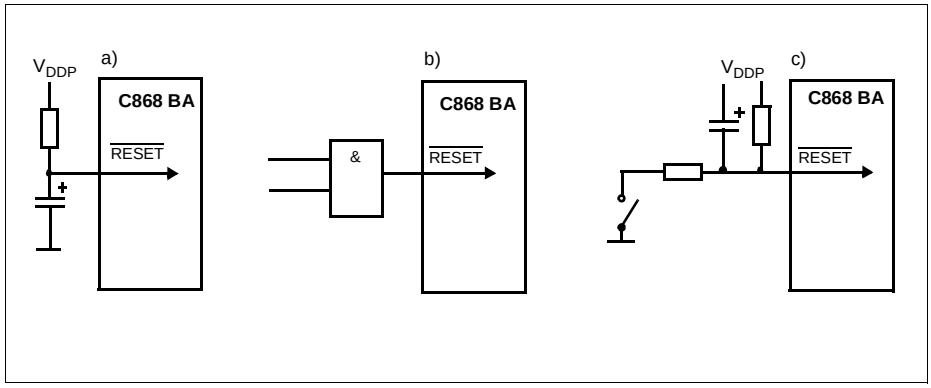

Figure 10 Reset Circuitries

An on-chip analog circuit detects brownout, if the core voltage V_{DDC} dips below the threshold voltage $V_{THRESHOLD}$ momentarily while $\overline{\text{RESET}}$ pin is high. If this detection is active for tbd usec then the device will reset. When V_{DDC} recovers by exceeding $V_{THRESHOLD}$ while $\overline{\text{RESET}}$ is high, the reset is released once PLL is locked for 4096 clocks. Bit BO in the PMCON0 register is set when brownout detected if brownout detection was enabled, this bit is cleared by hardware reset $\overline{\text{RESET}}$ and software. All ports are tristated during brownout.

The $V_{THRESHOLD}$ has a nominal value of 1.47V, a minimum value of 1.1V and a maximum value of 1.8V.

Clock system

The C868 clock system consist of the on-chip oscillator, PLL and multiplexer stage. The programmable Slow Down Divider (SDD) divides the PLL output clock frequency by a factor of 1...32 which is specified via CMCON.REL. The system clock is switched from the PLL output to the output from the SDD when slowdown mode is selected.

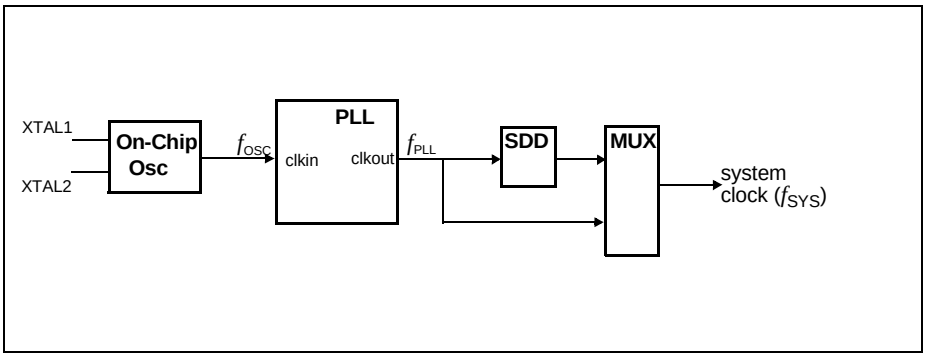

Figure 11 Block Diagram of the Clock Generation

The PLL output frequency is determined by:

$$f_{PLL} = f_{VCO} / K = \frac{15}{K} \times f_{OSC} \quad [1]$$

The range for the VCO frequency is given by:

$$100\ MHz \leq f_{VCO} \leq 160\ MHz \quad [2]$$

The relationship between the input frequency and VCO frequency is given by:

$$f_{VCO} = 15 \times f_{OSC} \quad [3]$$

This gives the range for the input frequency which is given by:

$$6.67\ MHz \leq f_{OSC} \leq 10.67\ MHz \quad [4]$$

Table 5 Output Frequencies f_{PLL} Derived from Various Output Factors

K-Factor		f_{PLL}		Duty Cycle [%]	Jitter
Selected Factor	**KDIV**	**f_{VCO} = 100 MHz**	**f_{VCO} = 160 MHz**		
2	000_B	50	80	50	linear depending on f_{VCO} at f_{VCO} =100MHz: +/-300ps at f_{VCO} =160MHz: +/-250ps additional jitter for odd Kdiv factors tbd.
4	010_B	25	40	50	
5[1)]	011_B	20	32	40	
6	100_B	16.67	26.67	50	
8	101_B	12.5	20	50	
9[1)]	110_B	11.11	17.78	44	
10	111_B	10	16	50	
16	001_B	6.25	10	50	

1) These odd factors should not be used (not tested because off the unsymmetrical duty cycle).

2) Shaded combinations should not be used because they are above the maximum CPU frequency of 40MHz.

Figure 12 shows the recommended oscillator circuitries for crystal and external clock operation.

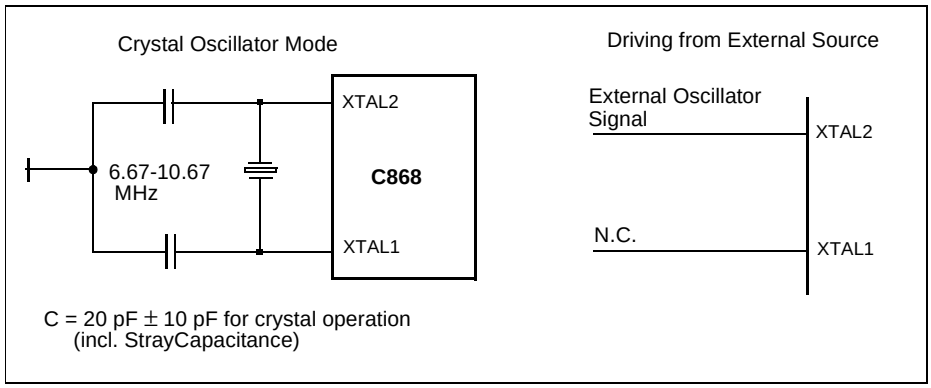

Figure 12 Recommended Oscillator Circuit

In this application the on-chip oscillator is used as a crystal-controlled, positive-reactance oscillator (a more detailed schematic is given in **Figure 13**). It is operated in its fundamental response mode as an inductive reactor in parallel resonance with a capacitor external to the chip. The crystal specifications and capacitances are non-critical. In this circuit tbd pF can be used as single capacitance at any frequency together with a good quality crystal. A ceramic resonator can be used in place of the crystal in cost-critical applications. If a ceramic resonator is used, the two capacitors normally have different values depending on the oscillator frequency. We recommend consulting the manufacturer of the ceramic resonator for value specifications of these capacitors.

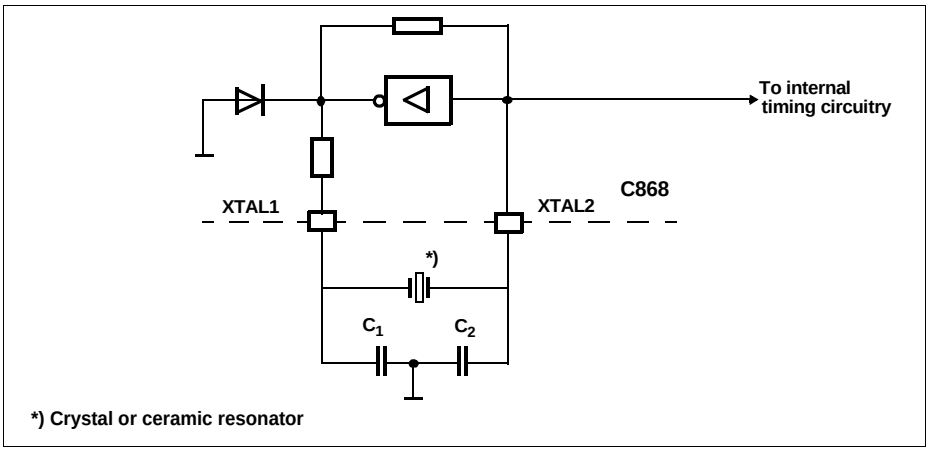

Figure 13 On-Chip Oscillator Circuitry

To drive the C868 with an external clock source, the external clock signal has to be applied to XTAL2, as shown in **Figure 14**. XTAL1 has to be left unconnected. A pullup resistor is suggested (to increase the noise margin), but is optional if V_{OH} of the driving gate corresponds to the V_{IH2} specification of XTAL2.

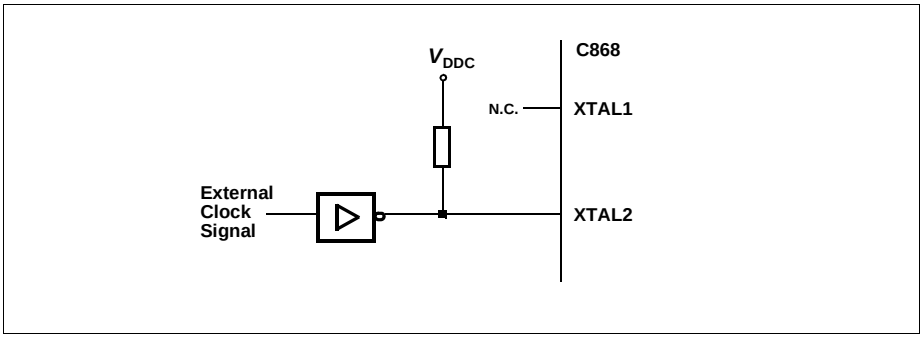

Figure 14 External Clock Source

0.1 Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions: the standard special function register area and the mapped special function register area. For accessing the mapped special function area, bit RMAP in special function register SYSCON0 must be set. All other special function registers are located in the standard special function register area which is accessed when RMAP is cleared (“0“).

SYSCON0
System Control Register 0 **[Reset value: XX10XXX1$_B$]**

7	6	5	4	3	2	1	0
-	**-**	**EALE**	**RMAP**	**-**	**-**	**-**	**XMAP0**
r	r	rw	rw	r	r	r	rw

The functions of the shaded bits are not described here

Field	Bits	Typ	Description
RMAP	4	rw	**Special Function Register Map Control** RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled. RMAP = 1 : The access to the mapped special function register area is enabled.
-	[7:2]	r	**reserved;** returns ’0’ if read; should be written with ’0’;

As long as bit RMAP is set, the mapped special function register area can be accessed. This bit is not cleared automatically by hardware. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set respectively by software.

The 109 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. All available SFRs whose address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, ..., $F0_H$, $F8_H$) are bit- addressable. Totally there are 128 directly addressable bits within the SFR area.

All SFRs are listed in **Table 6** and **Table 7**.In **Table 6** they are organized in groups which refer to the functional blocks of the C868-1R, C868-1S. **Table 7** illustrates the contents (bits) of the SFRs

Table 6 Special Function Registers - Functional Blocks

Block	Symbol	Name	Add-ress	Contents after Reset
C800 core	ACC	Accumulator	**$E0_H$**[1]	**00_H**
	B	B-Register	**$F0_H$**[1]	**00_H**
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	84_H	00_H
	PSW	Program Status Word Register	**$D0_H$**[1]	**00_H**
	SP	Stack Pointer	81_H	07_H
	SCON	Serial Channel Control Register	**98_H**[1]	**00_H**
	SBUF	Serial Data Buffer	99_H	00_H
	IEN0	Interrupt Enable Register 0	**$A8_H$**[1]	**$0X000000_B$**[2]
	IEN1	Interrupt Enable Register 1	$A9_H$	$XXXXX000_B$[2]
	IEN2	Interrupt Enable Register 2	AA_H	$XX0000XX_B$[2]
	IP0	Interrupt Priority Register 0	**$B8_H$**[1]	**$XX000000_B$**[2]
	IP1	interrupt Priority Register 1	AC_H	$XX000000_B$[2]
	TCON	Timer 0/1 Control Register	**88_H**[1]	**00_H**
	TMOD	Timer Mode Register	89_H	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	PCON	Power Control Register	87_H	$0XXX0000_B$[2]
Sys-tem	PMCON0	Wake-up Control Register	$8E_H$	$XXX00000_B$[2]
	CMCON	Clock Control Register	$8F_H$	10011111_B
	EXICON	External Interrupt Control Register	91_H	$XXXXXX00_B$[2]
	IRCON0	External Interrupt Request Register	92_H	$XXXXXX00_B$[2]
	IRCON1	Peripheral Interrupt Request Register	93_H	$XX0000X0_B$[2]
	PMCON1	Peripheral Management Ctrl Register	**$E8_H$**[1]	**$XXXXX000_B$**[2]
	PMCON2	Peripheral Management Status Register	**$F8_H$**[1]	**$XXXXX000_B$**[2]
	SCUWDT	SCU/Watchdog Control Register	**$C0_H$**[1]	**$X0X00000_B$**[2]
	VERSION	ROM Version Register	$F9_H$	00_H
	SYSCON0	System Control Register 0	AD_H	$XX10XXX1_B$[2]
	SYSCON1	System Control Register 1	AF_H	$00XXX0X0_B$[2]

1) Bit-addressable special function registers
2) "X" means that the value is undefined and the location is reserved
3) Register is mapped by bit RMAP in SYSCON0.4=1
4) Register is mapped by bit RMAP in SYSCON0.4=0

Table 6 Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Add-ress	Contents after Reset
A/D-Con-verter	ADCON0 ADCON1 ADDATH	A/D Converter Control Register 0 A/D Converter Control Register 1 A/D Converter Data Register	**$D8_H$** [1] $D9_H$ DB_H	**00_H** $XX000000_B$ [2] 00_H
Ports	P1 [4] P1DIR [3] P3 [4] P3DIR [3] P3ALT P1ALT	Port 1 Register Port 1 Direction Register Port 3 Register Port 3 Direction Register Port 3 Alternate Function Register Port 1 Alternate Function Register	**90_H** [1] **90_H** [1] **$B0_H$** [1] **$B0_H$** [1] $B1_H$ $B4_H$	**FF_H** **FF_H** **FF_H** **FF_H** 00_H $XXX00X00_B$ [2]
Watch-dog	WDTCON WDTREL WDTL WDTH	Watchdog Timer Control Register Watchdog Timer Reload Register Watchdog Timer, Low Byte Watchdog Timer, High Byte	$A2_H$ $A3_H$ $B2_H$ $B3_H$	$XXXXXX00_B$ [2] 00_H 00_H 00_H
Timer 2	T2CON T2MOD RC2H RC2L T2H T2L	Timer 2 Control Register Timer 2 Mode Register Timer 2 Reload/Capture, High Byte Timer 2 Reload/Capture, Low Byte Timer 2, High Byte Timer 2, Low Byte	**$C8_H$** [1] $C9_H$ CB_H CA_H CD_H CC_H	**00_H** $XXXXXXX0_B$ [2] 00_H 00_H 00_H 00_H

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Table 6 Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Add-ress	Contents after Reset
Cap-ture/ Com-pare Unit	T12L	Timer T12 Counter Register, Low Byte	EC_H	00_H
	T12H	Timer T12 Counter Register, High Byte	ED_H	00_H
	T13L	Timer T13 Counter Register, Low Byte	EE_H	00_H
	T13H	Timer T13 Counter Register, High Byte	EF_H	00_H
	T12PRL	Timer T12 Period Register, Low Byte	DE_H	00_H
	T12PRH	Timer T12 Period Register, High Byte	DF_H	00_H
	T13PRL	Timer T13 Period Register, Low Byte	$D2_H$	00_H
	T13PRH	Timer T13 Period Register, High Byte	$D3_H$	00_H
	CC60RL	Capture/Compare Ch 0 Reg, Low Byte	$C2_H$	00_H
	CC60RH	Capture/Compare Ch 0 Reg, High Byte	$C3_H$	00_H
	CC61RL	Capture/Compare Ch 1 Reg, Low Byte	$C4_H$	00_H
	CC61RH	Capture/Compare Ch 1 Reg, High Byte	$C5_H$	00_H
	CC62RL	Capture/Compare Ch 2 Reg, Low Byte	$C6_H$	00_H
	CC62RH	Capture/Compare Ch 2 Reg, High Byte	$C7_H$	00_H
	CC63RL	T13 Compare Register, Low Byte	$D4_H$	00_H
	CC63RH	T13 Compare Register, High Byte	$D5_H$	00_H
	T12DTCL	Timer T12 Dead Time Ctrl, Low Byte	$E6_H$	00_H
	T12DTCH	Timer T12 Dead Time Ctrl, High Byte	$E7_H$	00_H
	CMPSTATL	Compare Timer Status, Low Byte	$F4_H$	00_H
	CMPSTATH	Compare Timer Status, High Byte	$F5_H$	00_H
	CMPMODIFL	Compare Timer Modification, Low Byte	EA_H	00_H
	CMPMODIFH	Compare Timer Modification, High Byte	EB_H	00_H
	TCTR0L	Timer Control Register 0, Low Byte	$E2_H$	00_H
	TCTR0H	Timer Control Register 0, High Byte	$E3_H$	00_H
	TCTR2L[3]	Timer Control Register 2, Low Byte	$F2_H$	00_H
	TCTR4L[4]	Timer Control Register 4, Low Byte	$F2_H$	0_H
	TCTR4H[4]	Timer Control Register 4, High Byte	$F3_H$	00_H
	ISL	Cap/Com Interrupt Register, Low Byte	$E4_H$	00_H
	ISH	Cap/Com Interrupt Register, High Byte	$E5_H$	00_H
	PISELH	Port Input Selector Register, High Byte	BB_H	00_H

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Table 6 Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Add-ress	Contents after Reset
Cap-ture/ Com-pare Unit	ISSL[3]	Cap/Com Int Status Set Reg, Low Byte	BC_H	00_H
	ISSH[3]	Cap/Com Int Status Set Reg, High Byte	BD_H	00_H
	ISRL[4]	Cap/Com Int Status Reset Reg, Low Byte	BC_H	00_H
	ISRH[4]	Cap/Com Int Status Reset Reg,High Byte	BD_H	00_H
	INPL[3]	Cap/Com Int Node Ptr Reg, Low Byte	BE_H	40_H
	INPH[3]	Cap/Com Int Node Ptr Reg, High Byte	BF_H	39_H
	IENL[4]	Cap/Com Interrupt Register, Low Byte	BE_H	00_H
	IENH[4]	Cap/Com Interrupt Register, High Byte	BF_H	00_H
	CC60SRL	Cap/Com Channel 0 Shadow, Low Byte	FA_H	00_H
	CC60SRH	Cap/Com Channel 0 Shadow, High Byte	FB_H	00_H
	CC61SRL	Cap/Com Channel 1 Shadow, Low Byte	FC_H	00_H
	CC61SRH	Cap/Com Channel 1 Shadow, High Byte	FD_H	00_H
	CC62SRL	Cap/Com Channel 2 Shadow, Low Byte	FE_H	00_H
	CC62SRH	Cap/Com Channel 2 Shadow, High Byte	FF_H	00_H
	CC63SRL	T13 Compare Shadow Reg, Low Byte	$B6_H$	00_H
	CC63SRH	T13 Compare Shadow Reg, High Byte	$B7_H$	00_H
	MODCTRL[3]	Modulation Control Register, Low Byte	$D6_H$	00_H
	MODCTRH[3]	Modulation Control Register, High Byte	$D7_H$	00_H
	TRPCTRL	Trap Control Register, Low Byte	CE_H	00_H
	TRPCTRH	Trap Control Register, High Byte	CF_H	00_H
	PSLRL	Passive State Level Register, Low Byte	$A6_H$	00_H
	MCMOUTL[3]	MCM Output Register, Low Byte	DC_H	00_H
	MCMOUTH[3]	MCM Output Register, High Byte	DD_H	00_H
	MCMOUTSL[4]	MCM Output Shadow Register, Low Byte	DC_H	00_H
	MCMOUTSH[4]	MCM Output Shadow Register,High Byte	DD_H	00_H
	MCMCTRLL[4]	MCM Control Register, Low Byte	$D6_H$	00_H
	T12MSELL	T12 Cap/Com Mode Sel Reg, Low Byte	$F6_H$	00_H
	T12MSELH	T12 Cap/Com Mode Sel Reg, High Byte	$F7_H$	00_H

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Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
84_H	DPSEL	00_H	–	–	–	–	–	D2	D1	D0
87_H	PCON	$0XX0\ 0000_B$	SMOD	–	–	SD	GF1	GF0	PDE	IDLE
88_H	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89_H	TMOD	00_H	GATE 1	C/NT1	M1(1)	M0(1)	GATE 0	C/NT0	M1(0)	M0(0)
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8E_H$	PMCON0	$XXX0\ 0000_B$	–	–	–	EBO	BO	SDSTAT	WS	EPWD
$8F_H$	CMCON	$1001\ 1111_B$	KDIV2	KDIV1	KDIV0	REL4	REL3	REL2	REL1	REL0
90_H[2]	P1	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H[3]	P1DIR	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
91_H	EXICON	$XXXX\ XX00_B$	–	–	–	–	–	–	ESEL3	ESEL2
92_H	IRCON0	$XXXX\ XX00_B$	–	–	–	–	–	–	EXINT3	EXINT2
93_H	IRCON1	$XX00\ 00X0_B$	–	–	INP3	INP2	INP1	INP0	–	IADC
98_H	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$A2_H$	WDTCON	$XXXX\ XX00_B$	–	–	–	–	–	–	–	WDTIN
$A3_H$	WDTREL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$A6_H$	PSLRL	00_H	PSL63	–	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0
$A8_H$	IEN0	$0X00\ 0000_B$	EA	–	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IEN1	$XXXX\ X000_B$	–	–	–	–	–	EX3	EX2	EADC
AA_H	IEN2	$XX00\ 00XX_B$	–	–	EINP3	EINP2	EINP1	EINP0	–	–
AC_H	IP1	$XX00\ 0000_B$	–	–	.5	.4	.3	.2	.1	.0
AD_H	SYSCON0	$XX10\ XXX1_B$	–	–	EALE	RMAP	–	–	–	XMAP0
AF_H	SYSCON1	$00XX\ X0X0_B$	ESWC	SWC	_	_	_	BSLEN	_	SWAP
$B0_H$[2]	P3	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$B0_H$[3]	P3DIR	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$B1_H$	P3ALT	00_H	CC60	COUT60	CC61	COUT61	CC62	COUT62	CTRAP	COUT63
$B2_H$	WDTL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$B3_H$	WDTH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$B4_H$	P1ALT	$XXX0\ 0X00_B$	_	_	_	RxD	INT3	_	EXF2	TxD
$B6_H$	CC63SRL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$B7_H$	CC63SRH	00_H	.7	.6	.5	.4	.3	.2	.1	.0

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Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$B8_H$	IP0	$XX00\ 0000_B$	–	–	.5	.4	.3	.2	.1	.0
BB_H	PISELH	00_H	–	–	ISPOS2.1	ISPOS2.0	ISPOS1.1	ISPOS1.0	ISPOS0.1	ISPOS0.0
BC_H[3]	ISSL	00_H	ST12PM	ST12OM	SCC62F	SCC62R	SCC61F	SCC61R	SCC60F	SCC60R
BC_H[2]	ISRL	00_H	RT12PM	RT12OM	RCC62F	RCC62R	RCC61F	RCC61R	RCC60F	RCC60R
BD_H[3]	ISSH	00_H	–	SIDLE	SWHE	SCHE	–	STRPF	ST13PM	ST13CM
BD_H[2]	ISRH	00_H	–	RIDLE	RWHE	RCHE	–	RTRPF	RT13PM	RT13CM
BE_H[2]	IENL	00_H	ENT12PM	ENT12OM	ENCC62F	ENCC62R	ENCC61F	ENCC61R	ENCC60F	ENCC60R
BE_H[3]	INPL	00_H	INPCHE.1	INPCHE.0	INPCC62.1	INPCC62.0	INPCC61.1	INPCC61.0	INPCC60.1	INPCC60.0
BF_H[2]	IENH	00_H	–	ENIDLE	ENWHE	ENCHE	–	ENTRPF	ENT13PM	ENT13CM
BF_H[3]	INPH	00_H	–	–	INPT13.1	INPT13.0	INPT12.1	INPT12.0	INPERR.1	INPERR.0
$C0_H$	SCUWDT	00_H	–	PLLR	–	WDTR	WDTEOI	WDTDIS	WDTRS	WDTRE
$C2_H$	CC60RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CC60RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CC61RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CC61RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0

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Shaded registers are bit-addressable special function registers

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$C6_H$	CC62RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CC62RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$	T2CON	00_H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	XXXXXXX0$_B$	–	–	–	–	–	–	–	DCEN
CA_H	RC2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	RC2H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CE_H	TRPCTRL	00_H	–	–	–	–	–	TRPM2	TRPM1	TRPM0
CF_H	TRPCTRH	00_H	TRPPEN	TRPEN13	TRPEN5	TRPEN4	TRPEN3	TRPEN2	TRPEN1	TRPEN0
$D0_H$	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D2_H$	T13PRL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D3_H$	T13PRH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D4_H$	CC63RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D5_H$	CC63RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D6_H$[2]	MCMCTRLL	00_H	–	–	SWSYN1	SWSYN0	–	SWSEL2	SWSEL1	SWSEL0
$D6_H$[3]	MODCTRL	00_H	MCMEN	–	T12MODEN5	T12MODEN4	T12MODEN3	T12MODEN2	T12MODEN1	T12MODEN0

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Shaded registers are bit-addressable special function registers

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D7_H$[3]	MODCTRH	00_H	ECT13O	–	T13MODEN5	T13MODEN4	T13MODEN3	T13MODEN2	T13MODEN1	T13MODEN0
$D8_H$	ADCON0	00_H	ADST	ADBSY	ADM1	ADM0	CCU-ADEX	ADCH2	ADCH1	ADCH0
$D9_H$	ADCON1	$XX00\ 0000_B$	–	–	ADSTC2	ADSTC1	ADSTC0	ADCTC2	ADCTC1	ADCTC0
DB_H	ADDATH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
DC_H[3]	MCMOUTL	00_H	–	R	MCMP5	MCMP4	MCMP3	MCMP2	MCMP1	MCMP0
DC_H[2]	MCMOUTSL	00_H	STRMCM	–	MCMPS5	MCMPS4	MCMPS3	MCMPS2	MCMPS1	MCMPS0
DD_H[3]	MCMOUTH	00_H	–	–	CURH2	CURH1	CURH0	EXPH2	EXPH1	EXPH0
DD_H[2]	MCMOUTSH	00_H	STRHP	–	CURHS2	CURHS1	CURHS0	EXPHS2	EXPHS1	EXPHS0
DE_H	T12PRL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
DF_H	T12PRH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E0_H$	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E2_H$	TCTR0L	00_H	CTM	CDIR	STE12	T12R	T12PRE	T12CLK2	T12CLK1	T12CLK0
$E3_H$	TCTR0H	10_H	–	–	STE13	T13R	T13PRE	T13CLK2	T13CLK1	T13CLK0
$E4_H$	ISL	00_H	T12PM	T12OM	ICC62F	ICC62R	ICC61F	ICC61R	ICC60F	ICC60R
$E5_H$	ISH	00_H	–	IDLE	WHE	CHE	TRPS	TRPF	T13PM	T13CM

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Shaded registers are bit-addressable special function registers

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$E6_H$	T12DTCL	00_H		–	DTM5	DTM4	DTM3	DTM2	DTM1	DTM0
$E7_H$	T12DTCH	00_H	–	DTR2	DTR1	DTR0	–	DTE2	DTE1	DTE0
$E8_H$	PMCON1	$XXXX X000_B$	–	–	–	–	–	CCUDIS	T2DIS	ADCDIS
EA_H	CMPMODIFL	00_H	–	MCC63S	–	–	–	MCC62S	MCC61S	MCC60S
EB_H	CMPMODIFH	00_H	–	MCC63R	–	–	–	MCC62R	MCC61R	MCC60R
EC_H	T12L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
ED_H	T12H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
EE_H	T13L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
EF_H	T13H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F0_H$	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F2_H$[2]	TCTR4L	00_H	T12STD	T12STR	–	–	DTRES	T12RES	T12RS	T12RR
$F2_H$[3]	TCTR2L	00_H	–	T13TED1	T13TED0	T13TEC2	T13TEC1	T13TEC0	T13SSC	T12SSC
$F3_H$[2]	TCTR4H	00_H	T13STD	T13STR	–	–	–	T13RES	T13RS	T13RR
$F4_H$	CMPSTATL	00_H	–	CC63ST	–	–	–	CC62ST	CC61ST	CC60ST
$F5_H$	CMPSTATH	00_H	T13IM	COUT63PS	COUT62PS	CC62PS	COUT61PS	CC61PS	COUT60PS	CC60PS
$F6_H$	T12MSELL	00_H	MSEL613	MSEL612	MSEL611	MSEL610	MSEL603	MSEL602	MSEL601	MSEL600
$F7_H$	T12MSELH	00_H	–	–	–	–	MSEL623	MSEL622	MSEL621	MSEL620

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$F8_H$	PMCON2	$XXXX\ X000_B$	–	–	–	–	–	CCUST	T2ST	ADCST
$F9_H$	VERSION	00_H	PROT	VER6	VER5	VER4	VER3	VER2	VER1	VER0
FA_H	CC60RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
FB_H	CC60RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
FC_H	CC61RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
FD_H	CC61RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
FE_H	CC62RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
FF_H	CC62RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Ports

The C868 has two kinds of ports. The first kind is push-pull ports instead of the traditional quasi-bidirectional ports. The ports belonging to this kind are lsb of port 1 which is a 5-bit I/O port and port 3 which is an eight-bit I/O port. When configured as inputs, these ports will be high impedance with Schmitt trigger feature. Port 3 is alternate for capture/ compare functions whereas, port 1 has alternate functions for some of the pins.

The second kind is input ports which are shared by msb of port 1 which is a 3-bit input port, the interrupts, timer 2 inputs, capture/compare hall inputs and analog inputs.

Timer 0 and 1

Timer 0 and 1 can be used in four operating modes as listed in **Table 8**:

Table 8 Timer 0 and 1 Operating Modes

Mode	Description	TMOD		System Clock
		M1	M0	
0	8-bit timer with a divide-by-32 prescaler	0	0	f_{SYS}/(12*32)
1	16-bit timer	0	1	f_{SYS}/12
2	8-bit timer with 8-bit autoreload	1	0	
3	Timer 0 used as one 8-bit timer and one 8-bit timer timer 1 stops	1	1	

The register is incremented every machine cycle. Since the machine cycle consist of twelve oscillator periods, the count rate is 1/12th of the system frequency. External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate to facilitate pulse width measurements. **Figure 15** illustrates the input clock logic.

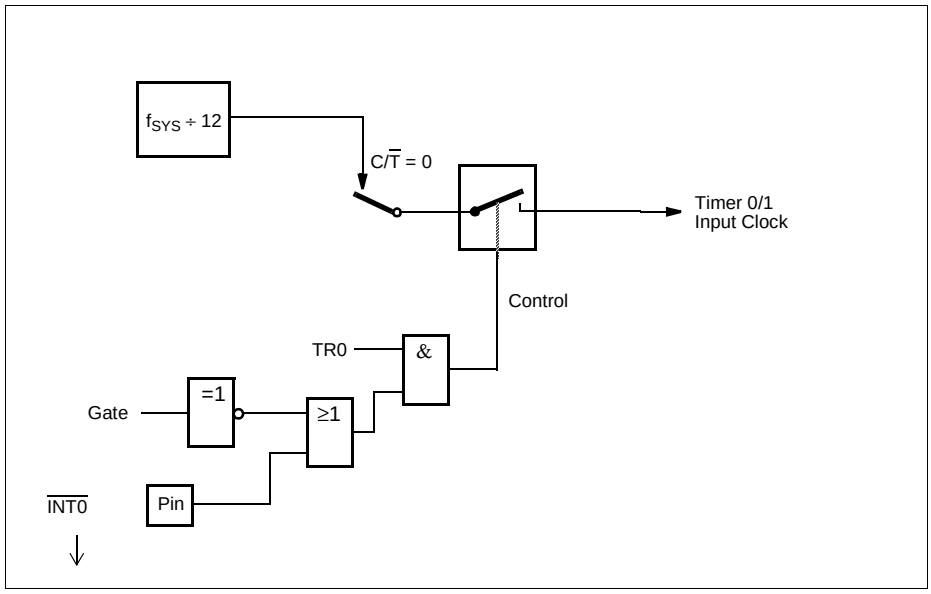


Figure 15 Timer 0 and 1 Input Clock Logic

Timer/Counter 2 with Compare/Capture/Capture

Timer 2 is a 16-bit timer/counter with an up/down count feature. It has three operating modes:

- 16-bit auto-reload mode (up or down counting)
- 16-bit capture mode
- Baudrate generator

Table 9 Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	T2EX	Remarks	System Clock	
	RCLK or TCLK	CP/RL2	TR2	DCEN	EXEN			Inte-rnal	T2
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	f_{SYS} /12	max f_{SYS} /24
	0	0	X	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	down counting		
	0	0	1	1	X	1	up counting		
16-bit Capture	0	1	1	X	0	X	16-bit Timer/ Counter (only up-counting)	f_{SYS} /12	max f_{SYS} /24
	0	1	1	X	1	↓	capture T2H,T2L-> RC2H,RC2L		
Baudrate Generator	1	X	1	X	0	X	no overflow interrupt request(TF2)	f_{SYS} /2	-
	1	X	1	X	1	↓	extra external interrupt (“Timer 2“)		
off	X	X	0	X	X	X	Timer 2 stops	-	-

Note: denotes a falling edge

Serial Interface (UART)

The serial port is a full duplex port capable of simultaneous transmit and receive functions. It is also receive-buffered; it can commence reception of a second byte before a previously-received byte has been read from the receive register. The serial port can operate in 3 modes as illustrated in **Table 10**.

Table 10 UART Operating Modes

Mode	SCON		Description
	SM1	SM0	
0	0	0	Reserved
1	0	1	8-bit UART, variable baudrate 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	9-bit UART, fixed baudrate 11 bits are transmitted (through TxD) or received (RxD)
3	1	1	9-bit UART, variable baudrate Similar to mode 2, except for the variable baudrate.

For clarification, some terms regarding the difference between “baudrate clock“ and “baudrate“ should be mentioned.

The serial interface requires a clock rate which is 16 times the baudrate for internal synchronization. Therefore, the baudrate generators must provide a “baudrate clock“ to the serial interface which divides it by 16, thereby resulting in the actual “baudrate“.

The baudrates in Mode 1 and 3 are determined by the timer overflow rate. These baudrates can be determined by Timer 1 or by Timer 2 or both (one for transmit, the other for receive.

Table 11 Serial Interface - Baud Rate Dependencies

Serial Interface Operating Modes	Active Control Bits		Baud Rate Calculation
	TCLK/ RCLK	SMOD	
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	0	x	Controlled by timer 1 overflow: ($2^{SMOD} \times$ Timer 1 overflow rate) / 32
	1	x	Controlled by baud rate generator ($2^{SMOD} \times$ Timer 2[1)] overflow rate) / 32
Mode 2 (9-bit UART)	–	0	f_{SYS} / 64
		1	f_{SYS} / 32

1) Timer 2 functioning as baudrate generator

Capture/Compare Unit (CCU6)

The CCU6 provides two independent timers (T12, T13), which can be used for PWM generation, especially for AC-motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel.
- Generation of a three-phase PWM supported (six outputs, individual signals for highside and lowside switches)
- 16 bit resolution, maximum count frequency = system clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode

Timer 13 Features

- One independent compare channel with one output
- 16 bit resolution, maximum count frequency = system clock
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported

Additional Features

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage
- Capture/compare unit can be powerdown in normal, idle and slow-down modes

The timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. The timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

Switching Examples

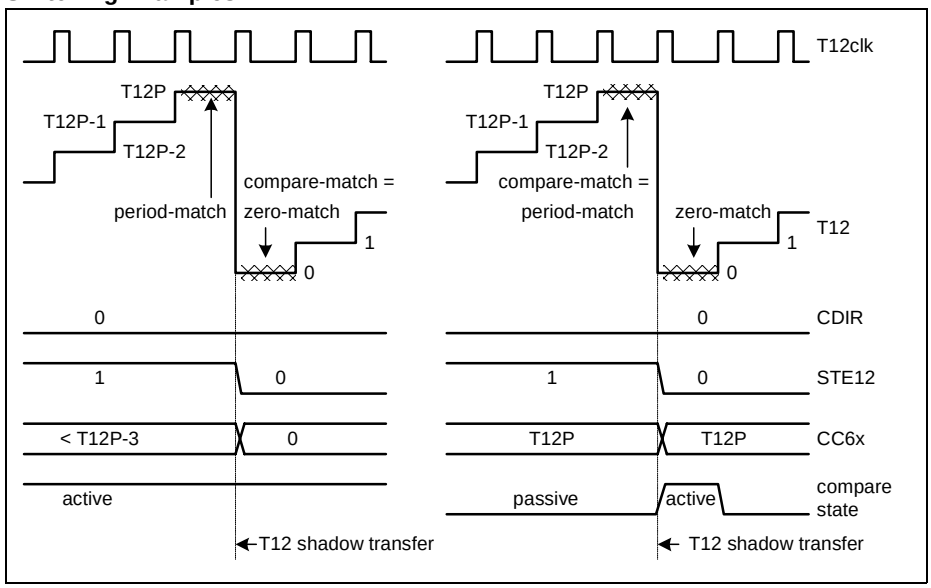


Figure 16 Edge-aligned mode with duty cycles near 100% and near 0%. Applicable to T13 as well.

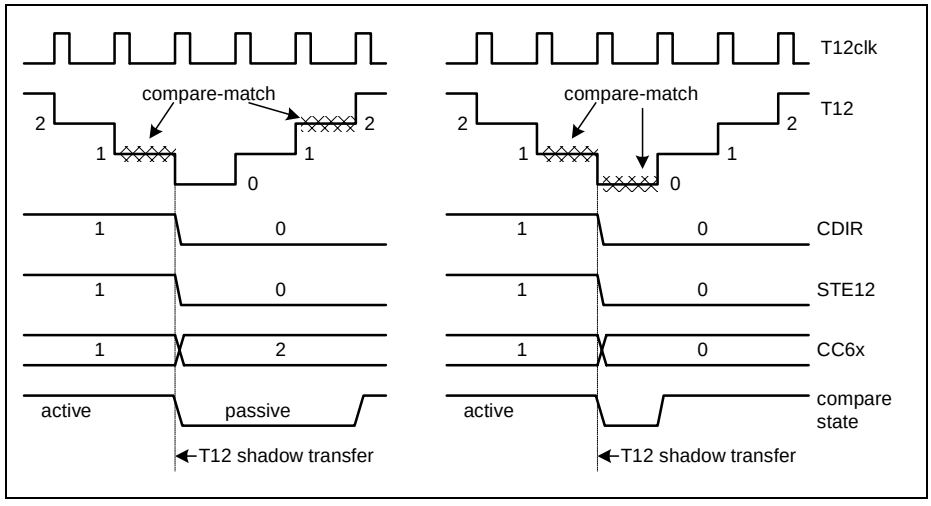


Figure 17 Centre-aligned mode with duty cycles near 100% and near 0%.

Dead-time Generation

The dead-time generation logic is built in a similar way for all three channels of T12. Each of the three channels works independently with its own dead-time counter and the trigger and enable signals.

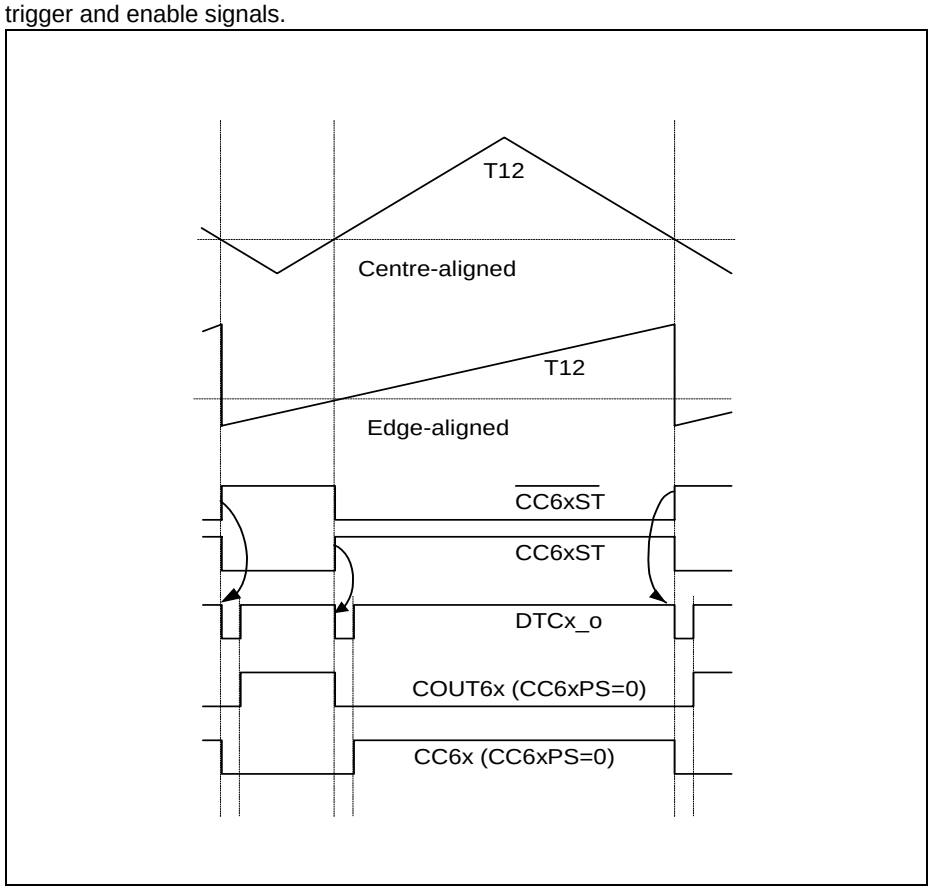


Figure 18 Dead-time generation for centre and edge aligned modes

Capture Mode

In capture mode the bits CC6xST indicate the occurrence of the selected capture event according to the bit fields MSEL6x. A rising and/or a falling edge on the pins CC6x can be selected as capture event, that is used to transfer the contents of timer T12 to the CC6xR and CC6xSR registers. In order to work in capture mode, the capture pins have to be configured as inputs.

Single Shot Mode

In single shot mode, the timer T12 stops automatically at the end of the its counting period.

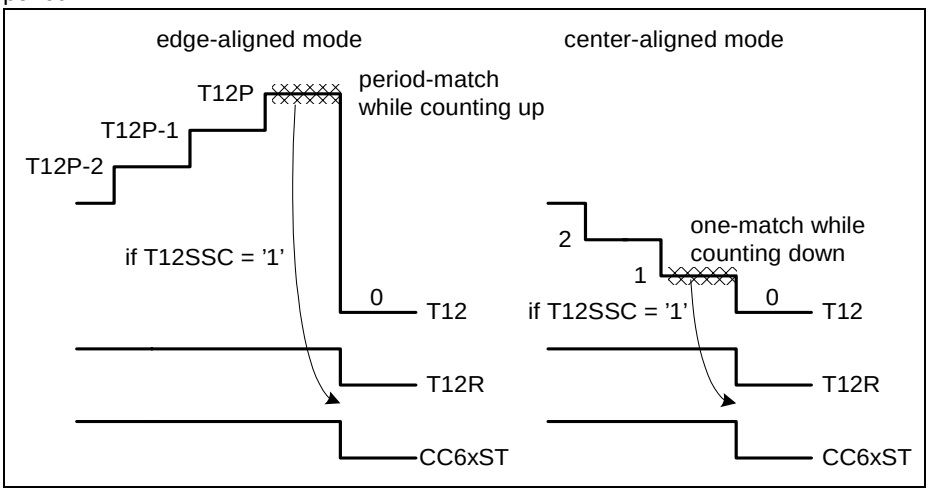


Figure 19 Single Shot Mode of T12, T13 is edge-aligned mode only.

Hysteresis-Like Control Mode

The hysteresis-like control mode (MSEL6x = '1001') offers the possibility to switch off the PWM output if the input CCPOSx becomes '0'. This can be used as a simple motor control feature by using a comparator indicating e.g. over current.

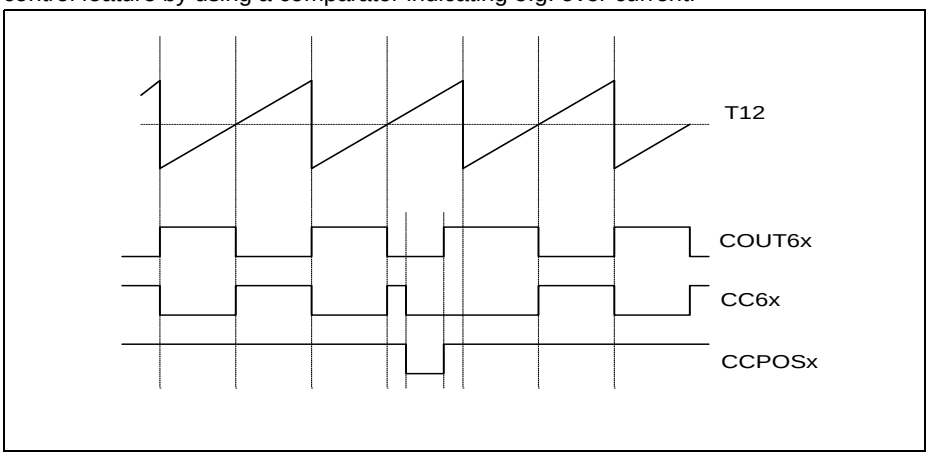
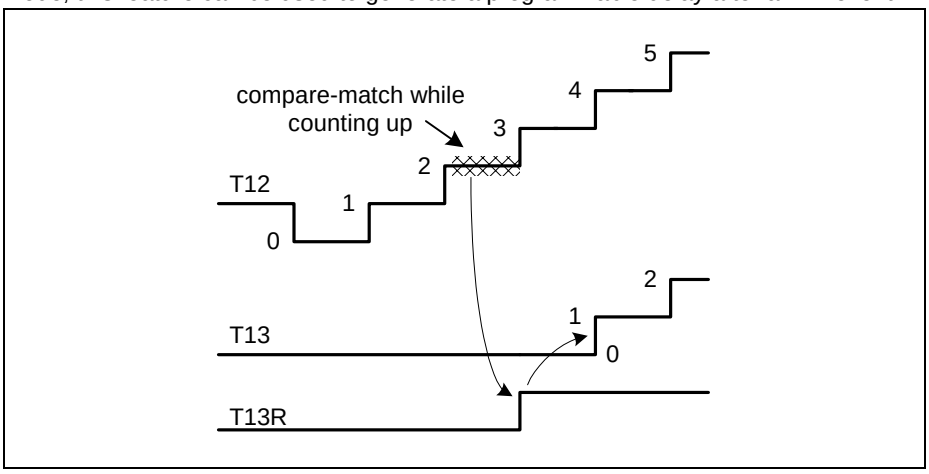


Figure 20 Hysteresis-like control mode

Synchronization of T13 to T12

The timer T13 can be synchronized on a T12 event. Combined with the single shot mode, this feature can be used to generate a programmable delay after a T12 event.



Synchronization of T13 to T12

Multi-channel Mode

The multi-channel mode offers a possibility to modulate all six T12-related output signals within one instruction. The bits in bit field MCMP are used to select the outputs that may become active. If the multi-channel mode is enabled (bit MCMEN='1'), only those outputs may become active, which have a '1' at the corresponding bit position in bit field MCMP.

This bit field has its own shadow bit field MCMPS, which can be written by SW. The transfer of the new value in MCMPS to the bit field MCMP can be triggered by and synchronized to T12 or T13 events. This structure permits the SW to write the new value, which is then taken into account by the HW at a well-defined moment and synchronized to a PWM period. This avoids unintended pulses due to unsynchronized modulation sources (T12, T13, SW).

Trap Handling

The trap functionality permits the PWM outputs to react on the state of the input pin $\overline{\text{CTRAP}}$. This functionality can be used to switch off the power devices if the trap input becomes active (e.g. as emergency stop).

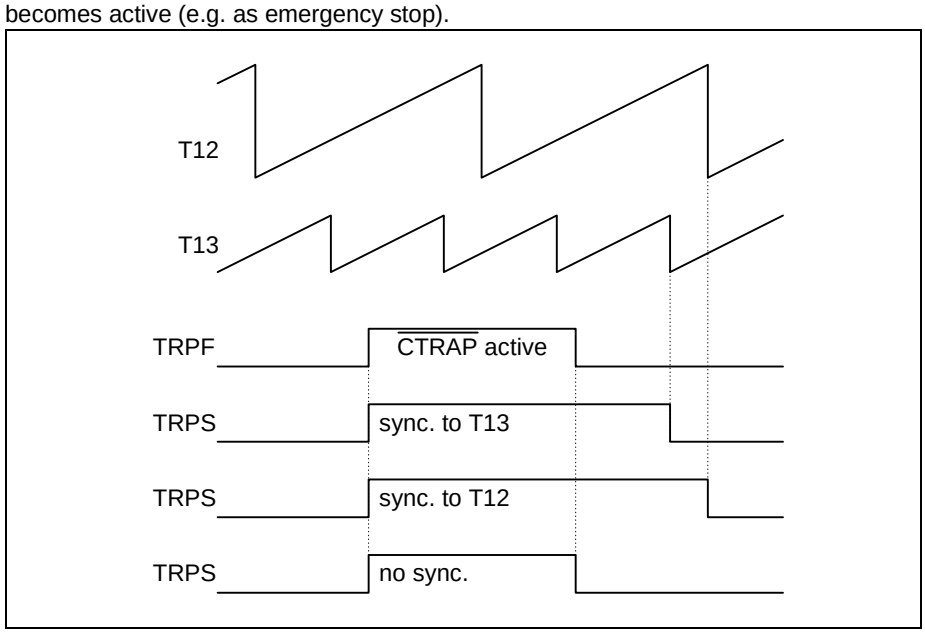


Figure 21 Trap State Synchronization (with TRM2=’0’)

Modulation control

The modulation control part combines the different modulation sources, six T12-related signals from the three compare channels, the T13-related signal and the multi-channel modulation signals. each modulation source can be individually enabled for each output line. Furthermore, the trap functionality is taken into account to disable the modulation of the corresponding output line during the trap state (if enabled).

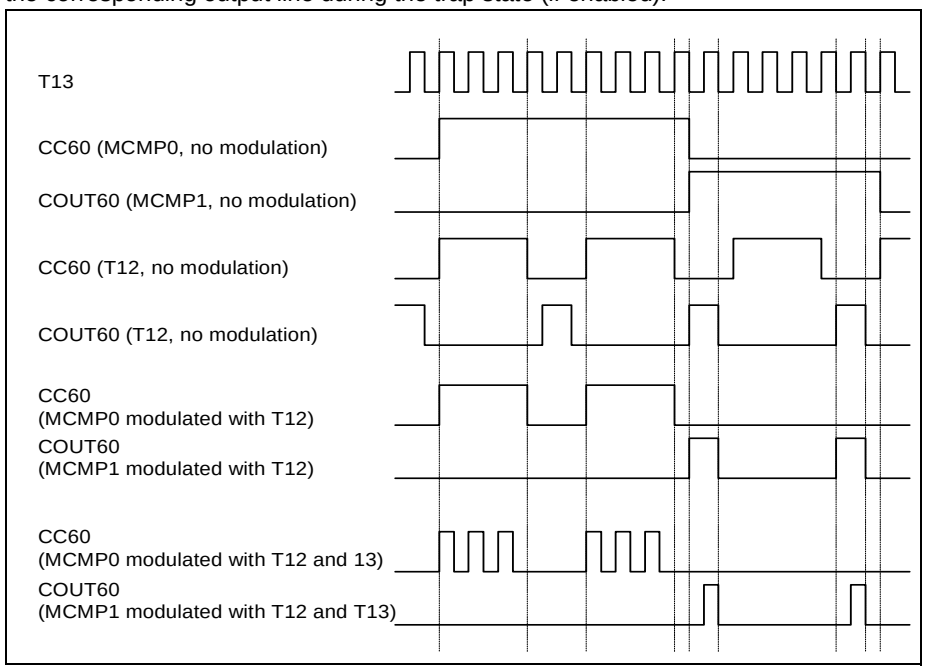


Figure 22 Modulation Control example for CC60 and COUT60.

Hall Sensor Mode

In **Brushless-DC motors** the next multi-channel state values depend on the pattern of the Hall inputs. There is a strong correlation between the **Hall pattern** (CURH) and the **modulation pattern** (MCMP). Because of different machine types the modulation pattern for driving the motor can be different. Therefore it is wishful to have a wide flexibility in defining the correlation between the Hall pattern and the corresponding modulation pattern. The CCU6 offers this by having a register which contains the actual Hall pattern (CURHS), the next expected Hall pattern (EXPHS) and its output pattern (MCMPS). At every correct Hall event (CHE, see figure *Hall Event Actions*) a new Hall pattern with its corresponding output pattern can be loaded (from a predefined table) by software into the register MCMOUTS. Loading this shadow register can also be done by a write action on MCMOUTS with bit STRHP = ’1’

The **sampling** of the Hall pattern (on CCPOSx) is done with the T12 clock. By using the dead-time counter DTC0 (mode MSEL6x= ’1000’) a hardware **noise filter** can be implemented to suppress spikes on the Hall inputs due to high di/dt in rugged inverter environment. In case of a Hall event the DTC0 is reloaded and starts counting. When the counter value of one is reached, the CCPOSx inputs are sampled (without noise and spikes) and are compared to the current Hall pattern (CURH) and to the expected Hall pattern (EXPH). If the sampled pattern equals to the current pattern the edge on CCPOSx was due to a noise spike and no action will be triggered (implicit noise filter). If the sampled pattern equals to the next expected pattern the edge on CCPOSx was a correct Hall event, the bit CHE is set which causes an interrupt and the resets T12 (for speed measurement, see description mode ’1000’ below).

This correct Hall event can be used as a transfer request event for register MCMOUTS. The transfer from MCMOUTS to MCMOUT transfers the new CURH-pattern as well as the next EXPH-pattern. In case of the sampled Hall inputs were neither the current nor the expected Hall pattern, the bit WHE (wrong Hall event) is set which also can cause an interrupt and sets the IDLE mode clearing MCMP (modulation outputs are inactive). To restart from IDLE the transfer request of MCMOUTS have to be initiated by software (bit STRHP and bitfields SWSEL/SWSYN).

Below is a table listing output (MCMP) for a BLDC motor.

Block Commutation Control Table

Mode	CCPOS0-CCPOS2 Inputs			CC60 - CC62 Outputs			COUT60 - COUT62 Outputs		
	CCPOS0	CCPOS1	CCPOS2	CC60	CC61	CC62	COUT60	COUT61	COUT62
Rotate left, 0° phase shift	1	0	1	inactive	inactive	active	inactive	active	inactive
	1	0	0	inactive	inactive	active	active	inactive	inactive
	1	1	0	inactive	active	inactive	active	inactive	inactive
	0	1	0	inactive	active	inactive	inactive	inactive	active
	0	1	1	active	inactive	inactive	inactive	inactive	active
	0	0	1	active	inactive	inactive	inactive	active	inactive
Rotate right	1	1	0	active	inactive	inactive	inactive	active	inactive
	1	0	0	active	inactive	inactive	inactive	inactive	active
	1	0	1	inactive	active	inactive	inactive	inactive	active
	0	0	1	inactive	active	inactive	active	inactive	inactive
	0	1	1	inactive	inactive	active	active	inactive	inactive
	0	1	0	inactive	inactive	active	inactive	active	inactive
Slow down	X	X	X	inactive	inactive	inactive	active	active	active
Idle[1)]	X	X	X	inactive	inactive	inactive	inactive	inactive	inactive

1) In case of the sampled Hall inputs were neither the current nor the expected Hall pattern, the bit WHE (wrong Hall event) is set which also can cause an interrupt and sets the IDLE mode clearing MCMP (modulation outputs are inactive).

For **Brushless-DC** motors there is a special mode (MSEL6x = ’1000b’) which is triggered by a change of the Hall-inputs (CCPOSx). This mode shows the capabilities of the CCU6. Here T12’s channel 0 acts in capture function, channel 1 and 2 in compare function (without output modulation) and the multi-channel-block is used to trigger the output switching together with a possible modulation of T13.
After the detection of a valid Hall edge the T12 count value is captured to channel 0 (representing the actual motor speed) and resets the T12. When the timer reaches the compare value in channel 1, the next multi-channel state is switched by triggering the shadow transfer of bit field MCMP (if enabled in bit field SWEN). This trigger event can be combined with several conditions which are necessary to implement a noise filtering (correct Hall event) and to synchronize the next multi-channel state to the modulation sources (avoiding spikes on the output lines). This compare function of channel 1 can be used as a phase delay for the position input to the output switching which is necessary if a sensorless back-EMF technique is used instead of Hall sensors. The compare value in channel 2 can be used as a time-out trigger (interrupt) indicating that the motors destination speed is far below the desired value which can be caused by a abnormal load change. In this mode the modulation of T12 has to be disabled (T12MODENx = ’0’).

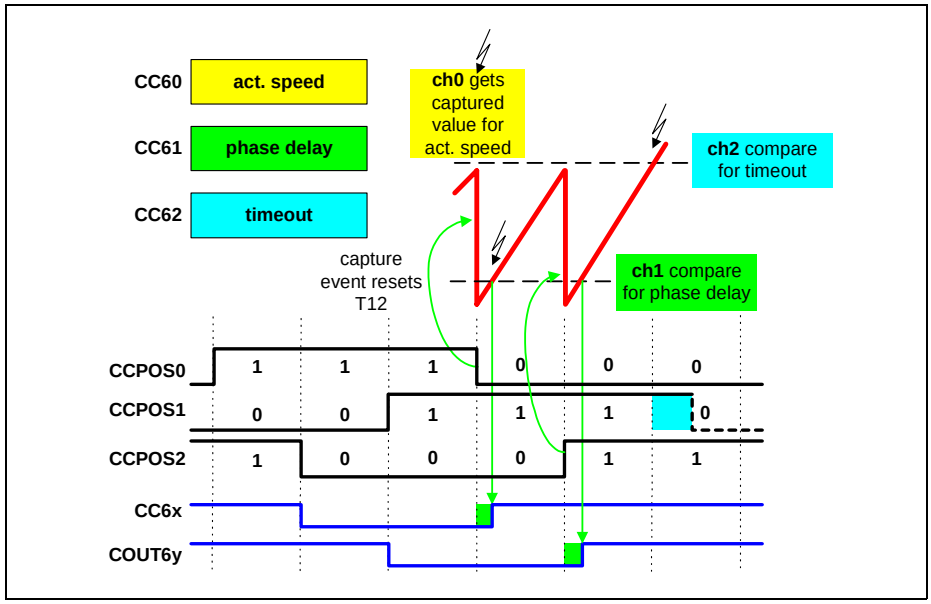


Figure 0-2 Timer T12 Brushless-DC Mode (MSEL6x = 1000)

A/D Converter

The C868 includes a high performance / high speed 8-bit A/D-Converter (ADC) with 5 analog input channels. It operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The A/D converter provides the following features:

- 5 multiplexed input channels, which can also be used as digital inputs
- 8-bit resolution with TUE of +/- 2 LSB8.
- Single or continuous conversion mode
- Start of conversion by software and hardware
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Powerdown in normal, idle and slow-down modes

The ADC supports two conversion modes - single and continuous conversions. For each mode, there are two ways in which conversion can be started - by software and by the T13PM signal from the CCU module.

Writing a ‘0’ to bit CCU_ADEX select conversion control by ADST. Writing a ’1’ to bit field ADST starts conversion on the channel that is specified by ADCH. In single conversion mode, bit field ADM is cleared to ’0’. This is the default mode selected after hardware reset. When a conversion is started, the channel specified is sampled. The busy flag ADBSY is set and ADST is cleared. When the conversion is completed, the interrupt request signal ADCIRQ is asserted possitively for 2 clocks and the 8-bit result together with the number of the converted channel is transferred to the result register ADDATH.

In continuous conversion mode, bit field ADM is set to ’1’. In this mode, the ADC repeatedly converts the channel specified by ADCH. Bit ADST is cleared at the beginning of the first conversion. The busy flag ADBSY is asserted until the last conversion is completed. At the end of each conversion, the interrupt request signal ADCIRQ will be activated. To stop conversion, ADM has to be reset by software. If the channel number ADCH is changed while continuous conversion is in progress, the new channel specified will be sampled in the conversions that follow.

A new request to start conversion will be allowed only after the completion of any conversion that is in progress.

Writing a ‘1’ to bit CCU_ADEX select conversion control by T13PM trigger signal from the CCU module.

Note: Caution must be taken when changing conversion start source. To change conversion source from software to hardware trigger, it is best to let remaining software conversion to complete before changing. To change conversion source from hardware trigger to software, it is best to change source first, let any

remaining hardware conversion to complete before beginning a software conversion.

Conversion and sample time control

The conversion and sample times are programmed via the bit fields ADCTC and ADSTC respectively of the register ADCON1. Bit field ADCTC (conversion time control) selects the internal ADC clock - adc_clk. Bit field ADSTC (sample time control) selects the sample time.

The total A/D conversion time is given by:

$$t_{ADCC} = 2/f_{SYS} + t_S + 8/adc\_clk \quad [5]$$

The sample time t_S is configured in periods of the selected internal ADC clock. The table below lists the possible combinations.

ADCTC	Clock Divider (TVC)	ADC Basic Clock adc_clk	ADSTC	Sample Time t_S (Periods of adc_clk, STC)
000 (default)	32	f_{SYS} / 32	000 (default)	2
001	28	f_{SYS} / 28	001	4
010	24	f_{SYS} / 24	010	6
011	20	f_{SYS} / 20	011	8
100	16	f_{SYS} / 16	100	10
101	12	f_{SYS} / 12	101	12
110	8	f_{SYS} / 8	110	14
111	4	f_{SYS} / 4	111	16

Interrupt System

The C868 provides 13 interrupt vectors with four priority levels. Nine interrupt requests are generated by the on-chip peripherals (timer 0, timer 1, timer 2, serial channel, A/D converter, and the capture/compare unit with 4 interrupts) and four interrupts may be triggered externally.

The wake-up from power-down mode interrupt has a special functionality which allows the software power-down mode to be terminated by a short negative pulse at pins CCPOS0/T2/INT0/AN0 or P1.4/RxD.

The 13 interrupt sources are divided into six groups. Each group can be programmed to one of the four interrupt priority levels. Additionally, 4 of these interrupt sources are channeled from 7 Capture/Compare (CCU6) interrupt sources.

Figure 23 to **Figure 28** give a general overview of the interrupt sources and illustrate the request and control flags.

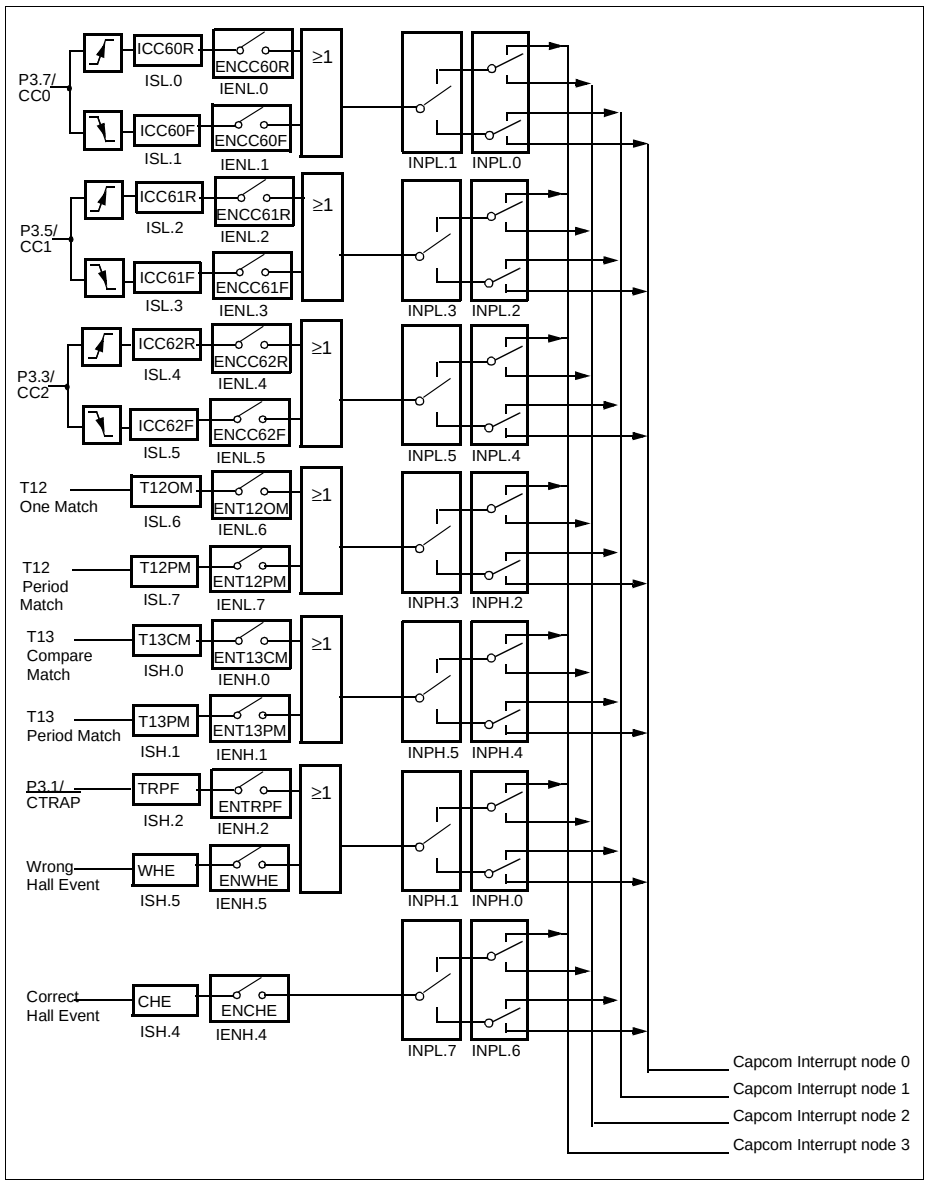


Figure 23 Capture/Compare module interrupt structure

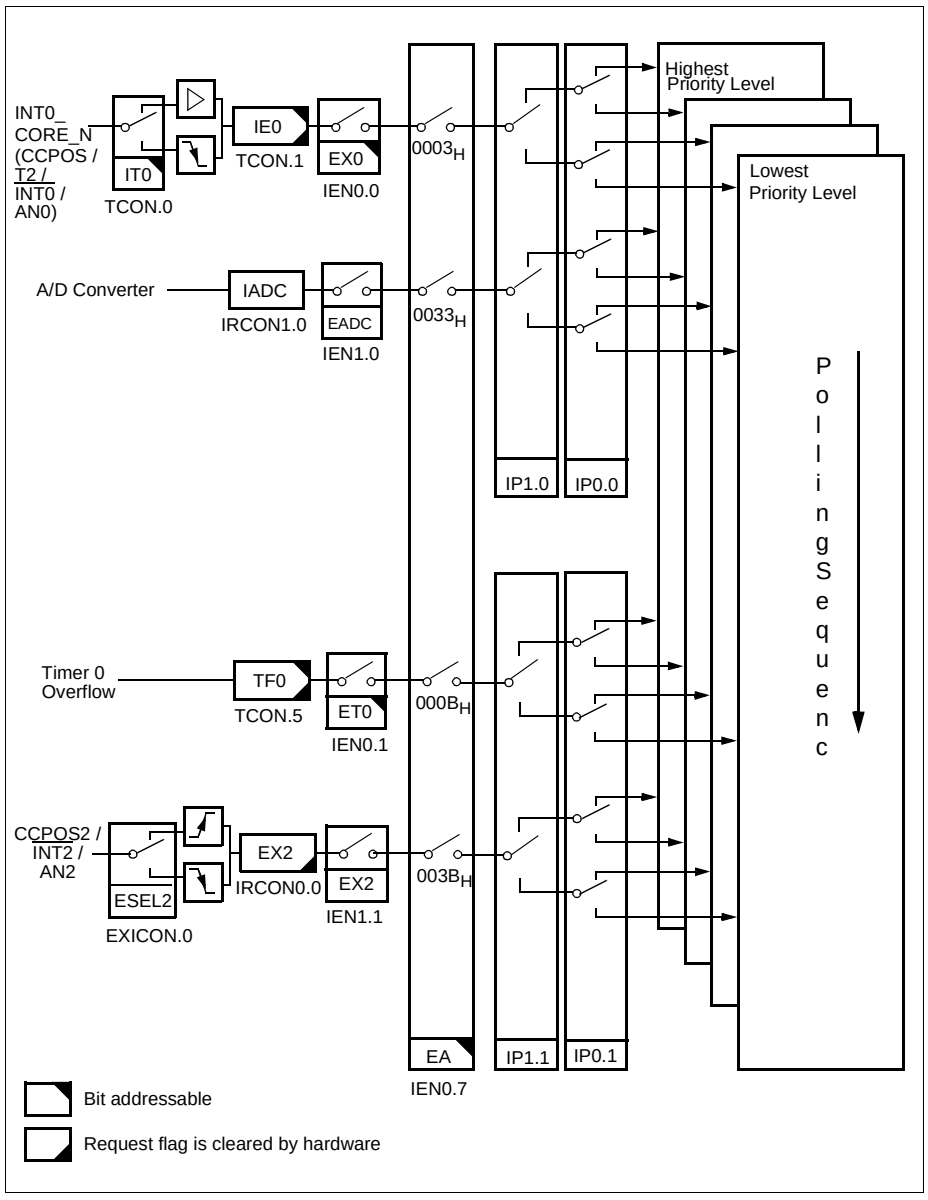


Figure 24 Interrupt Structure, Overview Part 1

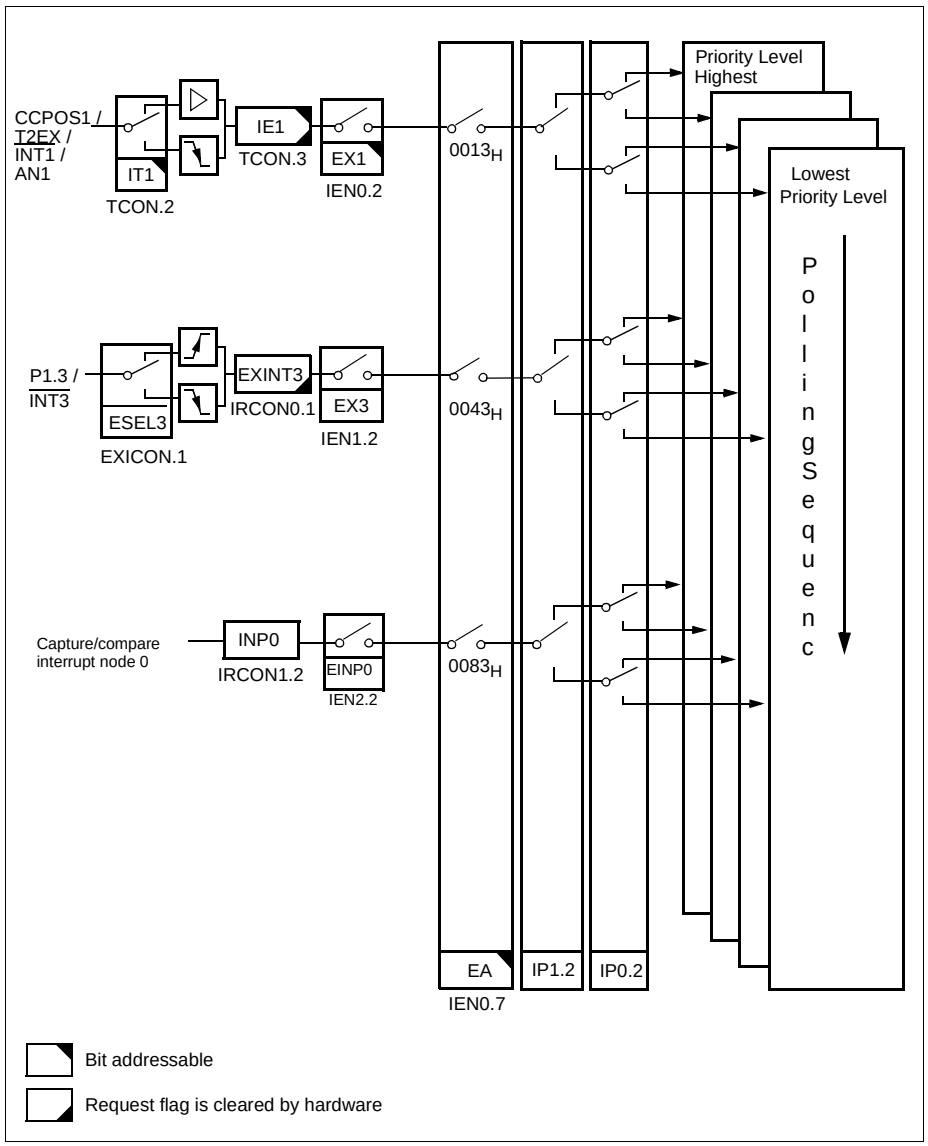


Figure 25 Interrupt Structure, Overview Part 2

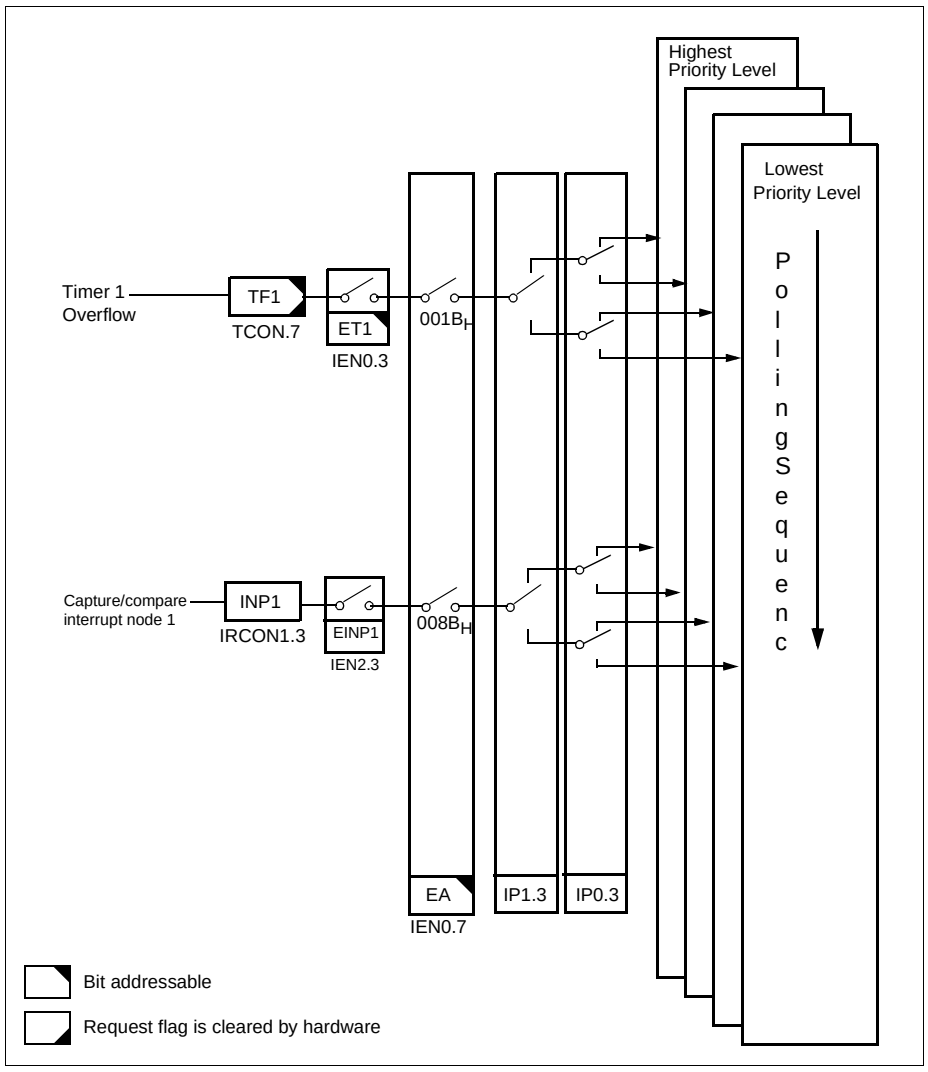


Figure 26 Interrupt Structure, Overview Part 3

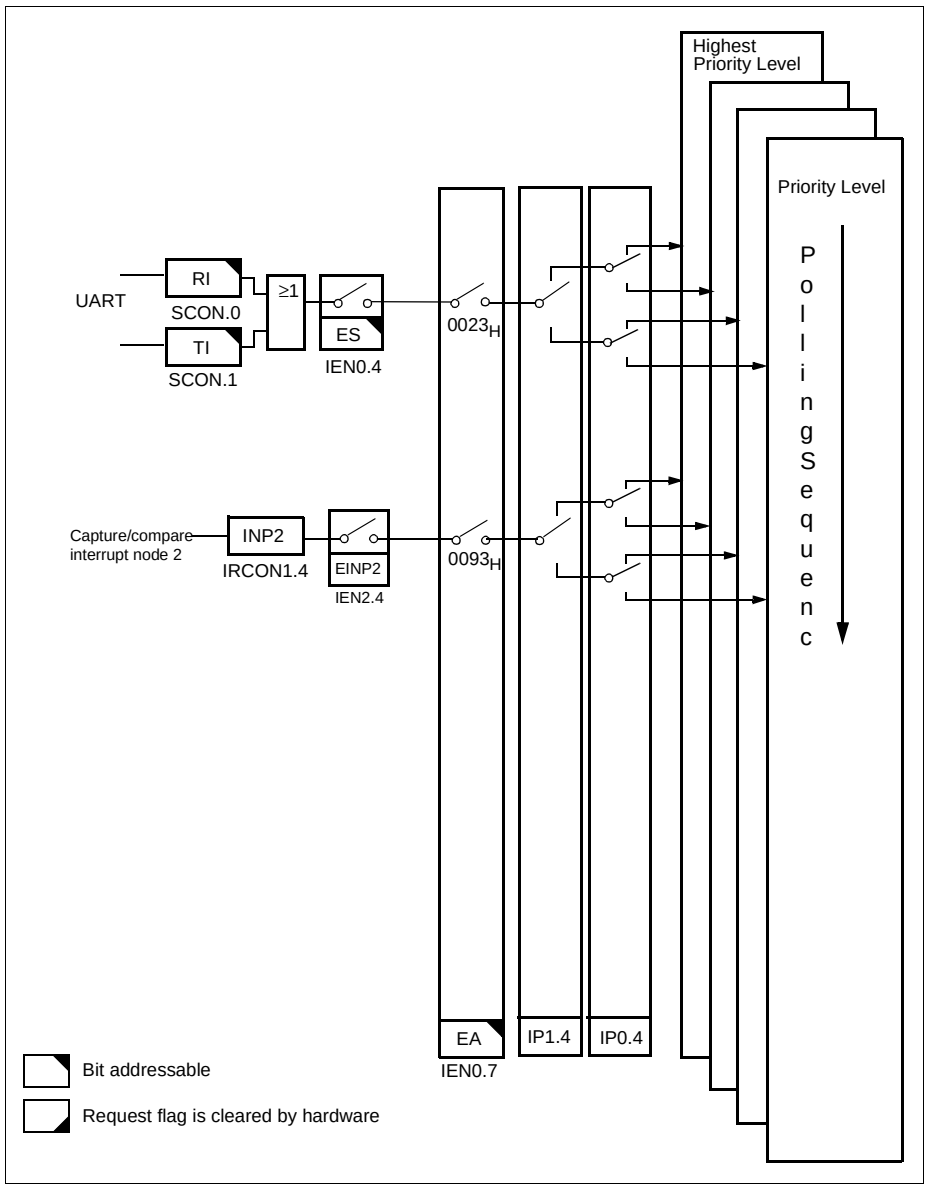


Figure 27 Interrupt Structure, Overview Part 4

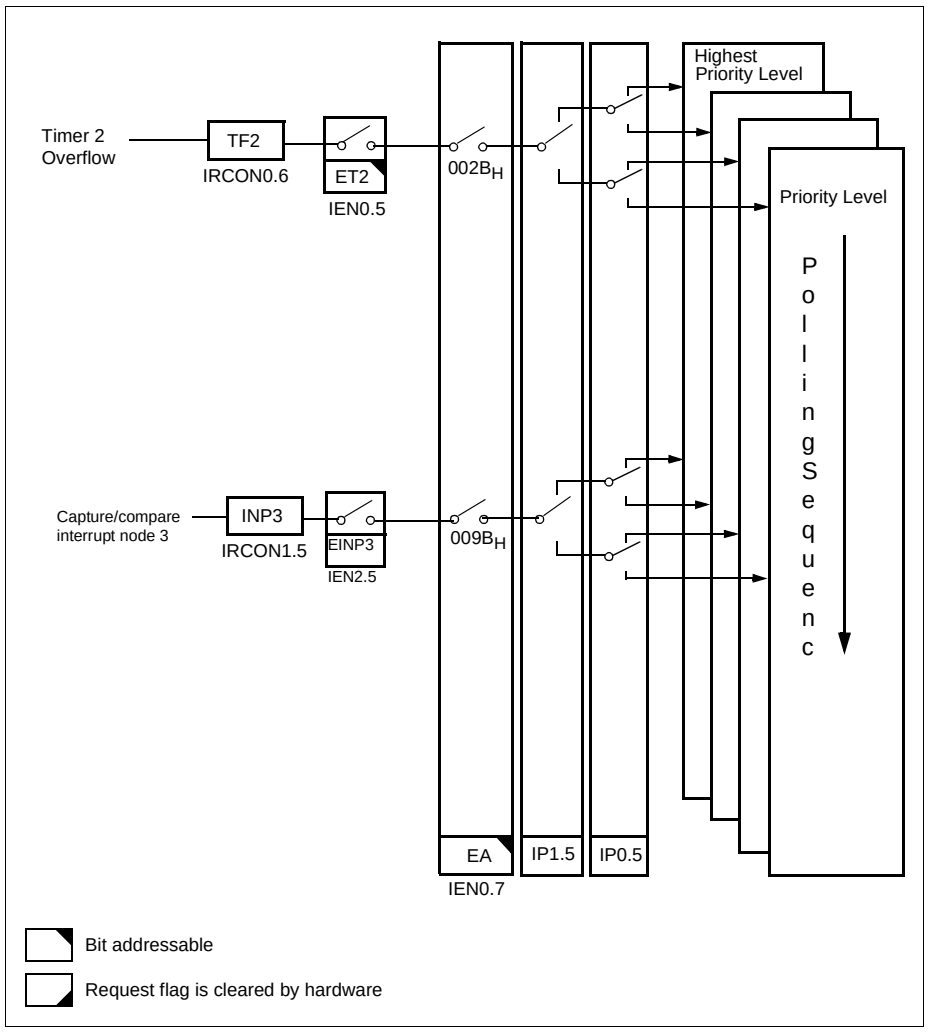


Figure 28 Interrupt Structure, Overview Part 5

Table 12 Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address(core connections)	Interrupt Request Flags
External Interrupt 0	0003_H(EX0)	IE0
Timer 0 Overflow	$000B_H$(ET0)	TF0
External Interrupt 1	0013_H(EX1)	IE1
Timer 1 Overflow	$001B_H$(ET1)	TF1
Serial Channel	0023_H(ES)	RI / TI
Timer 2 Overflow	$002B_H$(EX5)	TF2
A/D Converter	0033_H(EX6)	IADC
External Interrupt 2	$003B_H$(EX7)	IEX2
External Interrupt 3	0043_H(EX8)	IEX3
	$004B_H$(EX9)	
	0053_H(EX10)	
	$005B_H$(EX11)	
	0063_H(EX12)	
	$006B_H$(EX13)	
CAPCOM interrupt node 0	0083_H(EX14)	INP0[1)]
CAPCOM interrupt node 1	$008B_H$(EX15)	INP1[1)]
CAPCOM interrupt node 2	0093_H(EX16)	INP2[1)]
CAPCOM interrupt node3	$009B_H$(EX17)	INP3[1)]
	$00A3_H$(EX18)	
	$00AB_H$(EX19)	
	$00D3_H$(EX20)	
	$00DB_H$(EX21)	
	$00E3_H$(EX22)	
Wake-up from power-down mode	$007B_H$	–

[1)] Capture/compare has 10 interrupt sources channeled to the 4 interrupt nodes INP0..3. The 3 capture/compare ports has 3 pairs of interrupt request flags, ICC60R, ICC60F, ICC61R, ICC61F, ICC62R, ICC62F. The other flags are T12OM, T12PM, T13CM, T13PM, TRPF, WHE, CHE.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is to be serviced first. Thus, within each priority level there is a second priority structure determined by the polling sequence. This is illustrated in **Table 13**

.

Table 13 Interrupt Source Structure

Interrupt Group	Priority Bits of Interrupt Group	Interrupt Source Priority High Priority → Low Priority				Priority
0	IP0.0	EXINT0	IADC			High ↓
1	IP0.1	TF0	EXINT2			
2	IP0.2	EXINT1	EXINT3	INP0[1)]		
3	IP0.3	TF1		INP1[1)]		
4	IP0.4	RI + TI		INP2[1)]		Low
5	IP0.5	TF2		INP3[1)]		

1) Capture/compare has 10 interrupt sources channeled to the 4 interrupt nodes INP0..3. The 3 capture/compare ports has 3 pairs of interrupt request flags, ICC60R, ICC60F, ICC61R, ICC61F, ICC62R, ICC62F. The other flags are T12OM, T12PM, T13CM, T13PM, TRPF, WHE, CHE.

Within a column, the topmost interrupt is serviced first, then the second and the third, when available. The interrupt groups are serviced from left to right of the table. A low-priority interrupt can itself be interrupted by a higher-priority interrupt, but not by another interrupt of the same or a lower priority. An interrupt of the highest priority level cannot be interrupted by another interrupt source.

Fail Save Mechanisms

The C868 offers enhanced fail save mechanisms, which allow an automatic recovery from software upset or hardware failure :

a programmable watchdog timer (WDT), with variable time-out period from 12.8µs to 819.2µs at f_{SYS} = 40 MHz.

Programmable Watchdog Timer

To protect the system against software failure, the user's program has to clear this watchdog within a previously programmed time period. If the software fails to do this periodical refresh of the watchdog timer, an internal reset will be initiated. The software can be designed so that the watchdog times out if the program does not work properly. It also times out if a software error is based on hardware-related problems.

The watchdog timer in the C868 is a 16-bit timer, which is incremented by a count rate of $f_{SYS}/2$ upto $f_{SYS}/128$. The machine clock of the C868 is divided by a prescaler, a divide-by-two or a divide-by-128 prescaler. The upper 8 bits of the Watchdog Timer can be preset to a user-programmable value via a watchdog service access in order to vary the watchdog expire time. The lower 8 bits are reset on each service access. **Figure 29** shows the block diagram of the watchdog timer unit.

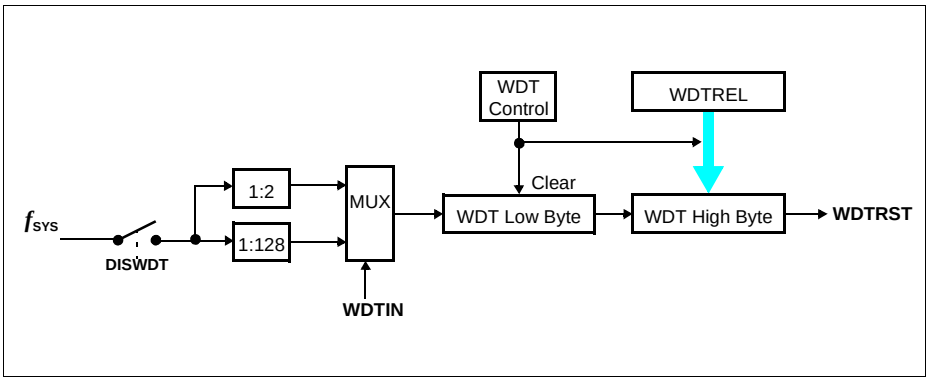


Figure 29 Block Diagram of the Programmable Watchdog Timer

After a reset, the Watchdog Timer is automatically enabled. If it is disabled, it cannot be enabled again during active mode of the device. If the software fails to clear the watchdog timer an internal reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software (status flag WDTR in SCUWDT is set). A refresh of the watchdog timer is done by setting bits WDTRE and WDTRS (in

SFR SCUWDT) consecutively. This double instruction sequence has been implemented to increase system security.

It must be noted, however, that the watchdog timer is halted during the idle mode and power-down mode of the processor (see section "Power Saving Modes"). It is not possible to use the idle mode in combination with the watchdog timer function. Therefore, even the watchdog timer cannot reset the device when one of the power saving modes has been entered accidentally.

The time period for an overflow of the Watchdog Timer is programmable in two ways :

- **the input frequency** to the Watchdog Timer can be selected via bit WDTIN in register WDTCON to be either $f_{SYS}/2$ or $f_{SYS}/128$.
- **the reload value** WDTREL for the high byte of WDT can be programmed in register WDTCON.

The period P_{WDT} between servicing the Watchdog Timer and the next overflow can therefore be determined by the following formula:

[0.1]

$$P_{WDT} = \frac{2^{(1+WDTIN*6)} * (2^{16} - WDTREL * 2^{8})}{f_{SYS}}$$

Table 14 lists the possible ranges for the watchdog time which can be achieved using a certain module clock. Some numbers are rounded to 3 significant digits.

Table 14 Watchdog Time Ranges

Reload value in WDTREL	Prescaler for f_{SYS}					
	2 (WDTIN = '0')			128 (WDTIN = '1')		
	40 MHz	20 MHz	16 MHz	40 MHz	20 MHz	16 MHz
FF_H	12.8 µs	25.6 µs	32.0 µs	819.2 µs	1.64 ms	2.05 ms
$7F_H$	1.65 ms	3.3 ms	4.13 ms	105.7 ms	211.3 ms	264 ms
00_H	3.28 ms	6.55 ms	8.19 ms	209.7 ms	419.4 ms	524 ms

For safety reasons, the user is advised to rewrite WDTCON each time before the Watchdog Timer is serviced.

Power Saving Modes

The C868 provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can also be used for further power reduction in idle mode.

- **Idle Mode**
  In the idle mode, the oscillator of the C868 continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the serial port, the A/D converter, the capture/compare unit, and all timers are further provided with the clock. The CPU status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode.
- **Slow Down Mode**
  In some applications, where power consumption and dissipation are critical, the controller might run for a certain time at reduced speed (for example, if the controller is waiting for an input signal). Since in CMOS devices, there is an almost linear dependence of the operating frequency and the power supply current, so, a reduction of the operating frequency results in reduced power consumption.
- **Software Power Down Mode**
  In the software power down mode, the on-chip oscillator which operates with the XTAL pins and the PLL are all stopped. Therefore, all functions of the microcontroller are stopped and only the contents of the on-chip RAM, XRAM and the SFR's are maintained. The port pins, which are controlled by their port latches, output the values that are held by their SFR's. The port pins which serve the alternate output functions show the values they had at the end of the last cycle of the instruction which initiated the power down mode. ALE is held at logic low level or high impedance if disabled. In the power down mode of operation, V_{DDP} can be reduced to minimize power consumption. It must be ensured, however, that V_{DDP} is not reduced before the power down mode is invoked, and that V_{DDP} is restored to its normal operating level before the power down mode is terminated.

Table 15 Power Saving Modes Overview

Mode	Entering	Leaving by	Remarks
Idle Mode	ORL PCON,#01_H	Occurance of any enabled interrupt	CPU clock is stopped; CPU maintains its data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Slow Down Mode	In normal mode: ORL PCON,#10_H	ANL PCON,#$0EF_H$ or Hardware Reset	Internal clock rate is reduced to a configurable factor of $^1/_2$ to $^1/_{32}$ of the system clock rate
	With idle mode: ORL PCON,#11_H	Occurance of any enabled interrupt to exit idle mode and the instruction ANL PCON,#$0EF_H$ to terminate slow down mode	CPU clock is stopped; CPU maintains all its data; Peripheral units are active (if enabled) and provided with a configurable factor of $^1/_2$ to $^1/_{32}$ of the system clock rate
		Hardware Reset	
Software Power Down mode	With external wake-up capability from power down enabled ORL PMCON0,#01_H (to wake-up via pin $\overline{INT0}$) or ORL PMCON0,#03_H (to wake-up via pin RxD) ORL PCON,#02_H	Hardware Reset	Oscillator is stopped; Contents of on-chip RAM and SFR's are maintained
		When $\overline{INT0}$ or RxD goes low for at least 10 µs (latch phase). But it is desired that the corresponding pin must be held at high level during the power down mode entry and up to the wake-up.	
	With external wake-up capability from power down disabled ORL PCON,#02_H	Hardware Reset	

Device Specifications

Absolute Maximum Ratings

Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature under bias	T_A	-40	125	°C	
Storage temperature	T_{STG}	-65	150	°C	-
Voltage on V_{DDP} pins with respect to ground (V_{SSP})	V_{DDP}	-0.3	4.6	V	-
Voltage on any pin except int/ analog and XTAL with respect to ground (V_{SSP})	V_{IN0}	-0.5	4.6	V	-
Voltage on any int/analog pin with respect to ground (V_{SSP})	V_{IN1}	-0.5	4.6	V	-
Voltage on XTAL pins with respect to ground (V_{SSC})	V_{IN2}	-0.5	4.6	V	-
Input current on any pin during overload condition	I_{OV}	-10	10	mA	-[1)]
Absolute sum of all input currents during overload condition	$\Sigma\|I_{OV}\|$	-	43	mA	-
Power dissipation	P_{DISS}	-	tbd	W	-

1) Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL2 etc.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN}>V_{DDP}$ or $V_{IN}<V_{SSP}$, $V_{IN2}>V_{DDC}$ or $V_{IN2}<V_{SSC}$) the voltage on V_{DDP} pin with respect to ground (V_{SSP}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C868. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage	V_{DDP}	3.0	3.6	V	Active mode, f_{SYSmax} = 40 MHz
		tbd	3.6	V	PowerDown mode[1]
Digital ground voltages	V_{SSC}, V_{SSP}	0		V	-
Ambient temperature	T_A	-40	85	°C	SAF-C868...
		-40	125	°C	SAK-C868...
Analog reference voltage	V_{AREF}	3.0V	V_{DDP} + 0.1	V	-
Analog ground voltage	V_{AGND}	V_{SSP} - 0.1	V_{SSP} + 0.1	V	-
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	-
External Clock	f_{OSC}	6.67	10.67	MHz	-
Input current on any pin during overload condition except int/ analog and XTAL	I_{OV0}	-5	5	mA	-[2][3]
int/analog pin	I_{OV1}	-2	5	mA	-[3][4]
XTAL pin	I_{OV2}	-5	5	mA	-[3][5]
Absolute sum of all input currents during overload condition	ΣI_{OV}	-	|20|	mA	-[3]

Notes:

1) Oscillator or external clock disabled.

2) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{OV} > V_{DDP}$ +0.5V or $V_{OV} < V_{SSP}$ -0.5V). The absolute sum of input currents on all port pins may not exceed 20mA. The suply voltages V_{DDP} and V_{SSP} must remain within the specified limits.

3) Not 100% tested, but guaranteed by design characterization.

4) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{OV} > tbd$ or $V_{OV} < V_{SSC}$ -0.5V). The absolute sum of input currents on all port pins may not exceed 20mA. The suply voltages V_{DDP} and V_{SSP} must remain within the specified limits.

5) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{OV} > V_{DDC}$ +0.5V or $V_{OV} < V_{SSC}$ -0.5V). The absolute sum of input currents on all port pins may not exceed 20mA. The suply voltages V_{DDP} and V_{SSP} must remain within the specified limits.

DC Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltages					–[1]
all except XTAL2, int/analog	V_{IL0}	-0.5	$0.3V_{DDP}$	V	
int/analog	V_{IL1}	-0.5	$0.3V_{DDC}$	V	
XTAL2	V_{IL2}	-0.5	$0.1V_{DDC}$	V	
Input high voltages					–
all except XTAL2, int/analog	V_{IH0}	$0.7V_{DDP}$	$V_{DDP}+0.5$	V	
int/analog	V_{IH1}	$0.7V_{DDC}$	$V_{DDP}+0.5$	V	
XTAL2	V_{IH2}	$0.7V_{DDC}$	$V_{DDC}+0.5$	V	
Output low voltage	V_{OL}	–	0.45	V	SAF-C868... I_{OL}=10mA
		–	0.55	V	SAK-C868... I_{OL}=10mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH}=10mA
Input leakage current (all except int/analog)	I_{LI0}	–	±0.5	uA	$0.4<V_{IN}<V_{DDP}$
Input leakage current (int/ analog)	I_{LI1}	–	±0.5	uA	$0.4<V_{IN}<V_{DDP}$[2]
Input low current (XTAL2)	I_{LI2}	–	±10	uA	$0.4<V_{IN}<V_{DDC}$
Digital supply voltage	V_{DDC}	2.25[3]	2.75	V	–
Blocking capacitor for V_{DDC}		136	470	nF	–[4]
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A= 25^0C

Note:

1) Interrupt/analog pins are input only and has CMOS characteristics whereas the other I/O pins have TTL characteristics.

2) The leakage current of interrupt/analog pins depends on the leakage current of the CMOS pad for the digital functions and the analog pad.

3) The V_{DDC} is measured under the following conditions:

Microcontroller in power down mode;$\overline{\text{RESET}}$ = V_{DDP}; XTAL2 = V_{SSC}; XTAL1 = N.C.; V_{AGND}= V_{SSP}; V_{AREF}= V_{DDP}; RxD/INT0 = V_{DDP}; all other pins are set to input and connected to gnd; ALE output disabled and connected to gnd; 20mA current sourced from the V_{DDC} pin.

4) Ceramic type (±20%) max ESR: 25mΩ ,max trace length to capacitor is 10mm.

Power Supply Current

Parameter			Symbol	Limit Values		Unit	Test Condition
				typ.[1]	max.[2]		
Active mode	C868-1S	40 MHz[3]	I_{DDP}	13.1	15.6	mA	[4]
	C868-1R	40 MHz[3]	I_{DDP}	13.5	15.5	mA	
Idle mode	C868-1S	40 MHz[3]	I_{DDP}	7.8	9.6	mA	[5]
	C868-1R	40 MHz[3]	I_{DDP}	7.9	9.1	mA	
Active mode with slow-down enabled	C868-1S	40 MHz[3]	I_{DDP}	3.5	4.4	mA	[6]
	C868-1R	40 MHz[3]	I_{DDP}	3.6	4.1	mA	
Idle mode with slow-down enabled	C868-1S	40 MHz[3]	I_{DDP}	3.4	4.2	mA	[7]
	C868-1R	40 MHz[3]	I_{DDP}	3.6	4.1	mA	
Power-down mode	C868-1S		I_{PDP}	240	300	uA	SAF-C868...[8]
				240	400	uA	SAK-C868...[8]
	C868-1R		I_{PDP}	240	300	uA	SAF-C868...[8]
				240	400	uA	SAK-C868...[8]

Note:

1) The typical I_{DDP} values are periodically measured at T_A = + 25 °C but not 100% tested.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = – 40 °C and V_{DDP} = 3.6 V).

3) System clock, set by using external clock of 10.67MHz and setting KDIV in CMCON to 010 (factor of 4)

4) I_{DDP} (active mode) is measured with:
XTAL2 driven with t_R, t_F = 5 ns, V_{IL1},V_{IL2} = V_{SSP} + 0.5 V, V_{IH1},V_{IH2} = V_{DDP} – 0.5 V; XTAL1 = N.C.;
RESET = V_{DDP}; all other pins are disconnected. ?I_{DDP} would be slightly higher if the crystal oscillator is used (approx. 1 mA).

5) I_{DDP} (idle mode) is measured with all output pins disconnected and with all peripheral disabled:
XTAL2 driven with t_R, t_F = 5 ns, V_{IL1},V_{IL2} = V_{SSP} + 0.5 V, V_{IH1},V_{IH2} = V_{DDP} – 0.5 V; XTAL1 = N.C.; $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected.

6) I_{DDP} (active mode with slow down mode) is measured with all output pins disconnected:
XTAL2 driven with t_R, t_F = 5 ns, V_{IL1},V_{IL2} = V_{SSP} + 0.5 V, V_{IH1},V_{IH2} = V_{DDP} – 0.5 V; XTAL1 = N.C.; $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected; the microcontroller is put into slow-down mode by software with the slow-down clock set to 1/32 of system clock.

7) I_{DDP} (idle mode with slow down mode) is measured with all output pins disconnected and with all peripheral disabled:
XTAL2 driven with t_R, t_F = 5 ns, V_{IL1},V_{IL2} = V_{SSP} + 0.5 V, V_{IH1},V_{IH2} = V_{DDP} – 0.5 V; XTAL1 = N.C.; $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected; the microcontroller is put into slow-down mode by software with the slow-down clock set to 1/32 of system clock.

8) I_{PDC} and I_{PDP} (power-down mode) are measured under the following conditions:
$\overline{\text{RESET}}$ = V_{DDP}; XTAL2 = V_{SSC}; XTAL1 = N.C.; V_{AGND}= V_{SSP}; V_{AREF}= V_{DDP}; RxD/INT0 = V_{DDP}; all other pins are set to input and connected to gnd; ALE output disabled and connected to gnd.

Power Supply Current Calculation Formulae

Parameter		Symbol	Formula[1)]
Active mode	C868-1S	I_{DDPtyp}	0.25* f_{SYS} + 3.1
		I_{DDPmax}	0.26 * f_{SYS} + 5.2
	C868-1R	I_{DDPtyp}	0.27* f_{SYS} + 2.7
		I_{DDPmax}	0.29 * f_{SYS} + 3.9
Idle mode	C868-1S	I_{DDPtyp}	0.13* f_{SYS} + 2.6
		I_{DDPmax}	0.13 * f_{SYS} + 4.0
	C868-1R	I_{DDPtyp}	0.13* f_{SYS} + 3.7
		I_{DDPmax}	0.15 * f_{SYS} + 3.1
Active mode with slow-down enabled	C868-1S	I_{DDPtyp}	0.01 * f_{SYS} + 3.1
		I_{DDPmax}	0.02 * f_{SYS} + 3.6
	C868-1R	I_{DDPtyp}	0.01 * f_{SYS} + 3.2
		I_{DDPmax}	0.01 * f_{SYS} + 3.7
Idle mode with slow-down enabled	C868-1S	I_{DDPtyp}	0.01* f_{SYS} + 3.0
		I_{DDPmax}	0.01 * f_{SYS} + 3.8
	C868-1R	I_{DDPtyp}	0.02* f_{SYS} + 2.8
		I_{DDPmax}	0.02 * f_{SYS} + 3.3

1) f_{SYS} is in MHz and results in mA.

A/D Converter Characteristics

(Operating Condition Parameters)

Parameter	Symbol	Limits		Unit	Test Condition
		min	max		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	64*t_{SYS} 52*t_{SYS} 48*t_{SYS} 40*t_{SYS} 32*t_{SYS} 24*t_{SYS} 16*t_{SYS} 8*t_{SYS}	512*t_{SYS} 448*t_{SYS} 384*t_{SYS} 320*t_{SYS} 256*t_{SYS} 192*t_{SYS} 128*t_{SYS} 64*t_{SYS}	ns	Prescaler/32 Prescaler/28 Prescaler/24 Prescaler/20 Prescaler/16 Prescaler/12 Prescaler/8 Prescaler/4
Conversion cycle time	t_{ADCC}	322*t_{SYS} 282*t_{SYS} 242*t_{SYS} 202*t_{SYS} 162*t_{SYS} 122*t_{SYS} 82*t_{SYS} 42*t_{SYS}	770*t_{SYS} 674*t_{SYS} 578*t_{SYS} 482*t_{SYS} 386*t_{SYS} 290*t_{SYS} 194*t_{SYS} 98*t_{SYS}	ns	Prescaler/32 Prescaler/28 Prescaler/24 Prescaler/20 Prescaler/16 Prescaler/12 Prescaler/8 Prescaler/4
Total unadjusted error	T_{UE}	– –	±2 ±3	LSB	$V_{AGND} \le V_{AIN} \le V_{AREF}$ 2) $V_{AGND} \le V_{AIN} \le V_{AREF}$ 3)
ADC input resistance	R_{AIN}	–	1.5	kΩ	4)5)
ADC input capacitance	C_{AIN}	–	10	pF	5)
ADC reference pin capacitance	C_{AREF}	–	40	pF	5)

Note:

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the maximum ratings. However, the conversion result in these cases will be 00_H or FF_H, respectively.

2) T_{UE} (max.) is tested at $-20 \le T_A \le 125$ °C; $V_{DDP} = 3.3$ V; $V_{AREF} = V_{DDP}$ V and $V_{SSP} = V_{AGND}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.

3) T_{UE} (max.) is tested at $-40 \le T_A < -20$ °C; $V_{DDP} \le 3.3$ V; $V_{AREF} = V_{DDP}$ and $V_{SSP} = V_{AGND}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.

4) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

5) Not 100% tested, but guaranteed by design characterization.

Clock calculation table for ADC

TVC[1)]	32								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	322	386	450	514	578	642	706	770	t_{SYS}
t_S	64	128	192	256	320	384	448	512	t_{SYS}

TVC[1)]	28								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	282	338	394	450	506	562	618	674	t_{SYS}
t_S	56	112	168	224	280	336	392	448	t_{SYS}

TVC[1)]	24								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	242	290	338	386	434	482	530	578	t_{SYS}
t_S	48	96	144	192	240	288	336	384	t_{SYS}

TVC[1)]	20								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	202	242	282	322	362	402	442	482	t_{SYS}
t_S	40	80	120	160	200	240	280	320	t_{SYS}

TVC[1)]	16								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	162	194	226	258	290	322	354	386	t_{SYS}
t_S	32	64	96	128	160	192	224	256	t_{SYS}

TVC[1)]	12								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	122	146	170	194	218	242	266	290	t_{SYS}
t_S	24	48	72	96	120	144	168	192	t_{SYS}

TVC[1)]	8								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	82	98	114	130	146	162	178	194	t_{SYS}
t_S	16	32	48	64	80	96	112	128	t_{SYS}

TVC[1)]	4								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	42	50	58	66	74	82	90	98	t_{SYS}
t_S	8	16	24	32	40	48	56	64	t_{SYS}

1) TVC is the clock divider specified by bit fields ADCTC.

2) STC is the sample time control specified by bit fields ADSTC.

3) t_{ADC} is t_{SYS}*TVC

AC Characteristics

(Operating Condition Apply)

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Ext Clock 6.67 to 10.67 MHz		
		min	max	
Oscillating period	t_{OSC}	93.75	150	ns
High time	t_1	46.875	75	ns
Low time	t_2	46.875	75	ns
Rise time	t_R	-	10	ns
Fall time	t_F	-	10	ns

ALE Characteristics

Parameter	Symbol	Limit Values		Unit
		System freq = 6.25MHz to 40MHz Duty Cycle 0.5		
		min	max	
ALE pulse width	t_{AWD}	50	320	ns
ALE period	t_{ACY}	150	960	ns

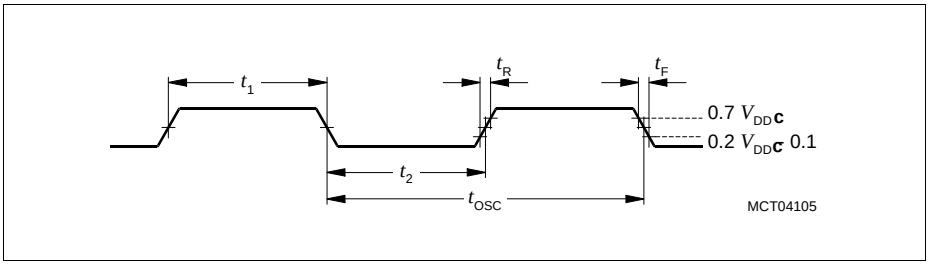


Figure 30 External Clock Drive on XTAL2

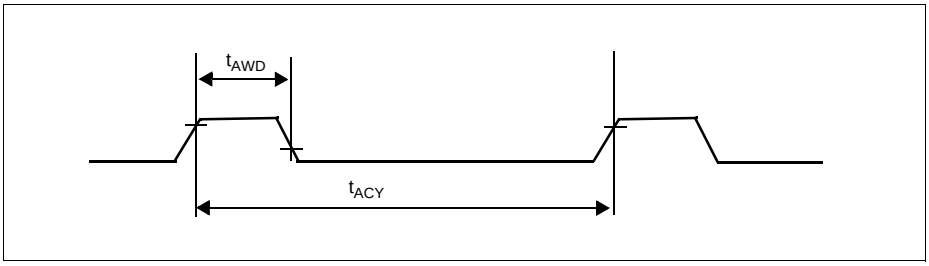
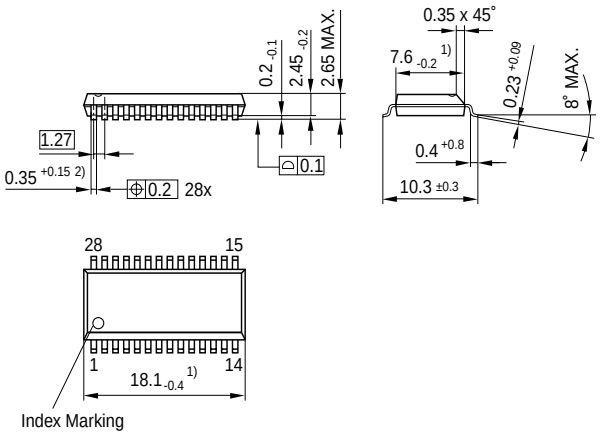


Figure 31 ALE Characteristic

Package Outlines

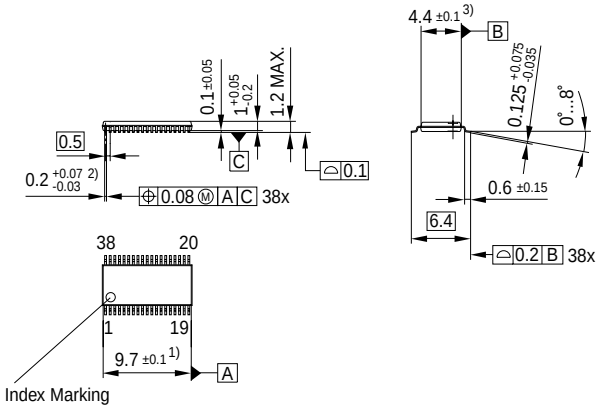
Plastic Package, P-DSO-28-1 for SAF-C868-1RG BA, SAF-C868-1SG BA SAF-C868A-1RG BA, SAF-C868A-1SG BA and SAF-C868P-1SG BA, SAK-C868-1RG BA, SAK-C868-1SG BA, SAK-C868A-1RG BA, SAK-C868A-1SG BA and SAK-C868P-1SG BA.



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

Figure 32 DSO-28-1 Package Outlines

Plastic Package, P-TSSOP-38-1 for SAF-C868-1RR BA, SAF-C868-1SR BA, SAF-C868A-1RR BA, SAF-C868A-1SR BA, SAF-C868P-1SR BA, SAK-C868-1RR BA, SAK-C868-1SR BA, SAK-C868A-1RR BA, SAK-C868A-1SR BA, and SAK-C868P-1SR BA.



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side
3) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 33 TSSOP-38-1 Package Outlines

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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Dr. Ulrich Schumacher

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