THE DATASHEET OF

LTC6087HDD#TRPBF

Dual/Quad 14MHz, Rail-to-Rail CMOS Amplifiers

FEATURES

- **Low Offset Voltage: 750μV Maximum**
- **Low Offset Drift: 5μV/°C Maximum**
- **Input Bias Current:**
  1pA (Typical at 25°C)
  15pA (Typical at 85°C)
- **Rail-to-Rail Inputs and Outputs**
- Gain Bandwidth Product: 14MHz
- CMRR: 70dB Minimum
- PSRR: 93dB Minimum
- Input Noise Voltage Density: 12nV/√Hz
- Supply Current: 1.05mA per Amp
- Shutdown Current: 2.3μA per Amp
- 2.7V to 5.5V Operation Voltage
- Available in 8-Lead MSOP and 10-Lead DFN Packages (LTC6087), 16-Lead SSOP and DFN Packages (LTC6088)

APPLICATIONS

- Portable Test Equipment
- Medical Equipment
- Audio
- Data Acquisition
- High Impedance Transducer Amplifier

DESCRIPTION

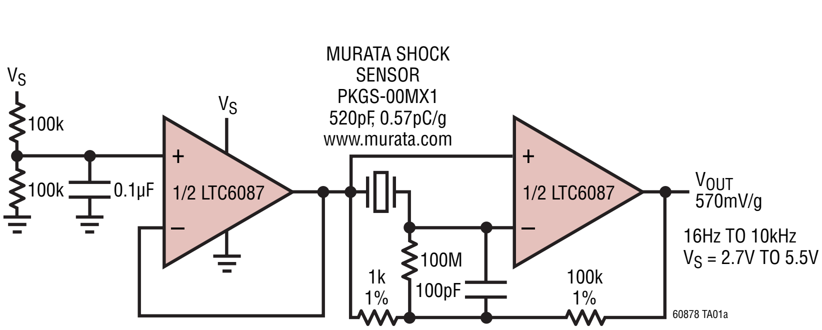
The LTC®6087/LTC6088 are dual/quad, low noise, low offset, rail-to-rail input/output, unity-gain stable CMOS operational amplifiers that feature 1pA of input bias current. A 14MHz gain bandwidth and 7.2V/μs slew rate, combined with low noise (10nV/√Hz) and a low 0.75mV offset, make the LTC6087/LTC6088 useful in a variety of applications. The 1.05mA supply current and the shutdown mode are ideal for signal processing applications which demand performance with minimal power.

The LTC6087/LTC6088 has an output stage which swings within 30mV of either supply rail to maximize signal dynamic range in low supply applications. The input common mode range includes the entire supply voltage. These op amps are specified on power supply voltages of 3V and 5V from –40°C to 125°C.

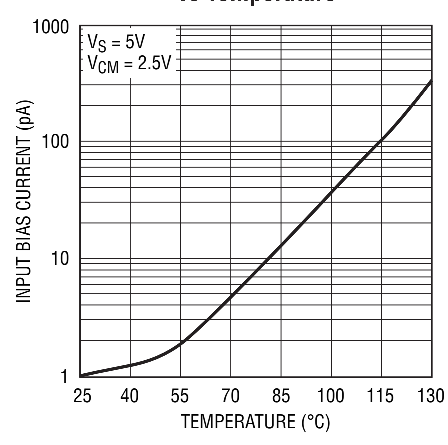
The dual amplifier LTC6087 is available in 8-lead MSOP and 10-lead DFN packages. The quad amplifier LTC6088 is available in 16-lead SSOP and DFN packages.

TYPICAL APPLICATION

Single Supply Shock/Vibration Sensor Amplifier



LTC6087 Input Bias Current vs Temperature



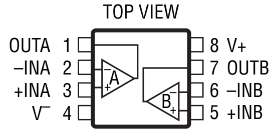
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to $V^–$) 6V
Input Voltage .... $V^–$ to V^+
Input Current .... ±10mA
$\overline{\text{SHDNA}}$/$\overline{\text{SHDNB}}$ Voltage .... $V^–$ to V^+
Output Short-Circuit Duration (Note 2) .... Indefinite
Operating Temperature Range (Note 3)
LTC6087C/LTC6088C ....–40°C to 85°C
LTC6087H/LTC6088H .... –40°C to 125°C

Specified Temperature Range (Note 4)
LTC6087C/LTC6088C .... 0°C to 70°C
LTC6087H/LTC6088H .... –40°C to 125°C
Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS8, GN16 Only .... 300°C

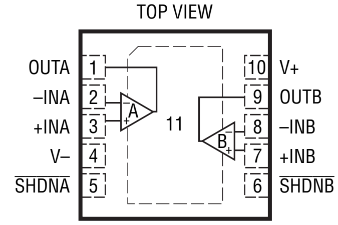
PIN CONFIGURATION

TOP VIEW



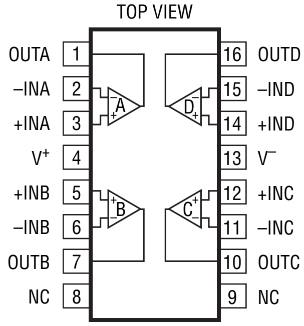
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 200°C/W

TOP VIEW



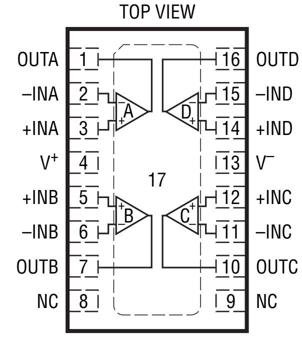
DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS $V^–$, MUST BE SOLDERED TO PCB

TOP VIEW



GN PACKAGE
16-LEAD PLASTIC SSOP NARROW
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

TOP VIEW



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS $V^–$, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LTC6087-X#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6087CDD#PBF	LTC6087CDD#TRPBF	LCTX	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6087HDD#PBF	LTC6087HDD#TRPBF	LCTX	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6087CMS8#PBF	LTC6087CMS8#TRPBF	LTCTY	8-Lead Plastic MSOP	–40°C to 85°C
LTC6087HMS8#PBF	LTC6087HMS8#TRPBF	LTCTY	8-Lead Plastic MSOP	–40°C to 125°C
LTC6088CDHC#PBF	LTC6088CDHC#TRPBF	6088	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6088HDHC#PBF	LTC6088HDHC#TRPBF	6088	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6088CGN#PBF	LTC6088CGN#TRPBF	6088	16-Lead Plastic SSOP	–40°C to 85°C
LTC6088HGN#PBF	LTC6088HGN#TRPBF	6088H	16-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 3V, $V^–$ = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX MIN	C SUFFIX TYP	C SUFFIX MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
V_{OS}	Offset Voltage (Note 5)	LTC6087MS8, LTC6088GN LTC6087DD, LTC6088DHC LTC6087MS8, LTC6088GN LTC6087DD, LTC6088DHC	 ● ●		±330 ±330	±750 ±1100 ±900 ±1350		±330 ±330	±750 ±1100 ±1100 ±1600	µV µV µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)	LTC6087MS8, LTC6088GN LTC6087DD, LTC6088DHC	● ●		±2 ±2	±5 ±5		±2 ±2	±5 ±5	µV/°C µV/°C
I_B	Input Bias Current (Notes 5, 7)	Guaranteed by 5V Test	 ●		1	 40		1	 500	pA pA
I_{OS}	Input Offset Current (Notes 5, 7)	Guaranteed by 5V Test	 ●		0.5	 30		0.5	 150	pA pA
e_n	Input Noise Voltage Density	f = 1kHz f = 10kHz			12 10			12 10		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Input Noise Voltage	0.1Hz to 10Hz			2.5			2.5		μV_{P-P}
i_n	Input Noise Current Density (Note 8)	f = 1Hz			0.56			0.56		$fA/\sqrt{Hz}$
	Input Common Mode Range		●	$V^–$		V^+	$V^–$		V^+	V
C_{IN}	Input Capacitance Differential Mode Common Mode	f = 100kHz			 2.7 4.2			 2.7 4.2		 pF pF
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V	 ●	64 63	80		64 61	80		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 5.5V	 ●	93 90	115		93 85	115		dB dB
V_{OUT}	Output Voltage, High (Referred to V^+)	No Load I_{SOURCE} = 1mA I_{SOURCE} = 5mA	● ● ●		5 25 120	15 50 210		5 25 120	20 50 230	mV mV mV
	Output Voltage, Low (Referred to $V^–$)	No Load I_{SINK} = 1mA I_{SINK} = 5mA	● ● ●		5 25 120	25 50 210		5 25 120	30 60 240	mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 3V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX MIN	C SUFFIX TYP	C SUFFIX MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	R_{LOAD} = 10k, 0.5V ≤ V_{OUT} ≤ 2.5V	 ●	500 300	3000		500 30	3000		V/mV V/mV
I_{SC}	Output Short-Circuit Current	Source and Sink	 ●	25 21	35		25 18	35		mA mA
SR	Slew Rate	A_V = 1			7.2			7.2		V/μs
GBW	Gain Bandwidth Product (f_{TEST} = 20kHz)	R_{LOAD} = 50k, V_{CM} = 1.5V	 ●	10 9	14		10 8	14		MHz MHz
Φ_0	Phase Margin	R_L = 10k, C_L = 5pF, A_V = 1, V_{CM} = V_S/2			45			45		Deg
t_S	Settling Time 0.1%	V_{STEP} = 2V, A_V = –1, R_L = 1k			1			1		μs
I_S	Supply Current (per Amplifier)	No Load	 ●		1.05 1.05	1.20 1.25		1.05 1.05	1.20 1.35	mA mA
	Shutdown Current (per Amplifier)	Shutdown, $V_{\overline{SHDNx}}$ ≤ 0.8V	●		0.2	1		0.2	1	μA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7		5.5	2.7		5.5	V
	Channel Separation	f_S = 10kHz			–120			–120		dB
	Shutdown Logic	$\overline{SHDNx}$ High $\overline{SHDNx}$ Low	● ●	2 		 0.8	2 		 0.8	V V
t_{ON}	Turn-On Time	$V_{\overline{SHDNx}}$ = 0.8V to 2V			6			6		μs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDNx}}$ = 2V to 0.8V			2			2		μs
	Leakage of $\overline{SHDN}$ Pin	$V_{\overline{SHDNx}}$ = 0V	●		0.1	0.5		0.1	0.5	μA

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 5V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX MIN	C SUFFIX TYP	C SUFFIX MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
V_{OS}	Offset Voltage (Note 5)	LTC6087MS8, LTC6088GN LTC6087DD, LTC6088DHC LTC6087MS8, LTC6088GN LTC6087DD, LTC6088DHC	 ● ●		±330 ±330	±750 ±1100 ±900 ±1350		±330 ±330	±750 ±1100 ±1100 ±1600	μV μV μV μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)	LTC6087MS8, LTC6088GN LTC6087DD, LTC6088DHC	● ●		±2 ±2	±5 ±5		±2 ±2	±5 ±5	μV/°C μV/°C
I_B	Input Bias Current (Notes 5, 7)		 ●		1	 40		1	 500	pA pA
I_{OS}	Input Offset Current (Notes 5, 7)		 ●		0.5	 30		0.5	 150	pA pA
e_n	Input Noise Voltage Density	f = 1kHz f = 10kHz			12 10			12 10		nV/√Hz nV/√Hz
	Input Noise Voltage	0.1Hz to 10Hz			2.5			2.5		$μV_{P-P}$
i_n	Input Noise Current Density (Note 8)	f = 1Hz			0.56			0.56		fA/√Hz
	Input Common Mode Range		●	V^-		V^+	V^-		V^+	V
C_{IN}	Input Capacitance Differential Mode Common Mode	f = 100kHz			 2.7 4.2			 2.7 4.2		 pF pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 5V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX MIN	C SUFFIX TYP	C SUFFIX MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	 ●	70 68	84		70 66	84		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 5.5V	 ●	93 90	115		93 85	115		dB dB
V_{OUT}	Output Voltage, High (Referred to V^+)	No Load I_{SOURCE} = 1mA I_{SOURCE} = 5mA	● ● ●		5 20 110	15 50 190		5 20 110	20 50 210	mV mV mV
	Output Voltage, Low (Referred to V^-)	No Load I_{SINK} = 1mA I_{SINK} = 5mA	● ● ●		5 20 110	25 50 200		5 20 110	30 60 220	mV mV mV
A_{VOL}	Large-Signal Voltage Gain	R_{LOAD} = 10k, 0.5V ≤ V_{OUT} ≤ 4.5V	 ●	1000 500	6000		1000 50	6000		V/mV V/mV
I_{SC}	Output Short-Circuit Current	Source and Sink	 ●	28 25	45		28 22	45		mA mA
SR	Slew Rate	A_V = 1			7.2			7.2		V/µs
GBW	Gain Bandwidth Product (f_{TEST} = 20kHz)	R_{LOAD} = 50k, V_{CM} = 2.5V	 ●	10 9	14		10 8	14		MHz MHz
Φ_0	Phase Margin	R_L = 10k, C_L = 5pF, A_V = 1, V_{CM} = V_S/2			47			47		Deg
t_S	Settling Time 0.1%	V_{STEP} = 2V, A_V = –1, R_L = 1k			0.8			0.8		µs
I_S	Supply Current (per Amplifier)	No Load	 ●		1.05 1.05	1.25 1.30		1.05 1.05	1.25 1.40	mA mA
	Shutdown Current (per Amplifier)	Shutdown, $V_{\overline{SHDNx}}$ ≤ 1.2V	●		2.3	5		2.3	5	µA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7		5.5	2.7		5.5	V
	Channel Separation	f_S = 10kHz			–120			–120		dB
	Shutdown Logic	$\overline{SHDNx}$ High $\overline{SHDNx}$ Low	● ●	3.5		 1.2	3.5		 1.2	V V
t_{ON}	Turn-On Time	$V_{\overline{SHDNx}}$ = 1.2V to 3.5V			6			6		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDNx}}$ = 3.5V to 1.2V			2			2		µs
	Leakage of $\overline{SHDN}$ Pin	$V_{\overline{SHDNx}}$ = 0V	●		0.4	1		0.4	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and the total output current.

Note 3: The LTC6087C/LTC6088C are guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6087H/LTC6088H are guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 4: The LTC6087C/LTC6088C are guaranteed to meet specified performance from 0°C to 70°C. The LTC6087C/LTC6088C are designed, characterized and expected to meet specified performance from –40°C to 125°C but are not tested or QA sampled at these temperatures. The LTC6087H/LTC6088H are guaranteed to meet specified performance from –40°C to 125°C.

Note 5: ESD (electrostatic discharge) sensitive device. ESD protection devices are used extensively internal to the LTC6087/LTC6088; however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 6: This parameter is not 100% tested.

Note 7: This specification is limited by high speed automated test capability. See Typical Performance Characteristic curves for actual performance.

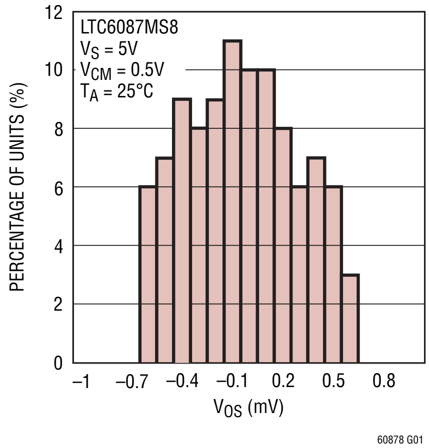
Note 8: Current noise is calculated from:

$$i_n = \sqrt{2qI_B},$$

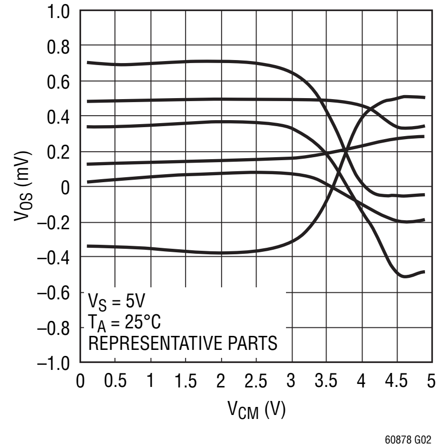
where q = 1.6 • 10^{-19} coulombs.

TYPICAL PERFORMANCE CHARACTERISTICS

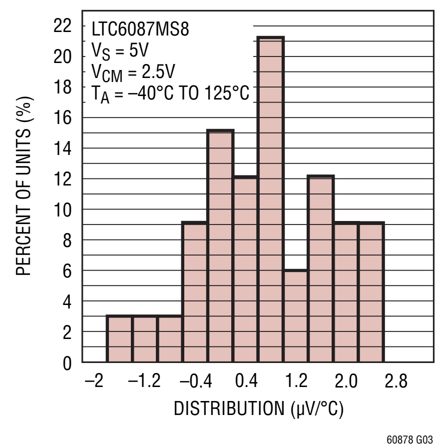
V_{OS} Distribution



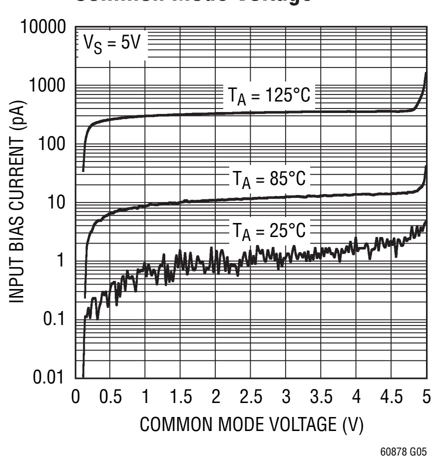
V_{OS} vs V_{CM}



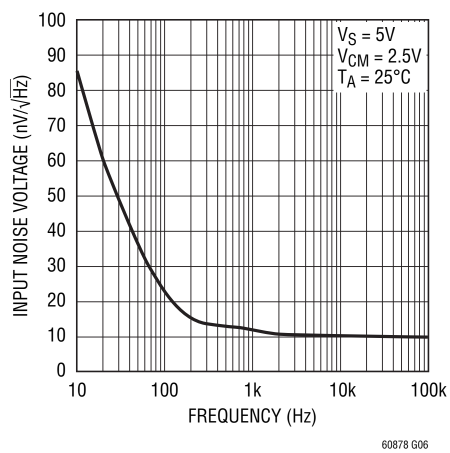
V_{OS} Drift Distribution



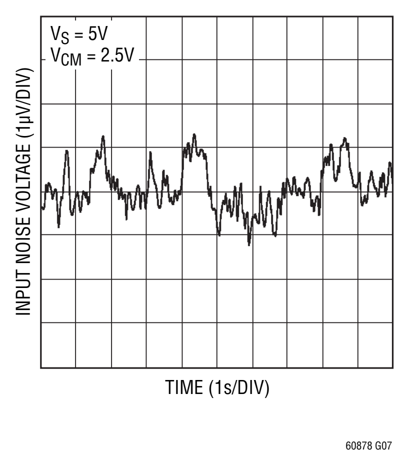
Input Bias Current vs Common Mode Voltage



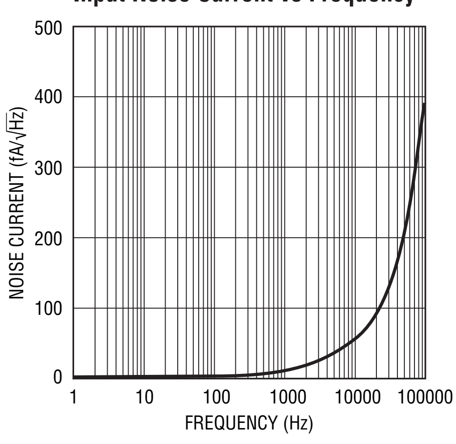
Input Noise Voltage vs Frequency



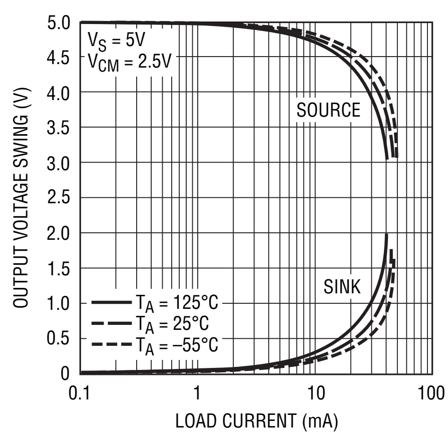
0.1Hz to 10Hz Output Voltage Noise



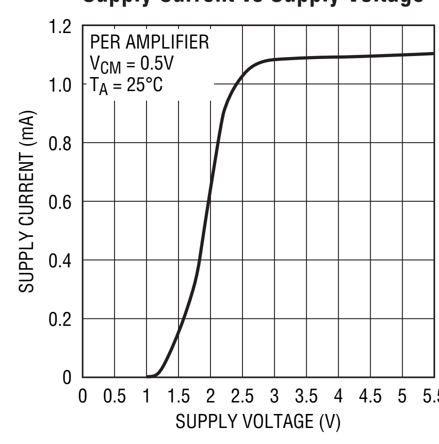
Input Noise Current vs Frequency



Output Voltage Swing vs Load Current

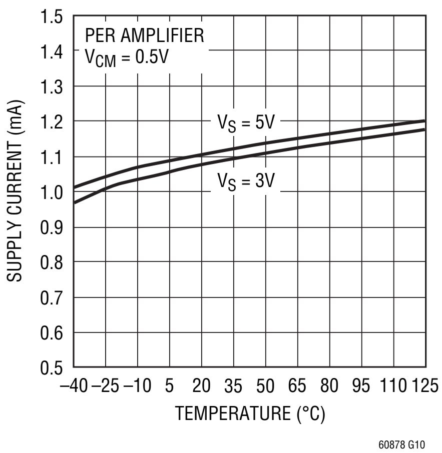


Supply Current vs Supply Voltage

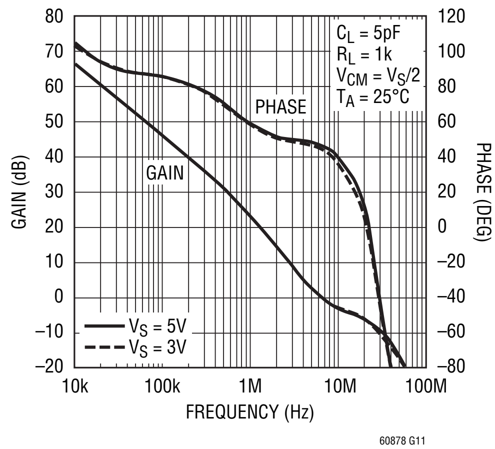


TYPICAL PERFORMANCE CHARACTERISTICS

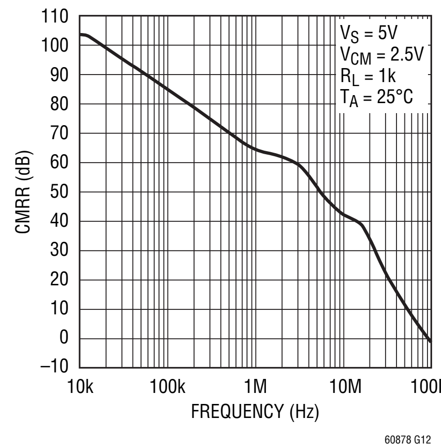
Supply Current vs Temperature



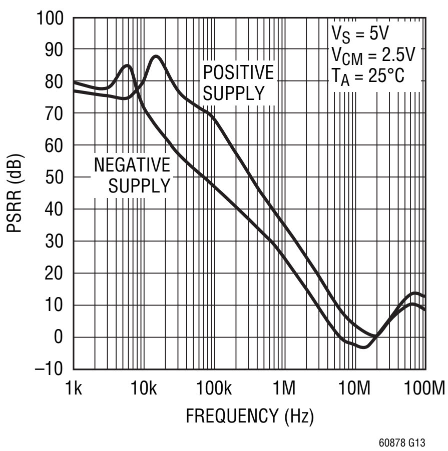
Open-Loop Gain vs Frequency



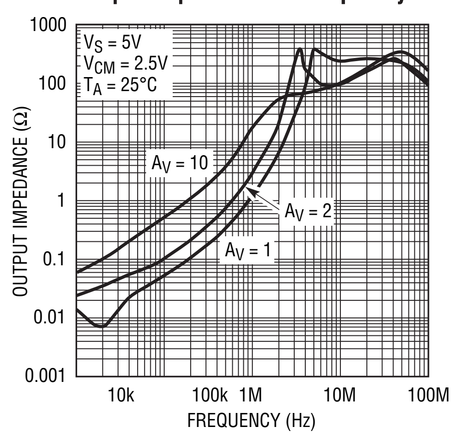
CMRR vs Frequency



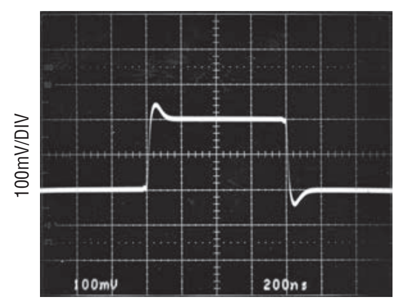
PSRR vs Frequency



Output Impedance vs Frequency

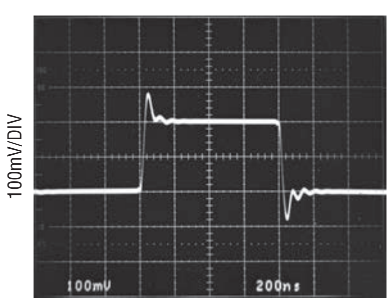


Small-Signal Response



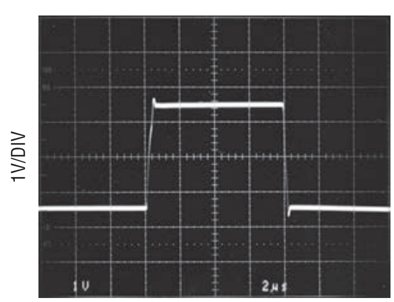
V_S = 5V 200ns/DIV
A_V = 1
R_L = ∞

Small-Signal Response



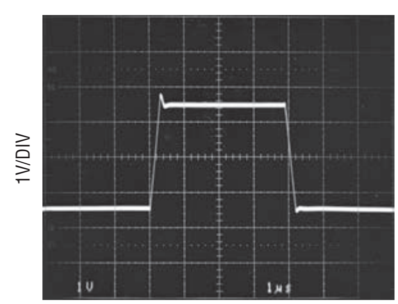
V_S = 5V 200ns/DIV
A_V = 1
R_L = ∞
C_L = 33pF

Large-Signal Response



V_S = 5V 2µs/DIV
A_V = 1
R_L = ∞

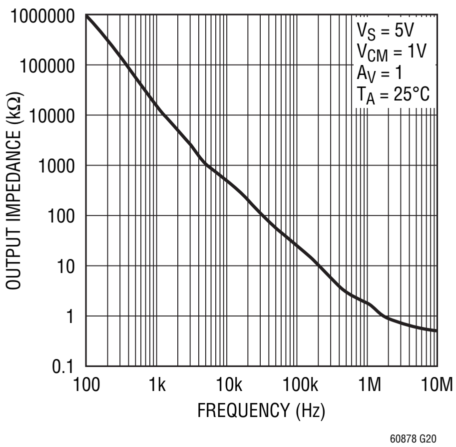
Large-Signal Response



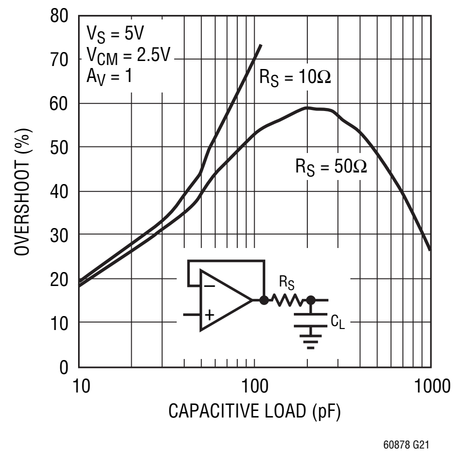
V_S = 5V 1µs/DIV
A_V = –1
R_L = 1k

TYPICAL PERFORMANCE CHARACTERISTICS

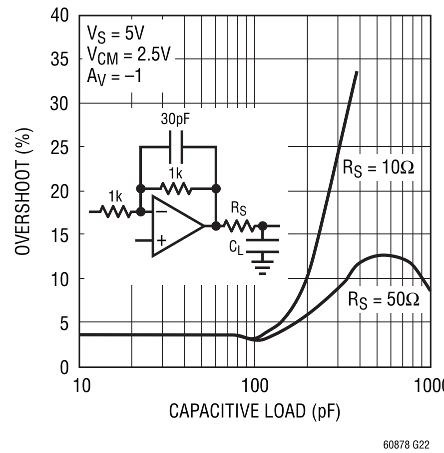
Disabled Output Impedance vs Frequency



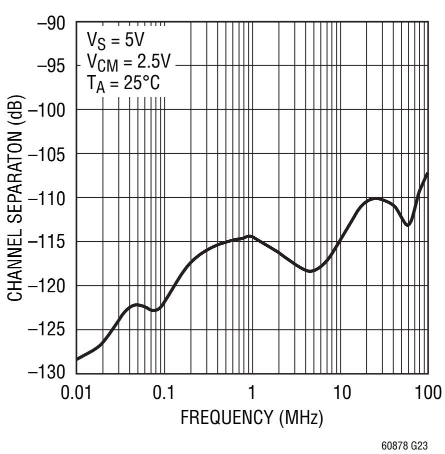
Overshoot vs Capacitive Load



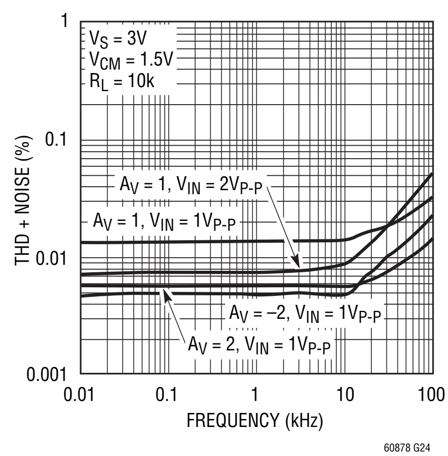
Overshoot vs Capacitive Load



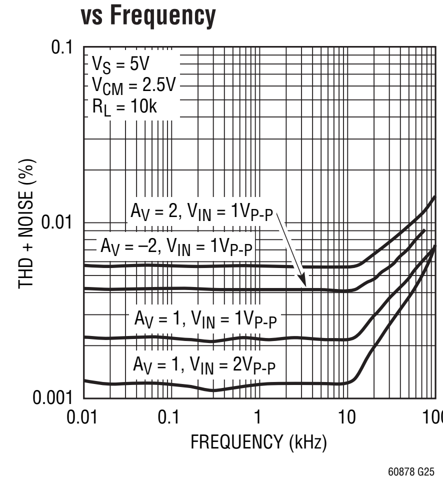
Channel Separation vs Frequency



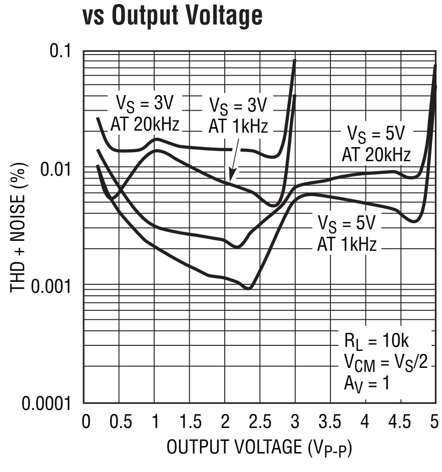
Total Harmonic Distortion + Noise vs Frequency



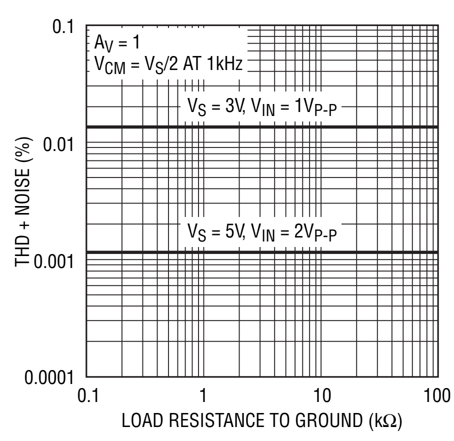
Total Harmonic Distortion + Noise vs Frequency



Total Harmonic Distortion + Noise vs Output Voltage



Total Harmonic Distortion + Noise vs Load Resistance



PIN FUNCTIONS

OUT: Amplifier Output.

–IN: Inverting Input.

+IN: Noninverting Input.

V+: Positive Supply.

V–: Negative Supply.

$\overline{\text{SHDNA}}$: Shutdown Pin of Amplifier A, active low and only available with the LTC 6087DD. An internal current source pulls the pin to V^+ when floating.

$\overline{\text{SHDNB}}$: Shutdown Pin of Amplifier B, active low and only available with the LTC 6087DD. An internal current source pulls the pin to V^+ when floating.

NC: Not internally connected

Exposed Pad: Connected to $V^–$.

APPLICATIONS INFORMATION

Rail-to-Rail Input

The input stage of LTC6087/LTC6088 combines both PMOS and NMOS differential pairs, extending its input common mode voltage to both positive and negative supply voltages. At high input common mode range, the NMOS pair is on. At low common mode range, the PMOS pair is on. The transition happens when the common voltage is between 1.3V and 0.9V below the positive supply.

Achieving Low Input Bias Current

The DD and DHC packages are leadless and make contact to the PCB beneath the package. Solder flux used during the attachment of the part to the PCB can create leakage current paths and can degrade the input bias current performance of the part. All inputs are susceptible because the backside paddle is connected to $V^–$ internally. As the input voltage or $V^–$ changes, a leakage path can be formed and alter the observed input bias current. For lowest bias current use the LTC6087/LTC6088 in the leaded MSOP/GN package. With fine PCB design rules, you can also provide a guard ring around the inputs.

For example, in high source impedance applications such as pH probes, photo diodes, strain gauges, et cetera, the low input bias current of these parts requires a clean board layout to minimize additional leakage current into a high impedance signal node. A mere 100GΩ of PC board resistance between a 5V supply trace and input trace near ground potential adds 50pA of leakage current. This leakage is far greater than the bias current of the operational amplifier. A guard ring around the high impedance input traces driven by a low impedance source equal to the input voltage prevents such leakage problems. The guard ring should extend as far as necessary to shield the high impedance signal from any and all leakage paths. Figure 1 shows the use of a guard ring in a unity-gain configuration. In this case the guard ring is connected to the output and is shielding the high impedance noninverting input from $V^–$. Figure 2 shows the inverting gain configuration.

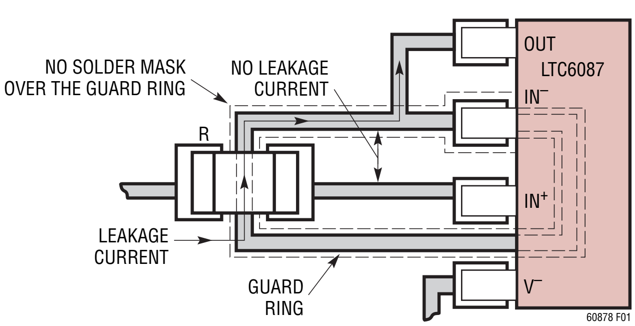


Figure 1. Sample Layout. Unity-Gain Configuration. Using Guard Ring to Shield High Impedance Input from Board Leakage

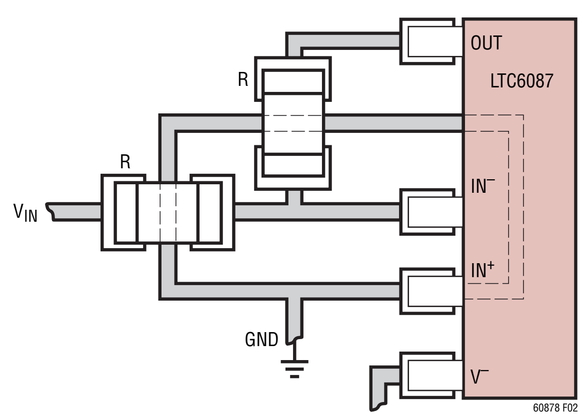


Figure 2. Sample Layout. Inverting Gain Configuration. Using Guard Ring to Shield High Impedance Input from Board Leakage

APPLICATIONS INFORMATION

Rail-to-Rail Output

The output stage of the LTC6087/LTC6088 swings within 30mV of the supply rails when driving high impedance loads, in other words when no DC load current is present. See the Typical Performance Characteristics for curves of output swing versus load current. The class AB design of the output stage enables the op amp to supply load currents which are much greater than the quiescent supply current. For example, the room temperature short circuit current is typically 45mA.

Capacitive Load

LTC6087/LTC6088 can drive capacitive load up to 100pF in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the output and the load further increases the amount of capacitance the amplifier can drive.

$\overline{\text{SHDN}}$ Pins

Pins 5 and 6 are used for power shutdown when the LTC6087 is in the DD package. If they are floating, internal current sources pull Pins 5 and 6 to V^+ and the amplifiers operate normally. In shutdown the amplifier output is high impedance and each amplifier draws less than 5µA current. This feature allows the part to be used in muxed output applications as shown in Figure 3.

ESD

The LTC6087/LTC6088 has reverse-biased ESD protection diodes on all inputs and outputs as shown in the Simplified Schematic. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to one hundred milliamps or less, no damage to the device will occur.

The amplifier input bias current is the leakage current of these ESD diodes. This leakage is a function of the temperature and common mode voltage of the amplifier, as shown in the Typical Performance Characteristics.

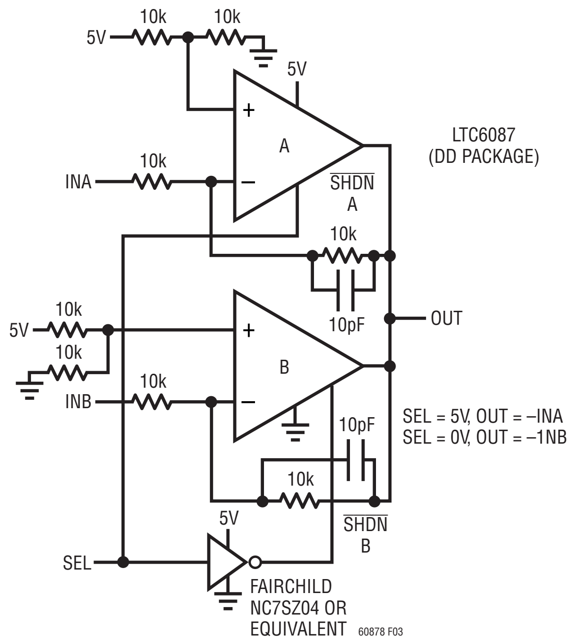


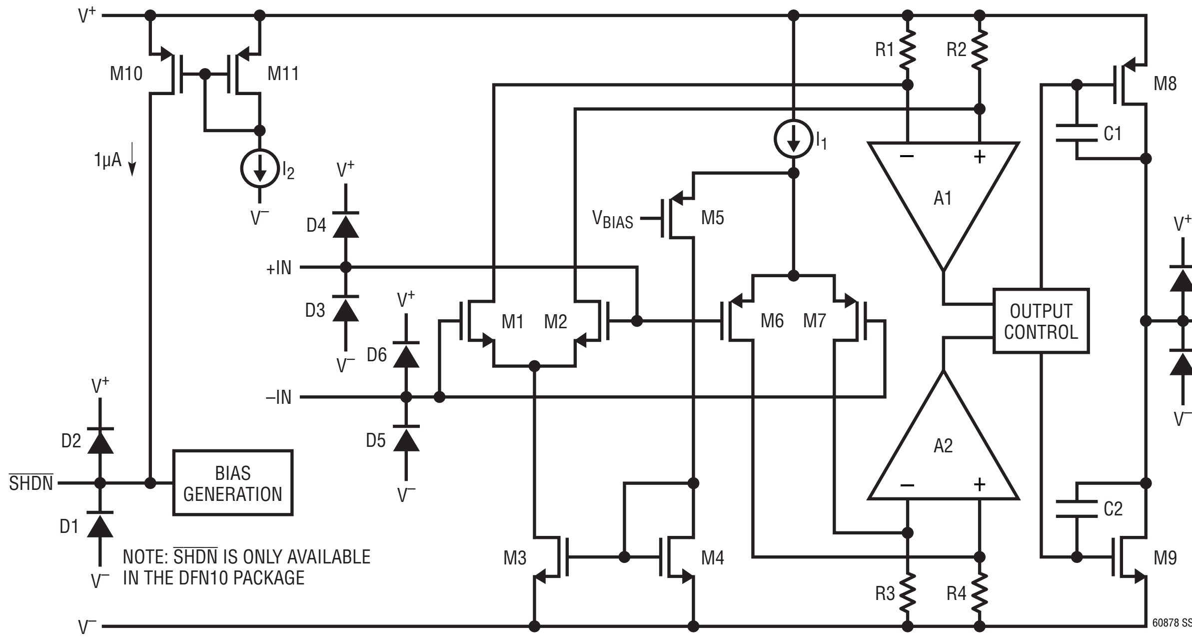
Figure 3. Inverting Amplifier with Muxed Output

Noise

In the frequency region above 1kHz, the LTC6087/LTC6088 shows good noise voltage performance. In this region, noise can be dominated by the total source resistance of the particular application. Specifically, these amplifiers exhibit the noise of a 10k resistor, meaning it is desirable to keep the source and feedback resistance at or below this value, i.e., $R_S + R_G||R_{FB} \le 10k$. Above this total source impedance, the noise voltage is dominated by the resistor.

At low frequency, noise current can be estimated from the expression in = $\sqrt{2qI_B}$, where q = 1.6 • 10^{-19} coulombs. Equating $\sqrt{4kTR\Delta f}$ and $R\sqrt{2qI_B\Delta f}$ shows that for source resistor below 50GΩ the amplifier noise is dominated by the source resistance. Noise current rises with frequency. See the curve Noise Current vs Frequency in the Typical Performance Characteristics section.

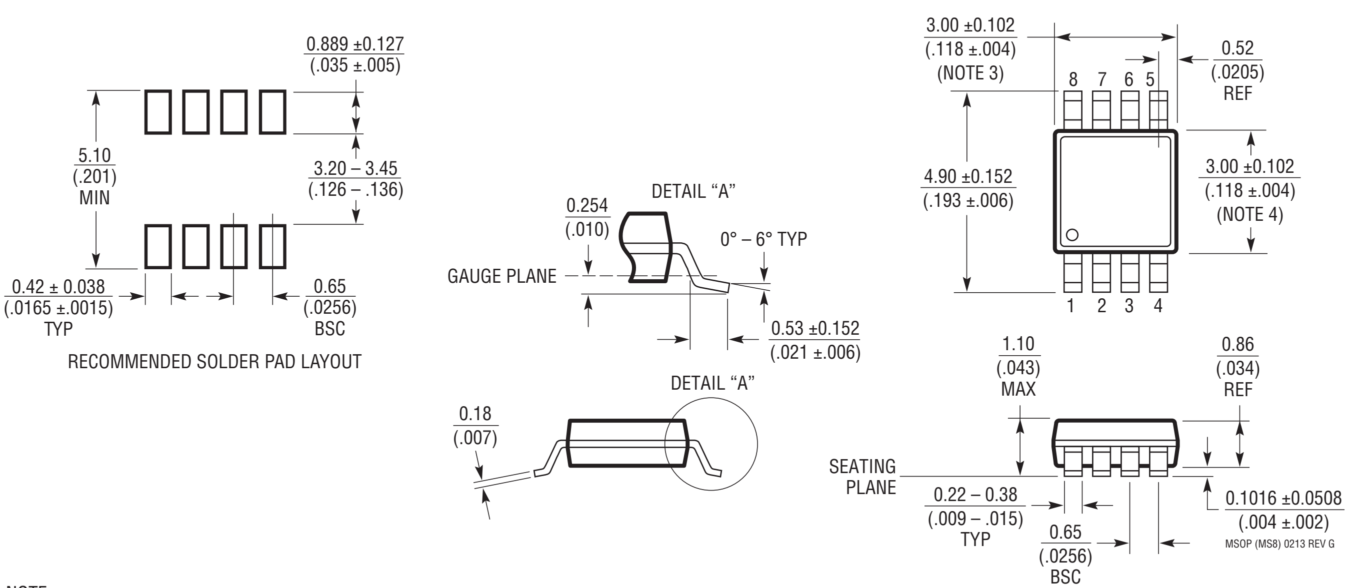
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6087#packaging for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

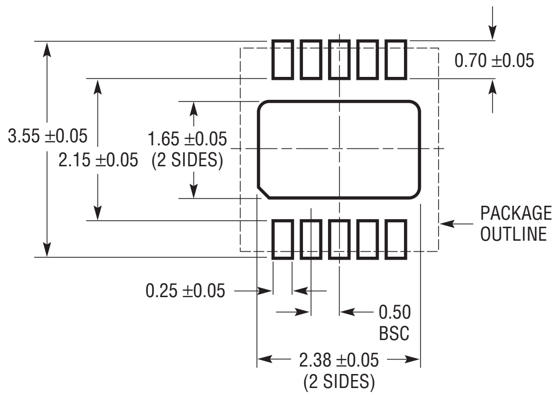


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

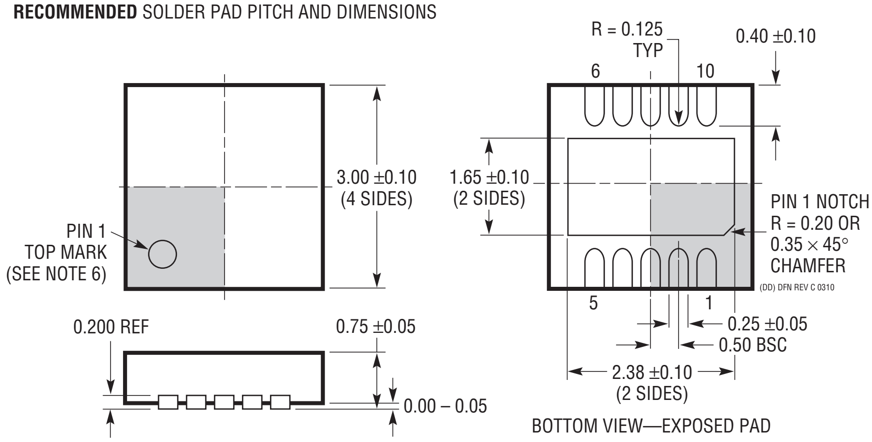
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6087#packaging for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

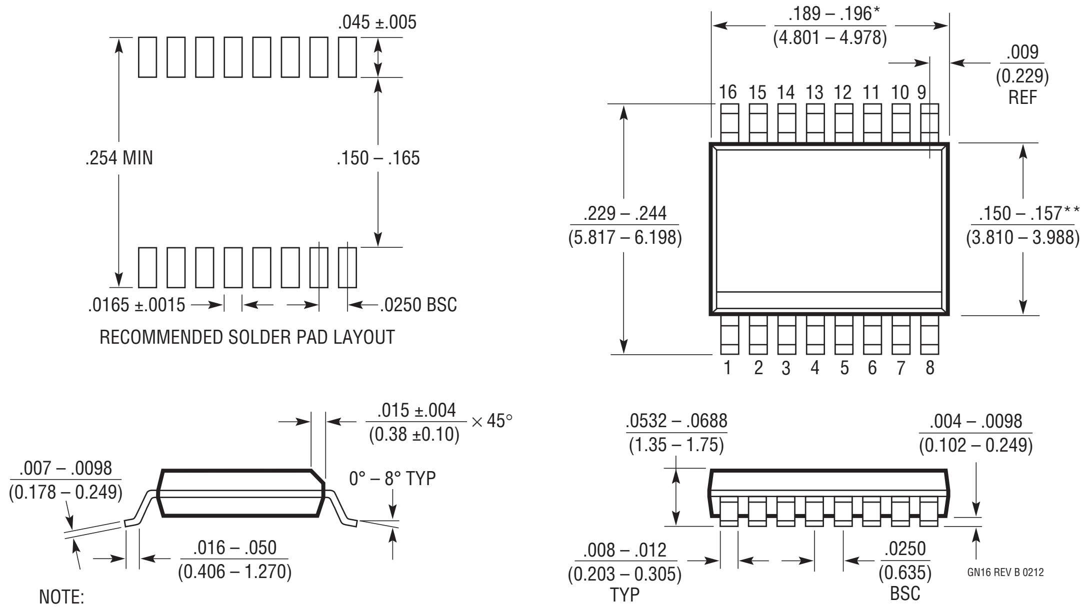


NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6087#packaging for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

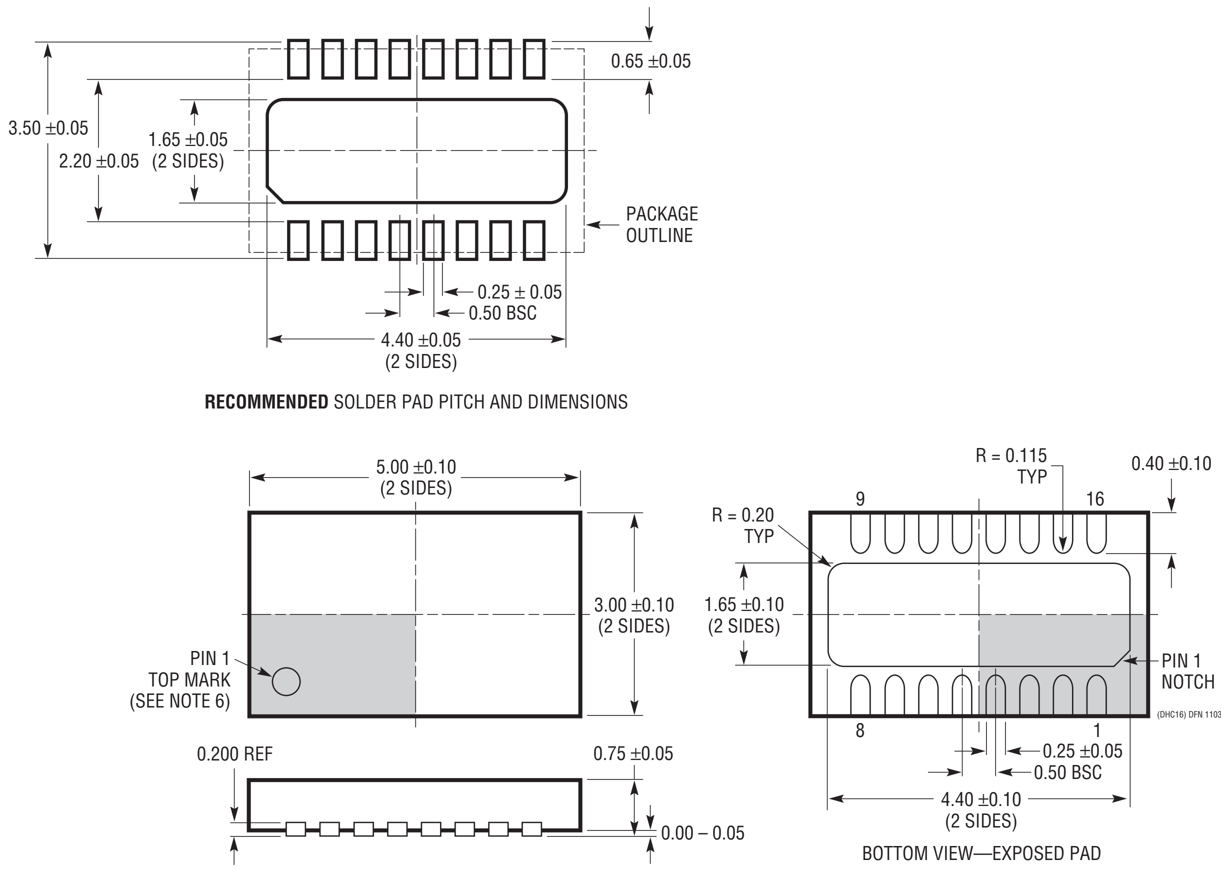
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6087#packaging for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706 Rev Ø)



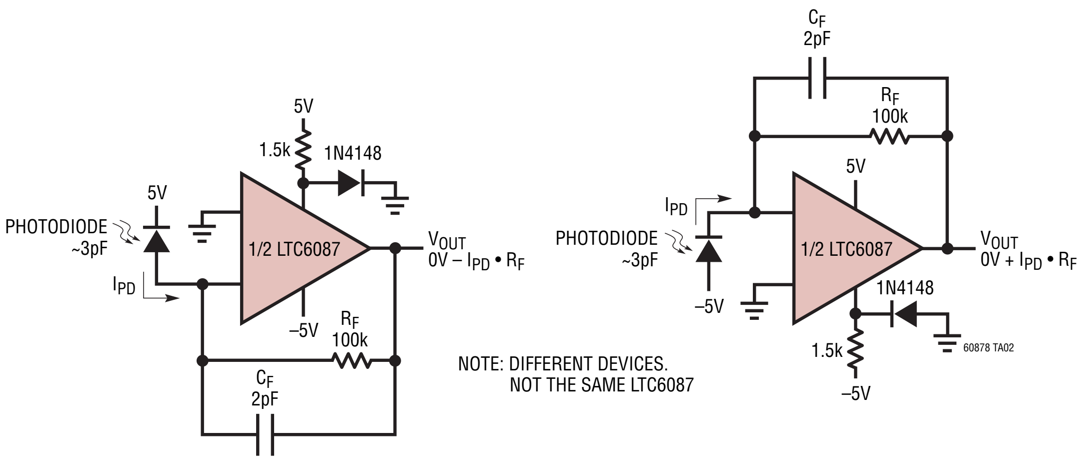
NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

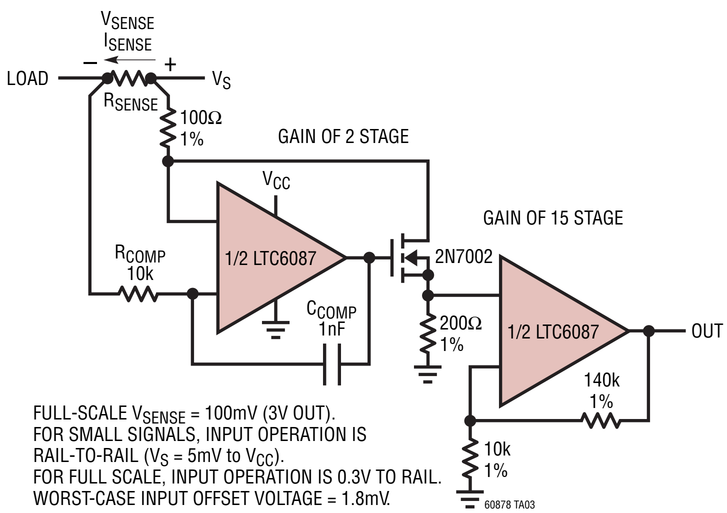
REV	DATE	DESCRIPTION	PAGE NUMBER
C	7/12	Corrected Supply Current value.	1
		Provided V_{CM} condition for GBW specification.	4, 5
D	6/17	Provided V_{CM} condition for Phase Margin specification.	4, 5

TYPICAL APPLICATIONS

Negative-Going and Positive-Going Photodiode TIAs on ±5V Supplies



Almost Rail-to-Rail (0.3V to V_{CC}) Gain-of-30 Current Sense Amplifier



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2051/LTC2052	Dual/Quad Zero-Drift Op Amps	3μV $V_{OS(MAX)}$, 30nV/°C V_{OS} Drift (MAX)
LTC6078/LTC6079	Dual/Quad Micropower Precision Rail-to-Rail Op Amps	25μV $V_{OS(MAX)}$, 0.7μV/°C V_{OS} Drift (MAX), 1pA $I_{BIAS(MAX)}$
LTC6240	Single Low Noise Rail-to-Rail Output Op Amp	7nV/$\sqrt{Hz}$ Noise, 1pA $I_{BIAS(MAX)}$, 10V/μs Slew Rate
LTC6241/LTC6242	Dual/Quad Low Noise Rail-to-Rail Output Op Amps	7nV/$\sqrt{Hz}$ Noise, 0.2pA I_{BIAS}, 18MHz Gain Bandwidth
LTC6244	Dual 50MHz Rail-to-Rail Op Amps	100μV $V_{OS(MAX)}$, 1pA I_{BIAS}, 40V/μs Slew Rate

LT 0617 REV D • PRINTED IN USA
www.linear.com/LTC6087