WINSOURCE
ELECTRONICS

THE DATASHEET OF

LM26LVCISD-XPE/NOPB

LM26LV and LM26LV-Q1 1.6-V, WSON-6 Factory Preset Temperature Switch and Temperature Sensor

1 Features

- Low 1.6-V Operation
- Low Quiescent Current
- Latching Function: Device Can Latch the Over Temperature Condition
- Push-Pull and Open-Drain Temperature Switch Outputs
- Wide Trip Point Range of 0°C to 150°C
- Very Linear Analog V_{TEMP} Temperature Sensor Output
- V_{TEMP} Output Short-Circuit Protected
- Accurate Over –50°C to 150°C Temperature Range
- Excellent Power Supply Noise Rejection
- LM26LVQISD-130 and LM26LVQISD-135 are AEC-Q100 Qualified and are Manufactured on an Automotive Grade Flow:
  - Device Temperature Grade 0: –40°C to 150°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3 A
  - Device CDM ESD Classification Level C6
  - Device MM ESD Classification Level M3

2 Applications

- Cell Phones and Wireless Transceivers
- Digital Cameras
- Battery Management Systems
- Automotive Applications
- Disk Drives
- Games and Appliances

3 Description

The LM26LV and LM26LV-Q1 are low-voltage, precision, dual-output, low-power temperature switches and temperature sensors. The temperature trip point (T_{TRIP}) can be preset at the factory to any temperature in the range of 0°C to 150°C in 1°C increments. Built-in temperature hysteresis (T_{HYST}) keeps the output stable in an environment of temperature instability.

In normal operation the LM26LV or LM26LV-Q1 temperature switch outputs assert when the die temperature exceeds T_{TRIP}. The temperature switch outputs will reset when the temperature falls below a temperature equal to (T_{TRIP} – T_{HYST}). The OVERTEMP digital output, is active-high with a push-pull structure, while the $\overline{\text{OVERTEMP}}$ digital output, is active-low with an open-drain structure.

The analog output, V_{TEMP}, delivers an analog output voltage with Negative Temperature Coefficient (NTC).

Driving the TRIP_TEST input high causes the digital outputs to be asserted for in-situ verification and causes the threshold voltage to appear at the VTEMP output pin, which could be used to verify the temperature trip point.

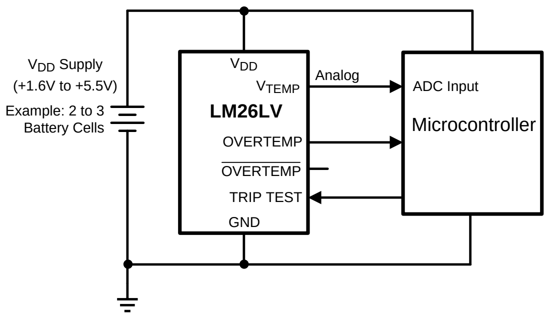
The LM26LV's and LM26LV-Q1's low minimum supply voltage makes them ideal for 1.8-V system designs. The wide operating range, low supply current, and excellent accuracy provide a temperature switch solution for a wide range of commercial and industrial applications.

Device Information(1)

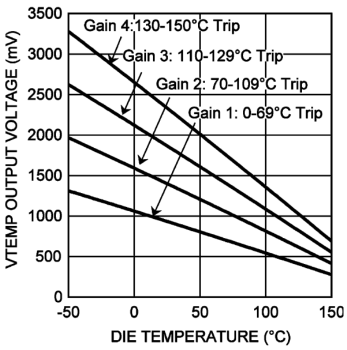
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM26LV, LM26LV-Q1	WSON (6)	2.20 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Redundant Protection and Monitoring



Typical Transfer Characteristic



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4 Revision History

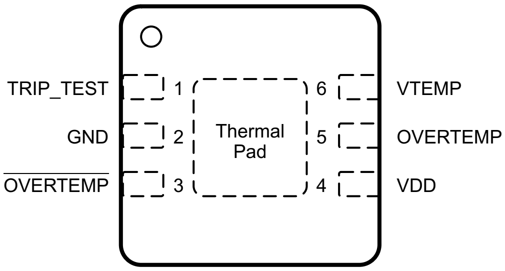
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (February 2013) to Revision G	Page
• Added *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Thermal Information* table, *Switching Characteristics* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated values in the *Thermal Information* table to align with JEDEC standards	5

Changes from Revision E (February 2013) to Revision F	Page
• Changed layout of National Semiconductor Data Sheet to TI format	1

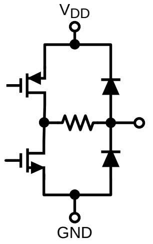
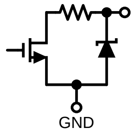
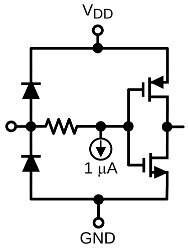
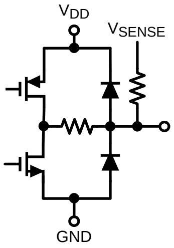
5 Pin Configuration and Functions

NGF Package
6-Pin WSON
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
GND	2	GND	Power supply ground	—
OVERTEMP	5	O	Overtemperature switch output. Active high, push-pull. Asserted when the measured temperature exceeds the trip point temperature or if TRIP_TEST = 1. This pin may be left open if not used.	
$\overline{\text{OVERTEMP}}$	3	O	Overtemperature switch output. Active low, open-drain (See *Determining the Pullup Resistor Value*). Asserted when the measured temperature exceeds the trip point temperature or if TRIP_TEST = 1. This pin may be left open if not used.	
TRIP_TEST	1	I	TRIP_TEST pin. Active high input. If TRIP_TEST = 0 (Default) then: $V_{TEMP} = V_{TS}$, temperature sensor output voltage. If TRIP_TEST = 1 then: OVERTEMP and $\overline{\text{OVERTEMP}}$ outputs are asserted and $V_{TEMP} = V_{TRIP}$, temperature trip voltage. This pin may be left open if not used.	
VDD	4	PWR	Positive supply voltage	—
VTEMP	6	O	V_{TEMP} analog voltage output. If TRIP_TEST = 0 then: $V_{TEMP} = V_{TS}$, temperature sensor output voltage. If TRIP_TEST = 1 then: $V_{TEMP} = V_{TRIP}$, temperature trip voltage. This pin may be left open if not used.	

Pin Functions (continued)

PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
Thermal Pad	—	—	The best thermal conductivity between the device and the PCB is achieved by soldering the DAP of the package to the thermal pad on the PCB. The thermal pad can be a floating node. However, for improved noise immunity the thermal pad must be connected to the circuit GND node, preferably directly to pin 2 (GND) of the device.	—

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply voltage	–0.3	6	V
Voltage at $\overline{\text{OVERTEMP}}$ pin	–0.3	6	V
Voltage at $\overline{\text{OVERTEMP}}$ and VTEMP pins	–0.3	V_{DD} + 0.5	V
TRIP_TEST input voltage	–0.3	V_{DD} + 0.5	V
Output current, any output pin	–7	7	mA
Input current at any pin(3)		5	mA
Maximum junction temperature, $T_{J(MAX)}$		155	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) For soldering specifications, see *Absolute Maximum Ratings for Soldering*.

(3) When the input voltage (V_I) at any pin exceeds power supplies (V_I < GND or V_I > V_{DD}), the current at that pin must be limited to 5 mA.

6.2 ESD Ratings: LM26LV

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)(3)	±300	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

(3) The machine model (MM) is a 200-pF capacitor charged to the specified voltage then discharged directly into each pin.

6.3 ESD Ratings: LM26LV-Q1

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		Machine model (MM)	±300	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.6		5.5	V
	Supply current		8		µA
T_A	Specified ambient temperature	–50		150	°C

6.5 Thermal Information

THERMAL METRIC[1]		LM26LV and LM26LV-Q1 NGF (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	121.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

Typical values apply for $T_A = T_J = 25°C$; minimum and maximum limits apply for $T_A = T_J = –50°C$ to 150°C, $V_{DD} = 1.6$ V to 5.5 V (unless otherwise noted).[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL SPECIFICATIONS						
I_S	Quiescent power supply current			8	16	µA
	Hysteresis		4.5	5	5.5	°C
OVERTEMP DIGITAL OUTPUT—ACTIVE HIGH, PUSH-PULL						
V_{OH}	Logic *High* output voltage	V_{DD} ≥ 1.6 V, Source ≤ 340 µA	V_{DD} – 0.2			V
		V_{DD} ≥ 2 V, Source ≤ 498 µA	V_{DD} – 0.2			
		V_{DD} ≥ 3.3 V, Source ≤ 780 µA	V_{DD} – 0.2			
		V_{DD} ≥ 1.6 V, Source ≤ 600 µA	V_{DD} – 0.45			
		V_{DD} ≥ 2 V, Source ≤ 980 µA	V_{DD} – 0.45			
		V_{DD} ≥ 3.3 V, Source ≤ 1.6 mA	V_{DD} – 0.45			
BOTH OVERTEMP AND $\overline{\text{OVERTEMP}}$ DIGITAL OUTPUTS						
V_{OL}	Logic *Low* output voltage	V_{DD} ≥ 1.6 V, Source ≤ 385 µA			0.2	V
		V_{DD} ≥ 2 V, Source ≤ 500 µA			0.2	
		V_{DD} ≥ 3.3 V, Source ≤ 730 µA			0.2	
		V_{DD} ≥ 1.6 V, Source ≤ 690 µA			0.45	
		V_{DD} ≥ 2 V, Source ≤ 1.05 mA			0.45	
		V_{DD} ≥ 3.3 V, Source ≤ 1.62 mA			0.45	
$\overline{\text{OVERTEMP}}$ DIGITAL OUTPUT—ACTIVE LOW, OPEN DRAIN						
I_{OH}	Logic *High* output leakage current[3]	T_A = 30°C		0.001	1	µA
		T_A = 150°C		0.025	1	

(1) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(2) Typical values apply for $T_J = T_A = 25°C$ and represent most likely parametric norm.
(3) The 1-µA limit is based on a testing limitation and does not reflect the actual performance of the part. Expect to see a doubling of the current for every 15°C increase in temperature. For example, the 1-nA typical current at 25°C would increase to 16 nA at 85°C.

Electrical Characteristics (continued)

Typical values apply for $T_A = T_J = 25°C$; minimum and maximum limits apply for $T_A = T_J = –50°C$ to 150°C, $V_{DD} = 1.6$ V to 5.5 V (unless otherwise noted).(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{TEMP} ANALOG TEMPERATURE SENSOR OUTPUT							
	VTEMP sensor gain	Gain 1 (trip point = 0°C to 69°C)			–5.1		mV/°C
		Gain 2 (trip point = 70°C to 109°C)			–7.7		
		Gain 3 (trip point = 110°C to 129°C)			–10.3		
		Gain 4 (trip point = 130°C to 150°C)			–12.8		
	VTEMP load regulation(4)	1.6 V ≤ V_{DD} < 1.8 V	Source ≤ 90 µA, $V_{DD} – V_{TEMP}$ ≥ 200 mV	–1	–0.1		mV
			Sink ≤ 100 µA, V_{TEMP} ≥ 260 mV		0.1	1	
		V_{DD} ≥ 1.8 V	Source ≤ 120 µA, $V_{DD} – V_{TEMP}$ ≥ 200 mV	–1	–0.1		
			Sink ≤ 200 µA, V_{TEMP} ≥ 260 mV		0.1	1	
		Source or sink = 100 µA			1		Ω
	Supply to VTEMP DC line regulation(5)	V_{DD} = 1.6 V to 5.5 V			0.29		mV
					74		µV/V
					–82		dB
C_L	VTEMP output load capacitance	Without series resistor. See *Capacitive Loads*.			1100		pF
TRIP_TEST DIGITAL INPUT							
V_{IH}	Logic *High* threshold voltage			V_{DD} – 0.5			V
V_{IL}	Logic *Low* threshold voltage					0.5	
I_{IH}	Logic *High* input current				1.5	2.5	µA
I_{IL}	Logic *Low* input current(3)				0.001	1	µA

(4) Source currents are flowing out of the LM26LV or LM26LV-Q1. Sink currents are flowing into the LM26LV or LM26LV-Q1.

(5) Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in *Voltage Shift*.

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{EN}	Time from power ON to digital output enabled(1)			1.1	2.3	ms
t_{VTEMP}	Time from power ON to analog temperature valid(1)	C_L = 0 pF to 1100 pF		1	2.9	ms

(1) Figure 1 and Figure 2 show the definitions of t_{EN} and t_{VTEMP}.

6.8 Accuracy Characteristics

See [1]

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
TRIP POINT ACCURACY					
Trip point accuracy[2]	T_A = 0°C to 150°C, V_{DD} = 5 V		–2.2	2.2	°C
V_{TEMP} ANALOG TEMPERATURE SENSOR OUTPUT ACCURACY[3]					
V_{TEMP} temperature accuracy[2]	Gain 1 trip point = 0°C to 69°C	T_A = 20°C to 40°C, V_{DD} = 1.6 V to 5.5 V	–1.8	1.8	°C
		T_A = 0°C to 70°C, V_{DD} = 1.6 V to 5.5 V	–2	2	
		T_A = 0°C to 90°C, V_{DD} = 1.6 V to 5.5 V	–2.1	2.1	
		T_A = 0°C to 120°C, V_{DD} = 1.6 V to 5.5 V	–2.2	2.2	
		T_A = 0°C to 150°C, V_{DD} = 1.6 V to 5.5 V	–2.3	2.3	
		T_A = –50°C to 0°C, V_{DD} = 1.7 V to 5.5 V	–1.7	1.7	
	Gain 2 trip point = 70°C to 109°C	T_A = 20°C to 40°C, V_{DD} = 1.8 V to 5.5 V	–1.8	1.8	
		T_A = 0°C to 70°C, V_{DD} = 1.9 V to 5.5 V	–2	2	
		T_A = 0°C to 90°C, V_{DD} = 1.9 V to 5.5 V	–2.1	2.1	
		T_A = 0°C to 120°C, V_{DD} = 1.9 V to 5.5 V	–2.2	2.2	
		T_A = 0°C to 150°C, V_{DD} = 1.9 V to 5.5 V	–2.3	2.3	
		T_A = –50°C to 0°C, V_{DD} = 2.3 V to 5.5 V	–1.7	1.7	
	Gain 3 trip point = 110°C to 129°C	T_A = 20°C to 40°C, V_{DD} = 2.3 V to 5.5 V	–1.8	1.8	
		T_A = 0°C to 70°C, V_{DD} = 2.5 V to 5.5 V	–2	2	
		T_A = 0°C to 90°C, V_{DD} = 2.5 V to 5.5 V	–2.1	2.1	
		T_A = 0°C to 120°C, V_{DD} = 2.5 V to 5.5 V	–2.2	2.2	
		T_A = 0°C to 150°C, V_{DD} = 2.5 V to 5.5 V	–2.3	2.3	
		T_A = –50°C to 0°C, V_{DD} = 3 V to 5.5 V	–1.7	1.7	
	Gain 4 trip point = 130°C to 150°C	T_A = 20°C to 40°C, V_{DD} = 2.7 V to 5.5 V	–1.8	1.8	
		T_A = 0°C to 70°C, V_{DD} = 3 V to 5.5 V	–2	2	
		T_A = 0°C to 90°C, V_{DD} = 3 V to 5.5 V	–2.1	2.1	
		T_A = 0°C to 120°C, V_{DD} = 3 V to 5.5 V	–2.2	2.2	
		T_A = 0°C to 150°C, V_{DD} = 3 V to 5.5 V	–2.3	2.3	
		T_A = –50°C to 0°C, V_{DD} = 3.6 V to 5.5 V	–1.7	1.7	

(1) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(2) Accuracy is defined as the error between the measured and reference output voltages, tabulated in Table 1 at the specified conditions of supply gain setting, voltage, and temperature (°C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.
(3) Changes in output due to self heating can be computed by multiplying the internal dissipation by the temperature thermal resistance.

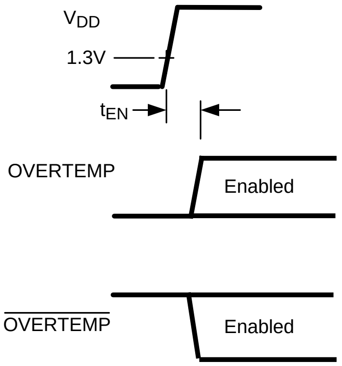


Figure 1. Definition of t_{EN}

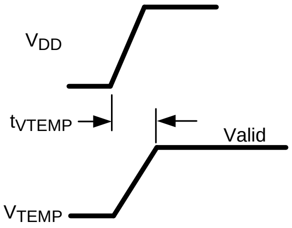


Figure 2. Definition of t_{VTEMP}

6.9 Typical Characteristics

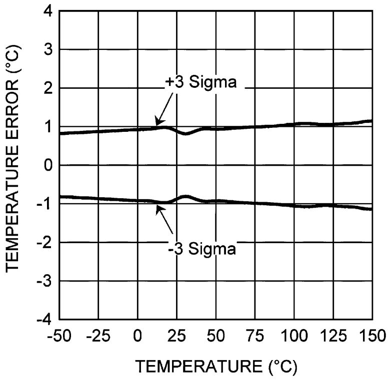


Figure 3. VTEMP Output Temperature Error vs Temperature

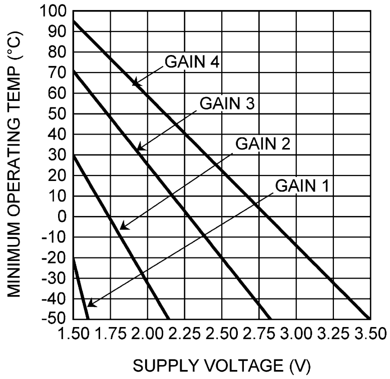


Figure 4. Minimum Operating Temperature vs Supply Voltage

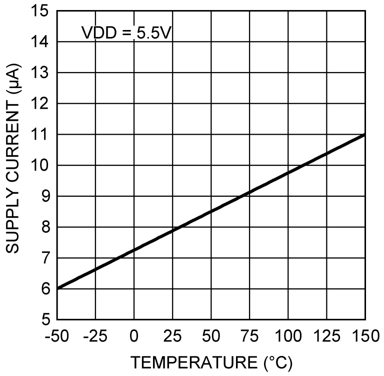


Figure 5. Supply Current vs Temperature

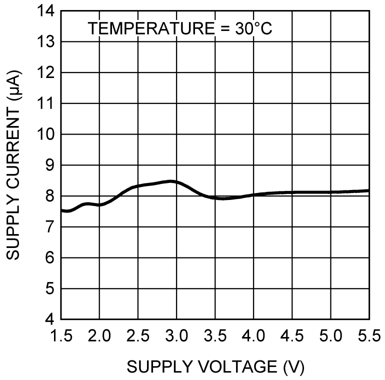
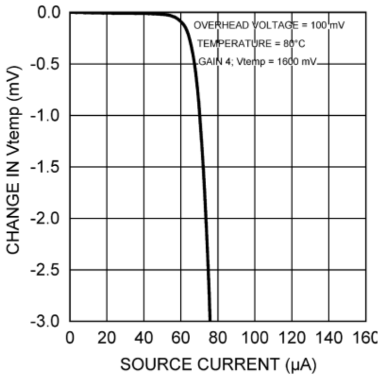
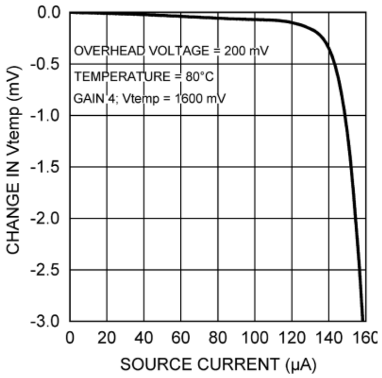


Figure 6. Supply Current vs Supply Voltage



100-mV overhead T_A = 80°C Sourcing current

Figure 7. Load Regulation [1]



200-mV overhead T_A = 80°C Sourcing Current

Figure 8. Load Regulation[1]

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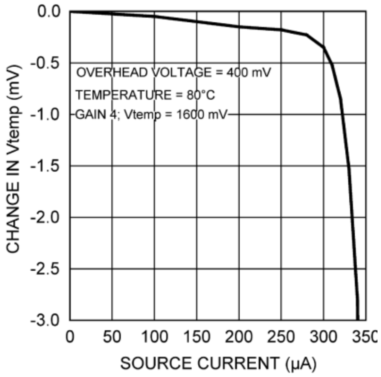
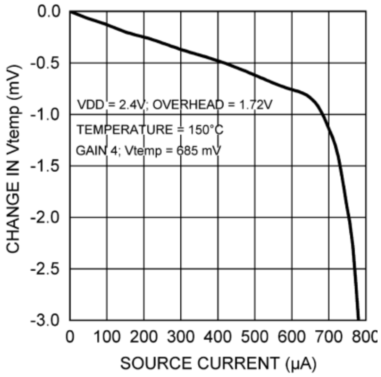
(1) The curves shown represent typical performance under worst-case conditions. Performance improves with larger V_{TEMP}, larger V_{DD}, and lower temperatures.

Typical Characteristics (continued)



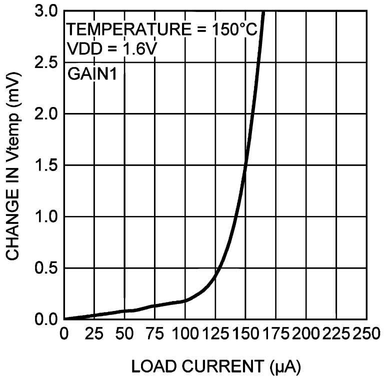
400-mV overhead T_A = 80°C Sourcing current

Figure 9. Load Regulation(1)



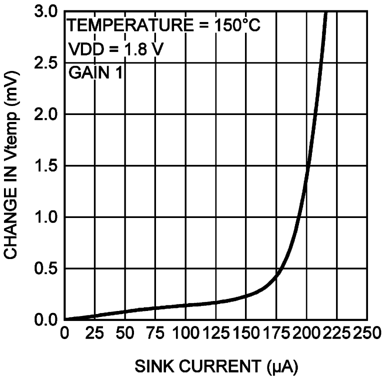
1.72-V overhead T_A = 150°C V_{DD} = 2.4 V Sourcing current

Figure 10. Load Regulation(1)



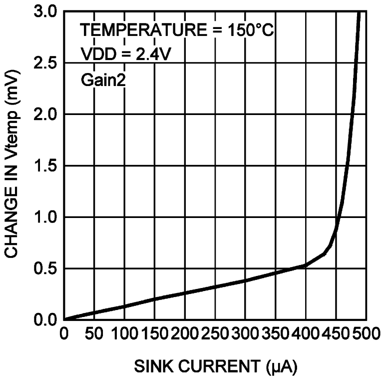
V_{DD} = 1.6 V Sinking Current

Figure 11. Load Regulation(1)



V_{DD} = 1.8 V Sinking Current

Figure 12. Load Regulation(1)



V_{DD} = 2.4 V Sinking Current

Figure 13. Load Regulation(1)

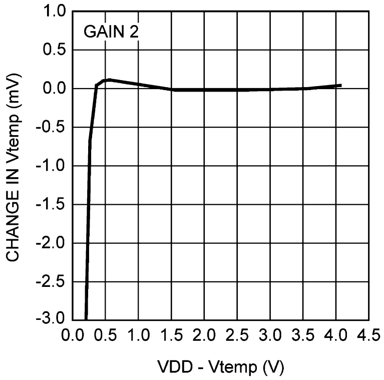


Figure 14. Change in V_{TEMP} vs Overhead Voltage

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(1) The curves shown represent typical performance under worst-case conditions. Performance improves with larger V_{TEMP}, larger V_{DD}, and lower temperatures.

Typical Characteristics (continued)

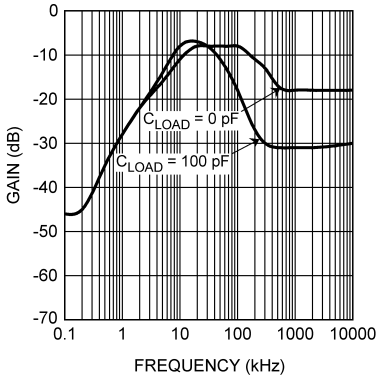
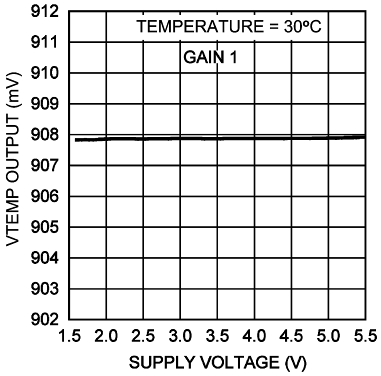
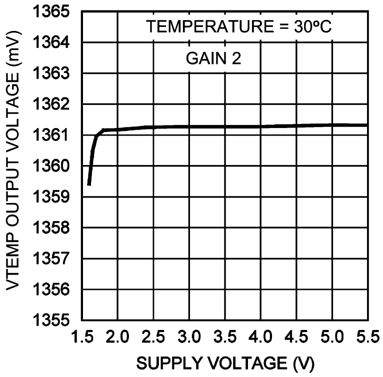


Figure 15. V_{TEMP} Supply-Noise Rejection vs Frequency



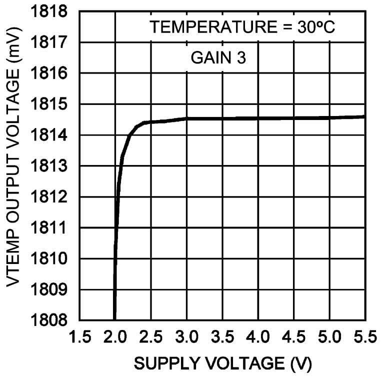
Gain 1 (Trip Points = 0°C tp 69°C)

Figure 16. Line Regulation V_{TEMP} vs Supply Voltage



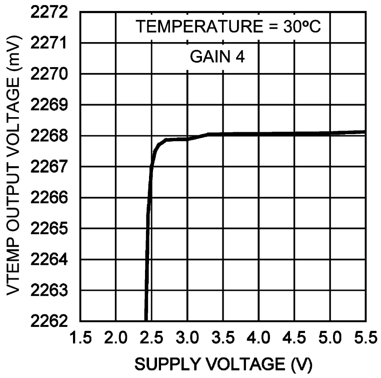
Gain 2 (Trip Points = 70°C to 109°C)

Figure 17. Line Regulation V_{TEMP} vs Supply Voltage



Gain 3 (Trip Points = 110°C to 129°C)

Figure 18. Line Regulation V_{TEMP} vs Supply Voltage



Gain 4 (Trip Points = 130°C to 150°C)

Figure 19. Line Regulation V_{TEMP} vs Supply Voltage

7 Detailed Description

7.1 Overview

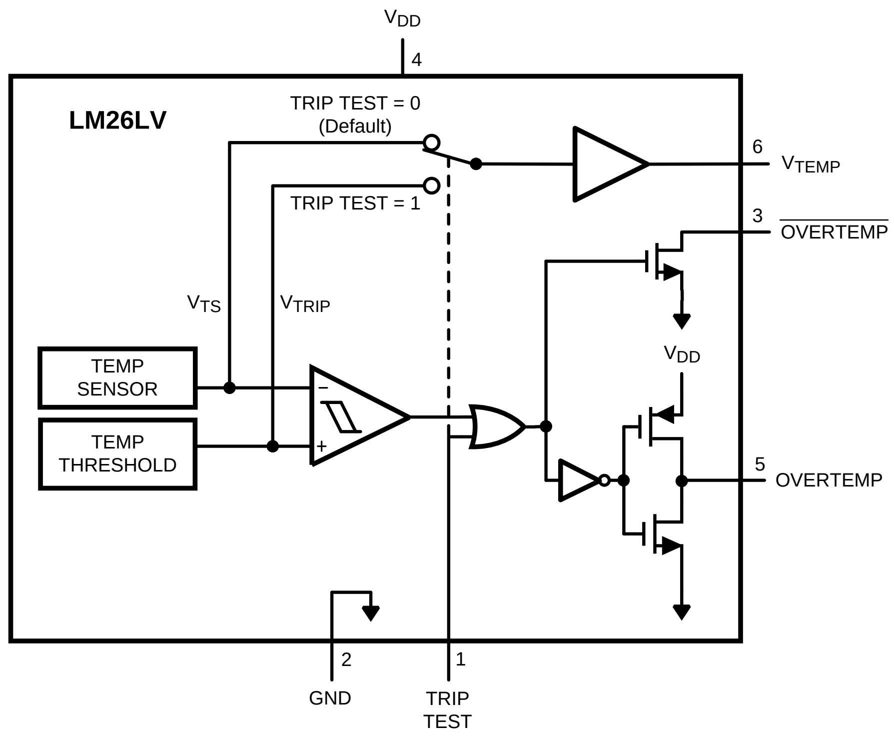
The LM26LV and LM26LV-Q1 are precision, dual-output, temperature switches with analog temperature sensor output. The trip temperature (T_{TRIP}) is factory selected by the order number. The V_{TEMP} class AB analog output provides a voltage that is proportional to temperature. The LM26LV and LM26LV-Q1 include an internal reference DAC (TEMP THRESHOLD), analog temperature sensor and analog comparator. The reference DAC is connected to one of the comparator inputs. The reference DAC output voltage (V_{TRIP}) is preprogrammed by TI. The result of the reference DAC voltage and the temperature sensor output comparison is provided on two output pins $\overline{\text{OVERTEMP}}$ and OVERTEMP.

The V_{TEMP} output has a programmable gain. The output gain has 4 possible settings as described in Table 1. The gain setting is dependent on the temperature trip point selected.

Built-in temperature hysteresis (T_{HYST}) prevents the digital outputs from oscillating. The OVERTEMP and $\overline{\text{OVERTEMP}}$ activates when the die temperature exceeds T_{TRIP} and releases when the temperature falls below a temperature equal to T_{TRIP} minus T_{HYST}. OVERTEMP is active-high with a push-pull structure. $\overline{\text{OVERTEMP}}$, is active-low with an open-drain structure. The comparator hysteresis is fixed at 5°C.

Driving the TRIP-TEST high activates the digital outputs. A processor can check the logic level of the OVERTEMP or $\overline{\text{OVERTEMP}}$, confirming that they changed to their active state. This allows for system production testing verification that the comparator and output circuitry are functional after system assembly. When the TRIP-TEST pin is high, the trip-level reference voltage appears at the V_{TEMP} pin. Tying OVERTEMP to TRIP-TEST latches the output after it trips. It can be cleared by forcing TRIP-TEST low or powering off the LM26LV or LM26LV-Q1.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 LM26LV and LM26LV-Q1 V_{TEMP} vs Die Temperature Conversion Table

The LM26LV and LM26LV-Q1 have one out of four possible factory-set gains, Gain 1 through Gain 4, depending on the range of the Temperature Trip Point. The V_{TEMP} temperature sensor voltage, in millivolts, at each discrete die temperature over the complete operating temperature range, and for each of the four Temperature Trip Point ranges, is shown in Table 1. This table is the reference from which the LM26LV and LM26LV-Q1 accuracy specifications (listed in *Accuracy Characteristics*) are determined. This table can be used, for example, in a host processor look-up table. See *The Second-Order Equation (Parabolic)* for the parabolic equation used in the Conversion Table.

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table

DIE TEMPERATURE (°C)	ANALOG OUTPUT VOLTAGE, V_{TEMP} (mV)(1)			
	GAIN 1	GAIN 2	GAIN 3	GAIN 4
–50	1312	1967	2623	3278
–49	1307	1960	2613	3266
–48	1302	1952	2603	3253
–47	1297	1945	2593	3241
–46	1292	1937	2583	3229
–45	1287	1930	2573	3216
–44	1282	1922	2563	3204
–43	1277	1915	2553	3191
–42	1272	1908	2543	3179
–41	1267	1900	2533	3166
–40	1262	1893	2523	3154
–39	1257	1885	2513	3141
–38	1252	1878	2503	3129
–37	1247	1870	2493	3116
–36	1242	1863	2483	3104
–35	1237	1855	2473	3091
–34	1232	1848	2463	3079
–33	1227	1840	2453	3066
–32	1222	1833	2443	3054
–31	1217	1825	2433	3041
–30	1212	1818	2423	3029
–29	1207	1810	2413	3016
–28	1202	1803	2403	3004
–27	1197	1795	2393	2991
–26	1192	1788	2383	2979
–25	1187	1780	2373	2966
–24	1182	1773	2363	2954
–23	1177	1765	2353	2941
–22	1172	1757	2343	2929
–21	1167	1750	2333	2916
–20	1162	1742	2323	2903
–19	1157	1735	2313	2891
–18	1152	1727	2303	2878
–17	1147	1720	2293	2866
–16	1142	1712	2283	2853
–15	1137	1705	2272	2841
–14	1132	1697	2262	2828
–13	1127	1690	2252	2815
–12	1122	1682	2242	2803

(1) V_{DD} = 5 V. Values are **bold** for each gain's respective trip point range.

Feature Description (continued)

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table (continued)

DIE TEMPERATURE (°C)	ANALOG OUTPUT VOLTAGE, V_{TEMP} (mV)[1]			
	GAIN 1	GAIN 2	GAIN 3	GAIN 4
–11	1116	1674	2232	2790
–10	1111	1667	2222	2777
–9	1106	1659	2212	2765
–8	1101	1652	2202	2752
–7	1096	1644	2192	2740
–6	1091	1637	2182	2727
–5	1086	1629	2171	2714
–4	1081	1621	2161	2702
–3	1076	1614	2151	2689
–2	1071	1606	2141	2676
–1	1066	1599	2131	2664
0	**1061**	1591	2121	2651
1	**1056**	1583	2111	2638
2	**1051**	1576	2101	2626
3	**1046**	1568	2090	2613
4	**1041**	1561	2080	2600
5	**1035**	1553	2070	2587
6	**1030**	1545	2060	2575
7	**1025**	1538	2050	2562
8	**1020**	1530	2040	2549
9	**1015**	1522	2029	2537
10	**1010**	1515	2019	2524
11	**1005**	1507	2009	2511
12	**1000**	1499	1999	2498
13	**995**	1492	1989	2486
14	**990**	1484	1978	2473
15	**985**	1477	1968	2460
16	**980**	1469	1958	2447
17	**974**	1461	1948	2435
18	**969**	1454	1938	2422
19	**964**	1446	1927	2409
20	**959**	1438	1917	2396
21	**954**	1431	1907	2383
22	**949**	1423	1897	2371
23	**944**	1415	1886	2358
24	**939**	1407	1876	2345
25	**934**	1400	1866	2332
26	**928**	1392	1856	2319
27	**923**	1384	1845	2307
28	**918**	1377	1835	2294
29	**913**	1369	1825	2281
30	**908**	1361	1815	2268
31	**903**	1354	1804	2255
32	**898**	1346	1794	2242
33	**892**	1338	1784	2230
34	**887**	1331	1774	2217
35	**882**	1323	1763	2204
36	**877**	1315	1753	2191
37	**872**	1307	1743	2178

Feature Description (continued)

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table (continued)

DIE TEMPERATURE (°C)	ANALOG OUTPUT VOLTAGE, V_{TEMP} (mV)[1]			
	GAIN 1	GAIN 2	GAIN 3	GAIN 4
38	**867**	1300	1732	2165
39	**862**	1292	1722	2152
40	**856**	1284	1712	2139
41	**851**	1276	1701	2127
42	**846**	1269	1691	2114
43	**841**	1261	1681	2101
44	**836**	1253	1670	2088
45	**831**	1245	1660	2075
46	**825**	1238	1650	2062
47	**820**	1230	1639	2049
48	**815**	1222	1629	2036
49	**810**	1214	1619	2023
50	**805**	1207	1608	2010
51	**800**	1199	1598	1997
52	**794**	1191	1588	1984
53	**789**	1183	1577	1971
54	**784**	1176	1567	1958
55	**779**	1168	1557	1946
56	**774**	1160	1546	1933
57	**769**	1152	1536	1920
58	**763**	1144	1525	1907
59	**758**	1137	1515	1894
60	**753**	1129	1505	1881
61	**748**	1121	1494	1868
62	**743**	1113	1484	1855
63	**737**	1105	1473	1842
64	**732**	1098	1463	1829
65	**727**	1090	1453	1816
66	**722**	1082	1442	1803
67	**717**	1074	1432	1790
68	**711**	1066	1421	1776
69	**706**	1059	1411	1763
70	701	**1051**	1400	1750
71	696	**1043**	1390	1737
72	690	**1035**	1380	1724
73	685	**1027**	1369	1711
74	680	**1019**	1359	1698
75	675	**1012**	1348	1685
76	670	**1004**	1338	1672
77	664	**996**	1327	1659
78	659	**988**	1317	1646
79	654	**980**	1306	1633
80	649	**972**	1296	1620
81	643	**964**	1285	1607
82	638	**957**	1275	1593
83	633	**949**	1264	1580
84	628	**941**	1254	1567
85	622	**933**	1243	1554
86	617	**925**	1233	1541

Feature Description (continued)

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table (continued)

DIE TEMPERATURE (°C)	ANALOG OUTPUT VOLTAGE, V_{TEMP} (mV)[1]			
	GAIN 1	GAIN 2	GAIN 3	GAIN 4
87	612	**917**	1222	1528
88	607	**909**	1212	1515
89	601	**901**	1201	1501
90	596	**894**	1191	1488
91	591	**886**	1180	1475
92	586	**878**	1170	1462
93	580	**870**	1159	1449
94	575	**862**	1149	1436
95	570	**854**	1138	1422
96	564	**846**	1128	1409
97	559	**838**	1117	1396
98	554	**830**	1106	1383
99	549	**822**	1096	1370
100	543	**814**	1085	1357
101	538	**807**	1075	1343
102	533	**799**	1064	1330
103	527	**791**	1054	1317
104	522	**783**	1043	1304
105	517	**775**	1032	1290
106	512	**767**	1022	1277
107	506	**759**	1011	1264
108	501	**751**	1001	1251
109	496	**743**	990	1237
110	490	735	**979**	1224
111	485	727	**969**	1211
112	480	719	**958**	1198
113	474	711	**948**	1184
114	469	703	**937**	1171
115	464	695	**926**	1158
116	459	687	**916**	1145
117	453	679	**905**	1131
118	448	671	**894**	1118
119	443	663	**884**	1105
120	437	655	**873**	1091
121	432	647	**862**	1078
122	427	639	**852**	1065
123	421	631	**841**	1051
124	416	623	**831**	1038
125	411	615	**820**	1025
126	405	607	**809**	1011
127	400	599	**798**	998
128	395	591	**788**	985
129	389	583	**777**	971
130	384	575	766	**958**
131	379	567	756	**945**
132	373	559	745	**931**
133	368	551	734	**918**
134	362	543	724	**904**
135	357	535	713	**891**

Feature Description (continued)

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table (continued)

DIE TEMPERATURE (°C)	ANALOG OUTPUT VOLTAGE, V_{TEMP} (mV)[1]			
	GAIN 1	GAIN 2	GAIN 3	GAIN 4
136	352	527	702	**878**
137	346	519	691	**864**
138	341	511	681	**851**
139	336	503	670	**837**
140	330	495	659	**824**
141	325	487	649	**811**
142	320	479	638	**797**
143	314	471	627	**784**
144	309	463	616	**770**
145	303	455	606	**757**
146	298	447	595	**743**
147	293	438	584	**730**
148	287	430	573	**716**
149	282	422	562	**703**
150	277	414	552	**690**

7.3.2 V_{TEMP} vs Die Temperature Approximations

The LM26LV's and LM26LV-Q1's V_{TEMP} analog temperature output is very linear. Table 1 and the equation in *The Second-Order Equation (Parabolic)* represent the most accurate typical performance of the V_{TEMP} voltage output versus temperature.

7.3.2.1 The Second-Order Equation (Parabolic)

The data from Table 1, or Equation 1, when plotted, has an umbrella-shaped parabolic curve. V_{TEMP} is in mV.

$$\text{GAIN1}: V_{TEMP} = 907.9 - 5.132 \times (T_{DIE} - 30°\text{C}) - 1.08^{-3} \times (T_{DIE} - 30°\text{C})$$
$$\text{GAIN2}: V_{TEMP} = 1361.4 - 7.701 \times (T_{DIE} - 30°\text{C}) - 1.6^{-3} \times (T_{DIE} - 30°\text{C})$$
$$\text{GAIN3}: V_{TEMP} = 1814.6 - 10.27 \times (T_{DIE} - 30°\text{C}) - 2.12^{-3} \times (T_{DIE} - 30°\text{C})$$
$$\text{GAIN4}: V_{TEMP} = 2268.1 - 12.838 \times (T_{DIE} - 30°\text{C}) - 2.64^{-3} \times (T_{DIE} - 30°\text{C}) \quad (1)$$

7.3.2.2 The First-Order Approximation (Linear)

For a quicker approximation, although less accurate than the second-order, over the full operating temperature range the linear formula below can be used. Using Equation 2, with the constant and slope in the following set of equations, the best-fit V_{TEMP} versus die temperature performance can be calculated with an approximation error less than 18 mV. V_{TEMP} is in mV.

$$\text{GAIN1}: V_{TEMP} = 1060 - 5.18 \times T_{DIE}$$
$$\text{GAIN2}: V_{TEMP} = 1590 - 7.77 \times T_{DIE}$$
$$\text{GAIN3}: V_{TEMP} = 2119 - 10.36 \times T_{DIE}$$
$$\text{GAIN4}: V_{TEMP} = 2649 - 12.94 \times T_{DIE} \quad (2)$$

7.3.2.3 *First-Order Approximation (Linear) Over Small Temperature Range*

For a linear approximation, a line can easily be calculated over the desired temperature range from Table 1 using the two-point equation:

$$V - V_1 = \left(\frac{V_2 - V_1}{T_2 - T_1} \right) \times (T - T_1)$$

where

- V is in mV
- T is in °C
- T_1 and V_1 are the coordinates of the lowest temperature
- T_2 and V_2 are the coordinates of the highest temperature (3)

For example, to determine the equation of a line with GAIN4, with a temperature from 20°C to 50°C, proceed using Equation 4, Equation 5, and Equation 6:

$$V - 2396\text{ mV} = \left(\frac{2010\text{ mV} - 2396\text{ mV}}{50°\text{C} - 20°\text{C}} \right) \times (T - 20°\text{C}) \tag{4}$$

$$V - 2396\text{ mV} = -12.8\text{ mV/°C} \times (T - 20°\text{C}) \tag{5}$$

$$V = -12.8\text{ mV/°C} \times (T - 20°\text{C}) + 2396\text{ mV} \tag{6}$$

Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

7.3.3 OVERTEMP and $\overline{\text{OVERTEMP}}$ Digital Outputs

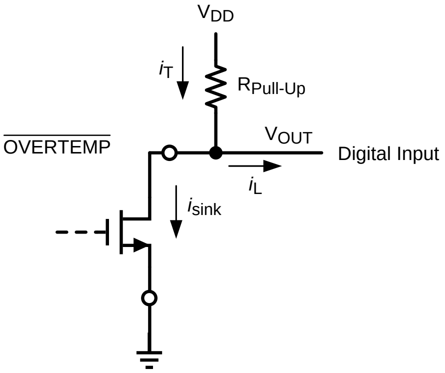
The OVERTEMP active high, push-pull output and the $\overline{\text{OVERTEMP}}$ active low, open-drain output both assert at the same time whenever the die temperature reaches the factory preset temperature trip point. They also assert simultaneously whenever the TRIP_TEST pin is set high. Both outputs deassert when the die temperature goes below the temperature trip point hysteresis. These two types of digital outputs enable the user the flexibility to choose the type of output that is most suitable for his design.

Either the OVERTEMP or the $\overline{\text{OVERTEMP}}$ digital output pins can be left open if not used.

7.3.3.1 *$\overline{\text{OVERTEMP}}$ Open-Drain Digital Output*

The $\overline{\text{OVERTEMP}}$ active low, open-drain digital output, if used, requires a pullup resistor between this pin and V_{DD}. The following section shows how to determine the pullup resistor value.

7.3.3.1.1 Determining the Pullup Resistor Value



The pullup resistor value is calculated at the condition of maximum total current, I_T, through the resistor. The total current is:

$$I_T = I_L + I_{SINK}$$

where

- I_T is the maximum total current through the pullup resistor at V_{OL}.
- I_L is the load current, which is very low for typical digital inputs. (7)

The pullup resistor maximum value can be found by using Equation 8.

$$R_{PULLUP} = \frac{V_{DD(MAX)} - V_{OL}}{I_T}$$

where

- $V_{DD(MAX)}$ is the maximum power supply voltage to be used in the customer's system.
- V_{OUT} is the Voltage at the $\overline{\text{OVERTEMP}}$ pin. Use V_{OL} for calculating the pullup resistor. (8)

7.3.3.1.1.1 Example Calculation

Suppose, for this example, a V_{DD} of 3.3 V ± 0.3 V, a CMOS digital input as a load, a V_{OL} of 0.2 V.

- For V_{OL} of 0.2 V the electrical specification for $\overline{\text{OVERTEMP}}$ shows a maximum I_{SINK} of 385 µA.
- Let I_L = 1 µA, then I_T is about 386 µA maximum. If 35 µA is selected as the current limit then I_T for the calculation becomes 35 µA.
- $V_{DD(MAX)}$ is 3.3 V + 0.3 V = 3.6 V, then calculate the pullup resistor as R_{PULLUP} = (3.6 – 0.2) / 35 µA = 97 kΩ.
- Based on this calculated value, select the closest resistor value in the tolerance family used.

In this example, if 5% resistor values are used, then the next closest value is 100 kΩ.

7.3.4 TRIP_TEST Digital Input

The TRIP_TEST pin simply provides a means to test the OVERTEMP and $\overline{\text{OVERTEMP}}$ digital outputs electronically by causing them to assert, at any operating temperature, as a result of forcing the TRIP_TEST pin high.

When the TRIP_TEST pin is pulled high the V_{TEMP} pin is at the V_{TRIP} voltage.

If not used, the TRIP_TEST pin may either be left open or grounded.

7.3.5 V_{TEMP} Analog Temperature Sensor Output

The V_{TEMP} push-pull output provides the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. See *Application and Implementation* for more discussion of this topic. The LM26LV and LM26LV-Q1 are ideal for applications which require strong source or sink current.

7.3.5.1 Noise Considerations

The LM26LV's and LM26LV-Q1's supply-noise rejection (the ratio of the AC signal on V_{TEMP} to the AC signal on V_{DD}) was measured during bench tests. The device's typical attenuation is shown in *Typical Characteristics*. A load capacitor on the output can help to filter noise.

For operation in very noisy environments, some bypass capacitance must be present on the supply within approximately 2 inches of the LM26LV or LM26LV-Q1.

7.3.5.2 Capacitive Loads

The V_{TEMP} Output handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, the V_{TEMP} can drive a capacitive load less than or equal to 1100 pF as shown in Figure 20. For capacitive loads greater than 1100 pF, a series resistor is required on the output, as shown in Figure 21, to maintain stable conditions.

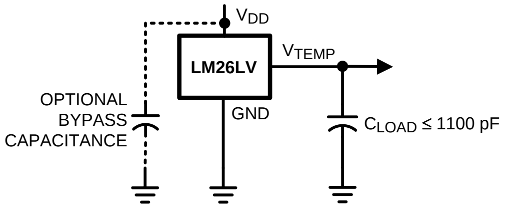


Figure 20. LM26LV or LM26LV-Q1 No Decoupling Required for Capacitive Loads Less Than 1100 pF.

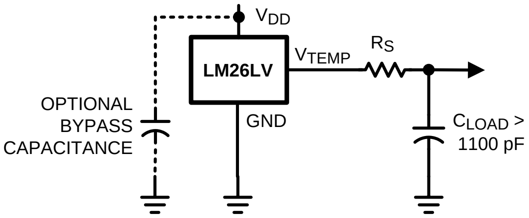


Figure 21. LM26LV or LM26LV-Q1 With Series Resistor for Capacitive Loading Greater Than 1100 pF

Table 2. Minimum Series Resistence for Capacitive Loads

C_{LOAD}	MINIMUM R_S
1.1 nF to 99 nF	3 kΩ
100 nF to 999 nF	1.5 kΩ
1 µF	800 Ω

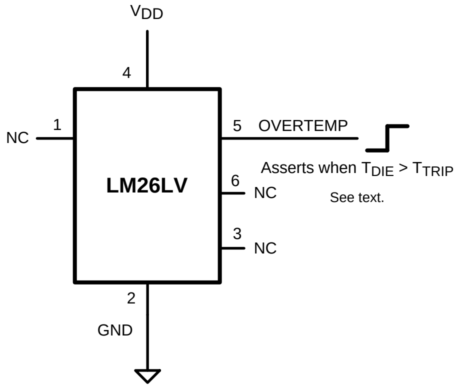
7.3.5.3 Voltage Shift

The LM26LV and LM26LV-Q1 are very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of V_{DD} and V_{TEMP}. The shift typically occurs when $V_{DD} – V_{TEMP} = 1$ V.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in V_{DD} or V_{TEMP}. Because the shift takes place over a wide temperature change of 5°C to 20°C, V_{TEMP} is always monotonic. The accuracy specifications *Accuracy Characteristics* already includes this possible shift.

7.4 Device Functional Modes

The LM26LV and LM26LV-Q1 have several modes of operation as detailed in the following drawings.



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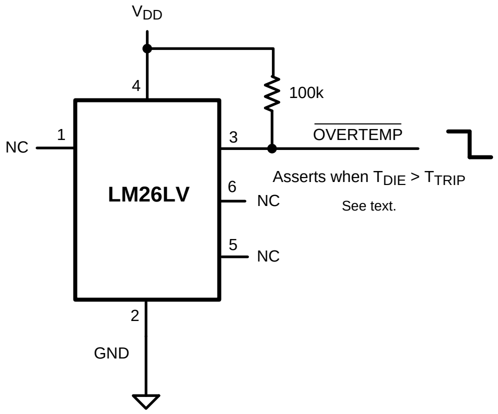

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Figure 22. Temperature Switch Using Push-Pull Output

Figure 23. Temperature Switch Using Open-Drain Output

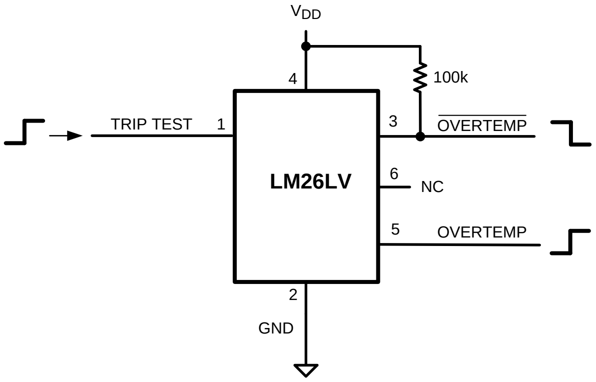

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Figure 24. TRIP_TEST Digital Output Test Circuit

The TRIP_TEST pin, normally used to check the operation of the OVERTEMP and $\overline{\text{OVERTEMP}}$ pins, may be used to latch the outputs whenever the temperature exceeds the programmed limit and causes the digital outputs to assert. As shown in Figure 25, when OVERTEMP goes high the TRIP_TEST input is also pulled high and causes OVERTEMP output to latch high and the $\overline{\text{OVERTEMP}}$ output to latch low. The latch can be released by either momentarily pulling the TRIP_TEST pin low (GND), or by toggling the power supply to the device. The resistor limits the current out of the $\overline{\text{OVERTEMP}}$ output pin.

Device Functional Modes (continued)

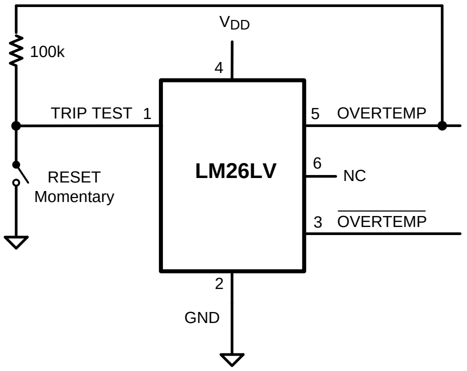

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Figure 25. Latch Circuit Using OVERTEMP Output

Alternately, the circuit in Figure 25 the 100 kΩ can be replaced with a short and the momentary reset switch may be removed. In this configuration, when OVERTEMP goes active high, it drives TRIP_TEST high. THRIP TEST high causes OVERTEMP to stay high. It is therefore latched. To release the latch, power down, then power up the LM26LV or LM26LV-Q1. The LM26LV and LM26LV-Q1 always come up in a released condition.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 ADC Input Considerations

The LM26LV and LM26LV-Q1 have an analog temperature sensor output V_{TEMP} that can be directly connected to an ADC (Analog-to-Digital Converter) input. Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LM26LV or LM26LV-Q1 temperature sensor. This requirement is easily accommodated by the addition of a capacitor (C_{FILTER}). The size of C_{FILTER} depends on the size of the sampling capacitor and the sampling frequency. Because not all ADCs have identical input stages, the charge requirements vary. This general ADC application is shown as an example only.

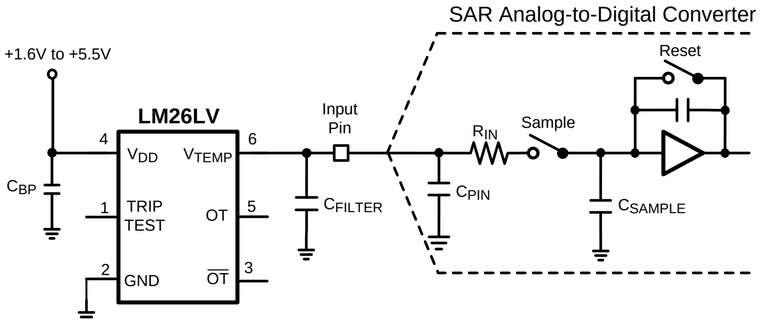

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Figure 26. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

8.2 Typical Application

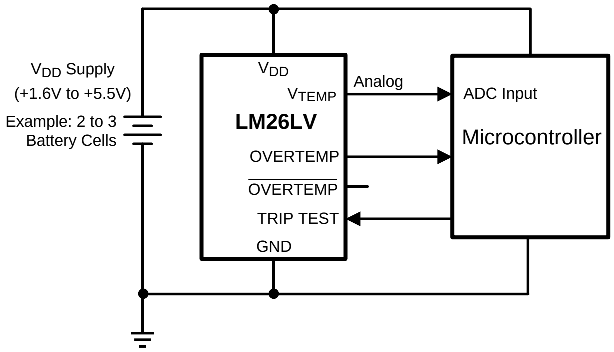

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Figure 27. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

PARAMETER	EXAMPLE VALUE
Temperature	0°C to 150°C (LM26LV), –40°C to 85°C for microcontroller
Accuracy	±2.3°C (Gain1, T_A = 0°C to 150°C)
V_{DD}	3.3 V
I_{DD}	8 µA

8.2.2 Detailed Design Procedure

The LM26LV and LM26LV-Q1 come with a factory preset trip point. See *Mechanical, Packaging, and Orderable Information* for available trip point options. Figure 27 shows the device's OVERTEMP output driving a microcontroller interrupt input to indicate an overtemperature event. In addition to the OVERTEMP output, a $\overline{\text{OVERTEMP}}$ output is available for use depending on the interrupt polarity of the microcontroller's interrupt pin. A VTEMP analog output is available to drive the microcontroller ADC input allowing the microcontroller to determine the sensing temperature of the LM26LV or LM26LV-Q1. The TRIP_TEST input is connected to a microcontroller output pin allowing the microcontroller to run on the fly electrical conductivity testing. For normal operation TRIP_TEST must be driven low by the microcontroller output. If no testing is required, the TRIP_TEST pin may be continuously grounded.

8.2.3 Application Curves

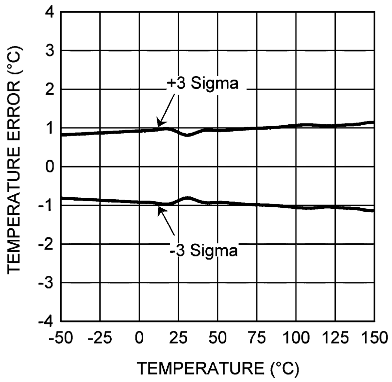

Figure 28. V_{TEMP} Analog Output Temperature Error

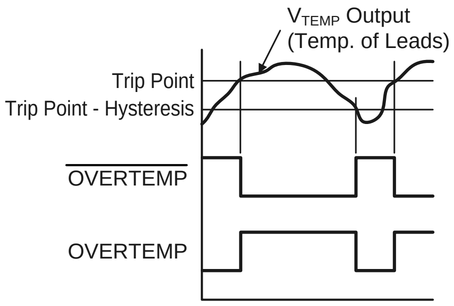

Figure 29. Switch Output Function

9 Power Supply Recommendations

Bypass capacitors are optional, and maybe required if the supply line is extremely noisy at high frequencies. TI recommends that a local supply decoupling capacitor be used to reduce noise. For noisy environments, TI recommends a 100-nF supply decoupling capacitor placed closed across the V_{DD} and GND pins of the LM26LV or LM26LV-Q1.

9.1 Power Supply Noise Immunity

The LM26LV and LM26LV-Q1 are virtually immune from false triggers on the OVERTEMP and $\overline{\text{OVERTEMP}}$ digital outputs due to noise on the power supply. Test have been conducted showing that, with the die temperature within 0.5°C of the temperature trip point, and the severe test of a 3 V***pp square wave "***noise" signal injected on the V_{DD} line, with V_{DD} from 2 V to 5 V, there were no false triggers.

10 Layout

10.1 Layout Guidelines

10.1.1 Mounting and Temperature Conductivity

The LM26LV or LM26LV-Q1 can be applied easily in the same way as other integrated-circuit temperature sensors. The devices can be glued or cemented to a surface.

The best thermal conductivity between the device and the PCB is achieved by soldering the DAP of the package to the thermal pad on the PCB. The temperatures of the lands and traces to the other leads of the LM26LV and LM26LV-Q1 also affect the temperature reading.

Alternatively, the LM26LV or LM26LV-Q1 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM26LV or LM26LV-Q1 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the V_{TEMP} output to ground or V_{DD}, the V_{TEMP} output from the LM26LV or LM26LV-Q1 is not correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The thermal resistance junction-to-ambient ($R_{\theta JA}$) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. The equation used to calculate the rise in the LM26LV's and LM26LV-Q1's die temperature is

$$T_J = T_A + R_{\theta JA} \times \left((V_{DD} \times I_Q) + (V_{DD} - V_{TEMP}) \times I_L \right)$$

where

- T_A is the ambient temperature
- I_Q is the quiescent current
- I_L is the load current on the output
- V_O is the output voltage (9)

For example, in an application where T_A = 30°C, V_{DD} = 5 V, I_{DD} = 9 µA, Gain 4, V_{TEMP} = 2231 mV, and I_L = 2 µA, the junction temperature would be 30.021°C, showing a self-heating error of only 0.021°C. Because the LM26LV's and LM26LV-Q1's junction temperature is the actual temperature being measured, minimize the load current that the V_{TEMP} output is required to drive. If $\overline{\text{OVERTEMP}}$ is used with a 100-k pullup resistor, and is asserted (low), then for this example the additional contribution is (152°C/W) × (5 V)^2 / 100 kΩ = 0.038°C for a total self-heating error of 0.059°C. *Thermal Information* shows the thermal resistance of the LM26LV and LM26LV-Q1.

10.2 Layout Example

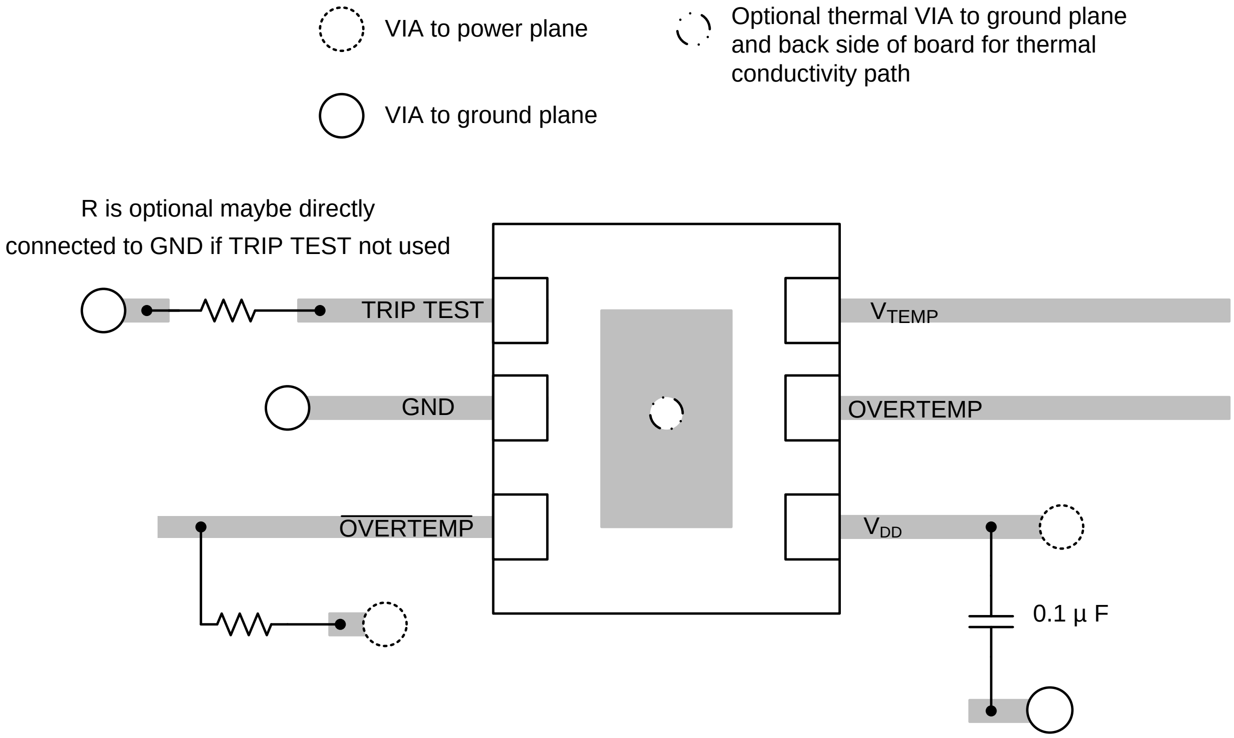

Figure 30. Typical Layout Example

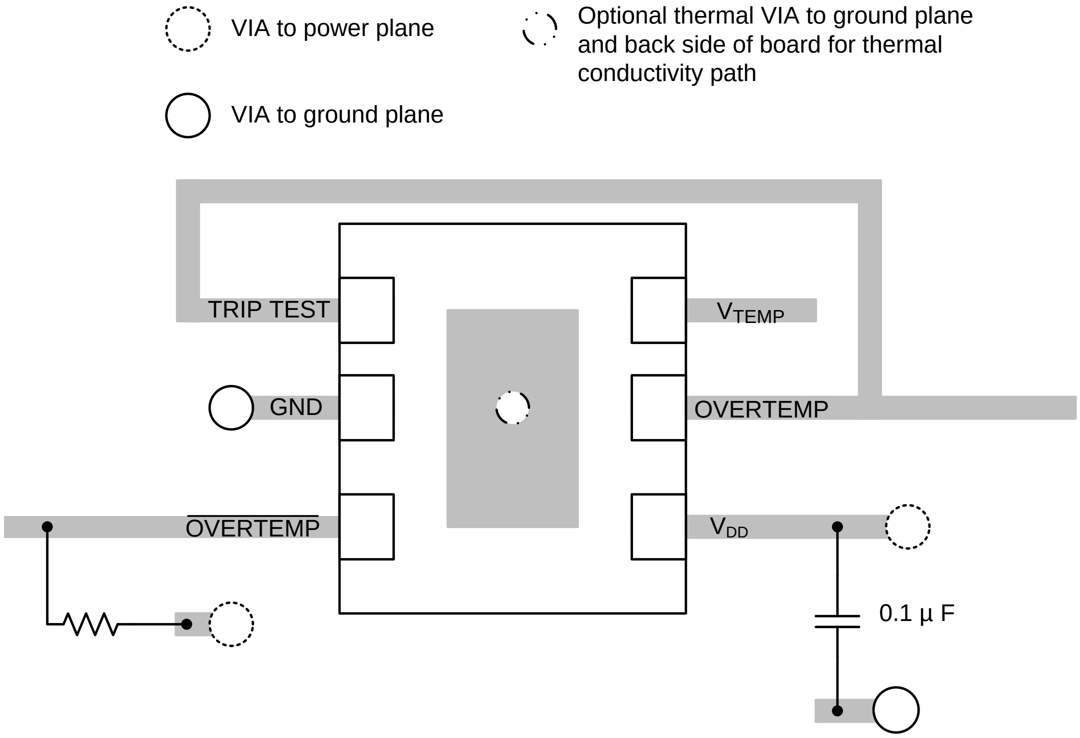

Figure 31. Latching Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Absolute Maximum Ratings for Soldering (SNOA549)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM26LV	Click here	Click here	Click here	Click here	Click here
LM26LV-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM26LVCISD-050/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	050	Samples
LM26LVCISD-060/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	060	Samples
LM26LVCISD-065/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	065	Samples
LM26LVCISD-070/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	070	Samples
LM26LVCISD-075/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	075	Samples
LM26LVCISD-080/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	080	Samples
LM26LVCISD-085/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	085	Samples
LM26LVCISD-090/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	090	Samples
LM26LVCISD-095/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	095	Samples
LM26LVCISD-100/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	100	Samples
LM26LVCISD-105/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	105	Samples
LM26LVCISD-110/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	110	Samples
LM26LVCISD-115/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	115	Samples
LM26LVCISD-120/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	120	Samples
LM26LVCISD-125/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	125	Samples
LM26LVCISD-135/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	135	Samples
LM26LVCISD-140/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	140	Samples

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM26LVCISD-145/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	145	Samples
LM26LVCISD-150/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	150	Samples
LM26LVCISDX-060/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	060	Samples
LM26LVCISDX-120/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	120	Samples
LM26LVQISD-130/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	Q30	Samples
LM26LVQISDX-130/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	Q30	Samples
LM26LVQISDX-135/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	Q35	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM26LV, LM26LV-Q1 :

- Catalog: LM26LV

- Automotive: LM26LV-Q1

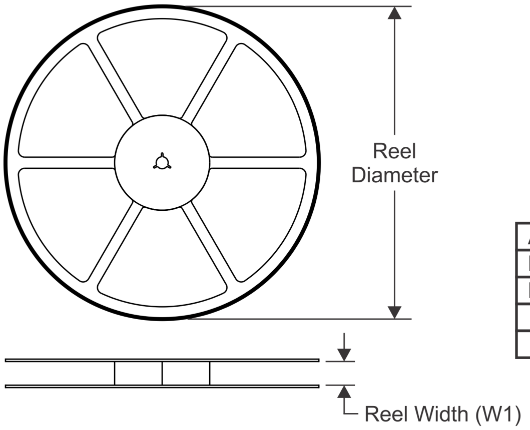
NOTE: Qualified Version Definitions:

  - Catalog - TI's standard catalog product

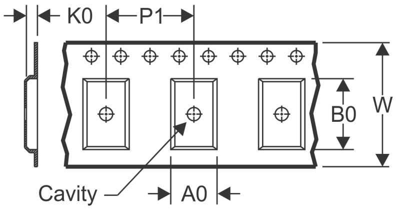
  - Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

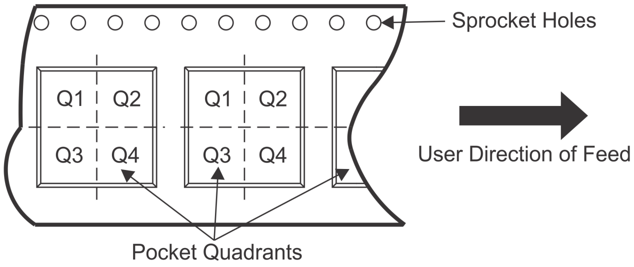


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

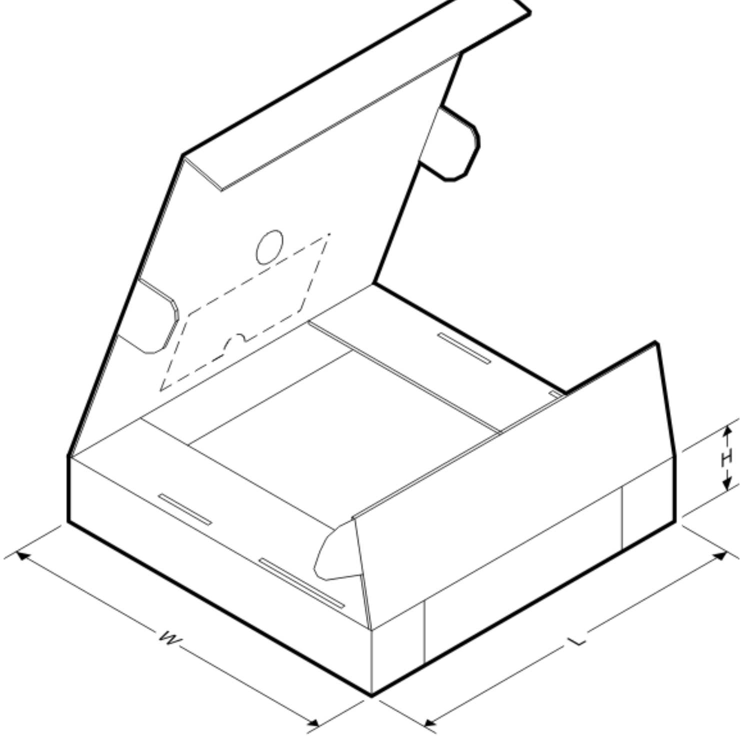


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM26LVCISD-050/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-060/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-065/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-070/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-075/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-080/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-085/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-090/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-095/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-100/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-105/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-110/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-115/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-120/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-125/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-135/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-140/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISD-145/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM26LVCISD-150/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISDX-060/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVCISDX-120/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVQISD-130/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVQISDX-130/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LM26LVQISDX-135/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1

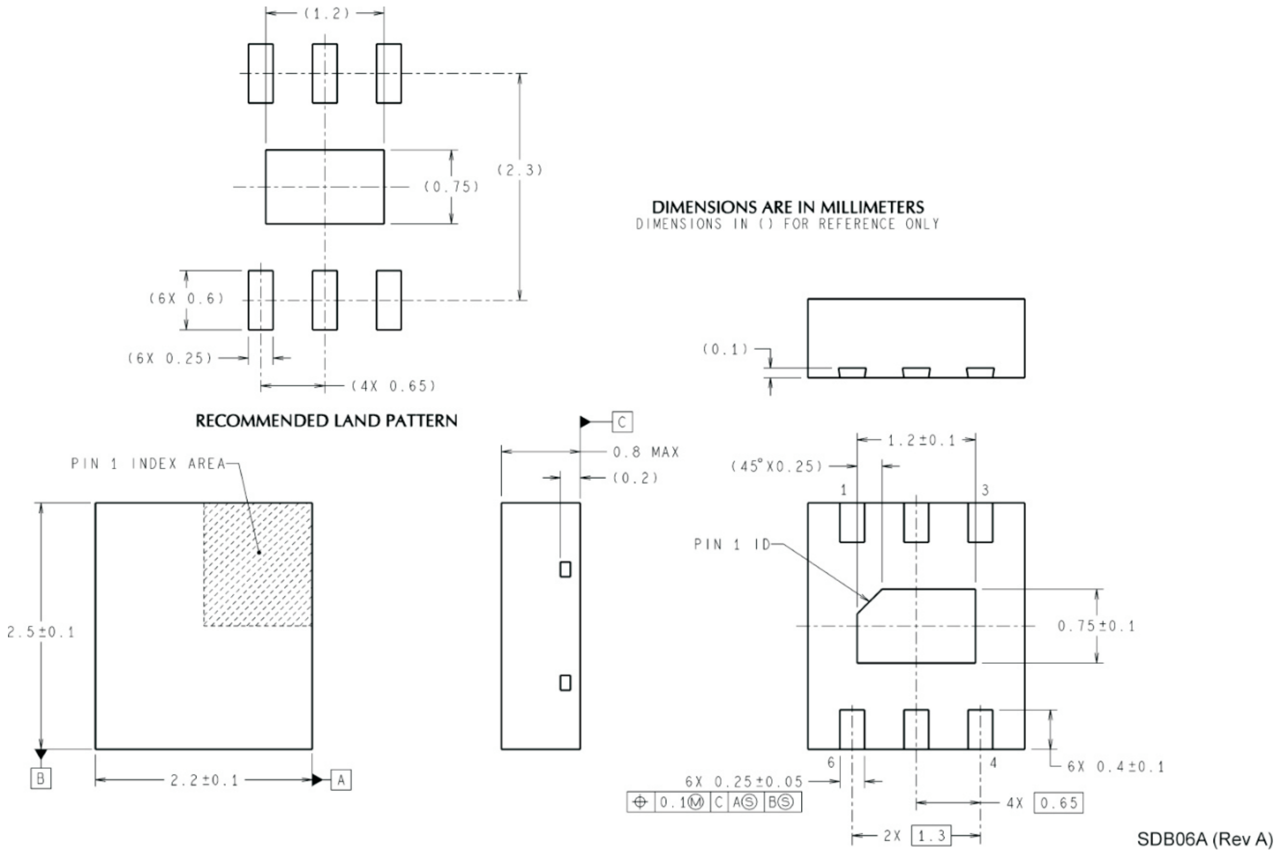
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM26LVCISD-050/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-060/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-065/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-070/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-075/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-080/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-085/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-090/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-095/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM26LVCISD-100/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-105/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-110/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-115/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-120/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-125/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-135/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-140/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-145/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISD-150/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVCISDX-060/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LM26LVCISDX-120/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LM26LVQISD-130/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LM26LVQISDX-130/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LM26LVQISDX-135/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0


(1.2)
(2.3)
(0.75)
(6X 0.6)
(6X 0.25)
(4X 0.65)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
C
0.8 MAX
(0.2)
PIN 1 INDEX AREA
2.5±0.1
B
2.2±0.1
A
1.2±0.1
(45°X0.25)
1
3
PIN 1 ID
0.75±0.1
6
4
6X 0.4±0.1
6X 0.25±0.05
⊕ 0.1Ⓜ C AⓈ BⓈ
4X 0.65
2X 1.3
SDB06A (Rev A)

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