



# THE DATASHEET OF DG445CY





# Improved, Quad, SPST Analog Switches

DG444/DG445

## General Description

Maxim's redesigned DG444/DG445 analog switches now feature on-resistance matching ( $4\Omega$  max) between switches and guaranteed on-resistance flatness over the signal range ( $9\Omega$  max). These low on-resistance switches conduct equally well in either direction. They guarantee low charge injection ( $10\text{pC}$  max), low power consumption ( $35\mu\text{W}$  max), and an electrostatic discharge (ESD) tolerance of  $2000\text{V}$  (min) per Method 3015.7. The new design offers lower off-leakage current over temperature (less than  $5\text{nA}$  at  $+85^\circ\text{C}$ ).

The DG444/DG445 are quad, single-pole/single-throw (SPST) analog switches. The DG444 has four normally closed switches and the DG445 has four normally open switches. Switching times are less than  $250\text{ns}$  for  $t_{\text{ON}}$  and less than  $70\text{ns}$  for  $t_{\text{OFF}}$ . Operation is from a single  $+10\text{V}$  to  $+30\text{V}$  supply, or bipolar  $\pm 4.5\text{V}$  to  $\pm 20\text{V}$  supplies. Maxim's improved DG444/DG445 continue to be fabricated with a  $44\text{V}$  silicon-gate process.

## Applications

Sample-and-Hold Circuits	Communication Systems
Test Equipment	Battery-Operated Systems
Heads-Up Displays	PBX, PABX
Guidance and Control Systems	Audio Signal Routing
Military Radios	Modems/Faxes

## New Features

- ◆ Plug-In Upgrades for Industry-Standard DG444/DG445
- ◆ Improved  $R_{\text{ON}}$  Match Between Channels ( $4\Omega$  max)
- ◆ Guaranteed  $R_{\text{FLAT(ON)}}$  Over Signal Range ( $9\Omega$  max)
- ◆ Improved Charge Injection ( $10\text{pC}$  max)
- ◆ Improved Off-Leakage Current Over Temperature ( $< 5\text{nA}$  at  $+85^\circ\text{C}$ )
- ◆ Withstand ESD ( $2000\text{V}$  min) per Method 3015.7

## Existing Features

- ◆ Low  $R_{\text{DS(ON)}}$  ( $85\Omega$  max)
- ◆ Single-Supply Operation  $+10\text{V}$  to  $+30\text{V}$   
Bipolar-Supply Operation  $\pm 4.5\text{V}$  to  $\pm 20\text{V}$
- ◆ Low Power Consumption ( $35\mu\text{W}$  max)
- ◆ Rail-to-Rail Signal Handling
- ◆ TTL/CMOS-Logic Compatible

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DG444CJ	$0^\circ\text{C}$ to $+70^\circ\text{C}$	16 Plastic DIP
DG444CY	$0^\circ\text{C}$ to $+70^\circ\text{C}$	16 Narrow SO
DG444C/D	$0^\circ\text{C}$ to $+70^\circ\text{C}$	Dice*
DG444DJ	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	16 Plastic DIP
DG444DY	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	16 Narrow SO

Ordering Information continued at end of data sheet.  
\*Contact factory for dice specifications.

## Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

**DIP/SO**

DG444	
LOGIC	SWITCH
0	ON
1	OFF

**Thin QFN**

SWITCHES SHOWN FOR LOGIC "0" INPUT

Pin Configurations continued at end of data sheet.

# Improved, Quad, SPST Analog Switches

## ABSOLUTE MAXIMUM RATINGS

(Voltage Referenced to V-)

V+ .....	44V
GND .....	25V
V <sub>L</sub> .....	(GND - 0.3V) to (V+ + 0.3V)
Digital Inputs V <sub>S</sub> , V <sub>D</sub> (Note 1) .....	(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) .....	30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) ..	100mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

6-Pin Narrow SO (derate 8.70mW/°C above +70°C) ..	696mW
16-Pin PDIP (derate 10.53mW/°C above +70°C) .....	842mW
16-Pin Thin QFN (derate 33.3mW/°C above +70°C) ..	2667mW
Operating Temperature Ranges	
DG444C/DG445C .....	0°C to +70°C
DG444D, E/DG445D, E .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C

**Note 1:** Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V<sub>L</sub> = 5V, GND = 0, V<sub>INH</sub> = 2.4V, V<sub>INL</sub> = 0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS		
<b>SWITCH</b>								
Analog Signal Range	V <sub>ANALOG</sub>	(Note 3)	-15		+15	V		
Drain-Source On-Resistance	R <sub>DSON</sub>	V+ = 13.5V, V- = -13.5V, V <sub>D</sub> = ±8.5V, I <sub>S</sub> = -10mA	T <sub>A</sub> = +25°C		50	85	Ω	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			100		
On-Resistance Match Between Channels (Note 4)	ΔR <sub>DSON</sub>	V <sub>D</sub> = ±10V, I <sub>S</sub> = -10mA	T <sub>A</sub> = +25°C			4	Ω	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			5		
On-Resistance Flatness (Note 4)	R <sub>FLAT(ON)</sub>	V <sub>D</sub> = ±5V, I <sub>S</sub> = -10mA	T <sub>A</sub> = +25°C			9	Ω	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			15		
Source Leakage Current (Note 5)	I <sub>S(OFF)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ±15.5V	T <sub>A</sub> = +25°C		-0.50	+0.01	+0.50	nA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		-5		+5	
Drain Off-Leakage Current (Note 5)	I <sub>D(OFF)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ±15.5V	T <sub>A</sub> = +25°C		-0.50	+0.01	+0.50	nA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		-5		+5	
Drain On-Leakage Current (Note 5)	I <sub>D(ON)</sub> or I <sub>S(ON)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ±15.5V	T <sub>A</sub> = +25°C		-0.50	+0.08	+0.50	nA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		-10		+10	
<b>INPUT</b>								
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2.4V, all others = 0.8V	-0.5	-0.00001	+0.5	μA		
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0.8V, all others = 2.4V	-0.5	-0.00001	+0.5	μA		

# Improved, Quad, SPST Analog Switches

DG444/DG445

## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, VL = 5V, GND = 0, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
<b>SWITCH</b>							
Power-Supply Range	V+, V-			±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1	-0.001	+1	µA
			TA = TMIN to TMAX	-5		+5	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1	-0.0001	+1	µA
			TA = TMIN to TMAX	-5		+5	
Logic Supply Current	IL	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1	-0.001	+1	µA
			TA = TMIN to TMAX	-5		+5	
Ground Current	IGND	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1	-0.0001	+1	µA
			TA = TMIN to TMAX	-5		+5	
<b>INPUT</b>							
Turn-On Time	tON	VS = ±10V, Figure 2	TA = +25°C		150	250	ns
Turn-Off Time	tOFF	DG444, VS = ±10V, Figure 2	TA = +25°C		90	120	ns
		DG445, VS = ±10V, Figure 2	TA = +25°C		110	170	ns
Charge Injection (Note 3)	Q	CL = 1nF, VGEN = 0, RGEN = 0Ω, Figure 3	TA = +25°C		5	10	pC
Off-Isolation Rejection Ratio (Note 6)	OIRR	RL = 50Ω, CL = 5pF, f = 1MHz, Figure 4	TA = +25°C		60		dB
Crosstalk (Note 7)		RL = 50Ω, CL = 5pF, f = 1MHz, Figure 5	TA = +25°C		100		dB
Source Off-Capacitance	CS(OFF)	f = 1MHz, Figure 6	TA = +25°C		4		pF
Drain Off-Capacitance	CD(OFF)	f = 1MHz, Figure 6	TA = +25°C		4		pF
Source On-Capacitance	CS(ON)	f = 1MHz, Figure 7	TA = +25°C		16		pF
Drain On-Capacitance	CD(ON)	f = 1MHz, Figure 7	TA = +25°C		16		pF

# Improved, Quad, SPST Analog Switches

## ELECTRICAL CHARACTERISTICS—Single Supply

( $V_+ = 12V$ ,  $V_- = 0$ ,  $V_L = 5V$ ,  $GND = 0$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS	
<b>SWITCH</b>							
Analog Signal Range	$V_{ANALOG}$	(Note 3)	0		12	V	
Drain-Source On-Resistance	$R_{DS(ON)}$	$V_+ = 10.8V$ ; $V_L = 5.25V$ ; $V_D = 3V, 8V$ ; $I_S = -10mA$	$T_A = +25^\circ C$	100	160	$\Omega$	
			$T_A = T_{MIN}$ to $T_{MAX}$		200		
<b>SUPPLY</b>							
Power-Supply Range	$V_+, V_-$		10.8		24.0	V	
Power-Supply Current	$I_+$	All channels on or off, $V_{IN} = 0V$ or $5V$	$T_A = +25^\circ C$	-1	+0.001	+1	$\mu A$
			$T_A = T_{MIN}$ to $T_{MAX}$	-5		+5	
Negative Supply Current	$I_-$	All channels on or off, $V_{IN} = 0V$ or $5V$	$T_A = +25^\circ C$	-1	-0.0001	+1	$\mu A$
			$T_A = T_{MIN}$ to $T_{MAX}$	-5		+5	
Logic Supply Current	$I_L$	All channels on or off, $V_{IN} = 0V$ or $5V$	$T_A = +25^\circ C$	-1	+0.001	+1	$\mu A$
			$T_A = T_{MIN}$ to $T_{MAX}$	-5		+5	
Ground Current	$I_{GND}$	All channels on or off, $V_{IN} = 0V$ or $5V$	$T_A = +25^\circ C$	-1	-0.0001	+1	$\mu A$
			$T_A = T_{MIN}$ to $T_{MAX}$	-5		+5	
<b>DYNAMIC</b>							
Turn-On Time	$t_{ON}$	$V_S = 8V$ , Figure 2		300	400	ns	
Turn-Off Time	$t_{OFF}$	$V_S = 8V$ , Figure 2		60	200	ns	
Charge Injection (Note 3)	$Q$	$C_L = 1nF$ , $V_{GEN} = 0$ , $R_{GEN} = 0\Omega$ , Figure 3		5	10	pC	

**Note 2:** Typical values are for **design aid only**, are not guaranteed, and are not subject to production testing. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

**Note 3:** Guaranteed by design.

**Note 4:** On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog signal range.

**Note 5:** Leakage parameters  $I_{S(OFF)}$ ,  $I_{D(OFF)}$ ,  $I_{D(ON)}$ , and  $I_{S(ON)}$  are 100% tested at the maximum rated hot temperature and guaranteed at  $+25^\circ C$ .

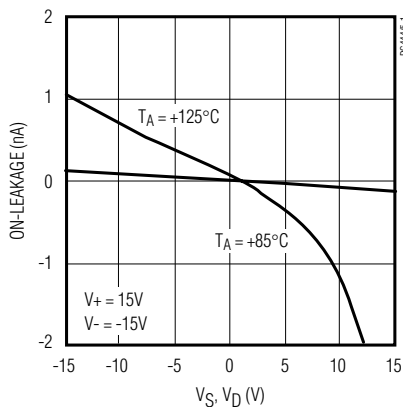
**Note 6:** Off-Isolation Rejection Ratio =  $20\log(V_D/V_S)$ ,  $V_D$  = output,  $V_S$  = input to off switch.

**Note 7:** Between any two switches.

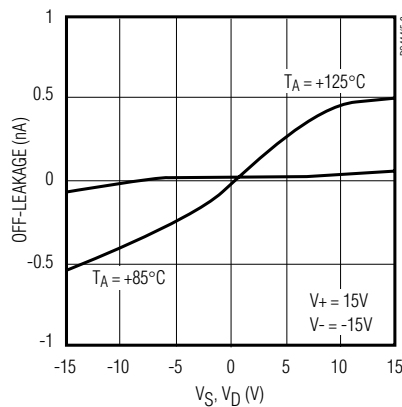
## Typical Operating Characteristics

( $T_A = +25^\circ C$ , unless otherwise noted.)

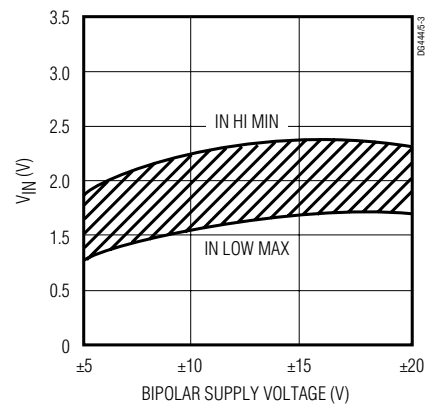
**ON-LEAKAGE CURRENTS**



**OFF-LEAKAGE CURRENTS**



**SWITCHING THRESHOLD vs. BIPOLAR SUPPLY VOLTAGE**



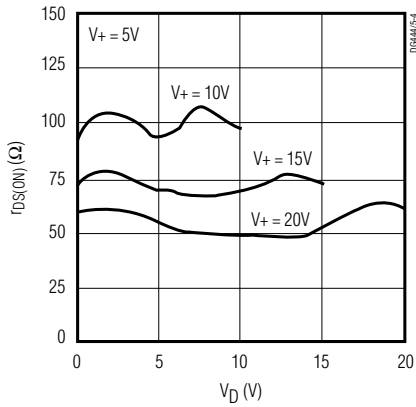
# Improved, Quad, SPST Analog Switches

## Typical Operating Characteristics

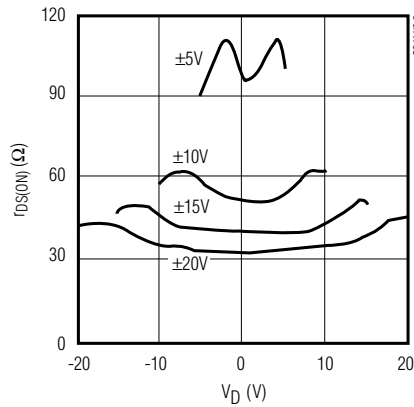
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

DG4444/DG4445

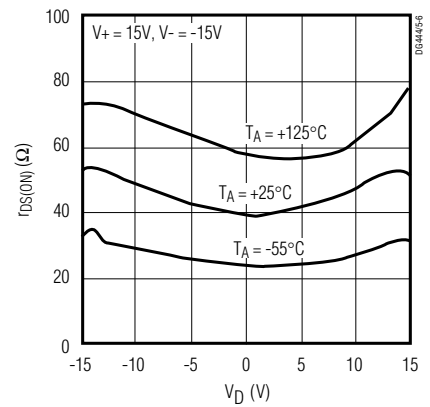
**ON-RESISTANCE vs.  $V_D$  AND UNIPOLAR-SUPPLY VOLTAGE**



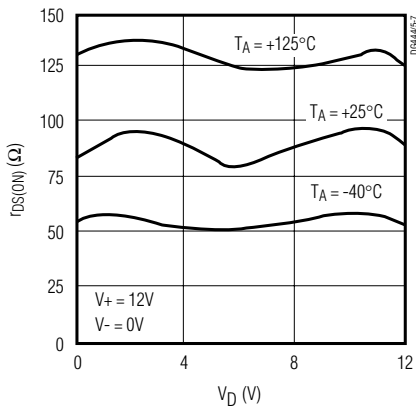
**ON-RESISTANCE vs.  $V_D$  AND BIPOLAR-SUPPLY VOLTAGE**



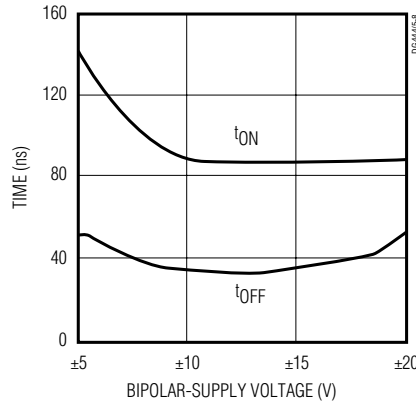
**ON-RESISTANCE vs.  $V_D$ , BIPOLAR-SUPPLY VOLTAGE AND TEMPERATURE**



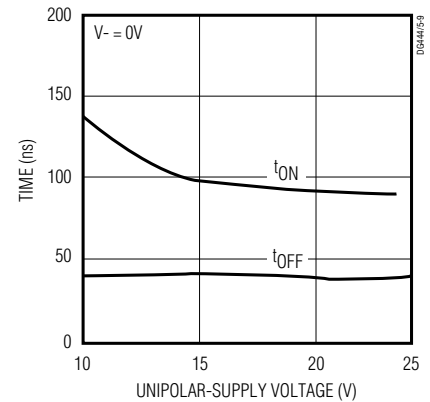
**ON-RESISTANCE vs.  $V_D$ , UNIPOLAR-SUPPLY VOLTAGE AND TEMPERATURE**



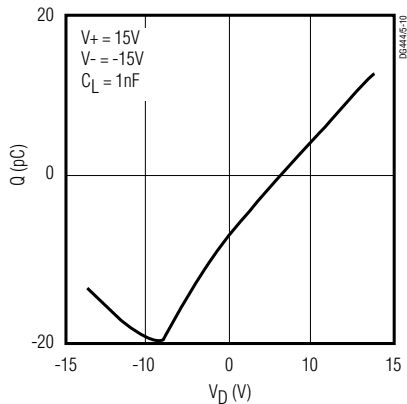
**SWITCHING TIME vs. BIPOLAR-SUPPLY VOLTAGE**



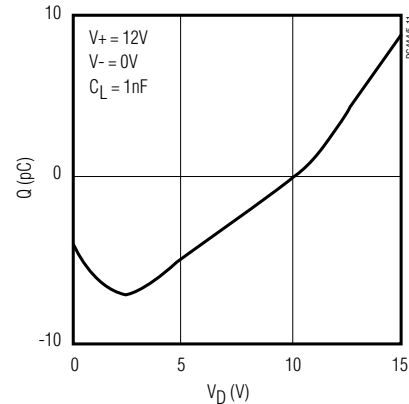
**SWITCHING TIME vs. UNIPOLAR-SUPPLY VOLTAGE**



**CHARGE INJECTION vs.  $V_D$  VOLTAGE**



**CHARGE INJECTION vs.  $V_D$  VOLTAGE**



# Improved, Quad, SPST Analog Switches

## Pin Description

PIN		NAME	FUNCTION
DIP/SO	THIN QFN		
1, 16, 9, 8	15, 14, 7, 6	IN1-IN4	Logic Control Inputs
2, 15, 10, 7	16, 13, 8, 5	D1-D4	Drain Outputs
3, 14, 11, 6	1, 12, 9, 4	S1-S4	Source Outputs
4	2	V-	Negative-Supply Voltage Input
5	3	GND	Ground
12	10	VL	Logic-Supply Voltage Input
13	11	V+	Positive-Supply-Voltage Input—Connected to Substrate
—	EP	PAD	Exposed Pad Connect Pad to V+

## Applications Information

### General Operation

- Switches are open when power is off.
- IN, D, and S should not exceed V+ or V-, even with the power off.
- Switch leakage is from each analog switch terminal to V+ or V-, not to other switch terminals.

### Operation with Supply Voltages Other than ±15V

Using supply voltages other than ±15V will reduce the analog signal range. The DG444/DG445 switches oper-

ate with ±4.5V to ±20V bipolar supplies or with a +10V to +30V single supply; connect V- to 0V when operating with a single supply. Also, all device types can operate with unbalanced supplies such as +24V and -5V. VL must be connected to +5V to be TTL compatible, or to V+ for CMOS-logic level inputs. The *Typical Operating Characteristics* graphs show typical on-resistance with ±20V, ±15V, ±10V, and ±5V supplies. (Switching times increase by a factor of two or more for operation at ±5V.)

### Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by VL, V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

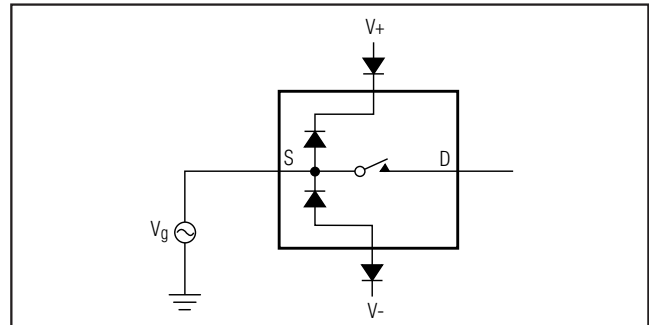


Figure 1. Overvoltage Protection Using External Blocking Diodes

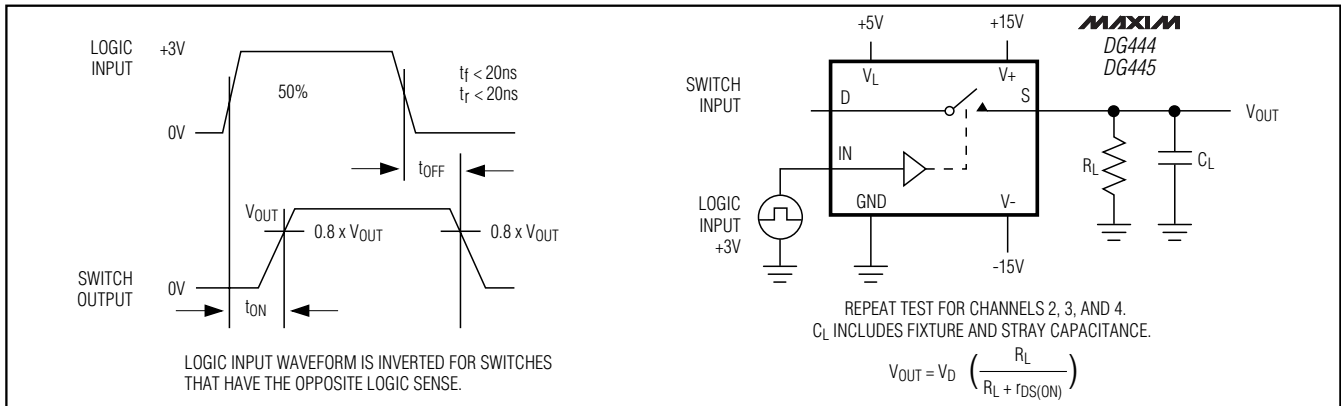


Figure 2. Switching Time

# Improved, Quad, SPST Analog Switches

**DG444/DG445**

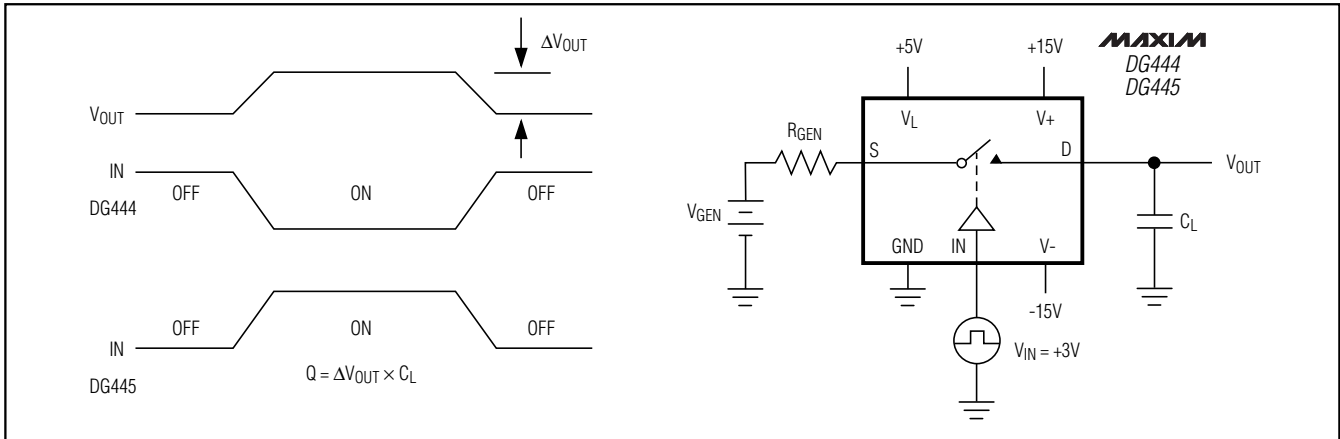


Figure 3. Charge Injection

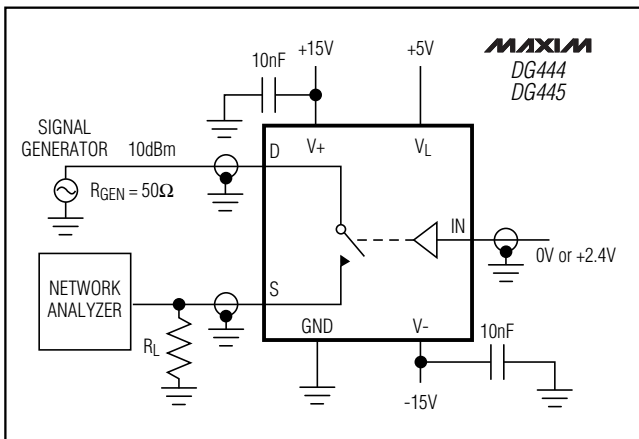


Figure 4. Off-Isolation Rejection Ratio

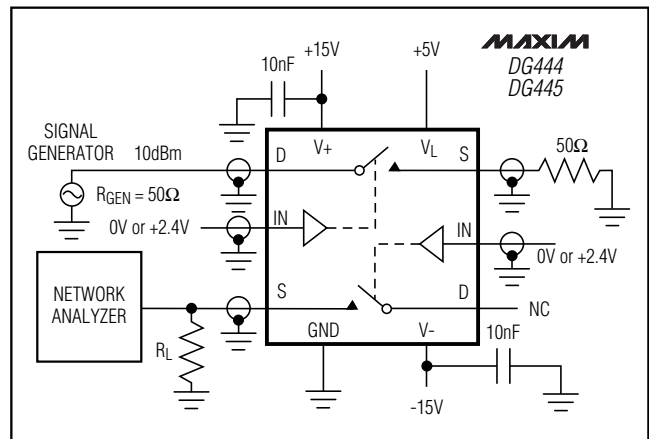


Figure 5. Crosstalk

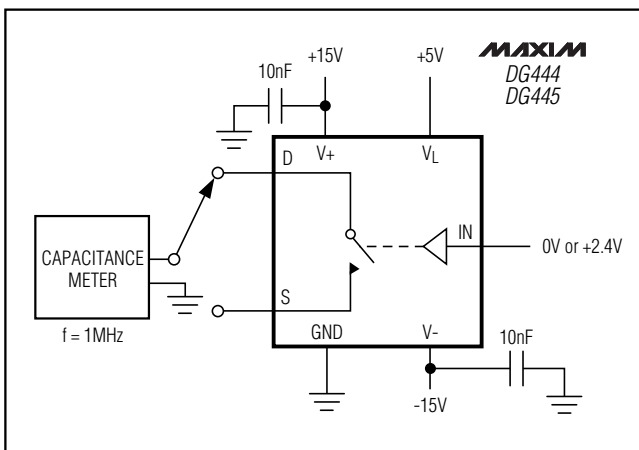


Figure 6. Source/Drain Off-Capacitance

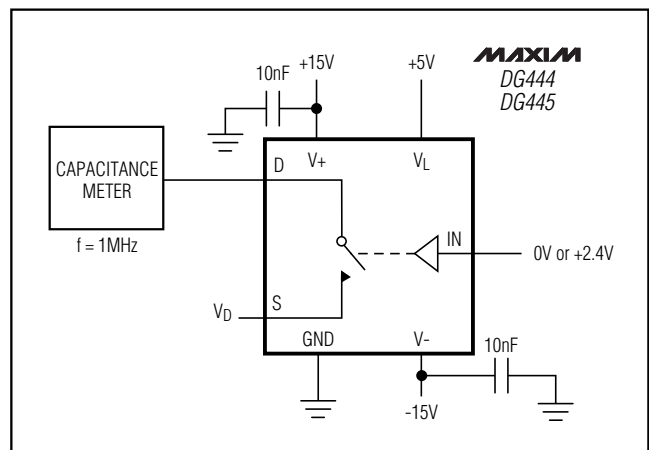
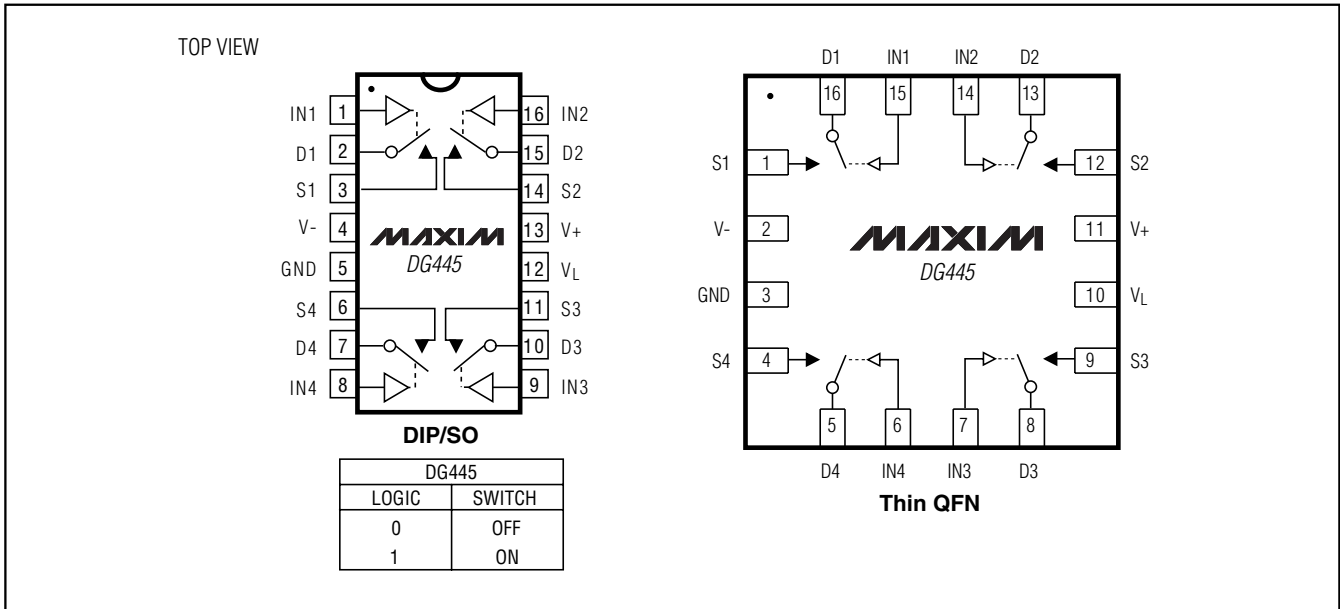


Figure 7. Source/Drain On-Capacitance

# Improved, Quad, SPST Analog Switches

## Pin Configurations/Functional Diagrams (continued)



## Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
DG444ETE	-40°C to +85°C	16 Thin QFN (5mm x 5mm)
<b>DG445CJ</b>	0°C to +70°C	16 Plastic DIP
DG445CY	0°C to +70°C	16 Narrow SO
DG445C/D	0°C to +70°C	Dice*
DG445DJ	-40°C to +85°C	16 Plastic DIP
DG445DY	-40°C to +85°C	16 Narrow SO
DG445ETE	-40°C to +85°C	16 Thin QFN (5mm x 5mm)

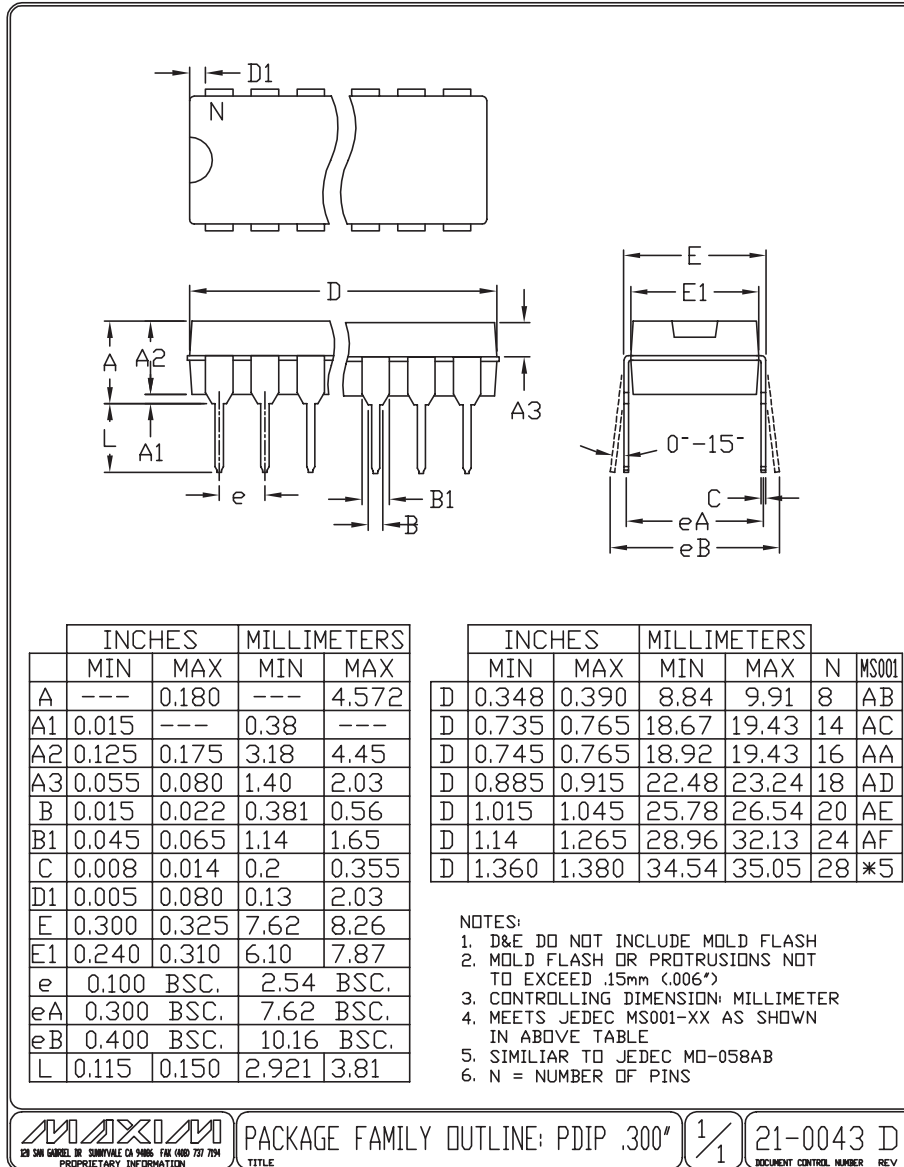
\*Contact factory for dice specifications.

# Improved, Quad, SPST Analog Switches

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

DG444/DG445



PDIPNLEFS



PACKAGE FAMILY OUTLINE: PDIP .300"

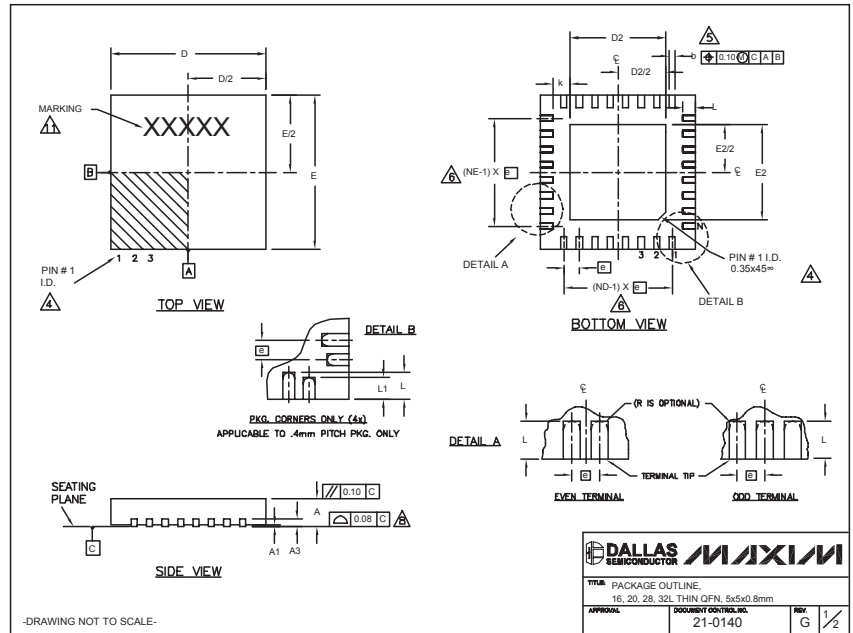
1/1

21-0043 D  
DOCUMENT CONTROL NUMBER REV

# Improved, Quad, SPST Analog Switches

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



COMMON DIMENSIONS												
PKG. SYMBOL	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
L1	-	-	-	-	-	-	-	-	-	-	-	-
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS											
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			±0.15		
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO			
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES			
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO			
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO			
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES			
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO			
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y			
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO			
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO			
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES			
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES			
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO			
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO			
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES			
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y			
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	N			
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO			
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES			
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO			
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO			

\*\*SEE COMMON DIMENSIONS TABLE

**DALLAS SEMICONDUCTOR MAXIM**

**TITLE** PACKAGE OUTLINE  
16, 20, 28, 32L THIN OFN, 5x5x0.8mm

**APPROVAL** DOCUMENT CONTROL NO. 21-0140 REV. G 2/2

-DRAWING NOT TO SCALE-



- NOTES:
- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
  - ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
  - N IS THE TOTAL NUMBER OF TERMINALS.
  - THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
  - DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
  - ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
  - DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
  - COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
  - DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
  - WARPAGE SHALL NOT EXCEED 0.10 mm.
  - MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
  - NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

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